



Method for preventing overvoltages, reactive power compensator, control system and computer program products

Field of the invention

The invention relates to the field of reactive power compensators, and in particular to means for preventing overvoltages in an electric power network caused by reactive power generated by reactive power compensators connected to the electric power network.

Background of the invention

Reactive power can be used to optimize power flow within an electric power network, denoted power network in the following. A reactive power compensator, for example a Static VAR (Volt-Ampere Reactive) Compensator (SVC), is a device frequently used within such power networks for combating disturbances within the network by means of reactive power. The SVC counteracts voltage drops in the power network by providing reactive power and is often able to handle overvoltages by absorbing reactive power.

To this end, the typical SVC comprises a bank of thyristor-switched capacitors (TSC), harmonic filters and thyristor-controlled inductive elements, also denoted reactors. These components of the SVC are controlled so as to provide the desired reactive power. In particular, if the power network's reactive load is capacitive (leading) the SVC uses the reactors to consume VARs from the network, thereby lowering the system voltage. If the power network's reactive load is inductive (lagging) the capacitor banks are used for supplying reactive power to the power network, thereby increasing the power network voltage.

When a power network fault occurs in the power network, a control system of the SVC orders the SVC to provide suitable

reactive power. In case of a short circuit fault, the SVC is run at full capacitive effect in order to support the power network voltage. However, if the load of the power network is low, the voltage support of the SVC, and in particular the
5 thyristor-switched capacitors and filters thereof, will give high temporary overvoltages in the power network immediately after the short circuit fault has been cleared. Overvoltages in the power network may, among other things, cause costly network device faults, and should thus obviously be avoided.

10 A prior art method of combating such overvoltages is to block the thyristor-switched capacitors during the time period that the power network voltage is depressed due to the short circuit fault. The SVC is then connected to the power network once the short circuit fault has been cleared.

15 However, there is a market demand to have the SVC connected to the power network at all times, and in particular to remain in operation during short-circuit faults. This demand derives from the desire to have the SVC increasing the voltage during power network faults.

20 In view of the above, it would be desirable to provide means for enabling the SVC to be connected to the power network even during power network faults.

Summary of the invention

It is an object of the invention to provide such means and
25 methods for enabling the SVC to be connected to the power network during power network faults, and in particular while still preventing overvoltages in the power network from occurring once the fault has been cleared.

It is another object of the invention to provide means and
30 methods for fast blocking of capacitors of the reactive power compensator upon a fault clearance.

It is still another object of the invention to enable the use of reactive power compensators during a power network fault, whereby the network voltage is constant or even slightly increasing.

5 These objects, among others, are achieved by means of a method, reactive power compensator, control system and computer program products as claimed in the appended claims.

In accordance with the invention a method is provided for preventing overvoltages in an electric power network caused by
10 reactive power generated by a reactive power compensator connected to the electric power network. The reactive power compensator comprises a thyristor-switched capacitor. The method is characterized by the steps of: measuring a voltage over a capacitor of the reactive power compensator, and
15 determining a need to block the thyristor-switched capacitor based on the capacitor voltage. By means of the invention, the reactive power compensator and in particular its capacitor banks can be connected to the electric power network during the power network fault, and blocked only after the clearance
20 of the power network fault. The reactive power compensator is thus used for voltage support during the power network fault. Overvoltages caused by the inability of the power network to, upon fault clearance, absorb the reactive power generated by the reactive power compensator, are avoided as action is taken
25 based on the measured capacitor voltage. The method provides a very fast control feature to a control system used for controlling a reactive power compensator, the feature enabling a fast switching out of the thyristor-switched capacitors at fast voltage recovery of the power network.

30 In accordance with an embodiment of the invention, the step of determining a need to block comprises the sub-steps of: processing the capacitor voltage, thereby obtaining a

processed capacitor voltage, measuring an instantaneous voltage over the capacitor, comparing the processed capacitor voltage with the instantaneous capacitor voltage, and blocking the thyristor-switched capacitors if the step of comparing
5 fulfils a predetermined criteria. This provides method steps that can easily be implemented by means of digital electronics.

In accordance with another embodiment of the invention, the predetermined criteria comprises one or both of following
10 criteria: 1) the instantaneous capacitor voltage divided by the processed capacitor voltage being larger than a factor k and the instantaneous capacitor voltage being larger than a first predetermined value, and/or 2) the instantaneous capacitor voltage being larger than a second predetermined
15 value. Flexible and easily implemented criteria for transmitting a blocking order to the thyristor-switched capacitors are thus enabled.

In accordance with still another embodiment of the invention, the step of processing comprises time delaying and/or low-pass
20 filtering the capacitor voltage. Yet additional processing steps can be implemented in dependence on need and the particular application at hand.

In accordance with yet another embodiment of the invention, the method is activated when a voltage measurement in the
25 reactive power compensator has indicated a negative sequence voltage. In accordance with this embodiment, the TSCs can be switched off already at the first current zero crossing following a fault clearance.

The invention also provides a reactive power compensator, a
30 control system for controlling such a reactive power compensator, and computer program products, whereby advantages corresponding to the above are achieved.

Further features and advantages thereof will become clear upon reading the following description of embodiments of the invention and the appended drawings.

Brief description of the drawings

5 Figure 1 illustrates a reactive power compensator connected to an electric power network.

Figure 2 illustrates a control system in accordance with the invention for controlling a reactive power compensator.

10 Figures 3a and 3b illustrate flow charts over steps of a method in accordance with the present invention.

Figure 4 illustrates a computer controlling the SVC in accordance with the invention.

Detailed description of embodiments of the invention

15 In order to provide a thorough understanding of the present invention, the functioning of a reactive power compensator, in the following exemplified by a SVC, is described in some more detail in the following.

20 The SVC can be controlled, by means of a control system, within a continuous range, wherein the range can be designed to span from absorbing to generating reactive power. In order to efficiently counteract voltage collapses due to short circuit faults, it is important that the SVC runs fully capacitive already during the power network fault.

25 The SVC comprises controllable branches, the thyristor-switched capacitors (TSCs) and thyristor-controlled reactors (TCRs), which both are controlled by "point on wave" switching. The TCRs are fired on a certain voltage angle that gives the desired current. The TSCs are switched on at the voltage angle giving a minimum of transients in its current.

At the initiation and clearing of the power network fault, the voltage across the TCR and TSC branches makes almost instantaneous angle changes. In addition to this, higher order transient voltages appear. Line to line faults are most
5 severe, the three line to line voltages that were 120 degrees apart in steady state, then change to two voltages 180 degrees away from the third. This is an almost instantaneous 60 degree jump. A thyristor valve firing system must identify this angular change and adapt the instants for firing pulses to the
10 thyristor valves. In case it fails, the thyristor valve will misfire and large transient currents may occur in the TSCs and a large DC current in the TCRs.

The controllable branches of the SVC are synchronized by means of the thyristor valve firing synchronization system. The
15 thyristor valve firing synchronization system is based on a phase locked loop (PLL) and a correction signal for negative sequence voltage content and rapid angular changes in the positive sequence voltage. The PLL works on the positive sequence voltage on the SVC medium voltage busbar.

20 The thyristor valve firing synchronization system rapidly tracks changes in the angles for the different phases. During the first half cycle following a short circuit in the power network, it is however a bit unclear what the angles are due to the fact that it takes some time to extract the positive
25 and negative phase sequences in the voltage.

In the prior art solution, mentioned in the introductory part, the SVC runs with the TSCs blocked. At a network fault, the SVC control system will act and block the TSCs and the time for this action is about one cycle.

30 At a three-phase fault the change in positive sequence voltage angle is normally moderate, although it may become so low that it is impossible to define an angle, resulting in that it is

not possible to fire the thyristor valves. All thyristor valves are blocked a certain time period after a low voltage, for example due to a short circuit in the power network. The thyristor valves are deblocked again after a time period after a voltage recovery.

During a short circuit in the power network, the positive sequence voltage is depressed. The SVC runs fully capacitive. In case of the power network having a small load, a temporary overvoltage may occur at fault clearing, as was described in the introductory part of the present application. The primary reason for the overvoltage is that the power network cannot absorb the reactive power generated by the SVC. The prior art control system is arranged to wait until the power network voltage has exceeded its set voltage until the control system can start reducing the susceptance order to the SVC. This inevitably results in an overvoltage with a duration of at least one cycle. Many prior art SVCs do not run capacitively until after the fault has cleared because there are no efficient ways to resolve this problem.

From the above, the need for faster switching out of the TSC at fast voltage recovery can be established. In accordance with the present invention, a control function is provided for meeting this need.

Figure 1 illustrates a reactive power compensator, exemplified in the following by a Static VAR Compensator (SVC) 1, in accordance with the invention. The SVC 1 is connected to an electric power network 2, denoted power network in the following, via a transformer 3 and a medium voltage busbar (MVB) 4, the transformer 3 and MVB 4 being part of the SVC.

A first branch 5 connected to the MVB 4 comprises a filter device. The first branch 5 is in the following denoted filter device. The filter device comprises, for example, one or more

tuned filters generating a certain reactive power at the power network frequency.

A second controllable branch 6 comprises a thyristor-switched capacitor (TSC) and is connected to the MVB 4. The second
5 controllable branch 6 is in the following denoted TSC. The TSC 6 comprises one or more capacitors 9 and reactors 10 series-connected to anti-parallel pairs thyristor valves 11 that switches on and off the capacitors 9. A capacitor switching operation is typically completed within one cycle of the
10 fundamental frequency of the power network 2.

Finally, a third controllable branch 7 connected to the MVB 4 comprises a thyristor controlled reactor(s) (TCR). The third controllable branch 7 is in the following denoted TCR. The TCR 7 comprises one or more reactors (inductors) 12 series-
15 connected to anti-parallel pairs of thyristor valves 13, that controls the reactive power by varying the current amplitude flowing through the reactors 12. The current can be changed by varying the thyristor valve firing angle, which angle can typically be fully changed within one cycle of the fundamental
20 frequency of the power network 2.

It is noted that the SVC 1 may comprise any number of filter devices, TSCs and TCRs. Further, although illustrated in the figures as a single capacitor it is noted that the filter devices, TSCs and TCRs may comprise any number of capacitors,
25 for example arranged in capacitor banks.

A control system 15 controls the functioning of the SVC 1. The control system 15 comprises, among other things, a voltage regulator 16 and a firing synchronization system 17 comprising thyristor firing pulse units.

30 The voltage regulator 16, e.g. a PI regulator, obtains an error signal that is the difference between a set reference

voltage V_{ref} and a voltage $V_{measured}$ measured in the power network 2. In conventional manner, the voltage regulator 16 acts to minimize the error signal.

5 The firing synchronization system 17 controls the TSC 6 and the TCR 7 of the SVC by providing control signals, or thyristor firing orders, to the thyristor valves 11, 13.

The invention is based on that at least one main voltage on the medium voltage busbar 4 of the SVC 1 drops substantially during a power network fault. In particular, at short
10 circuits, at least one line to line voltage on the SVC medium voltage busbar 5 becomes depressed.

When the power network fault is cleared, this voltage raises fast. In accordance with the invention, this increase in voltage, or voltage rise, is used in order to rapidly perform
15 regulation actions. The voltage rise has to be detected quickly, while fast voltage transients simultaneously have to be disregarded.

After some experimental work, the inventor of the present invention found a way of reliably detecting the voltage rise
20 occurring after a fault has been cleared. The line to line voltage on the medium voltage busbar 4 that have become depressed is measured with a minimum time delay on one of the conducting capacitors 9 of the TSCs 6. The voltage is preferably measured with a resistive voltage divider, although
25 other methods are conceivable.

As an alternative, the voltage on the capacitor 8 of the filter device 5 may be measured. This also provides a reliable measurement, fulfilling the requirements of minimum delay measurement and insensitive to fast voltage transients.

30 Figure 2 illustrates the inventive feature of the control system 15 in accordance with the invention. The voltage over

the capacitors 9 of the TSC 6, or in an alternative embodiment the voltage over the capacitors 8 of the filter device 5, is thus measured. This digital signal is denoted V_{cap} in the following and is input to a rectifier device 21. The signal
5 output from the rectifier device 21 is denoted V_i and is input to a low-pass filter 22 and possibly processed in yet additional ways, illustrated in the figure by a box 23. The signal is also time-delayed after which it is input to a first comparator device 25. The signal V_i when processed (22, 23) and
10 time delayed (24) is denoted V_p .

The unprocessed signal, the instantaneous value of V_{cap} , output from the rectifier device 21, i.e. V_i , is also input to the first comparator device 25. The first comparator device 25 is arranged to compare the instantaneous capacitor voltage V_i to
15 the processed voltage V_p .

The signal V_i is further input to a second comparator device 26 and to a third comparator device 27. The second and third comparator devices 26 and 27 are arranged to compare the signal V_i with predetermined values X and Y, respectively.

20 The output from the first comparator device 25 is input to an AND gate 28 as is the output from the second comparator device 26. The output from the AND gate 28 is input to a fourth comparator device 29. In particular, if the instantaneous voltage V_i is larger than the processed voltage V_p , and if the
25 instantaneous voltage V_i further is above a certain level X, then the AND gate 28 outputs HIGH (digital value 1) to the fourth comparator device 29. The output from the fourth comparator device 29 forms the basis for a decision on whether or not to cancel the firing orders for the TSCs 6. For the
30 case of the AND gate 28 outputting HIGH, the fourth comparator device 29 then outputs an order to cancel the firing order to the TSC 6.

As a safety measure, the output from the third comparator device 27 is input to the fourth comparator device 29. If the instantaneous capacitor voltage, represented by signal V_i , exceeds a certain value Y , but is lower than kV_p , then the firing orders are cancelled irrespective of the output from the first and second comparator devices 25 and 26, respectively. The output from the third comparator device 27 is thus a safety measure, wherein it is sufficient that the voltage value exceeds a certain predetermined value for the firing order to the TSC 6 to be cancelled.

Thus, if either of the inputs to the fourth comparator device 29 is HIGH, then a firing order to the TSC 6 is cancelled.

Purely as an illustration, typical settings are described in the following as a non-limiting example. It is realized that any settings are possible, suitably set in dependence on the application at hand. Exemplary settings for the parameters X and Y are thus 0.9 and 1.5 pu (per unit) respectively. For example, if the signal V_i exceeds $X = 0.9$ pu and it is at least twice the processed voltage V_p , the firing orders for the TSC 5 are cancelled from block 28 (figure 2). If, on the other hand, the signal exceeds $Y = 1.5$ pu but not twice the processed voltage V_p , the firing orders for the TSC 5 are cancelled from block 27 (figure 2). In case the signal is smaller than twice the processed voltage V_p and also smaller than $Y=1.5$ pu no action will follow.

Figure 3a illustrates a flow chart over steps of a method in accordance with the present invention. The method 30 begins at step 31, wherein a capacitor voltage V_{cap} is determined by measuring. This capacitor voltage V_{cap} may be the voltage over the TSC 6 capacitors 9 or the voltage over the filter device 5 capacitors 8. The voltage may be measured by means of a resistive voltage divider.

The method comprises the second step 32 of determining a need for blocking the thyristor-switched capacitors 6, based on the measured capacitor voltage V_{cap} .

In an embodiment of the invention, the measured capacitor
5 voltage V_{cap} is processed as described earlier, providing a signal V_p , and is then compared to an instantaneous capacitor voltage V_i . If the instantaneous capacitor voltage V_i is, for example, double the signal V_p , then a blocking order (cancelling of firing orders) is sent to the TSCs 6.

10 Other criteria may be used alternatively or in combination with the above comparison. For example, if the instantaneous capacitor voltage V_i is above a certain level, then the blocking order is sent to the TSCs 6.

The above embodiment is illustrated in figure 3b. The step of
15 determining a need to block 32, or disconnect, then comprises the first sub-step of processing 33 the capacitor voltage V_{cap} , thereby obtaining the processed capacitor voltage, i.e. the signal V_p . The second sub-step comprises measuring 34 the instantaneous capacitor voltage V_i over the chosen capacitor (8
20 or 9) of the SVC 1. The third sub-step comprises comparing 35 the processed capacitor voltage, i.e. signal V_p with the instantaneous capacitor voltage, i.e. signal V_i . This can be implemented in any suitable manner. The fourth sub-step comprises blocking 36 the TSC 6 if the previous step of
25 comparing 35 fulfils some predetermined criteria.

As mentioned, the predetermined criteria may comprise one or both of following criteria: the instantaneous capacitor voltage, i.e. signal V_i , divided by the processed capacitor voltage, i.e. signal V_p , being larger than a factor k , i.e. V_i
30 $> kV_p$, and the signal V_i being larger than a first predetermined value X ; and/or the signal V_i being larger than a

second predetermined value Y. These criteria have been described with reference to figure 2.

It is noted that the order of the steps of the method 30 can be changed. For example, step 34 can be performed before or
5 simultaneously as step 33.

The method 30 may comprise yet additional steps. The step of processing 33 may for example comprise a number of sub-steps, such as time delaying and/or low-pass filtering the capacitor voltage V_{cap} , as described earlier.

10 The above method can be activated at a particular instant. Namely, at all major power network faults, the conventional SVC voltage measurements will during a short period of time indicate a negative sequence voltage. The method may be activated when such a pulse having an amplitude over a certain
15 level. During the power network fault, at least one capacitor voltage will become low. In accordance with the invention, the TSCs are blocked when certain criteria is fulfilled, for example when one of the capacitor voltages have doubled.

By means of the invention, the TSCs can be switched off
20 already at the first current zero crossing following a fault clearance.

Further yet, with reference to figure 4, the invention provides a computer program product 41 loadable into the internal memory of a computer 40 that controls a reactive
25 power compensator, such as the SVC 1. The computer program product 41 comprises software code portions for carrying out the method as described above, when it is run on the computer 40. The computer program product 41 can be stored on a computer readable storage medium 42, comprising computer
30 readable program code means for causing the computer 40 of the SVC 1 to carry out the method as described.

Actual test runs in a power network have been done. The SVC 1 responds quickly to the fault, it goes fully capacitive in one and a half cycle. During the fault, the system voltage is constant or even increasing slightly. It can be noted that the
5 unfaulted phase voltages do not drop much. At the fault clearing the faulted phase recovers instantaneously. In the tests, the SVC reduced its output somewhat (about 100 MVAR) and ran at 500 MVars for about 4 cycles, thereafter it gradually reduced its output to about 200 Mvars during the
10 next 5 cycles. It stayed at this output during the recorded period of 30 s.

In summary, by means of the invention, the end of fault clearances is detected very fast and the TSCs can then quickly be blocked so as to not cause overvoltages. Further, the TCRs
15 of the SVC 1 can quickly be forced to full inductive operation.

Claims

1. A method (30) for preventing overvoltages in an electric power network (2) after a power network fault, said overvoltage being caused by reactive power generated by a reactive power compensator (1) connected to said electric power network (2), said reactive power compensator (1) comprising a thyristor-switched capacitor (6), **characterized by** the steps of:

- measuring (31) a voltage (V_{cap}) over a capacitor (8, 9) of said reactive power compensator (1),

- determining (32) a need to block said thyristor-switched capacitors (6) based on said capacitor voltage (V_{cap}).

2. The method as claimed in claim 1, wherein said step of determining a need to block comprises the steps of:

- processing (33) said capacitor voltage (V_{cap}), thereby obtaining a processed capacitor voltage (V_p),

- measuring (34) an instantaneous voltage (V_i) over said capacitor (8, 9) of said reactive power compensator (1),

- comparing (35) said processed capacitor voltage (V_p) with said instantaneous capacitor voltage (V_i), and

- blocking (36) said thyristor-switched capacitors (6) if said step of comparing (35) fulfils a predetermined criteria.

3. The method as claimed in claim 2, wherein said predetermined criteria comprises one or both of following criteria:

- said instantaneous capacitor voltage (V_i) divided by said processed capacitor voltage (V_p) being larger than a factor k

and said instantaneous capacitor voltage (V_i) being larger than a first predetermined value (X), and/or

- said instantaneous capacitor voltage (V_i) being larger than a second predetermined value (Y).

5 4. The method as claimed in claim 2, wherein said step of processing (33) comprises time delaying and/or low-pass filtering said capacitor voltage (V_{cap}).

5. The method as claimed in any of the preceding claims, wherein said method (30) is activated when a voltage
10 measurement in said reactive power compensator (1) has indicated a negative sequence voltage.

6. The method as claimed in any of the preceding claims, wherein said capacitor (8, 9) of said reactive power compensator (1) comprises a capacitor (9) of said thyristor-
15 switched capacitor (6) or a capacitor (8) of a filter device (5) comprised in said reactive power compensator (1).

7. A reactive power compensator (1) comprising means for performing the method as claimed in any of claims 1-6.

8. A control system (8) for controlling a reactive power
20 compensator (1), characterized by means for performing the method as claimed in any of claims 1-6.

9. A computer program product (41) loadable into the internal memory of a computer (40) controlling a reactive power compensator (1), comprising software code portions for
25 carrying out the method as claimed in any of claims 1-6 when said product is run on said computer (40).

10. A computer program product (41) stored on a computer readable storage medium (42), comprising computer readable program code means for causing a computer (40) of a reactive

power compensator (1) to carry out the method as claimed in any of claims 7-12.

1/3

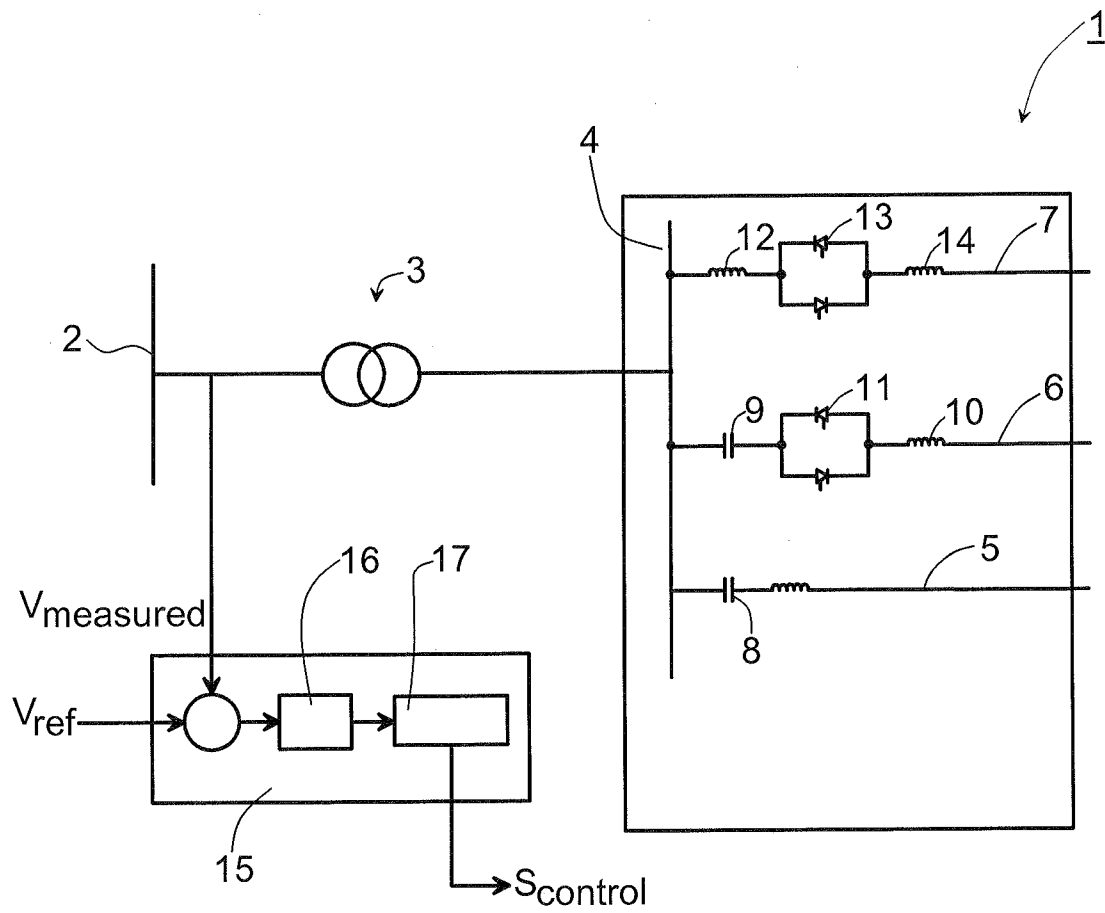


Fig. 1

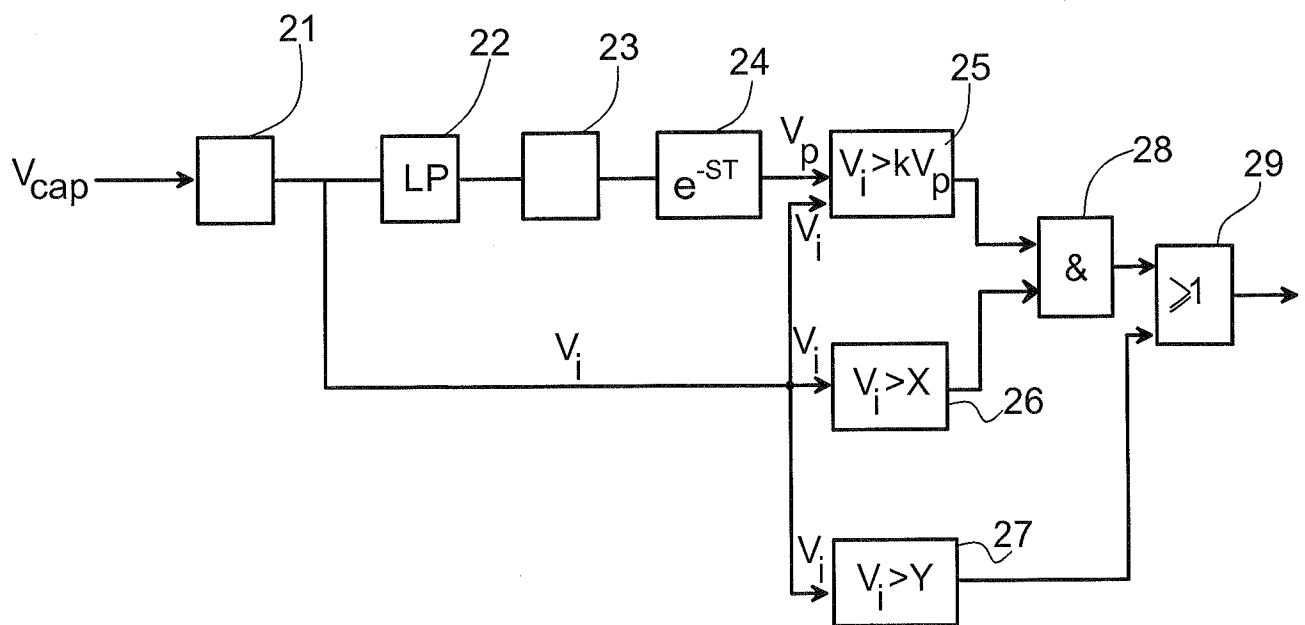


Fig. 2

2/3

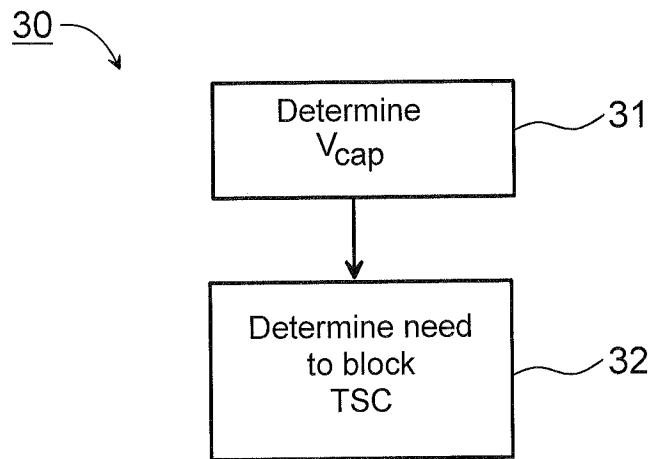


Fig. 3a

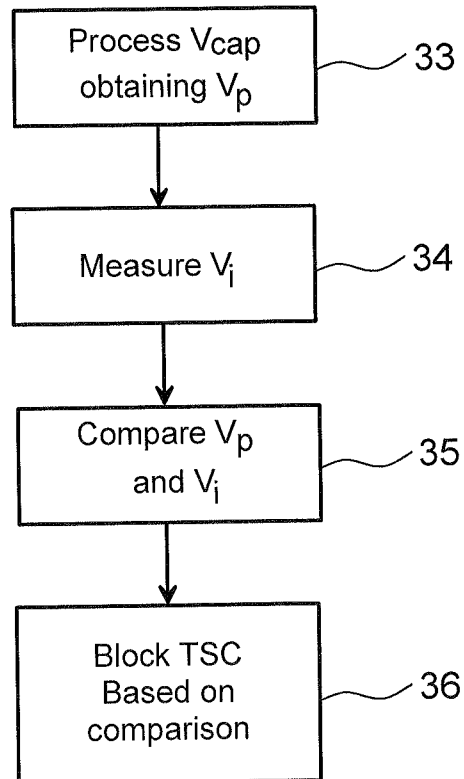


Fig. 3b

3/3

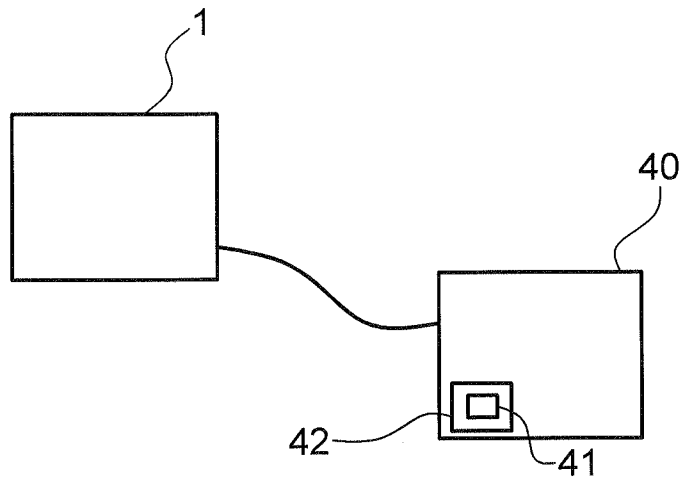


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2009/053060

A. CLASSIFICATION OF SUBJECT MATTER

INV. H02J3/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	AL-MUBARAK A H ET AL: "Preventing voltage collapse by large SVCs at power system faults" POWER SYSTEMS CONFERENCE AND EXPOSITION, 2009. PES '09. IEEE/PES, IEEE, PISCATAWAY, NJ, USA, 15 March 2009 (2009-03-15), pages 1-9, XP031450756 ISBN: 978-1-4244-3810-5 the whole document	1-10
A	US 5 969 509 A (THORVALDSSON BJOERN [SE]) 19 October 1999 (1999-10-19) the whole document	
A	US 2005/194944 A1 (FOLTS DOUGLAS C [US] ET AL) 8 September 2005 (2005-09-08) the whole document	
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

14 January 2010

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Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2009/053060

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>MANDAL S ET AL: "Coordinated capacitor bank switching using SVC controls" POWER AND ENERGY SOCIETY GENERAL MEETING - CONVERSION AND DELIVERY OF ELECTRICAL ENERGY IN THE 21ST CENTURY, 2008 IEEE, IEEE, PISCATAWAY, NJ, USA, 20 July 2008 (2008-07-20), pages 1-7, XP031304327 ISBN: 978-1-4244-1905-0 the whole document</p>	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2009/053060

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