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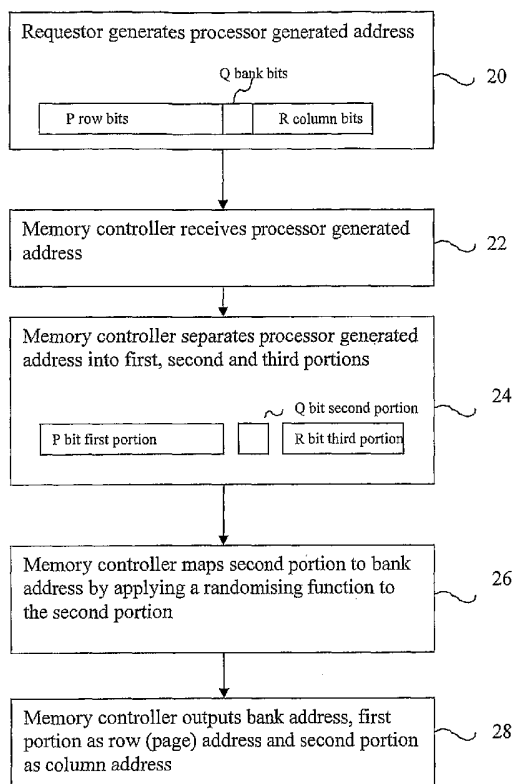
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(54) Title: A MEMORY CONTROLLER



(57) Abstract: A memory controller maps a processor generated address to a banked DRAM address by applying a randomising function which results in the banks appearing in an irregular and non-cyclic order in the conceptual memory map. Incremental addressing by two or more requestors is thereby more evenly distributed amongst the banks of DRAM to improve average access speed.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A Memory Controller

FIELD OF THE INVENTION

5 This invention relates to a memory controller for controlling access to a Random Access Memory (RAM) device and in particular to a memory controller for random bank allocation of a banked RAM device. The invention is particularly suitable for addressing a banked Dynamic RAM (DRAM) device. The method and apparatus have particular application for use with processors running a wide
10 range of applications including 3-d graphics applications and in particular for operations such as reading bit-maps from memory and reading lists of polygons to be rendered.

BACKGROUND OF THE INVENTION

15 Main memory for computers is commonly provided by Dynamic Random Access Memory (DRAM) devices. Each DRAM device consists of a large array of memory capacitors which are arranged in rows and columns. To operate on a memory location in the array a control circuit calculates the row of the location, places the row address on the DRAM's address pins and toggles the address
20 select (RAS) pin causing the DRAM to read the row address. The DRAM connects the selected row to the sense amplifiers. The control circuit then calculates the column of the location, places the column address on the DRAM's address pins, and toggles the Column Address Select (CAS) pin causing the DRAM to read the column address which it uses to select the output of the sense
25 amplifier corresponding to the selected column. Once the control circuit has selected a first row, it can select several columns from the first row by successively placing different column addresses on the address pins and toggling the CAS whilst keeping the first row selected. The resulting access time for successive operations is reduced and the technique is particularly useful for
30 accessing data stored at successive addresses in memory. Hence, access times for addressing further columns in the same row (page) are shorter than access times for addressing a new page. When banking is used, the address of a location in DRAM also incorporates a bank address specifying the bank. Fastest access times are possible when the bank and row addresses are kept constant
35 from one access to the next. If the row address (page) is altered and the bank address kept constant, slowest access results. If the row address is altered and

the bank address is simultaneously altered, there is potential for the access speed to be somewhere between the slowest and fastest access time. Hence when implementing a DRAM addressing system for banked DRAM, it is advantageous to arrange the system such that when a row address is changed, the bank address is likely to change simultaneously. Fast-page access mode is only available if the page can be kept open between memory accesses and a bank is only able to keep one page open for fast-page access. Therefore, a page in a bank can only be kept open if the next memory access to that bank is to another location within the open page or if the next memory access is to a different bank. The restrictions of fast-page access mean that it is only possible to swap between requestors without any access speed slow down if the requestors are each accessing an open page.

Known memory organisations for banked memory include high-order interleave, low-order interleave and some intermediate order interleave systems. A memory system using high-order interleave uses the high order address bits to select a particular bank of memory. Thus, the address bits which specify the bank are placed at the top of the memory map and the bank contains a block of consecutive addresses. Conceptually, the N banks appear as blocks of memory utilising $1/N$ of the address space each. When used with DRAM it makes particular sense to use the intermediate P bits of the processor generated address to address the row (page) of the DRAM and the least significant R bits of the processor generated address as the column address of the DRAM. Figure 1 shows schematically how the conceptual memory map is organised with the banks each occupying $1/4$ of the address space and the pages occupying $1/(N-1)$ of each bank. The column address (not shown in the schematic) would be used to specify a particular column of a page. If multiple processors, or requestors, each use a different bank of memory, all the banks can transfer data simultaneously. When the number of requestors exceeds the number of banks of memory, it becomes difficult to assign requestors to banks to ensure that access speeds are maximised. Assuming four banks specified using 2 bank bits, row addresses of 12 row bits and column addresses of 8 column bits, a high-order interleave system, or most significant bit (msb) addressing mode, would have an address map as follows:

35

AddressMap = Bank[1 downto 0] & Row[11 downto 0] & Column[7 downto 0]

where & is the VHDL concatenate operator.

- 5 In a low-order interleave system, consecutive addresses are placed in alternate banks by using the least significant address bits to specify the bank. A requestor therefore needs to access more than one of the banks as it executes its program or transfers data. When low-order interleave is employed, reading a number of consecutive locations in the memory map cycles through the same number of
- 10 banks and hence one requestor may effectively lock open a page for each bank preventing other requestors from achieving fast memory access. Low-order interleave can, therefore, result in a memory conflict if two requestors request simultaneous access to the same bank of memory.
- 15 Intermediate-order interleave systems can also be designed. By designing an appropriate intermediate-order interleave system, it is possible for a number of requestors each to keep a page open as long as the pages map into different banks. For a memory arranged into N banks, it is possible for N requestors each to have a page open in one of the N banks and hence intermediate-order
- 20 interleave can be particularly useful in a system with a plurality of requestors. For DRAM with banking, a particularly useful address map is one in which the most significant bits specify the row (page) address, the intermediate bits specify the bank address and the least significant bits specify the column address. This type of interleaving, which we term least significant bit (lsb) addressing, places
- 25 consecutive addresses in the same bank for a whole page, then changes bank at the end of the page. Figure 2a shows schematically how the conceptual memory map is organised with the pages each occupying $1/(N-1)$ of the address space and the banks occupying $1/4$ of each page. The column address (not shown in the schematic) would be used to specify a particular column of a page in a
- 30 particular bank. The order that the banks appear in the conceptual memory map is the same for each page in lsb addressing. When lsb addressing is used, instead of carefully trying to place requestors in different banks, the aim is to randomise the placement of requestors in banks.

For example consider the lsb addressing mode where the most significant P bits of the address map are used to specify the row address, the next most significant Q bits of the address map are used to specify the bank address and the least most significant R bits are used to specify the column address. Assuming a four
5 bank system requiring Q=2 bank bits, and row and column addresses having respectively P=12 row bits and R=8 column bits, the memory map will cycle through the four banks (0,1,2,3) every 32KB (assuming an 8KB row (or page)). The conceptual address map for the lsb addressing mode is:

10 AddressMap= Row[11 downto 0] & Bank[1 downto 0] & Column[7 downto 0]

This intermediate-order interleave system is designed to change bank each page which helps to ensure fast access speeds.

15 SUMMARY OF THE INVENTION

We have appreciated that a problem with lsb addressing is that there is at least one common memory access pattern that results in a slow overall memory access speed due to the need to access consecutively different row addresses in
20 the same bank. This can occur when more than one requestor (processor, device or the like) requires access to consecutive addresses in the memory, a second requestor likewise requires access to consecutive addresses in the memory and both requestors happen to require access to the same bank. As the two requestors increment the addresses they are accessing, the location being
25 addressed in the DRAM repeatedly falls in the same bank and the access time is maximised resulting in poor overall performance.

We have appreciated that this problem is due to the cyclic nature of the order that the banks appear in the conceptual memory map. By memory map we mean the
30 table that relates processor generated addresses arranged in ascending or descending order to a corresponding row, bank and column address of a banked RAM device. By "conceptual" we mean that the conceptual memory map may never physically exist as a look-up table, list or the like; a row, bank and column address may be generated on-the-fly by applying a suitable mapping function to
35 processor generated address. We have appreciated that by substantially

randomising the order in which the banks appear in the conceptual memory map, the problem can be ameliorated. By randomising the order in which the banks appear in the conceptual memory map we mean arranging the conceptual memory map such that the order of the banks at a first row (page) address is
5 randomly different from that at a second and subsequent row addresses. Although the order of banks may have to be repeated for more than one page (assuming the number of banks to be small compared to the number of pages) the random way in which the bank order is repeated means that two requestors consecutively addressing the memory and happening to address the same bank
10 at one stage in the addressing are unlikely to continue sequentially to access the same bank as they increment their addressing.

The invention is defined in the claims to which reference is now directed.

15

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 is a schematic showing high-order interleave applied to a banked
20 memory;

Figure 2a is a schematic showing an intermediate-order interleave applied to a banked memory;

25 Figure 2b is a schematic showing the randomised least significant bit addressing mode applied to a banked memory in accordance with the invention;

Figure 3 is schematic diagram of a computer system in accordance with the
invention;

30

Figure 4 is schematic flow-chart showing mapping of the processor generated address to a bank, row and column address in accordance with a preferred embodiment of the invention; and

Figure 5 is a schematic diagram showing in more detail the configuration of the memory controller in accordance with a preferred embodiment of the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

- 5 The invention is based on the appreciation that by using intermediate-order interleaving and forcing the order of the banks in the conceptual memory map to be irregular and non-cyclic, the average access speed of memory can be improved for a multiple requestor computer system. We term this randomised lsb addressing. Figure 2b shows schematically how the conceptual memory map
- 10 is organised with the highest order bits specifying the row (page) address and each page occupying $1/(N-1)$ of the address space, the next most significant bits specifying the bank with each bank occupying $1/4$ of each page address space. The column address (not shown in the schematic) would be used to specify a particular column of a page. Of particular note is the fact that the order that the
- 15 banks appear is random and hence differs between pages.

- It will be immediately apparent to the skilled man that any number of randomising functions could be used to implement randomised lsb addressing. Any function which, when applied, maps the bits used to specify the bank in an uncorrelated
- 20 manner so that the result is a random order of banks in the conceptual memory map would meet the requirements of the randomised lsb addressing scheme. In the presently preferred embodiment, a portion of the processor generated address is used to generate the randomising function.

- 25 Figure 3 shows a computer system 10 comprising a plurality of requestors 12a, 12b, ..., 12c, a memory controller 14 and a memory 16 comprising four banks of DRAM 18a, 18b, 18c and 18d. The requestors 12 are coupled to the memory controller 14. The requestors 12 may be separate processors or devices. The requestors 12 input processor generated addresses to the memory controller 14
- 30 and may transfer data to memory or receive data from memory via the memory controller 14. The memory controller 14 is coupled to each of the banks of DRAM 18a, 18b, 18c and 18d and outputs DRAM addresses comprising row, bank and column addresses to the DRAM. The memory controller 14 may receive data from a DRAM bank or cause data to be written to a DRAM bank.
- 35 The timing and addressing protocols required for reading from and writing to a

DRAM device are provided by the memory controller 14 and are not discussed here in detail. A function of the memory controller 14 is to take a processor generated address and map it into a DRAM address by applying a randomising function which results in the banks appearing in an irregular and non-cyclic order in the conceptual memory map. Incremental addressing by two or more requestors is thereby more evenly distributed amongst the banks of RAM to improve average access speed by reducing conflicts generated when two separate processors attempt to access the same bank but a different row of DRAM.

10

Figure 4 is a flowchart showing a preferred method of mapping the processor generated address into bank, row and column addresses for the banked DRAM. A requestor generates a processor generated address 20. The memory controller receives the processor generated address 22 and separates the processor generated address into three portions, the first portion relating to the row address, the second portion relating to the bank and the third portion relating to the column address 24. The P most significant bits of the processor generated address are used as the first portion and are directly used to specify the row address of DRAM. In the presently preferred embodiment, P=12 and the twelve most significant bits of the processor generated address are used as the row address. The third portion is formed by taking the R least significant bits of the processor generated address. In the presently preferred embodiment the eight least significant bits of the processor generated address are used directly as the column address of DRAM. In order to achieve the randomisation of the bank order in the conceptual memory map, the intermediate Q bits (that is the Q next most significant bits after the P most significant bits of the processor generated address) are used to generate a bank address to select the bank of DRAM. In the presently preferred embodiment, there are four banks of DRAM and Q=2. The memory controller 14 is configured to map the second portion to a bank address by applying a randomising function to the second portion 26, the application of the randomising function having the effect of randomising the order in which the banks occur in the conceptual memory map relating the addresses generated by the processor to the addresses of the RAM device. The memory controller outputs the bank address, row (page) address and column address 28

in accordance with the timing and addressing protocols required by the particular DRAM device.

In the presently preferred embodiment, the bank address is formulated using both
 5 the bits of the processor generated address used to specify the row and also the
 Q next most significant bits (or bank bits of the processor generated address).
 The R bit third portion 34 is used as the column address and is not used in the
 randomising function in the presently preferred embodiment. Figure 5 shows
 schematically more detail of the configuration of the memory controller 14. The
 10 bits used for specifying the row (the most significant P bits of the processor
 generated address) 30 are taken and applied as an input to a randomiser 36.
 The randomiser 36 maps the input to an uncorrelated, but reproducible, output
 producing a randomising function. In the presently preferred embodiment, the
 randomiser 36 is based on the "Lucifer" encryption system and is basically a
 15 cascade of 4 bit lookup tables and exclusive-or gates. The steps performed by
 the randomiser 36 are (i) taking each nibble of the input word and putting them
 through one of two 4-bit look-up tables, (ii) XORing the results of the look-up
 tables and (iii) XORing the top 2 bits of the result with the bottom 2 bits. A
 suitable randomiser may be implemented by the following C code:

```

20  UINT32 SboxRandSimple(UINT32 Seed)
    {

25      UINT32 Sbox0[]={12, 15, 7, 10, 14, 13, 11, 0, 2, 6, 3, 1, 9,
        4, 5, 8};
        UINT32 Sbox1[]={7, 2, 14, 9, 3, 11, 0, 4, 12, 13, 1, 10, 6,
        15, 8, 5};

30      UINT32 Stage1[8];
        UINT32 Stage2;

        UINT32 Result;

35      Stage1[0]=Sbox0[Seed & 0xF];
        Stage1[1]=Sbox1[(Seed>>4) & 0xF];
        Stage1[2]=Sbox0[(Seed>>8) & 0xF];
        Stage1[3]=Sbox1[(Seed>>12) & 0xF];
        Stage1[4]=Sbox0[(Seed>>16) & 0xF];
40      Stage1[5]=Sbox1[(Seed>>20) & 0xF];
        Stage1[6]=Sbox0[(Seed>>24) & 0xF];
        Stage1[7]=Sbox1[(Seed>>28) & 0xF];
  
```

```

        Stage2=Stage1[0] ^ Stage1[1] ^ Stage1[2] ^ Stage1[3]
                ^ Stage1[4] ^ Stage1[5] ^ Stage1[6] ^ Stage1[7];

5      Result=(Stage2 & 3) ^ (Stage2 >>2);

        return(Result);
10    }

```

The randomising function is applied by supplying the output of the randomiser 36 as one of two inputs to an exclusive-or gate 38, the second input to the exclusive-or being the Q bank bits of the processor generated address 32. The output of the exclusive-or 38 is used as the bank address to select the bank. The resulting order of banks in the conceptual memory map is substantially randomised. For example, with four banks the order may be of the type [0 3 2 1], [1 0 2 3], [3 1 0 2] and so on in a substantially non-repeating, irregular way. This fulfils the requirement that the order in which the banks appear in the conceptual memory map is irregular and prevents the cyclic ordering which can result in slow memory access.

The conceptual address map for the randomised lsb addressing mode is shown schematically in figure 2b and can be expressed as:

AddressMap= Row[11 downto 0] & Bank[randomised function of first and second portions of the processor generated address] & Column[7 downto 0]

Whilst the mapping of the bank bits to a bank address has been described in terms of a hardware solution, the mapping could be implemented in software. For example, a look up table could be used in which the most significant bits of the processor generated address (relating to the row address) could be used to access a row of the look up table and the next most significant bits to access a column of the table which would yield a bank address which met the required random order criterion. Other software and/or hardware implementations are within the implementation abilities of the skilled man.

With respect to the above description, it is to be realised that equivalent apparatus and methods are deemed readily apparent to one skilled in the art, and

- all equivalent apparatus and methods to those illustrated in the drawings and described in the specification are intended to be encompassed by the present invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact
- 5 construction and operation shown and described, and accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention. It should be noted that features described at different points of the description may be used in combinations other than those particularly described or shown.

CLAIMS

1. A computer system comprising a processor, a banked random access
5 memory (RAM) device and a memory controller, the memory controller being
coupled to the processor and to the banked random access memory device and
being configured to map an address generated by the processor to a RAM
address specifying a bank, row and column of a memory location in the RAM
device, wherein the memory controller is configured to:
- 10 a) receive a processor generated address;
b) separate the processor generated address into a first portion relating to a
row, a second portion relating to a bank, and a third portion relating to a column;
c) use the first portion and third portion respectively as the row and column
addresses of the RAM device;
- 15 d) map the second portion to a bank address by applying a randomising
function to the second portion, application of the randomising function having the
effect of substantially randomising the order in which the banks occur in the
conceptual memory map relating the addresses generated by the processor to
the addresses of the RAM device;
- 20 e) output the row, bank and column addresses to the RAM device.
2. A computer system according to claim 1, wherein the memory controller is
configured to use the P most significant bits of the processor generated address
as the first portion, the Q next most significant bits of the processor generated
25 address as the second portion and the R least significant bits of the processor
generated address as the third portion.
3. A computer system according to either claim 1 or claim 2, wherein the
memory controller is configured in hardware.
- 30 4. A computer system according to either claim 1 or claim 2, wherein the
memory controller is configured in software.
5. A computer system according to any of the preceding claims, wherein the
35 banked RAM device is banked DRAM.

6. A computer system according to any of the preceding claims, wherein the memory controller is configured to use the processor generated address to generate the randomising function.
- 5
7. A computer system according to claim 6, wherein the memory controller is configured to use part of the processor generated address to generate the randomising function.
- 10
8. A computer system according to claim 7, wherein the memory controller is configured to use the first portion of the processor generated address to generate the randomising function.
9. A computer system according to any of the preceding claims, wherein the
- 15 memory controller is configured to apply the randomising function by performing an exclusive-or operation on the randomising function and the second portion of the processor generated address.
10. A memory controller for mapping an address generated by a processor to
- 20 a RAM address, the memory controller being configured to:
- (i) receive an address from a processor, the address relating to a portion of memory to be accessed;
 - (ii) separate the address into a first portion relating to a row address of a RAM device, a second portion relating to a bank address of a RAM device, and a
 - 25 third portion relating to a column address of a RAM device;
 - (iii) map the second portion to a bank address by applying a randomising function to the second portion, application of the randomising function having the effect of substantially randomising the order in which the banks of the RAM device occur in the conceptual memory map relating the addresses received from
 - 30 the processor to the memory location to be accessed in the RAM device;
 - (iv) output to a RAM device the first portion as a row address, the third portion as a column address and the mapped second portion as a bank address.
11. A memory controller according to claim 10, configured to use the P most
- 35 significant bits of the processor generated address as the first portion, the Q next

most significant bits of the processor generated address as the second portion and the R least significant bits of the processor generated address as the third portion.

5 12. A memory controller according to either claim 10 or claim 11, configured to use the processor generated address to generate the randomising function.

13. A memory controller according to claim 12, configured to use part of the processor generated address to generate the randomising function.

10

14. A memory controller according to claim 13, configured to use the first portion of the processor generated address to generate the randomising function.

15 15. A memory controller according to any of claims 10 to 14, configured to apply the randomising function by performing an exclusive-or operation on the randomising function and the second portion of the processor generated address.

20 16. A method of accessing a memory location in a RAM device configured as a plurality of banks, each bank comprising an array of rows and columns, the method comprising the steps of:

- a) receiving a first address generated by a processor;
- b) separating the first address into a first portion relating to a row, a second portion relating to a bank, and a third portion relating to a column;
- 25 c) using the first portion and third portion respectively as the row and column addresses of the RAM device;
- d) mapping the second portion to a bank address by applying a randomising function to the second portion, the application of the randomising function having the effect of substantially randomising the order in which the banks occur in the
- 30 conceptual memory map relating the addresses generated by the processor to the RAM device addresses;
- e) accessing the memory location of the RAM device identified by the row, bank and column addresses.

17. A method according to claim 16 wherein step (b) is performed on a first address of length (P+Q+R) bits and comprises performing the following operations in any order:
- 5 (i) separating the P most significant bits of the first address to form the first portion;
 - (ii) separating the intermediate Q bits of the first address to form the second portion, the intermediate Q bits being located in the first address between the P most significant bits and R least significant bits; and
 - 10 (iii) separating the R least significant bits of the first address to form the third portion.
18. A method according to either claim 16 or claim 17, further comprising the steps:
- f) receiving a second address generated by a second processor;
 - 15 g) separating the second address into a first portion relating to a row, a second portion relating to a bank, and a third portion relating to a column;
 - h) using the first portion and third portion respectively as the row and column addresses of the second processor access to RAM device;
 - i) mapping the second portion generated in step (g) to a bank address for
20 the second processor access to RAM device by applying a randomising function to the second portion, the application of the randomising function having the effect of substantially randomising the order in which the banks occur in the conceptual memory map relating the addresses generated by the processor to the RAM device addresses;
 - 25 e) accessing the memory location of the RAM device required by the second processor and identified by the row, bank and column addresses generated in steps (f) to (j), whereby when the first and second processors successively increment the first and second addresses the likelihood of the same bank being repeatedly addressed by both processors is reduced.
 - 30
19. A method according to any of claims 16 to 18, wherein the randomising function is generated using the processor generated address.
20. A method according to claim 19, wherein the randomising function is
35 generated using part of the processor generated address.

21. A method according to claim 20, wherein the randomising function is generated using the first portion of the processor generated address.
- 5 22. A method according to any of claims 16 to 21, wherein the randomising function is applied to the second portion by performing an exclusive-or operation on the randomising function and the second portion of the processor generated address.
- 10 23. A computer which in operation performs the steps of any of method claims 16 to 22.
24. A computer system substantially as hereinbefore described with reference to any of figures 2b to 5 of the drawings.
- 15 25. A memory controller substantially as hereinbefore described with reference to any of figures 2b to 5 of the drawings.

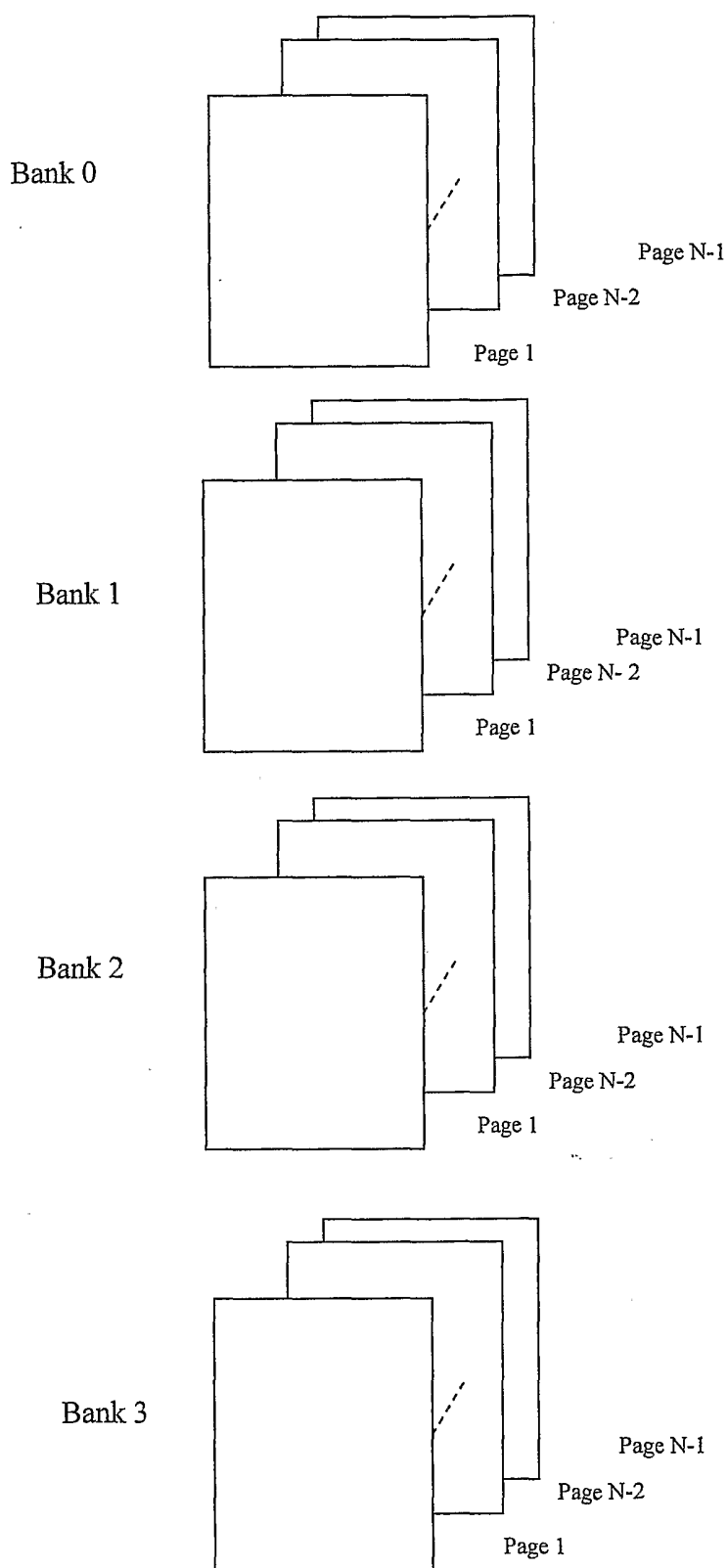


Fig 1

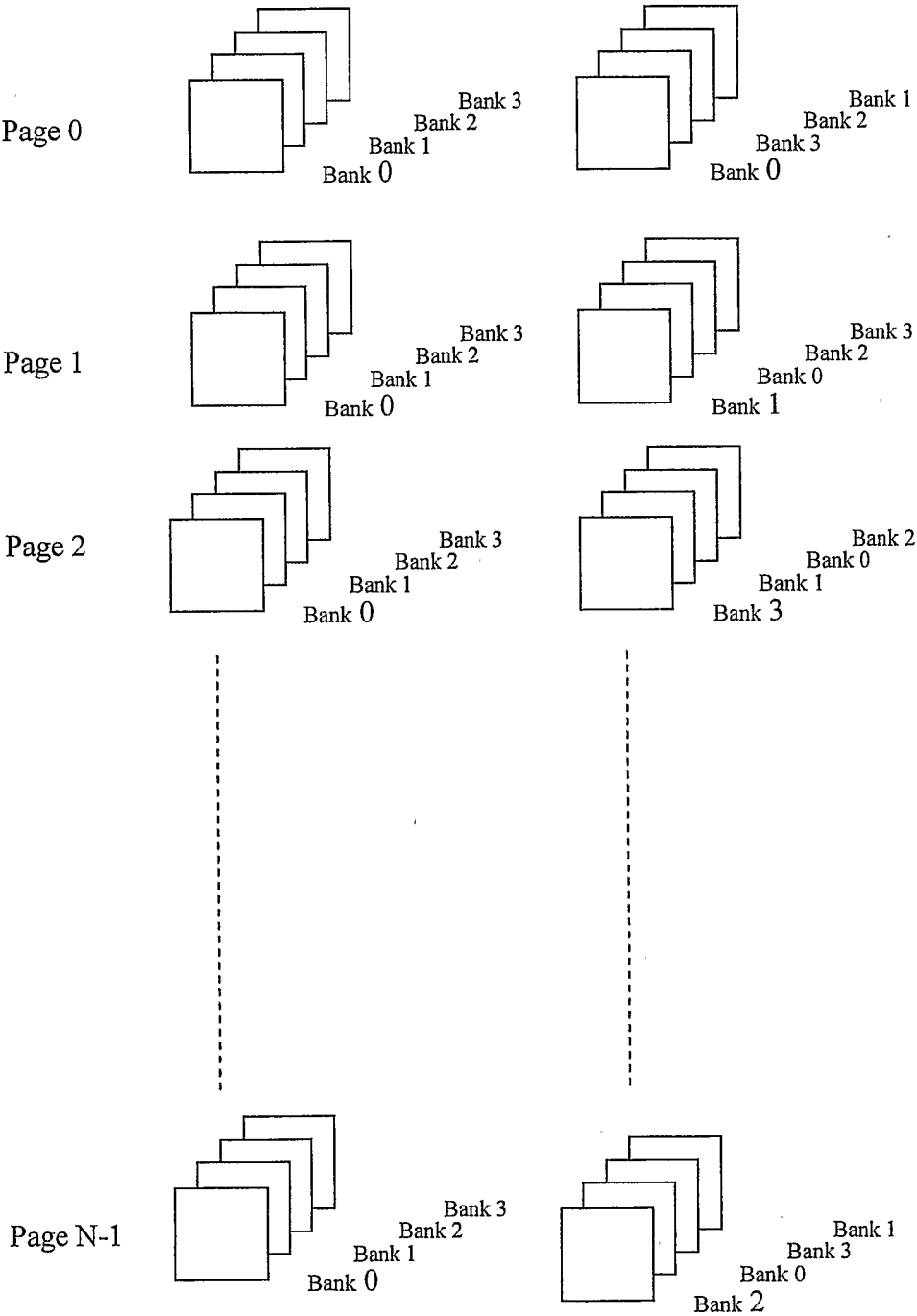


Fig 2a

Fig 2b

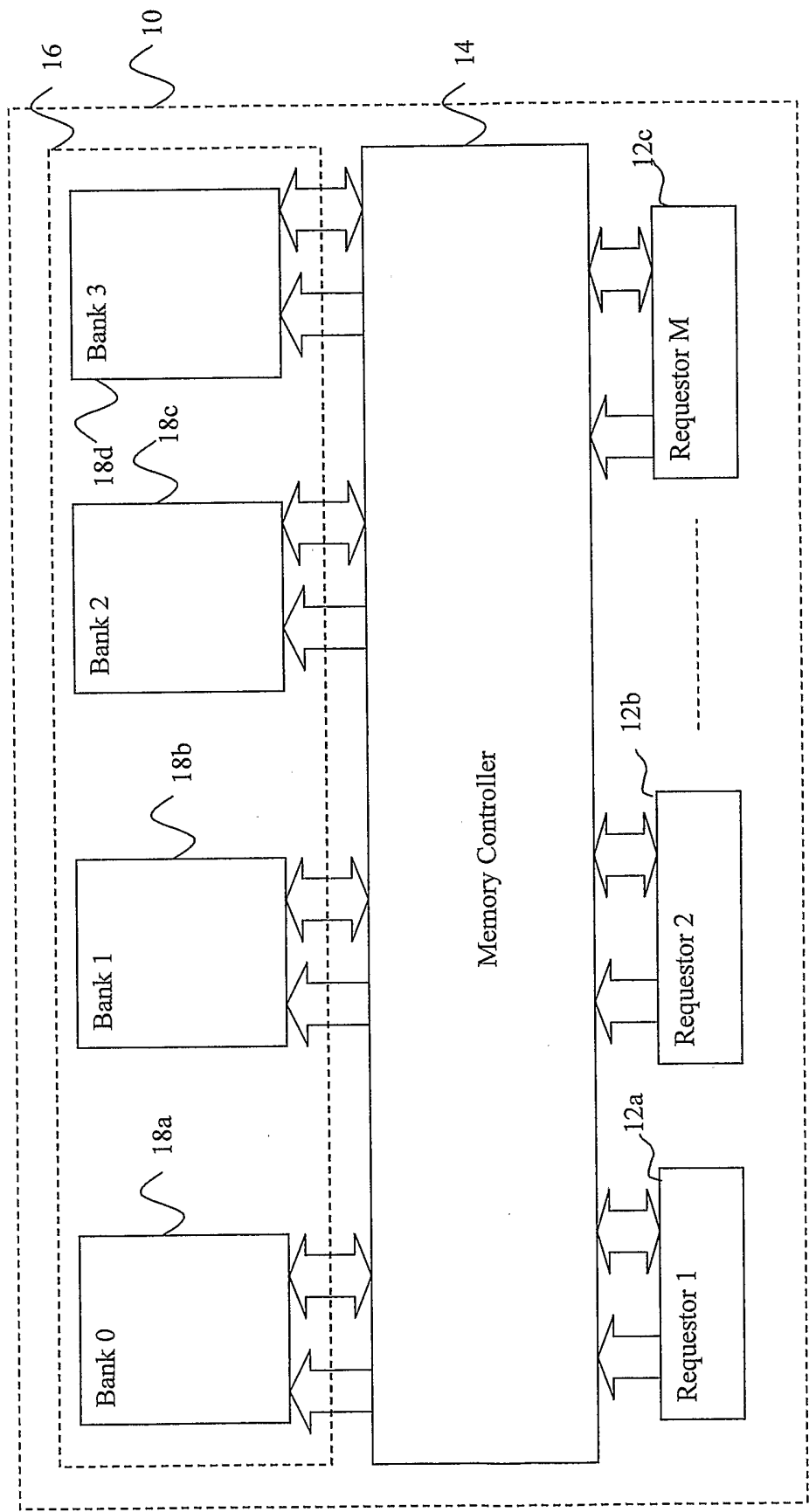


Fig 3

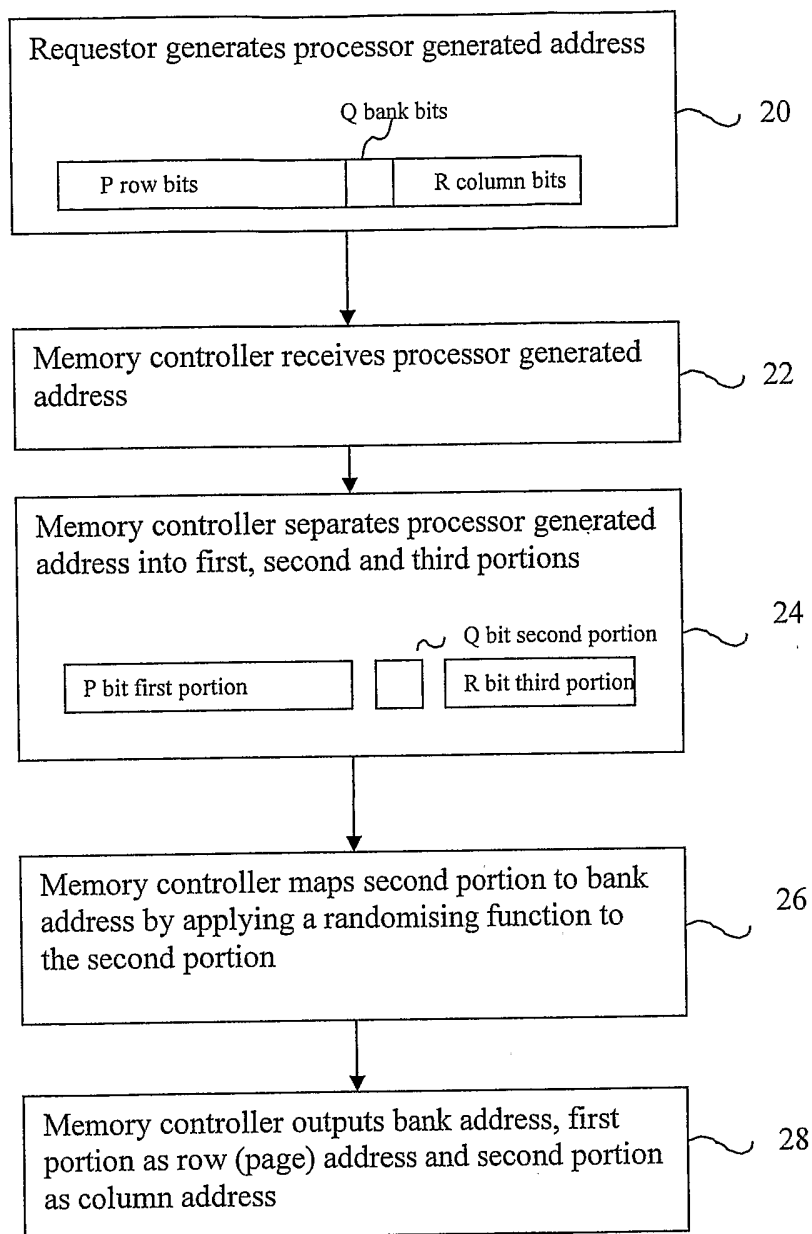


Fig 4

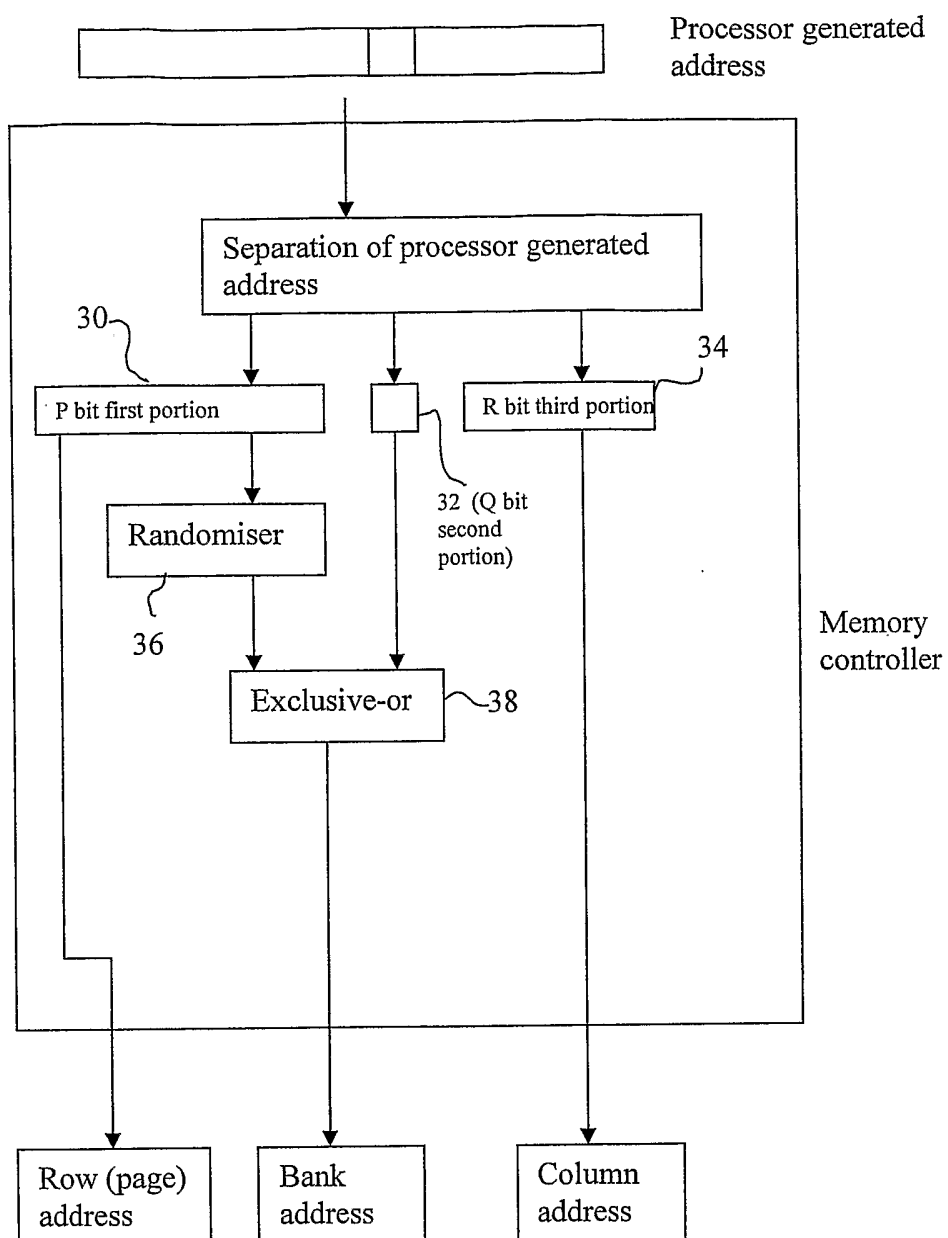


Fig 5

INTERNATIONAL SEARCH REPORT

PCT/GB2005/003153

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F12/02 G11C8/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/133730 A1 (HARRAND MICHEL ET AL) 8 July 2004 (2004-07-08) figures 1,2 paragraph '0009! - paragraph '0010! paragraph '0048! - paragraph '0049! paragraph '0067! -----	1-23

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

28 October 2005

Date of mailing of the international search report

07/11/2005

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INTERNATIONAL SEARCH REPORT

PCT/GB2005/003153

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☒ Claims Nos.: 24, 25
because they relate to subject matter not required to be searched by this Authority, namely:
The subject-matter of claims 24 and 25 relates to figures without mentioning the technical features of the invention and therefore these claims are not allowable according to Article 6 and Rule 6.2.a, and 6.3.a PCT.
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

Information on patent family members

PCT/GB2005/003153

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004133730	A1	08-07-2004	NONE