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(54) Title: QUANTUM DOT DEVICES

(57) Abstract: Quantum dot devices, and related systems and methods, are disclosed herein. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gate lines above the quantum well stack; a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines; and an array of regularly spaced magnet lines.

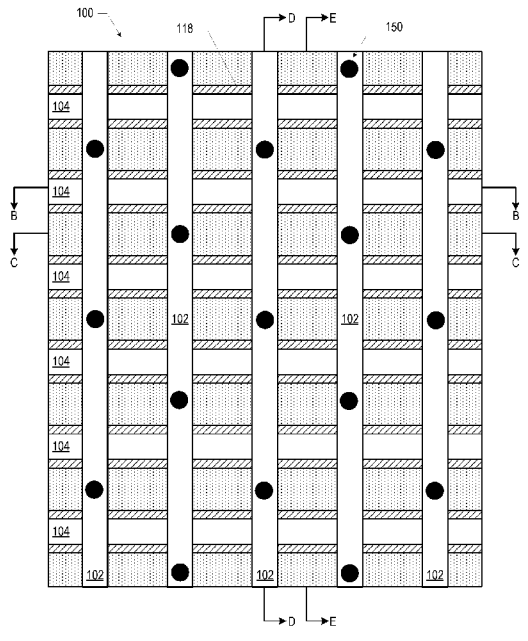


FIG. 1A

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QUANTUM DOT DEVICES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1A-E are various views of a quantum dot device, in accordance with various embodiments.

[0004] FIGS. 2A-U illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0005] FIG. 3 is a view of a quantum dot device, in accordance with various embodiments.

[0006] FIGS. 4A-D are various views of a quantum dot device, in accordance with various embodiments.

[0007] FIGS. 5A-C illustrate various example dimensions of a quantum dot device, in accordance with various embodiments.

[0008] FIGS. 6A-C illustrate various electrical configurations that may be used to perform quantum operations on a quantum dot device, in accordance with various embodiments.

[0009] FIG. 7 illustrates an interconnect arrangement for a quantum dot device, in accordance with various embodiments.

[0010] FIGS. 8A-C are various views of a quantum dot device with a magnetic field grating, in accordance with various embodiments.

[0011] FIGS. 9A-C are various views of a quantum dot device with another magnetic field grating, in accordance with various embodiments.

[0012] FIGS. 10A-C are various views of a quantum dot device with another magnetic field grating, in accordance with various embodiments.

[0013] FIGS. 11A-C are various views of a quantum dot device with another magnetic field grating, in accordance with various embodiments.

[0014] FIGS. 12A-C are various views of a quantum dot device with another magnetic field grating, in accordance with various embodiments.

[0015] FIGS. 13A-C are various views of a quantum dot device with another magnetic field grating, in accordance with various embodiments.

[0016] FIGS. 14A-C are various views of a quantum dot device having a sparser array of quantum dot gates than the quantum dot device of FIG. 1, in accordance with various embodiments.

[0017] FIG. 15 is a top view of another quantum dot device having a sparser array of quantum dot gates than the quantum dot device of FIG. 1, in accordance with various embodiments.

[0018] FIGS. 16A-B illustrate quantum dot devices with elements at opposite faces of a quantum well stack, in accordance with various embodiments.

[0019] FIGS. 17A-H illustrate various embodiments of a quantum well stack that may be included in a quantum dot device, in accordance with various embodiments.

[0020] FIG. 18 shows top views of a wafer and dies that may include any of the quantum dot devices disclosed herein.

[0021] FIG. 19 is a cross-sectional side view of a device assembly that may include any of the quantum dot devices disclosed herein.

[0022] FIG. 20 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0023] Quantum dot devices, and related systems and methods, are disclosed herein. In some embodiments, a quantum dot device may include a quantum well stack; a plurality of first gate lines above the quantum well stack; a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines; and an array of regularly spaced magnet lines.

[0024] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0025] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be

practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0026] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments. Terms like "first," "second," "third," etc. do not imply a particular ordering, unless otherwise specified.

[0027] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0028] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide.

[0029] The disclosure may use the singular term "layer," but the term "layer" should be understood to refer to assemblies that may include multiple different material layers. The accompanying drawings are not necessarily drawn to scale. For ease of discussion, all the lettered sub-figures associated with a particular numbered figure may be referred to by the number of that figure; for example, FIGS. 1A-E may be referred to as "FIG. 1," FIGS. 2A-U may be referred to as "FIG. 2," etc.

[0030] FIGS. 1A-E are various views of a quantum dot device 100, in accordance with various embodiments. FIG. 1A is a top view of a portion of the quantum dot device 100 with some of the materials removed so that the quantum dot gate lines and barrier gate lines 104 are visible. Although many of the drawings and description herein may refer to a particular set of lines or gates as "barrier" or "quantum dot" lines or gates, respectively, this is simply for ease of discussion, and in other embodiments, the role of "barrier" and "quantum dot" lines and gates may be switched (e.g.,

barrier gates may instead act as quantum dot gates, and vice versa). FIGS. 1B-E are side cross-sectional views of a quantum dot device 100; in particular, FIG. 1B is a view through the section B-B of FIG. 1A, FIG. 1C is a view through the section C-C of FIG. 1A, FIG. 1D is a view through the section D-D of FIG. 1A, and FIG. 1E is a view through the section E-E of FIG. 1A.

[0031] As used herein, during operation of the quantum dot device 100, electrical signals (e.g., voltages, radio frequency (RF), and/or microwave signals) may be provided to a quantum dot gate (and neighboring gates) to cause a quantum dot (e.g., an electron spin-based quantum dot) to form in a quantum well stack 146 under the quantum dot gate. Electrical signals (e.g., voltages, RF, and/or microwave signals) may be provided to a barrier gate to control the potential energy barrier between adjacent quantum dots.

[0032] In the quantum dot device 100 of FIG. 1, a gate dielectric 114 is disposed on a quantum well stack 146. A quantum well stack 146 may include at least one quantum well layer 152 (not shown in FIG. 1, but discussed below) in which quantum dots may be localized during operation of the quantum dot device 100; examples of quantum well stacks 146 are discussed below with reference to FIG. 17. The gate dielectric 114 may be any suitable material, such as a high-k material. Multiple parallel barrier gate lines 104 are disposed on the gate dielectric 114, and spacer material 118 is disposed on side faces of the barrier gate lines 104. In some embodiments, a patterned hardmask 110 may be disposed on the barrier gate lines 104 (with the pattern corresponding to the pattern of the barrier gate lines 104), and the spacer material 118 may extend up the sides of the hardmask 110, as shown. In some embodiments, an additional hardmask 112 may be disposed on the hardmask 110 (such that there are two hardmasks above the barrier gate lines 104), and this additional hardmask 112 may be patterned as illustrated in FIG. 1D to extend over adjacent pairs of barrier gate lines 104. As shown in FIGS. 1B and 1D, in some embodiments, additional insulating material 128 (e.g., an interlayer dielectric (ILD)) may be disposed on this additional hardmask 112. In some embodiments, insulating material 128 (e.g., an ILD) may be disposed between the two hardmasks 110 and 112. The barrier gate lines 104may provide barrier gates during operation of the quantum dot device 100, as discussed below. Different ones of the barrier gate lines 104 may be separately electrically controlled.

[0033] Multiple parallel quantum dot gate lines 102 may be disposed over the multiple parallel barrier gate lines 104. As illustrated in FIG. 1A, the quantum dot gate lines 102 may be arranged perpendicular to the barrier gate lines 104. As illustrated in FIG. 1D, the area between adjacent pairs of barrier gate line 104/spacer material 118 structures may be alternatingly filled with an insulating material 128 (e.g., an ILD) and the quantum dot gate lines 102. The quantum dot gate lines 102 may extend over the additional hardmask 112 and additional insulating material 128 above the barrier

gate lines 104, and may extend down into the space between adjacent ones of the barrier gate line 104/spacer material 118 structures. The metal of the quantum dot gate lines 102 that extends between adjacent ones of the barrier gate line 104/spacer material 118 structures may provide a quantum dot gate 150 during operation of the quantum dot device 100 such that quantum dots form in the quantum well stack 146 below the quantum dot gates 150, as discussed below. The quantum dot gates 150 may alternate with stubs 122 that do not extend as far toward the quantum well stack 146, as shown. Multiple ones of the quantum dot gates 150 in a quantum dot gate line 102 are electrically continuous due to the continuous metal of the quantum dot gate lines 102 over the barrier gates 160; different ones of the quantum dot gate lines 102 may be separately electrically controlled. As illustrated in FIGS. 1B and 1C, upper portions of the quantum dot gate lines 102 may have spacer material 118 disposed on the top and side faces. Different portions of the quantum dot gate lines 102 may also have gate dielectric 114 disposed on the bottom and side faces, as shown.

[0034] Although FIG. 1 illustrates a particular number of quantum dot gate lines 102 and barrier gate lines 104, this is simply for illustrative purposes, and any number of quantum dot gate lines 102 and barrier gate lines 104 may be included in a quantum dot device 100. Other examples of quantum dot gate line 102 and barrier gate line 104 arrangements are discussed below with reference to FIGS. 3, 4, and 6-8. Electrical interconnects (e.g., vias and conductive lines) may contact the quantum dot gate lines 102 and barrier gate lines 104 in any desired manner; some example arrangements are discussed below with reference to FIG. 7. Examples of methods of performing quantum operations with the quantum dot device 100 of FIG. 1 (or similar devices) are discussed below with reference to FIGS. 6A-C.

[0035] Not illustrated in FIG. 1, but illustrated in FIG. 4, are accumulation regions 162 that may be electrically coupled to the quantum well layer of the quantum well stack 146. The accumulation regions 162 may be regions in which carriers accumulate (e.g., due to doping, or due to the presence of large electrodes that pull carriers into the quantum well layer), and may serve as reservoirs of carriers that can be selectively drawn into the areas of the quantum well layer under the quantum dot gates (e.g., by controlling the voltages on the quantum dot gates 150 and the barrier gates 160) to form carrier-based quantum dots (e.g., electron or hole quantum dots). The accumulation regions 162 may be spaced apart from the gate lines by a thin layer of an intervening dielectric material (not shown). In other embodiments (e.g., as discussed below with reference to FIG. 17), a quantum dot device 100 may not include lateral accumulation regions 162, but may instead include doped layers within the quantum well stack 146. These doped layers may provide the carriers to the quantum well layer. Any combination of accumulation regions 162 (e.g., doped or non-doped) or doped layers

in a quantum well stack 146 may be used in any of the embodiments of the quantum dot devices 100 disclosed herein.

[0036] FIGS. 2A-U illustrate various example stages in the manufacture of a quantum dot device 100, in accordance with various embodiments. The views illustrated in FIGS. 2A-H are taken along the cross section of FIG. 1D, the view illustrated in FIG. 2I is a top view similar to the top view of FIG. 1A, and the views illustrated in FIGS. 2J-U are taken along the cross section of FIG. 1C.

[0037] FIG. 2A illustrates an assembly including a quantum well stack 146, a gate dielectric 114 disposed on the quantum well stack 146, a barrier gate metal 108 disposed on the gate dielectric 114, a hardmask 110 disposed on the barrier gate metal 108, a template material 132 disposed on the hardmask 110, and a patterned photoresist 130 disposed on the template material 132. The photoresist 130 may be any suitable material, and may be patterned using any suitable technique. In some embodiments, the template material 132 may be amorphous silicon, or any other suitable material.

[0038] FIG. 2B illustrates an assembly subsequent to patterning the template material 132 of the assembly of FIG. 2A in accordance with the pattern of the photoresist 130, then removing the photoresist 130. Any suitable etch process may be used to pattern the template material 132.

[0039] FIG. 2C illustrates an assembly subsequent to providing spacer material 134 on side faces of the patterned template material 132 of the assembly of FIG. 2B. The spacer material 134 of FIG. 2C may be formed by depositing a conformal layer of the spacer material 134 over the patterned template material 132, then performing a directional etch to etch the spacer material 134 "downward," leaving the spacer material 134 on the sides of the patterned template material 132. The spacer material 134 may be an insulating material, for example.

[0040] FIG. 2D illustrates an assembly subsequent to removing the template material 132 from the assembly of FIG. 2C. The template material 132 may be removed using any suitable etch process.

[0041] FIG. 2E illustrates an assembly subsequent to etching the hardmask 110 and the barrier gate metal 108 of the assembly of FIG. 2D in accordance with the pattern provided by the spacer material 134 (i.e., the hardmask 110 and barrier gate metal 108 not masked by the spacer material 134 may be removed) to form barrier gate lines 104. Any suitable etch process may be used to pattern the hardmask 110 and the barrier gate metal 108. In some embodiments, as shown, the etch may stop at the gate dielectric 114, while in other embodiments, the etch may continue through the gate dielectric 114.

[0042] FIG. 2F illustrates an assembly subsequent to removing the spacer material 134 of the assembly of FIG. 2E. Any suitable technique may be used.

[0043] FIG. 2G illustrates an assembly subsequent to providing spacer material 118 on side faces of the patterned hardmask 110 and the barrier gate lines 104 of the assembly of FIG. 2F. The spacer material 118 of FIG. 2G may be formed using the techniques discussed above with reference to FIG. 2C, for example.

[0044] FIG. 2H illustrates an assembly subsequent to providing an insulating material 128 on the assembly of FIG. 2G. The insulating material 128 may be, for example, an ILD. In some embodiments, the insulating material 128 may fill the area above the gate dielectric 114 between adjacent portions of spacer material 118 and extend over the hardmask 110, as shown. In some embodiments, the insulating material 128 may be planarized after deposition (e.g., using a chemical mechanical polishing (CMP) technique). FIG. 2I is a "top" view of the assembly of FIG. 2H, with some of the insulating material 128 removed to show the barrier gate lines 104.

[0045] FIG. 2J is a cross-sectional view through the dashed line of FIG. 2I, subsequent to providing an additional hardmask 112 on the insulating material 128 of FIG. 2I, as well as providing additional insulating material 128, template material 136, and a patterned photoresist 138. The additional insulating material 128 may take the form of any of the insulating materials 128 discussed above with reference to FIG. 2H. The additional hardmask 112 may take the form of any of the hardmasks discussed above with reference to FIG. 2A. The template material 136 and patterned photoresist 138 may take the form of any of the template materials and patterned photoresists, respectively, discussed above with reference to FIG. 2A.

[0046] FIG. 2K illustrates an assembly subsequent to patterning the template material 136 of the assembly of FIG. 2J in accordance with the pattern of the photoresist 138, then removing the photoresist 138. Any suitable etch process may be used to pattern the template material 136.

[0047] FIG. 2L illustrates an assembly subsequent to providing spacer material 140 on side faces of the patterned template material 136 of the assembly of FIG. 2K. The spacer material 140 of FIG. 2L may be formed using the techniques discussed above with reference to FIG. 2C, for example.

[0048] FIG. 2M illustrates an assembly subsequent to removing the template material 136 from the assembly of FIG. 2L. The template material 136 may be removed using any suitable etch process.

[0049] FIG. 2N illustrates an assembly subsequent to depositing additional template material 144 on the assembly of FIG. 2M, planarizing that additional template material 144, and depositing additional photoresist 148 on the additional template material 144. The additional photoresist 148 may be deposited using any suitable technique, such as spin coating.

[0050] FIG. 2O illustrates an assembly subsequent to forming openings in the photoresist 148 of the assembly of FIG. 2N to expose alternating portions of the additional template material 144, as

shown. The openings may be formed using via lithography, or any other suitable process, and may have a circular cross section when viewed from above.

[0051] FIG. 2P illustrates an assembly subsequent to etching the additional template material 144, the insulating material 128, the gate dielectric 114, and the additional hardmask 112 in accordance with the pattern provided by the patterned photoresist 148 and spacer material 140 (i.e., the additional template material 144, the insulating material 128, the gate dielectric 114, and the additional hardmask 112 not masked by the photoresist 148 or the spacer material 140 may be removed). Any suitable etch process may be used to pattern the additional template material 144, the additional hardmask 112, the gate dielectric 114, and the insulating material 128. In some embodiments, as shown, the etch may continue through the gate dielectric 114, while in other embodiments, the etch may stop without removing any of the gate dielectric 114.

[0052] FIG. 2Q illustrates an assembly subsequent to removing the photoresist 148 and the additional template material 144 of the assembly of FIG. 2P. Any suitable technique may be used.

[0053] FIG. 2R illustrates an assembly subsequent to depositing a conformal gate dielectric 114 over the assembly of FIG. 2Q, followed by the deposition and planarization of a metal to form the quantum dot gate lines 102 (e.g., by CMP). The assembly of FIG. 2R thus includes alternating stubs 122 (which may not provide gate functionality during operation) and quantum dot gates 150 (which extend closer to the quantum well stack 146, and thus may provide gate functionality during operation).

[0054] FIG. 2S illustrates an assembly subsequent to removing the spacer material 140 of the assembly of FIG. 2R. Any suitable technique may be used.

[0055] FIG. 2T illustrates an assembly subsequent to providing spacer material 118 on the assembly of FIG. 2S. In some embodiments, the spacer material 118 may be conformal, and may be directionally etched as discussed previously. In some embodiments, some of the spacer material 118 may remain on "top" of the quantum dot gate lines 102, as well as on the side faces of the quantum dot gate lines 102.

[0056] FIG. 2U illustrates an assembly subsequent to providing an insulating material 128 on the assembly of FIG. 2T. The insulating material 128 may be, for example, an ILD. In some embodiments, the insulating material 128 may fill the area above the insulating material 128 between adjacent portions of spacer material 118. In some embodiments, the insulating material 128 may be planarized after deposition (e.g., using CMP). The assembly of FIG. 2U may take the form of the quantum dot device 100 illustrated in FIG. 1.

[0057] FIG. 3 is a view of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 3 schematically illustrates a quantum dot device 100 having a two-dimensional

arrangement of barrier gates 160 and quantum dot gates 150. In some embodiments, the quantum dot device 100 schematically illustrated in FIG. 3 may take the form of any of the quantum dot devices 100 discussed above with reference to FIGS. 1 and 2. In such embodiments, multiple ones of the barrier gates 160 illustrated in FIG. 3 as connected by a barrier gate line 104 may physically take the form of a single elongated barrier gate, as discussed above with reference to FIG. 3, while multiple ones of the quantum dot gates 150 illustrated in FIG. 3 as connected by a quantum dot gate line 102 may take the form of an electrically continuous structure having alternating quantum dot gates 150 and stubs 122, as discussed above.

[0058] In FIG. 3, barrier gates 160 arranged along a barrier gate line 104 are electrically continuous, and thus any voltage applied to a barrier gate line 104 will be applied to all of the barrier gates 160 along that line. Similarly, quantum dot gates 150 arranged along a quantum dot gate line 102 are electrically continuous, and thus any voltage applied to a quantum dot gate line 102 will be applied to all of the quantum dot gates 150 along that line. In the quantum dot device 100 of FIG. 3, the barrier gate lines 104 are parallel to each other, the quantum dot gate lines 102 are parallel to each other, and the barrier gate lines 104 are perpendicular to the quantum dot gate lines 102.

[0059] The quantum dot gates 150 in the quantum dot device 100 of FIG. 3 (and the other quantum dot devices 100 disclosed herein) are arranged as points in a grid, and different ones of the quantum dot gate lines 102 are electrically coupled to different diagonals in that grid. The barrier gates 160 in the quantum dot device 100 of FIG. 3 (and the other quantum dot devices 100 disclosed herein) are arranged as points in a grid, and different ones of the barrier gate lines 104 are electrically coupled to different rows in that grid. The grid underlying the quantum dot gates 150 is rotated 45 degrees with reference to the grid underlying the barrier gates 160.

[0060] In the quantum dot device 100 of FIG. 3, the quantum dot gates 150 in each nearest neighbor pair have a barrier gate disposed between them. The quantum dot gate lines 102 connect quantum dot gates 150 along the diagonal of the underlying grid. As discussed in further detail below, during operation of the quantum dot device 100 of FIG. 3, quantum interactions between nearest neighbor quantum dots under different ones of the quantum dot gates 150 may be controlled in part by the potential energy barrier provided by the intervening barrier gates 160.

[0061] FIGS. 4A-D are various views of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 4A is a "top" view similar to the views of FIGS. 1A and 3, FIG. 4B is a cross-sectional view corresponding to the arrow marked "B" in FIG. 4A, FIG. 4C is a cross-sectional view similar to that of FIG. 1B (and corresponding to the arrow marked "C" in FIG. 4A), and FIG. 4D is a cross-sectional view similar to that of FIG. 1D (and corresponding to the arrow marked "D" in FIG. 4A). The embodiment illustrated in FIG. 4 is substantially similar to that discussed above with

reference to FIGS. 1 and 2, except that the gate dielectric 114 does not extend continuously over the quantum well stack 146, but is instead separately disposed between different portions of the gate metals and the quantum well stack 146. Such an arrangement may be manufactured by not initially depositing a gate dielectric 114, and instead depositing the gate dielectric 114 just prior to depositing the gate metal. FIGS. 4B-D also include some example dimensions for example embodiments of the quantum dot devices 100 disclosed herein, as well as illustrating the location of quantum dots (shown as "e-" electron-spin-based quantum dots) under the quantum dot gates 150. In some embodiments, the distance 164 may be between 5 nanometers and 300 nanometers (e.g., between 5 nanometers and 200 nanometers, between 50 nanometers and 200 nanometers, between 75 nanometers and 125 nanometers, between 80 nanometers and 90 nanometers, or approximately 84 nanometers). In some embodiments, the distance 166 may be between 5 nanometers and 300 nanometers (e.g., between 5 nanometers and 200 nanometers, between 25 nanometers and 100 nanometers, between 40 nanometers and 80 nanometers, or approximately 70 nanometers). In some embodiments, the distance 168 may be between 5 nanometers and 300 nanometers (e.g., between 5 nanometers and 200 nanometers, between 80 nanometers and 200 nanometers., between 100 nanometers and 150 nanometers, or approximately 120 nanometers). Comparing FIGS. 4B and 4D, nearest neighbor quantum dots (e.g., on the "diagonal") may be substantially closer together than quantum dots under adjacent quantum dot gates in a single quantum dot gate line 102, and thus the nearest neighbor quantum dots may be close enough to interact (while those under adjacent quantum dot gates in a single quantum dot gate line 102 may not be close enough to interact). Quantum operations using the quantum dot devices 100 disclosed herein may thus be said to take place "on the diagonal," as discussed in further detail below.

[0062] FIGS. 5A-C illustrate various example dimensions of a quantum dot device 100, in accordance with various embodiments. For example, as illustrated in FIG. 5A, when the quantum dot gate lines 102 have a pitch of 60 nanometers, and the barrier gate lines 104 have a pitch of 60 nanometers, two quantum dots that form under nearest neighbor quantum dot gates (along the "diagonal") may be spaced apart by approximately 85 nanometers. As illustrated in FIG. 5B, when the quantum dot gate lines 102 have a pitch of 45 nanometers, and the barrier gate lines 104 have a pitch of 45 nanometers, two quantum dots that form under nearest neighbor quantum dot gates may be spaced apart by approximately 64 nanometers. As illustrated in FIG. 5C, when the quantum dot gate lines 102 have a pitch of 60 nanometers, and the barrier gate lines 104 have a pitch of 45 nanometers (or vice versa), two quantum dots that form under nearest neighbor quantum dot gates may be spaced apart by approximately 75 nanometers. Any other desired pitches or combinations of pitches may be used to pattern the quantum dot gate lines 102 and/or the barrier gate lines 104.

[0063] FIGS. 6A-C illustrate various electrical configurations that may be used to perform quantum operations in a quantum dot device 100, in accordance with various embodiments. The quantum dot device 100 schematically illustrated in FIGS. 6A-C may take the form of any of the quantum dot devices 100 disclosed herein. The voltages applied to the gate lines, as discussed below with reference to FIGS. 6A-C, may be controlled by any suitable control circuitry 175 (illustrated in FIG. 7). The control circuitry 175 may include multiplexers or other suitable circuitry for selectively applying voltages to various ones of the gate lines. In particular, the control circuitry 175 may be configured to provide an adjustable voltage to a selected barrier gate line 104 while leaving other barrier gate lines 104 at a constant voltage, as suitable. The control circuitry 175 may also be configured to provide microwave pulses and DC voltage to each quantum dot gate line 102 separately, and hold DC voltages constant during operation, as suitable.

[0064] FIG. 6A illustrates an electrical configuration in which quantum dots are formed under quantum dot gates (indicated by the green circles), but no quantum dot interactions take place. In the configuration of FIG. 6A, all the quantum dot gate lines 102 may be supplied with voltages (indicated as Vtuned) in FIG. 6A that allow the quantum dot gates associated with different quantum dot gate lines 102 to be at essentially similar energy levels, and thus not likely to engage in quantum interaction across different quantum dot gate lines 102. Note that the particular voltage value corresponding to Vtuned for a particular quantum dot gate line 102 may be different from the particular voltage value corresponding to Vtuned for a different quantum dot gate line 102; however, the voltages on each of the quantum dot gate lines 102 may be set to a "tuned" value (that may differ between quantum dot gate lines 102) that limits or prevents quantum interaction between quantum dots forming under the different quantum dot gate lines 102. Similarly, the barrier gate lines 104 may be supplied with voltages (indicated as Voff) that may be sufficient to provide a high potential energy barrier between the quantum dot gates on either side of the barrier gate lines 104. Note that the particular voltage value corresponding to Voff for a particular barrier gate line 104 may be different than the particular voltage value corresponding to Voff for another barrier gate line 104; however, the voltages on each of the barrier gate lines 104 may be set to an "off" value (that may differ between barrier gate lines 104) that limits or prevents quantum interaction between quantum dots forming on either side of each barrier gate line 104. The sequence of voltages applied to the quantum dot and barrier gate lines 104 may allow each of the quantum dots to be occupied by a single electron (or more than one electron, or a single hole, or more than one hole, or zero carriers), and, as noted above, the voltage Voff on the barrier gate lines 104 may be sufficient to provide a high potential energy barrier between nearest neighbor quantum dots and thereby limit or prevent quantum interaction.

[0065] FIG. 6B illustrates an electrical configuration that may implement a Pauli gate (or "NOT") operation on a particular quantum dot (identified in FIG. 6B by "π"). In some embodiments, the quantum dot device 100 may include a set of magnet lines 151 above or below the quantum dot gates (e.g., such that the quantum dot gates are disposed between the set of magnet lines 151 and the quantum well stack 146). Examples of arrangements of magnet lines 151 are discussed below with reference to FIGS. 8-13. Different magnet lines 151 arrayed along a quantum dot gate line 102 may have different associated frequencies. These frequencies may be engineered to take particular values, or different magnet lines 151 may have different frequencies due to process variations. In some embodiments, each magnet line 151 (or set of magnet lines 151) may act as an "antenna" for directing energy of a matching frequency to an associated quantum dot. To perform a Pauli gate operation, a microwave pulse (e.g., in the gigahertz range) may be applied to the quantum dot gate line 102 that includes the quantum dot gate associated with the quantum dot π. The frequency of the microwave pulse may allow the quantum dot π to be selected by the field gradient generated by the magnet lines 151, and thus the microwave pulse may change only the state of the quantum dot π (and not other quantum dots disposed below the same quantum dot gate line 102). The voltages on the other quantum dot gate lines 102 may remain fixed, and the voltages on the barrier gate lines 104 may also remain fixed to confine the Pauli gate operation to the quantum dot π.

[0066] FIG. 6C illustrates an electrical configuration that may implement an exchange gate operation on a pair of nearest neighbor ("diagonal") quantum dots (identified in FIG. 6C by "1" and "2"). An exchange gate may allow the quantum dots 1 and 2 to undergo a quantum interaction by appropriately adjusting the potential energy around them, as described below. The barrier gate line 104 that separates the quantum dots 1 and 2 may have its voltage adjusted to a value (Von) that lowers the potential energy barrier between the quantum dots 1 and 2 low enough for them to interact; other barrier gate lines 104 may maintain voltages (Voff) in which quantum dots separated by the associated barrier gates 160 do not interact (as discussed above with reference to FIG. 6A). The voltage applied to the quantum dot gate line 102 associated with quantum dot 1 (labeled gate line "x") and the voltage applied to the quantum dot gate line 102 associated with quantum dot 2 (labeled gate line "x+1") may be made different from each other to provide some energy for their interaction. All of the quantum dot gate lines 102 on the same "side" as the quantum dot gate line 102 x (i.e., the quantum dot gate lines 102 0,...,x-1) may have mutually tuned voltages (which may differ between different quantum dot gate lines 102, as discussed above with reference to FIG. 6A) that tunes these quantum dot gate lines 102 to the quantum dot gate line 102 x (in FIG. 6C, indicated as Vtuned) so that quantum dots formed under different ones of these quantum dot gate lines 102 0,...,x may not interact. Similarly, all of the quantum dot gate lines 102 on the same "side" as the

quantum dot gate line 102 x+1 (i.e., the quantum dot gate lines 102 x+2,...,x+n) may have mutually tuned voltages (which may differ between different quantum dot gate lines 102, as discussed above with reference to FIG. 6A) that tunes these quantum dot gate lines 102 to the quantum dot gate line 102 x+1 (in FIG. 6C, indicated as Vde-tuned) so that quantum dots formed under different ones of the quantum dot gate lines 102 x+1,...,x+n may not interact. In this manner, the interaction of quantum dots in the quantum dot device 100 of FIG. 6C may be limited to the interaction of quantum dots 1 and 2. Any pair of nearest neighbor quantum dots may be selectively allowed to interact using such a technique.

[0067] FIG. 7 illustrates an interconnect arrangement for a quantum dot device 100, in accordance with various embodiments. The quantum dot device 100 schematically illustrated in FIG. 7 may take the form of any of the quantum dot devices 100 disclosed herein, and interconnects may be made to the barrier gate lines 104 and the quantum dot gate lines 102 in any desired manner. In FIG. 7, each gate line may be routed out to a bond pad for connection to a processing device or other control device to control the voltages on the gate lines (e.g., to perform any of the operations discussed above with reference to FIGS. 6A-C).

[0068] As noted above, any of the quantum dot devices 100 disclosed herein may include magnet lines 151 that, during operation of the quantum dot device 100, may generate magnetic fields to selectively "address" different quantum dots. More generally, the magnet lines 151 may be used to generate magnetic fields to create an energy difference in the quantum states of a quantum dot (e.g., in the two spin states of an electron spin-based quantum dot). The quantum states of a quantum dot may also be manipulated by application of RF energy, creating a quantum bit capable of computation.

[0069] The magnetic field experienced by different ones of the quantum dots may be a function of the distance and angle of that quantum dot from the different ones of the magnet lines 151, as known in the art. As noted above, different ones of the quantum dots may be driven (e.g., their spin states manipulated) by matching the resonance of the magnetic field with the resonance of the quantum dot. For example, the quantum dot device 100 may implement electron spin resonance (ESR) and/or electron dipole spin resonance (EDSR) techniques for quantum state manipulation.

[0070] In some embodiments, the magnet lines 151 may be formed of a magnetic material, such as a ferromagnetic material, cobalt, iron, or nickel. In such embodiments, the magnet lines 151 may generate a magnetic field even in the absence of an applied current (although a current may also be applied to tune the magnetic field of magnetic magnet lines 151). EDSR techniques may be implemented in such embodiments to drive transitions between different quantum states in quantum dots that form under the quantum dot gates 150. In some embodiments, the magnet lines

151 may be formed of a conductive (but not necessarily magnetic) material, such as a superconducting material (e.g., aluminum, titanium nitride, niobium titanium, or niobium titanium nitride). DC and/or AC currents may be passed through such non-magnetic magnet lines 151 to generate magnetic field gradients as desired. ESR techniques may be implemented in such embodiments to drive transitions between different quantum states in quantum dots that form under the quantum dot gates 150.

[0071] One or more magnet lines 151 may be included in a quantum dot device 100 in any desired manner. FIGS. 8-13 illustrate several example quantum dot devices 100 including different arrangements of magnet lines 151. Any of the magnet lines 151 discussed herein may include a magnetic material or a non-magnetic conductive material, as discussed above. In FIGS. 8-13, a hardmask 157 is illustrated as separating the magnet lines 151 from the structures below, but this is simply illustrative. In the embodiments illustrated in FIGS. 8-13, the quantum dot devices 100 include three or more magnet lines 151 that are regularly spaced (e.g., with approximately equal space between them) and have substantially the same width; in other embodiments, parallel magnet lines 151 may have different spacings between different adjacent pairs, and/or different widths.

[0072] FIG. 8 illustrates a quantum dot device 100 including an array of magnet lines 151 running parallel to and in-between adjacent ones of the quantum dot gate lines 102. In particular, FIG. 8A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 8B is a cross-sectional view along the section B-B of FIG. 8A (analogous to the view of FIG. 1B), and FIG. 8C is a cross-sectional view along the section E-E of FIG. 8A (analogous to the view of FIG. 1E). In FIG. 8, the array of magnet lines 151 is shown above the quantum dot gate lines 102 (so that the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be formed closer to the quantum well stack 146 than the quantum dot gate lines 102, substantially simultaneously with the quantum dot gate lines 102 (e.g., patterned at the stages represented by FIGS. 2P-Q), or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A). The dimensions and spacing of the magnet lines 151 of the quantum dot device 100 of FIG. 8 (and in the other quantum dot devices 100 disclosed herein) may take any of the forms of the dimensions and spacing of the quantum dot gate lines 102, for example.

[0073] FIG. 9 illustrates a quantum dot device 100 including an array of magnet lines 151 running parallel to and above (e.g., vertically aligned with) the quantum dot gate lines 102. In particular, FIG. 9A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 9B is a cross-sectional view along the section B-B of FIG. 9A (analogous to the view of FIG. 1B), and FIG. 9C is a

cross-sectional view along the section D-D of FIG. 9A (analogous to the view of FIG. 1D). In FIG. 9A, the magnet lines 151 are shaded partially transparently to indicate the quantum dot gate lines 102 under the magnet lines 151. In FIG. 9, the array of magnet lines 151 is shown above the quantum dot gate lines 102 (so that the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be between the quantum dot gate lines 102 and the quantum well stack 146, or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A).

[0074] FIG. 10 illustrates a quantum dot device 100 including an array of magnet lines 151 running parallel to and in-between adjacent ones of the barrier gate lines 104. In particular, FIG. 10A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 10B is a cross-sectional view along the section C-C of FIG. 10A (analogous to the view of FIG. 1C), and FIG. 8C is a cross-sectional view along the section D-D of FIG. 10A (analogous to the view of FIG. 1D). In FIG. 10, the array of magnet lines 151 is shown above the barrier gate lines 104 and the quantum dot gate lines 102 (so that the barrier gate lines 104 and the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be closer to the quantum well stack 146 than the barrier gate lines 104, formed substantially simultaneously with the barrier gate lines 104 (e.g., patterned at the stages represented by FIGS. 2A-E), or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A).

[0075] FIG. 11 illustrates a quantum dot device 100 including an array of magnet lines 151 running parallel to and above (e.g., vertically aligned with) the barrier gate lines 104. In particular, FIG. 11A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 11B is a cross-sectional view along the section B-B of FIG. 11A (analogous to the view of FIG. 1B), and FIG. 11C is a cross-sectional view along the section D-D of FIG. 11A (analogous to the view of FIG. 1D). In FIG. 11A, the magnet lines 151 are shaded partially transparently to indicate the quantum dot gate lines 102 under the magnet lines 151. In FIG. 11, the array of magnet lines 151 is shown above the quantum dot gate lines 102 (so that the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be between the quantum dot gate lines 102 and the quantum well stack 146, between the barrier gate lines 104 and the quantum well stack 146, or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A).

[0076] FIG. 12 illustrates a quantum dot device 100 including an array of magnet lines 151 running "diagonally" relative to the quantum dot gate lines 102 and the barrier gate lines 104, and between

the diagonal lines of quantum dot gates 150. In particular, FIG. 12A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 12B is a cross-sectional view along the section C-C of FIG. 12A (analogous to the view of FIG. 1C), and FIG. 12C is a cross-sectional view along the section D-D of FIG. 12A (analogous to the view of FIG. 1D). In FIG. 12A, the magnet lines 151 are shaded partially transparently to show the quantum dot gate lines 102 and the barrier gate lines 104 under the magnet lines 151. In FIG. 12, the array of magnet lines 151 is shown above the barrier gate lines 104 and the quantum dot gate lines 102 (so that the barrier gate lines 104 and the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be closer to the quantum well stack 146 than the barrier gate lines 104 and/or the quantum dot gate lines 102, or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A).

[0077] FIG. 13 illustrates a quantum dot device 100 including an array of magnet lines 151 running diagonally relative to the quantum dot gate lines 102 and the barrier gate lines 104, and above (e.g., vertically aligned with) the diagonal lines of quantum dot gates 150. In particular, FIG. 13A is a top view of the quantum dot device 100 (analogous to the view of FIG. 1A), FIG. 13B is a cross-sectional view along the section C-C of FIG. 13A (analogous to the view of FIG. 1B), and FIG. 13C is a cross-sectional view along the section D-D of FIG. 13A (analogous to the view of FIG. 1D). In FIG. 13A, the magnet lines 151 are shaded partially transparently to show the quantum dot gate lines 102 and the barrier gate lines 104 under the magnet lines 151. In FIG. 13, the array of magnet lines 151 is shown above the quantum dot gate lines 102 (so that the quantum dot gate lines 102 are closer to the quantum well stack 146 than the magnet lines 151 are), but this is simply illustrative. In other embodiments, the magnet lines 151 may be closer to the quantum well stack 146 than the barrier gate lines 104 and/or the quantum dot gate lines 102, or formed at the opposite face of the quantum well stack 146 (e.g., as discussed below with reference to FIG. 16A).

[0078] Any suitable technique may be used to form the magnet lines 151 disclosed herein. For example, in some embodiments, an additive technique may be used in which a photoresist may be patterned on an insulating material (or stack of insulating materials, including an anti-reflective coating (ARC), a hardmask, an ILD), the insulating material may be etched in accordance with the patterned photoresist to form cavities, the cavities may be filled with the magnetic or non-magnetic conductive material of the magnet lines 151, then the overburden of the material of the magnet lines 151 may be polished away (e.g., by CMP), leaving the magnet lines 151. In other embodiments, other fabrication techniques may be used (e.g., subtractive, semi-additive, etc.).

[0079] Some quantum dot devices 100 may include multiple different ones of the arrays of magnet lines 151 illustrated in FIGS. 8-13. For example, a quantum dot device 100 may include an array of magnet lines 151 arranged as illustrated in FIG. 8, and may also include an array of magnet lines 151 arranged as illustrated in FIG. 9.

[0080] In some embodiments, the quantum dot gate lines 102 and/or the barrier gate lines 104 may themselves act as magnet lines; in some such embodiments, additional magnet lines 151 (such as any of those discussed above) may or may not be included in a quantum dot device 100. Such gate lines may serve two purposes: to provide a localized electrostatic potential that helps to confine or otherwise affect a quantum dot, and to provide a magnetic field gradient that allows a quantum dot to be driven between different quantum states (e.g., spin states). As discussed above with reference to the magnet lines 151, ESR techniques may be implemented when a gate line includes a superconducting material to drive transitions between different quantum states in quantum dots that form under the quantum dot gates 150.

[0081] In some embodiments in which a gate line (e.g., a quantum dot gate line 102 and/or a barrier gate line 104) acts as a magnet line, the metal of that gate line (e.g., the metal of that gate line, such as the metal of the barrier gate lines 104 or the metal of the quantum dot gate lines 102) may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, any of the gate lines may include palladium, gold, copper, nickel, ruthenium, or cobalt. In such embodiments, application of an appropriate AC or DC current (e.g., by the control circuitry 175) to the gate line may cause a desired magnetic field to be generated. In some embodiments in which a gate line acts as a magnet line, the metal of that gate line may be a magnetic material, such as cobalt, iron, or nickel. In such embodiments, the gate line may generate a magnetic field even in the absence of an applied current (although a current may also be applied to tune the magnetic field of magnetic gate lines). As discussed above with reference to the magnet lines 151, EDSR techniques may be implemented when a gate line includes a magnetic material to drive transitions between different quantum states in quantum dots that form under the quantum dot gates 150.

[0082] The quantum dot device 100 of FIG. 1 has a particular regular pattern of quantum dot gates 150 (e.g., as illustrated in the top view of FIG. 1A). In some embodiments of the quantum dot devices 100 disclosed herein, the pattern of quantum dot gates 150 may be sparser than the pattern of FIG. 1 (e.g., some of the quantum dot gate 150 illustrated in FIG. 1 may be replaced by stubs 122).

[0083] FIGS. 14A-C are various views of a quantum dot device 100 having a sparser array of quantum dot gates 150 than the quantum dot device 100 of FIG. 1, in accordance with various embodiments. In particular, FIG. 14A is a top view of a quantum dot device (analogous to the view

of FIG. 1A), FIG. 14B is a view through the section B-B of FIG. 14A (analogous to the view of FIG. 1C), and FIG. 14C is a view through the section C-C of FIG. 14A (also analogous to the view of FIG. 1C). In the quantum dot device 100 of FIG. 14, each quantum dot gate 150 has two nearest neighbors; in the quantum dot device 100 of FIG. 1, a quantum dot gate 150 in the interior of an array of quantum dot gates 150 may have 8 nearest neighbors (two nearest neighbors in the longitudinal direction of the quantum dot gate lines 102, two nearest neighbors in the longitudinal direction of the barrier gate lines 104, and four "diagonal" nearest neighbors). Compared to the quantum dot device 100 of FIG. 1, quantum dots that form under different ones of the quantum dot gate 150 of FIG. 14 may experience reduced interference from neighboring quantum dot gates 150, and thus may exhibit fewer undesirable, unintended interactions (at the expense of fewer quantum dot gates 150 per unit area). Spacing two quantum dot gates 150 further apart may reduce interference between the quantum dots associated with those quantum dot gates 150 (e.g., due to the passive barrier provided by the intervening portion of the quantum well stack 146), and having a barrier gate line 104 between the two quantum dot gates 150 may enable the isolation between the quantum dots to be more actively and strongly controlled.

[0084] Quantum dot devices 100 with "sparser" arrays of quantum dot gates 150 may be used in any of a number of ways. For example, in FIG. 14A, three of the barrier gate lines 104 are labeled as B1-B3, respectively, three of the quantum dot gate lines 102 are labeled as D1-D3, respectively, and four of the quantum dot gates 150 are labeled as Q1-Q4, respectively. During operation of the quantum dot device 100 of FIG. 14, if it is desired to form and control quantum dots in the quantum well stack 146 under the quantum dot gates Q1 and Q2, then electrical signals may be selectively applied to the quantum dot gate lines D1 and D2 to control the potentials under those gate lines D1 and D2 (and thereby under the quantum dot gates Q1 and Q2, respectively), and electrical signals may be selectively applied to the barrier gate line B2 to adjust the potential barrier between the quantum dots under the quantum dot gates Q1 and Q2. The quantum dot under the quantum dot gate Q1 may be isolated from any quantum dots under the quantum dot gate Q3 by providing appropriate electrical signals to the barrier gate line B3; similarly, the quantum dot under the quantum dot gate Q2 may be isolated from any quantum dots under the quantum dot gate Q4 by providing appropriate electrical signals to the barrier gate line B1.

[0085] The "sparse" arrangement quantum dot gate 150 in FIG. 14 is simply illustrative, and quantum dot gates 150 may be replaced with stubs 122, or vice versa, in any of the embodiments of quantum dot devices 100 disclosed herein. For example, FIG. 15 is a top view of another quantum dot device 100 having a sparser array of quantum dot gates than the quantum dot device 100 of FIG.

1, in accordance with various embodiments. The quantum dot device 100 of FIG. 15 has a greater density of quantum dot gates 150 than the quantum dot device 100 of FIG. 14.

[0086] Although FIGS. 8-13 illustrate quantum dot devices 100 in which the magnet lines 151, the barrier gate lines 104, and the quantum dot gate lines 102 are disposed at one face of the quantum well stack 146 (e.g., all disposed "above" the quantum well stack 146), in some embodiments, the magnet lines 151 and the barrier gate lines 104/quantum dot gate lines 102 may be disposed at the opposite face of the quantum well stack 146. For example, FIG. 16A provides a side cross-sectional view of a quantum dot device 100 that shares many structural features with the quantum dot device 100 of FIG. 1, but may include an array of magnet lines 151 at one face of the quantum well stack 146, and the barrier gate lines 104/quantum dot gate lines 102 at the opposite face of the quantum well stack 146. The array of magnet lines 151 of FIG. 16A may take any of the forms discussed above with reference to FIGS. 8-13. The quantum dot device 100 of FIG. 16A may be formed by performing the operations discussed above with reference to FIGS. 2A-2U, flipping the result over, and fabricating the magnet lines 151 on the "other side" of the quantum well stack 146. Although a particular example is illustrated in FIG. 16A, any of the quantum dot devices 100 disclosed herein may include one or more magnet lines 151 at an opposite face of a quantum well stack 146 relative to the barrier gate lines 104/quantum dot gate lines 102.

[0087] FIG. 16B is a cross-sectional view of a double-sided quantum dot device 100, in accordance with various embodiments. The quantum dot device 100 of FIG. 16B may be formed by performing the operations discussed above with reference to FIG. 2, flipping the result over, and performing the same operations on the "other side" of the quantum well stack 146. The quantum well stack 146 may itself include two quantum well layers, one in which quantum dots may be formed by the gates on the corresponding side of the quantum well stack 146, and the other in which quantum dots may be formed by the gates on the other, corresponding side of the quantum well stack 146. In some embodiments, the quantum dots formed in one of the quantum well layers may act as the "active" quantum dots in the quantum dot device 100, and the quantum dots formed in the other of the quantum well layers may act as the "read" quantum dots, sensing the state of the active quantum dots for readout (e.g., through the corresponding gates and other interconnects).

[0088] FIGS. 17A-H illustrate various examples of quantum well stacks 146 that may provide the quantum well stacks 146 of any of the embodiments of the quantum dot devices 100 disclosed herein. In some embodiments, the layers of the quantum well stacks 146 may be grown on a substrate (e.g., a silicon or germanium wafer), and on each other, by epitaxy. The quantum well stacks 146 illustrated in FIGS. 17A-C include a single quantum well layer 152, and the quantum well stacks 146 illustrated in FIGS. 17D-H include two quantum well layers 152 (e.g., as appropriate for a

double-sided device, as discussed above with reference to FIG. 16). Generally, the quantum well stack 146 included in a quantum dot device 100 may include one quantum well layer 152 or more than two quantum well layers 152; elements may be omitted from the quantum well stacks 146, or added to the quantum well stacks 146, discussed with reference to FIG. 17 to achieve such embodiments, as appropriate. Layers other than the quantum well layer(s) 152 in a quantum well stack 146 may have higher threshold voltages for conduction than the quantum well layer(s) 152 so that when the quantum well layer(s) 152 are biased at their threshold voltages, the quantum well layer(s) 152 conduct and the other layers of the quantum well stack 146 do not. This may avoid parallel conduction in both the quantum well layer(s) 152 and the other layers, and thus avoid compromising the strong mobility of the quantum well layer(s) 152 with conduction in layers having inferior mobility. In some embodiments, silicon used in a quantum well stack 146 may be isotopically enriched 28Si. In some embodiments, germanium used in a quantum well stack 146 may be isotopically enriched 70Ge, 72Ge, or 74Ge.

[0089] FIG. 17A is a cross-sectional view of a quantum well stack 146 including only a quantum well layer 152. The quantum well layer 152 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. The gate dielectric 114 may be disposed on the upper surface of the quantum well layer 152. In some embodiments, the quantum well layer 152 of FIG. 17A may be formed of intrinsic silicon, and the gate dielectric 114 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the silicon oxide. Embodiments in which the quantum well layer 152 of FIG. 17A is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. In some embodiments, the quantum well layer 152 of FIG. 17A may be formed of intrinsic germanium, and the gate dielectric 114 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, the quantum well layer 152 may be strained, while in other embodiments, the quantum well layer 152 may not be strained. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 17A may take any suitable values. For example, in some embodiments, the thickness of the quantum well layer 152 (e.g., intrinsic silicon or germanium) may be between 0.8 microns and 1.2 microns.

[0090] FIG. 17B is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154. The quantum well stack 146 may be disposed on a substrate such that

the barrier layer 154 is disposed between the quantum well layer 152 and the substrate. The barrier layer 154 may provide a potential barrier between the quantum well layer 152 and the substrate. As discussed above with reference to FIG. 17A, the quantum well layer 152 of FIG. 17B may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate is formed of silicon, the quantum well layer 152 of FIG. 17B may be formed of silicon, and the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer 152 is formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 17B may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between 0 nanometers and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 nanometers and 30 nanometers.

[0091] FIG. 17C is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154-1, as well as a buffer layer 176 and an additional barrier layer 154-2. The quantum well stack 146 may be disposed on a substrate such that the buffer layer 176 is disposed between the barrier layer 154-1 and the substrate. The buffer layer 176 may be formed of the same material as the barrier layer 154, and may be present to trap defects that form in this material as it is grown on the substrate. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 154-1. In particular, the barrier layer 154-1 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the substrate to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 17C may take any suitable values. For example, in some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between 0.3 microns and 4 microns (e.g., 0.3-2 microns, or 0.5 microns). In some embodiments, the thickness of the barrier layer 154-1 (e.g., silicon germanium) may be between 0 nanometers and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 nanometers and 30 nanometers (e.g., 10 nanometers). The barrier layer 154-2, like the

barrier layer 154-1, may provide a potential energy barrier around the quantum well layer 152, and may take the form of any of the embodiments of the barrier layer 154-1. In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between 25 nanometers and 75 nanometers (e.g., 32 nanometers).

[0092] As discussed above with reference to FIG. 17B, the quantum well layer 152 of FIG. 17C may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate is formed of silicon, the quantum well layer 152 of FIG. 17C may be formed of silicon, and the barrier layer 154-1 and the buffer layer 176 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the substrate to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth.

[0093] In some embodiments, the quantum well layer 152 of FIG. 17C may be formed of germanium, and the buffer layer 176 and the barrier layer 154-1 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the substrate to a nonzero percent (e.g., 70%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth. In some embodiments of the quantum well stack 146 of FIG. 17C, the buffer layer 176 and/or the barrier layer 154-2 may be omitted.

[0094] FIG. 17D is a cross-sectional view of a quantum well stack 146 including only a quantum well layer 152-1, a barrier layer 154, and a quantum well layer 152-2. A "single-sided" version of the quantum well stack 146 of FIG. 17D would include only a quantum well layer 152. In some embodiments, the quantum well layers 152 of FIG. 17D may be formed of intrinsic silicon, and the gate dielectrics 114 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the

intrinsic silicon and the proximate silicon oxide. Embodiments in which the quantum well layers 152 of FIG. 17D are formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. In some embodiments, the quantum well layers 152 of FIG. 17D may be formed of intrinsic germanium, and the gate dielectrics 114 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the proximate germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, the quantum well layers 152 may be strained, while in other embodiments, the quantum well layers 152 may not be strained.

[0095] The barrier layer 154 of FIG. 17D may provide a potential barrier between the quantum well layer 152-1 and the quantum well layer 152-2. In some embodiments in which the quantum well layers 152 of FIG. 17D are formed of silicon, the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layers 152 are formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)).

[0096] The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 17D may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between 0 nanometers and 400 nanometers. In some embodiments, the thickness of the quantum well layers 152 (e.g., silicon or germanium) may be between 5 nanometers and 30 nanometers.

[0097] FIG. 17E is a cross-sectional view of a quantum well stack 146 including quantum well layers 152-1 and 152-2, a barrier layer 154-2 disposed between the quantum well layers 152-1 and 152-2, and additional barrier layers 154-1 and 154-3. In the quantum dot device 100, the barrier layer 154-1 may be disposed between the quantum well layer 152-1 and the gate dielectric 114-1 (see, e.g., FIG. 16). The barrier layer 154-3 may be disposed between the quantum well layer 152-2 and the gate dielectric 114-2 (see, e.g., FIG. 16). In some embodiments, the barrier layer 154-3 may be formed of a material (e.g., silicon germanium), and when the quantum well stack 146 is being grown on a substrate, the barrier layer 154-3 may include a buffer region of that material. This buffer region may trap defects that form in this material as it is grown on the substrate, and in some embodiments, the buffer region may be grown under different conditions (e.g., deposition temperature or growth rate) from the rest of the barrier layer 154-3. In particular, the rest of the barrier layer 154-3 may be grown under conditions that achieve fewer defects than the buffer region. In some embodiments, the buffer region may be lattice mismatched with the quantum well layer(s) 152 in a quantum well stack 146, imparting biaxial strain to the quantum well layer(s) 152.

[0098] The barrier layers 154-1 and 154-3 may provide potential energy barriers around the quantum well layers 152-1 and 152-2, respectively, and the barrier layer 154-1 may take the form of any of the embodiments of the barrier layer 154-3 discussed herein. In some embodiments, the barrier layer 154-1 may have a similar form as the barrier layer 154-3, but may not include a "buffer region" as discussed above; in the quantum dot device 100, the barrier layer 154-3 and the barrier layer 154-1 may have substantially the same structure. The barrier layer 154-2 may take the form of any of the embodiments of the barrier layer 154 discussed above with reference to FIG. 17D. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 17E may take any suitable values. For example, in some embodiments, the thickness of the barrier layers 154-1 and 154-3 (e.g., silicon germanium) in the quantum dot device 100 may be between 0 nanometers and 400 nanometers. In some embodiments, the thickness of the quantum well layers 152 (e.g., silicon or germanium) may be between 5 nanometers and 30 nanometers (e.g., 10 nanometers). In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between 25 nanometers and 75 nanometers (e.g., 32 nanometers).

[0099] FIGS. 17F-G illustrate examples of quantum well stacks 146 including doped layer(s) 137. As noted above, doped layer(s) 137 may be included in a quantum well stack 146 instead of or in addition to an accumulation region 162.

[0100] FIG. 17F is a cross-sectional view of a quantum well stack 146 including a buffer layer 176, a barrier layer 155-2, a quantum well layer 152-2, a barrier layer 154-2, a doped layer 137, a barrier layer 154-1, a quantum well layer 152-1, and a barrier layer 155-1.

[0101] The buffer layer 176 may be formed of the same material as the barrier layer 155-2, and may be present to trap defects that form in this material as it is grown. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 155-2. In particular, the barrier layer 155-2 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies to the barrier layer 155-2; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent to a nonzero percent (e.g., 30%) at the barrier layer 155-2. The buffer layer 176 may be grown beyond its critical layer thickness such that it is substantially free of stress from the underlying base (and thus may be referred to as "relaxed"). In some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between 0.3 microns and 4 microns (e.g., between 0.3 microns and 2 microns, or 0.5 microns). In some embodiments, the buffer layer 176 may be lattice mismatched with the

quantum well layer(s) 152 in a quantum well stack 146, imparting biaxial strain to the quantum well layer(s) 152.

[0102] The barrier layer 155-2 may provide a potential energy barrier proximate to the quantum well layer 152-2. The barrier layer 155-2 may be formed of any suitable materials. For example, in some embodiments in which the quantum well layer 152 is formed of silicon or germanium, the barrier layer 155-2 may be formed of silicon germanium. In some embodiments, the thickness of the barrier layer 155-2 may be between 0 nanometers and 400 nanometers (e.g., between 25 and 75 nanometers).

[0103] The quantum well layer 152-2 may be formed of a different material than the barrier layer 155-2. Generally, a quantum well layer 152 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152. Embodiments in which the quantum well layer 152 is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. Embodiments in which a quantum well layer 152 is formed of intrinsic germanium may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, a quantum well layer 152 may be strained, while in other embodiments, a quantum well layer 152 may not be strained. The thickness of a quantum well layer 152 may take any suitable values; in some embodiments, a quantum well layer 152 may have a thickness between 5 nanometers and 30 nanometers.

[0104] In the quantum well stack 146 of FIG. 17F, the doped layer 137 may be "shared" by the two quantum well layers 152 in the quantum well stack 146, in that the doped layer 137 provides carriers to the quantum well layer 152-1 and the quantum well layer 152-2 during use. In the quantum dot device 100, the quantum well layer 152-1 may be disposed between the doped layer 137 and the gate dielectric 114-1, while the quantum well layer 152-2 may be disposed between the doped layer 137 and the gate dielectric 114-2. The doped layer 137 of FIG. 17F may be doped with an n-type material (e.g., for an electron-type quantum dot device 100) or a p-type material (e.g., for a hole-type quantum dot device 100). In some embodiments, the doping concentration of the doped layer 137 may be between $10^{17}/cm^3$ and $10^{20}/cm^3$ (e.g., between $10^{17}/cm^3$ and $10^{18}/cm^3$). The thickness (i.e., z-height) of the doped layer 137 may depend on the doping concentration, among other factors, and in some embodiments, may be between 5 nanometers and 50 nanometers (e.g., between 20 nanometers and 30 nanometers).

[0105] A doped layer 137 may be formed using any of a number of techniques. In some embodiments, a doped layer 137 may be formed of an undoped base material (e.g., silicon germanium) that is doped in situ during growth of the base material by epitaxy. In some embodiments, a doped layer 137 may initially be fully formed of an undoped base material (e.g.,

silicon germanium), then a layer of dopant may be deposited on this base material (e.g., a monolayer of the desired dopant), and an annealing process may be performed to drive the dopant into the base material. In some embodiments, a doped layer 137 may initially be fully formed of an undoped base material (e.g., silicon germanium), and the dopant may be implanted into the lattice (and, in some embodiments, may be subsequently annealed). In some embodiments, a doped layer 137 may be provided by a silicon germanium layer (e.g., with 90% germanium content) doped with an n-type dopant. In general, any suitable technique may be used to form a doped layer 137.

[0106] The barrier layer 154-2 may not be doped, and thus may provide a barrier to prevent impurities in the doped layer 137 from diffusing into the quantum well layer 152-2 and forming recombination sites or other defects that may reduce channel conduction and thereby impede performance of the quantum dot device 100. In some embodiments of the quantum well stack 146 of FIG. 17F, the doped layer 137 may include a same material as the barrier layer 154-2, but the barrier layer 154-2 may not be doped. For example, in some embodiments, the doped layer 137 and the barrier layer 154-2 may both be silicon germanium. In some embodiments in which the quantum well layer 152-2 is formed of silicon, the barrier layer 154-2 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer 152-2 is formed of germanium, the barrier layer 154-2 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thickness of the barrier layer 154-2 may depend on the doping concentration of the doped layer 137, among other factors discussed below, and in some embodiments, may be between 5 nanometers and 50 nanometers (e.g., between 20 nanometers and 30 nanometers).

[0107] The barrier layer 154-1 may provide a barrier to prevent impurities in the doped layer 137 from diffusing into the quantum well layer 152-1, and may take any of the forms described herein for the barrier layer 154-2. Similarly, the quantum well layer 152-1 may take any of the forms described herein for the quantum well layer 152-2. The barrier layer 155-1 may provide a potential energy barrier proximate to the quantum well layer 152-1 (as discussed above with reference to the barrier layer 155-2 and the quantum well layer 152-2), and may take any of the forms described herein for the barrier layer 155-2.

[0108] The thickness of a barrier layer 154 may impact the ease with which carriers in the doped layer 137 can move into a quantum well layer 152 disposed on the other side of the barrier layer 154. The thicker the barrier layer 154, the more difficult it may be for carriers to move into the quantum well layer 152; at the same time, the thicker the barrier layer 154, the more effective it may be at preventing impurities from the doped layer 137 from moving into the quantum well layer 152. Additionally, the diffusion of impurities may depend on the temperature at which the quantum

dot device 100 operates. Thus, the thickness of the barrier layer 154 may be adjusted to achieve a desired energy barrier and impurity screening effect between the doped layer 137 and the quantum well layer 152 during expected operating conditions.

[0109] In some embodiments of the quantum well stack 146 of FIG. 17F (e.g., those included in "single-sided" quantum dot devices 100), only a single quantum well layer 152 may be included. For example, the layers 154-1 and 152-1 may be omitted, and gates may be formed proximate to the barrier layer 155-1 such that the quantum well layer 152-1 is disposed between the gates and the doped layer 137. In other embodiments, the layers 154-1, 152-1, and 155-2 may be omitted, and gates may be formed proximate to the doped layer 137. In some embodiments, the buffer layer 176 and/or the barrier layer 155-2 may be omitted from the quantum well stack 146 of FIG. 17F.

[0110] FIG. 17G is a cross-sectional view of a quantum well stack 146 that is similar to the quantum well stack 146 of FIG. 17F, except that in the place of the single doped layer 137 shared by two quantum well layers 152, the quantum well stack 146 of FIG. 17G includes two different doped layers 137-2 and 137-1 (spaced apart by a barrier layer 155-3). In such an embodiment, the doped layer 137-2 may provide a source of carriers for the quantum well layer 152-2, and the doped layer 137-1 may provide a source of carriers for the quantum well layer 152-1. The barrier layer 155-3 may provide a potential barrier between the two doped layers 137, and may take any suitable form. Generally, the elements of the quantum well stack 146 of FIG. 17G may take the form of any of the corresponding elements of the quantum well stack 146 of FIG. 17F. The doped layers 137-1 and 137-2 may have the same geometry and material composition, or may have different geometries and/or material compositions.

[0111] FIG. 17H is a cross-sectional view of a quantum well stack 146 in which two doped layers 137-1 and 137-2 are disposed toward the "outside" of the quantum well stack 146, rather than the "inside" of the quantum well stack 146, as illustrated in FIGS. 17F and 17G. In particular, the quantum well layer 152-2 is disposed between the doped layer 137-2 and the quantum well layer 152-1, and the quantum well layer 152-1 is disposed between the doped layer 137-1 and the quantum well layer 152-2. In the quantum dot device 100, the doped layer 137-1 may be disposed between the quantum well layer 152-1 and the gate dielectric 114-1, while the doped layer 137-2 may be disposed between the quantum well layer 152-2 and the gate dielectric 114-2. In the quantum well stack 146 of FIG. 17H, a barrier layer 155-3 provides a potential barrier between the quantum well layers 152-1 and 152-2 (rather than between the doped layers 137-1 and 137-2, as illustrated in the quantum well stack 146 of FIG. 17G). Generally, the elements of the quantum well stack 146 of FIG. 17H may take the form of any of the corresponding elements of the quantum well stack 146 of FIGS. 17D-G.

[0112] In some particular embodiments in which the quantum dot device 100 is a "single-sided" device with only one set of gates, the quantum well stack 146 may include a silicon base, a buffer layer 176 of silicon germanium (e.g., with 30% germanium content), then a doped layer 137 formed of silicon germanium doped with an n-type dopant, a thin barrier layer 154 formed of silicon germanium (e.g., silicon germanium with 70% germanium content), a silicon quantum well layer 152, and a barrier layer 155 formed of silicon germanium (e.g., with 30% germanium content); in such an embodiment, the gates may be disposed on the barrier layer 155. In some other particular embodiments in which the quantum dot device 100 is a "single-sided" device with only one set of gates, the quantum well stack 146 may include a silicon base, a doped layer 137 formed of silicon doped with an n-type dopant, a thin barrier layer 154 formed of silicon germanium, and a silicon quantum well layer 152; in such an embodiment, the gates may be disposed on the silicon quantum well layer 152.

[0113] FIG. 18 shows top views of a wafer 450 and dies 452 that may be formed from the wafer 450; the dies 452 may include any of the quantum dot devices 100 disclosed herein. The wafer 450 may include semiconductor material and may include one or more dies 452 having conventional and quantum dot device elements formed on a surface of the wafer 450. Each of the dies 452 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum dot device. After the fabrication of the semiconductor product is complete, the wafer 450 may undergo a singulation process in which each of the dies 452 is separated from one another to provide discrete "chips" of the semiconductor product. A die 452 may include one or more quantum dot devices 100 and/or supporting circuitry to route electrical signals to the quantum dot devices (e.g., interconnects including conductive vias and lines, or any control circuitry 175, as discussed above with reference to FIG. 7), as well as any other integrated circuit (IC) components. In some embodiments, the wafer 450 or the die 452 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 452. For example, a memory array formed by multiple memory devices may be formed on a same die 452 as a processing device (e.g., the processing device 2002 of FIG. 20) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0114] FIG. 19 is a cross-sectional side view of a device assembly 400 that may include any of the embodiments of the quantum dot devices 100 disclosed herein. The device assembly 400 includes a number of components disposed on a circuit board 402. The device assembly 400 may include components disposed on a first face 440 of the circuit board 402 and an opposing second face 442 of the circuit board 402; generally, components may be disposed on one or both faces 440 and 442.

[0115] In some embodiments, the circuit board 402 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 402. In other embodiments, the circuit board 402 may be a package substrate or flexible board.

[0116] The device assembly 400 illustrated in FIG. 19 includes a package-on-interposer structure 436 coupled to the first face 440 of the circuit board 402 by coupling components 416. The coupling components 416 may electrically and mechanically couple the package-on-interposer structure 436 to the circuit board 402, and may include solder balls (as shown in FIG. 19), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0117] The package-on-interposer structure 436 may include a package 420 coupled to an interposer 404 by coupling components 418. The coupling components 418 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 416. Although a single package 420 is shown in FIG. 19, multiple packages may be coupled to the interposer 404; indeed, additional interposers may be coupled to the interposer 404. The interposer 404 may provide an intervening substrate used to bridge the circuit board 402 and the package 420. The package 420 may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices 100) or may be a conventional IC package, for example. In some embodiments, the package 420 may include a quantum dot device die (e.g., a die that includes one or more quantum dot devices 100) coupled to a package substrate (e.g., by flip chip connections). Generally, the interposer 404 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 404 may couple the package 420 (e.g., a die) to a ball grid array (BGA) of the coupling components 416 for coupling to the circuit board 402. In the embodiment illustrated in FIG. 19, the package 420 and the circuit board 402 are attached to opposing sides of the interposer 404; in other embodiments, the package 420 and the circuit board 402 may be attached to a same side of the interposer 404. In some embodiments, three or more components may be interconnected by way of the interposer 404.

[0118] The interposer 404 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 404 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 404 may include metal interconnects 408 and vias 410,

including but not limited to through-silicon vias (TSVs) 406. The interposer 404 may further include embedded devices 414, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as RF devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 404. The package-on-interposer structure 436 may take the form of any of the package-on-interposer structures known in the art.

[0119] The device assembly 400 may include a package 424 coupled to the first face 440 of the circuit board 402 by coupling components 422. The coupling components 422 may take the form of any of the embodiments discussed above with reference to the coupling components 416, and the package 424 may take the form of any of the embodiments discussed above with reference to the package 420. The package 424 may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices 100) or may be a conventional IC package, for example. In some embodiments, the package 424 may include a quantum dot device die (e.g., a die that includes one or more quantum dot devices 100) coupled to a package substrate (e.g., by flip chip connections).

[0120] The device assembly 400 illustrated in FIG. 19 includes a package-on-package structure 434 coupled to the second face 442 of the circuit board 402 by coupling components 428. The package-on-package structure 434 may include a package 426 and a package 432 coupled together by coupling components 430 such that the package 426 is disposed between the circuit board 402 and the package 432. The coupling components 428 and 430 may take the form of any of the embodiments of the coupling components 416 discussed above, and the packages 426 and 432 may take the form of any of the embodiments of the package 420 discussed above. Each of the packages 426 and 432 may be a quantum dot device package (e.g., a package that includes one or more quantum dot devices 100) or may be a conventional IC package, for example. In some embodiments, one or both of the packages 426 and 432 may take the form of any of the embodiments of a quantum dot device package (e.g., a package that includes one or more quantum dot devices 100) disclosed herein, and may include a die coupled to a package substrate (e.g., by flip chip connections).

[0121] FIG. 20 is a block diagram of an example quantum computing device 2000 that may include any of the quantum dot devices 100 disclosed herein. A number of components are illustrated in FIG. 20 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to

one or more PCBs (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 20, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0122] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum dot devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0123] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance

of a write operation, control the clearing of quantum bits, control the performance of any of the operations discussed above with reference to FIGS. 6A-C, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0124] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0125] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 10 Kelvin or less (e.g., 5 Kelvin or less, or 2 Kelvin or less). In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0126] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may

communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0127] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0128] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0129] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0130] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display.

[0131] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0132] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0133] The quantum computing device 2000 may include a GPS device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0134] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0135] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0136] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a

printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0137] Any suitable materials may be used in various ones of the embodiments disclosed herein. For example, in some embodiments, the gate dielectric 114 may be a multilayer gate dielectric. The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114. The spacer materials (e.g., the spacer material 118, 134, or 140) may be any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The insulating materials 128 may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride, for example. Hardmasks (e.g., the hardmasks 110, 112, and 157) may be formed of silicon nitride, silicon carbide, or another suitable material.

[0138] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0139] Example 1 is a quantum dot device, including: a quantum well stack; a plurality of first gate lines above the quantum well stack; and a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines; wherein the first gate lines or the second gate lines include a magnetic material.

[0140] Example 2 may include the subject matter of Example 1, and may further specify that the magnetic material includes cobalt or nickel.

[0141] Example 3 may include the subject matter of any of Examples 1-2, and may further specify that the first gate lines are at least partially between the second gate lines and the quantum well stack.

[0142] Example 4 may include the subject matter of any of Examples 1-3, and may further specify that the first gate lines have a pitch between 5 nanometers and 200 nanometers.

[0143] Example 5 may include the subject matter of Example 4, and may further specify that the second gate lines have a pitch between 5 nanometers and 200 nanometers.

[0144] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines.

[0145] Example 7 may include the subject matter of Example 6, and may further specify that an interior quantum dot gate has at least 8 nearest neighbor quantum dot gates.

[0146] Example 8 may include the subject matter of Example 6, and may further specify that an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

[0147] Example 9 is a method of manufacturing a quantum dot device, including: forming a quantum well stack; forming a plurality of first gate lines above the quantum well stack; and forming a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines; wherein the first gate lines or the second gate lines include a magnetic material.

[0148] Example 10 may include the subject matter of Example 9, and may further specify that the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

[0149] Example 11 may include the subject matter of any of Examples 9-10, and may further specify that the quantum well stack includes a layer of silicon.

[0150] Example 12 is a method of performing a quantum computing operation, including: applying voltages to first gate lines and second gate lines of a quantum dot device to form a quantum dot in a quantum well stack of the quantum dot device, wherein the first gate lines are oriented perpendicular to the second gate lines; and applying currents to the first gates or the second gates to generate a magnetic field gradient as part of causing a quantum state of the quantum dot to change.

[0151] Example 13 may include the subject matter of Example 12, and may further specify that the first gate lines or the second gate lines include a magnetic material.

[0152] Example 14 may include the subject matter of Example 12, and may further specify that the first gate lines or the second gate lines include a superconducting material.

[0153] Example 15 may include the subject matter of any of Examples 12-14, and may further specify that the quantum dot is a spin-based quantum dot.

[0154] Example 16 is a quantum dot device, including: a quantum well stack; a plurality of first gate lines above the quantum well stack; and a plurality of second gate lines above the quantum well

stack; wherein the second gate lines are perpendicular to the first gate lines, the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

[0155] Example 17 may include the subject matter of Example 16, and may further specify that the interior quantum dot gate has 4 nearest neighbor quantum dot gates.

[0156] Example 18 may include the subject matter of Example 16, and may further specify that the interior quantum dot gate has 2 nearest neighbor quantum dot gates.

[0157] Example 19 may include the subject matter of any of Examples 16-19, and may further specify that the first gate lines or the second gate lines include a magnetic material or a superconducting material.

[0158] Example 20 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes a quantum well stack, a plurality of first gate lines above the quantum well stack, a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines; a non-quantum processing device, coupled to the quantum processing device, to control electrical signals applied to the first and second gate lines; and a memory device to store data generated during operation of the quantum processing device; wherein the first gate lines include a magnetic material, or the first gate lines include a superconducting material and the non-quantum processing device is to control current applied to the first gate lines to cause the first gate lines to generate a magnetic field gradient.

[0159] Example 21 may include the subject matter of Example 20, and may further include a cooling apparatus to maintain a temperature of the quantum processing device below 10 Kelvin.

[0160] Example 22 may include the subject matter of any of Examples 20-21, and may further specify that the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0161] Example 23 may include the subject matter of any of Examples 20-22, and may further specify that the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

[0162] Example 24 may include the subject matter of any of Examples 20-23, and may further specify that the quantum well stack includes a layer of silicon and a layer of silicon oxide between the layer of silicon and the first gate lines.

[0163] Example 25 may include the subject matter of any of Examples 20-24, and may further specify that electron-based or hole-based quantum dots are formed in the quantum well stack during operation of the quantum processing device.

[0164] Example 26 may include the subject matter of any of Examples 20-25, and may further specify that the non-quantum processing device is further to read out signals from the quantum processing device.

[0165] Example 27 may include the subject matter of any of Examples 20-26, and may further specify that the non-quantum processing device is further to process the read-out signals.

Claims

1. A quantum dot device, comprising:

a quantum well stack;

a plurality of first gate lines above the quantum well stack; and

a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines;

wherein the first gate lines or the second gate lines include a magnetic material.

2. The quantum dot device of claim 1, wherein the magnetic material includes cobalt or nickel.

3. The quantum dot device of claim 1, wherein the first gate lines are at least partially between the second gate lines and the quantum well stack.

4. The quantum dot device of claim 1, wherein the first gate lines have a pitch between 5 nanometers and 200 nanometers.

5. The quantum dot device of claim 4, wherein the second gate lines have a pitch between 5 nanometers and 200 nanometers.

6. The quantum dot device of claim 1, wherein the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines.

7. The quantum dot device of claim 6, wherein an interior quantum dot gate has at least 8 nearest neighbor quantum dot gates.

8. The quantum dot device of claim 6, wherein an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

9. A method of manufacturing a quantum dot device, including:

forming a quantum well stack;

forming a plurality of first gate lines above the quantum well stack; and

forming a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines;

wherein the first gate lines or the second gate lines include a magnetic material.

10. The method of claim 9, wherein the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

11. The method of any of claims 9-10, wherein the quantum well stack includes a layer of silicon.

12. A method of performing a quantum computing operation, comprising:

applying voltages to first gate lines and second gate lines of a quantum dot device to form a quantum dot in a quantum well stack of the quantum dot device, wherein the first gate lines are oriented perpendicular to the second gate lines; and

applying currents to the first gates or the second gates to generate a magnetic field gradient as part of causing a quantum state of the quantum dot to change.

13. The method of claim 12, wherein the first gate lines or the second gate lines include a magnetic material.

14. The method of claim 12, wherein the first gate lines or the second gate lines include a superconducting material.

15. The method of any of claims 12-14, wherein the quantum dot is a spin-based quantum dot.

16. A quantum dot device, comprising:

a quantum well stack;

a plurality of first gate lines above the quantum well stack; and

a plurality of second gate lines above the quantum well stack;

wherein the second gate lines are perpendicular to the first gate lines, the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

17. The quantum dot device of claim 16, wherein the interior quantum dot gate has 4 nearest neighbor quantum dot gates.

18. The quantum dot device of claim 16, wherein the interior quantum dot gate has 2 nearest neighbor quantum dot gates.

19. The quantum dot device of any of claims 16-19, wherein the first gate lines or the second gate lines include a magnetic material or a superconducting material.

20. A quantum computing device, comprising:

a quantum processing device, wherein the quantum processing device includes a quantum well stack, a plurality of first gate lines above the quantum well stack, a plurality of second gate lines above the quantum well stack, wherein the second gate lines are perpendicular to the first gate lines;

a non-quantum processing device, coupled to the quantum processing device, to control electrical signals applied to the first and second gate lines; and

a memory device to store data generated during operation of the quantum processing device;

wherein the first gate lines include a magnetic material, or the first gate lines include a superconducting material and the non-quantum processing device is to control current applied to the first gate lines to cause the first gate lines to generate a magnetic field gradient.

21. The quantum computing device of claim 20, further comprising:

a cooling apparatus to maintain a temperature of the quantum processing device below 10 Kelvin.

22. The quantum computing device of claim 20, wherein the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

23. The quantum computing device of any of claims 20-22, wherein the second gate lines include quantum dot gates extending toward the quantum well stack between one or more adjacent pairs of first gate lines, and an interior quantum dot gate has fewer than 8 nearest neighbor quantum dot gates.

24. The quantum computing device of any of claims 20-22, wherein the quantum well stack includes a layer of silicon and a layer of silicon oxide between the layer of silicon and the first gate lines.

25. The quantum computing device of any of claims 20-22, wherein electron-based or hole-based quantum dots are formed in the quantum well stack during operation of the quantum processing device.

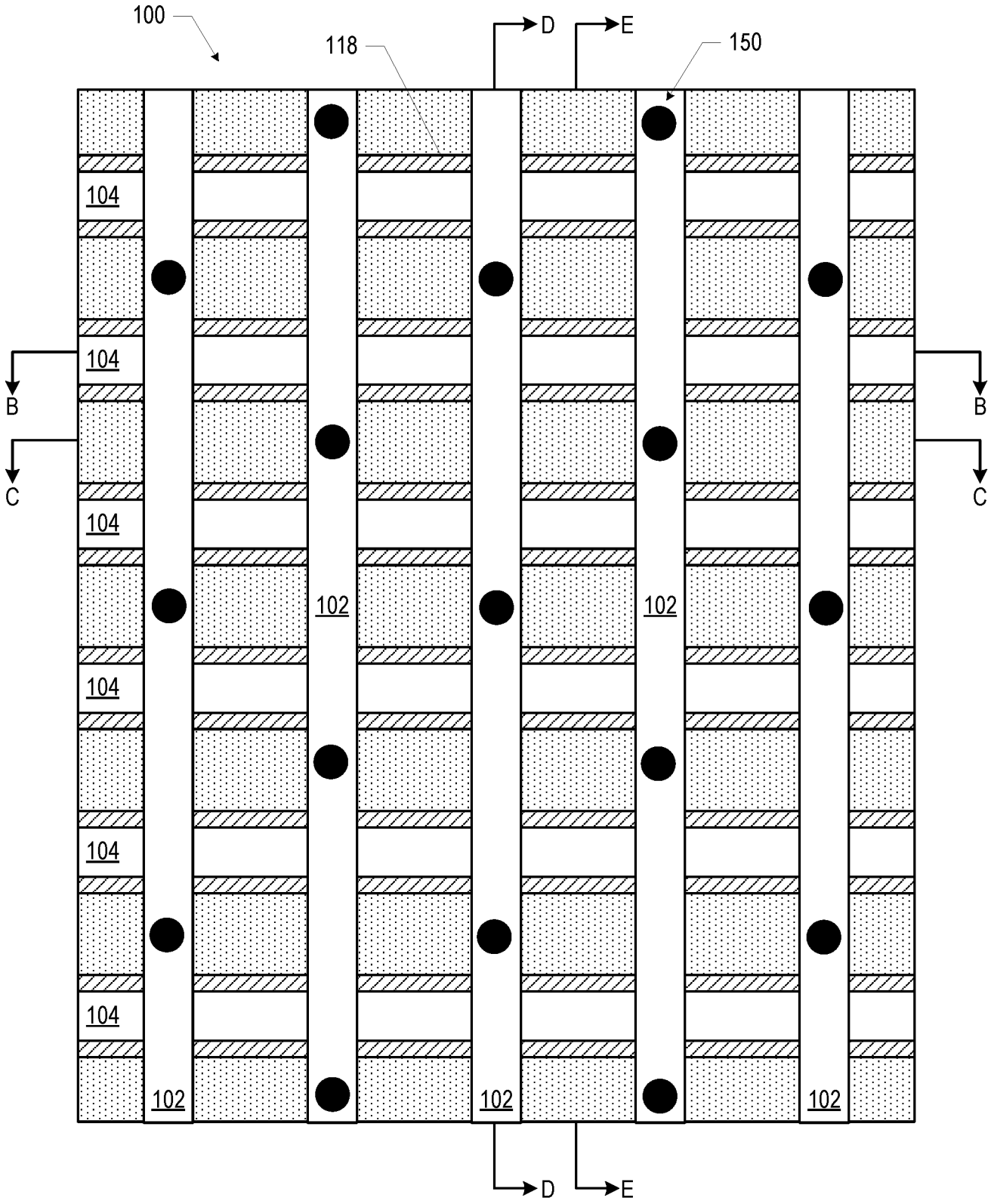

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FIG. 1A

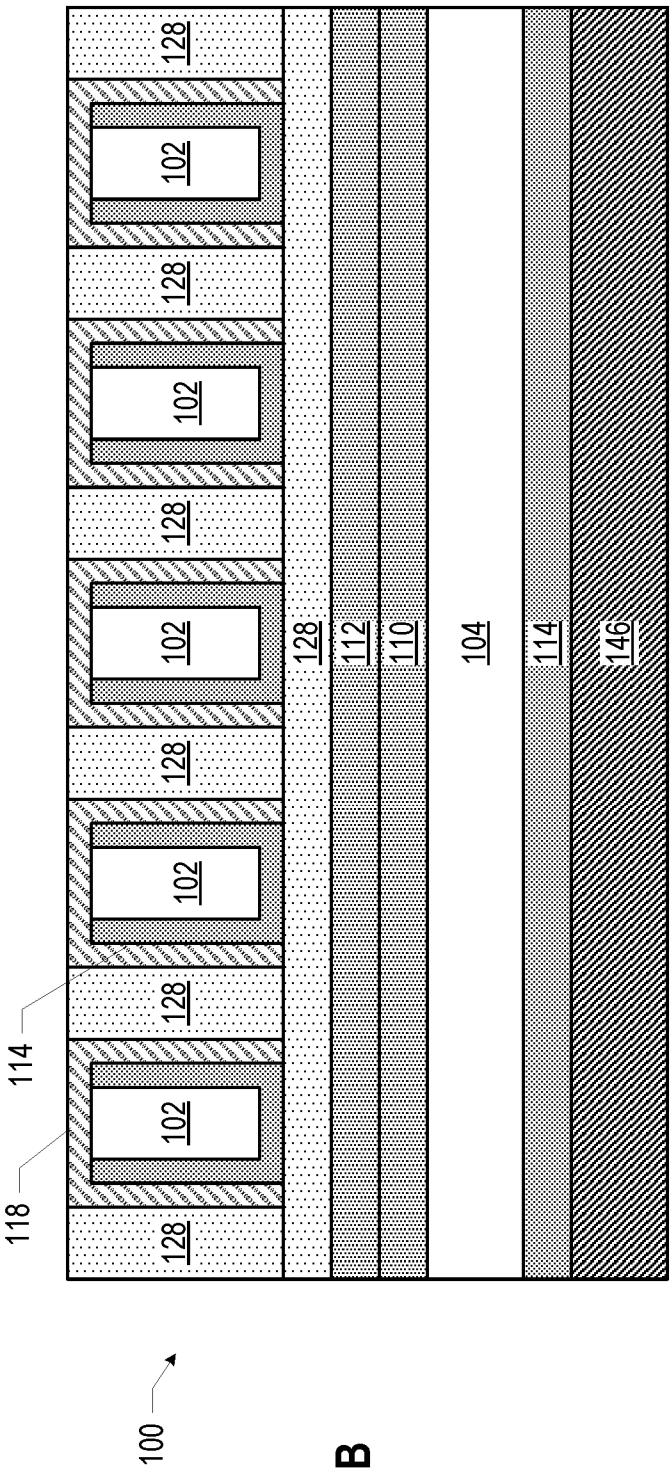

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FIG. 1B

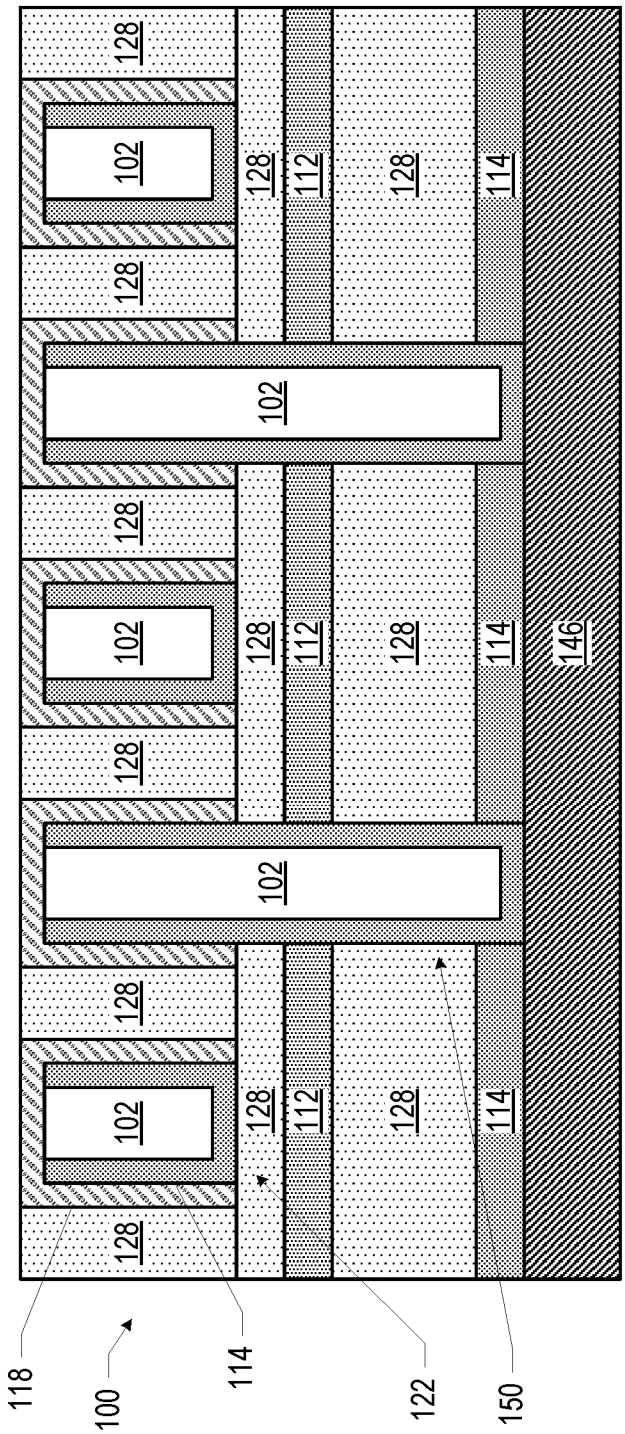

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FIG. 1C

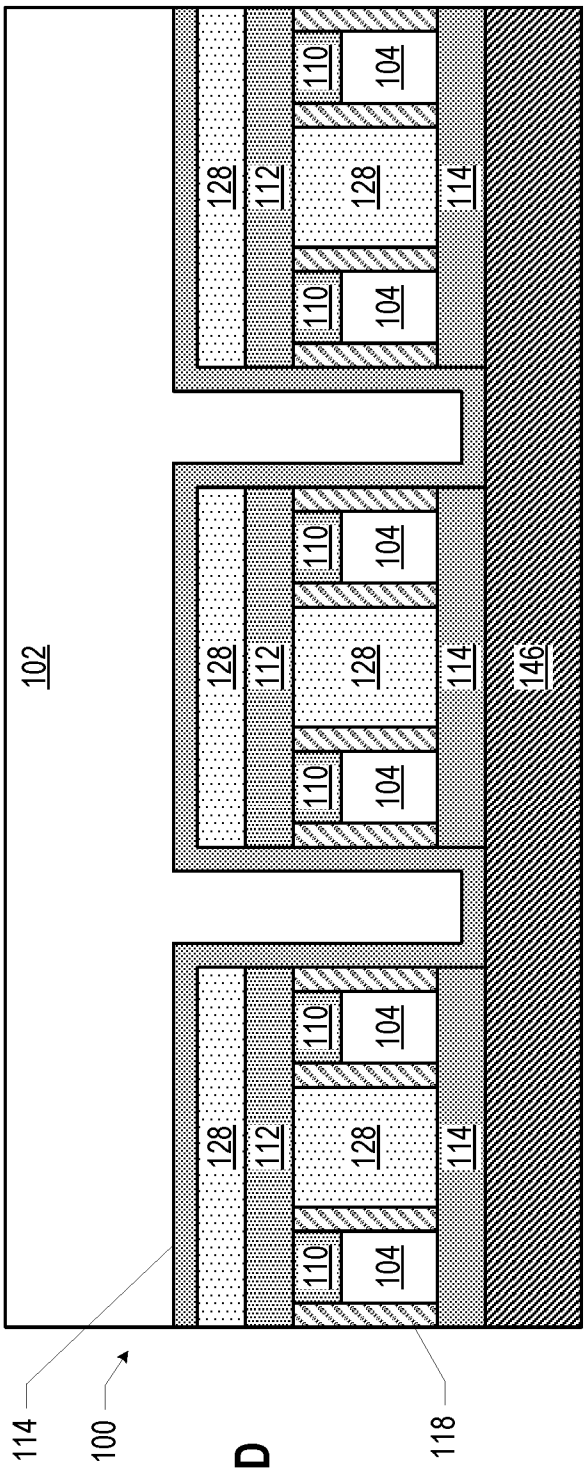

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FIG. 1D

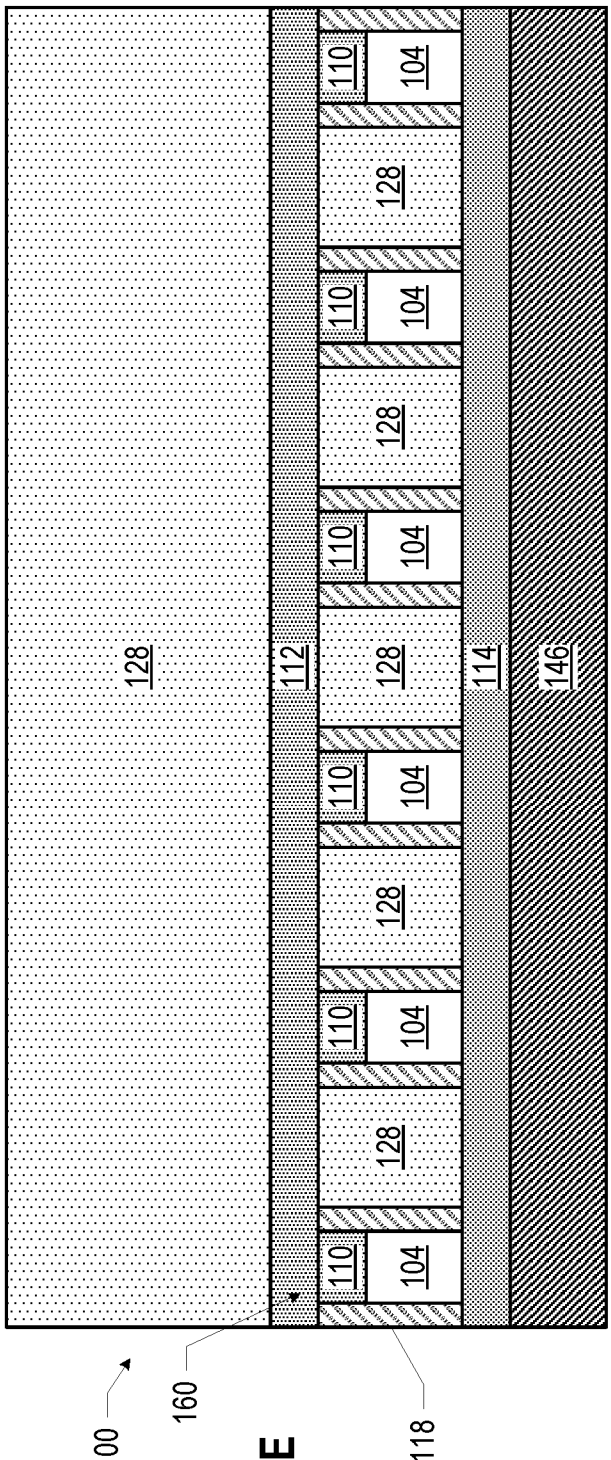

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FIG. 1E

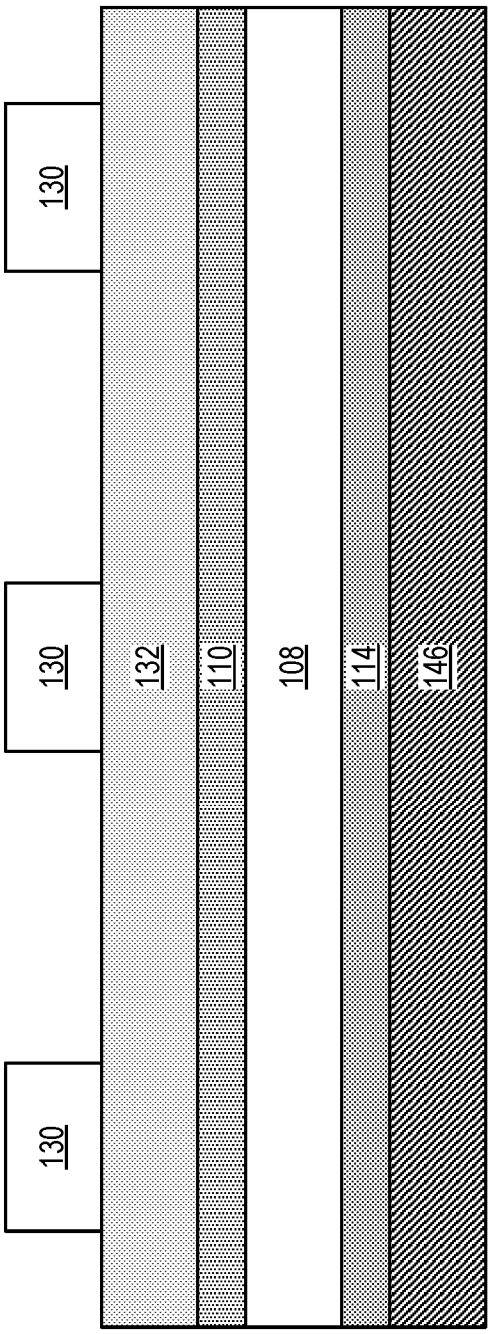


FIG. 2A

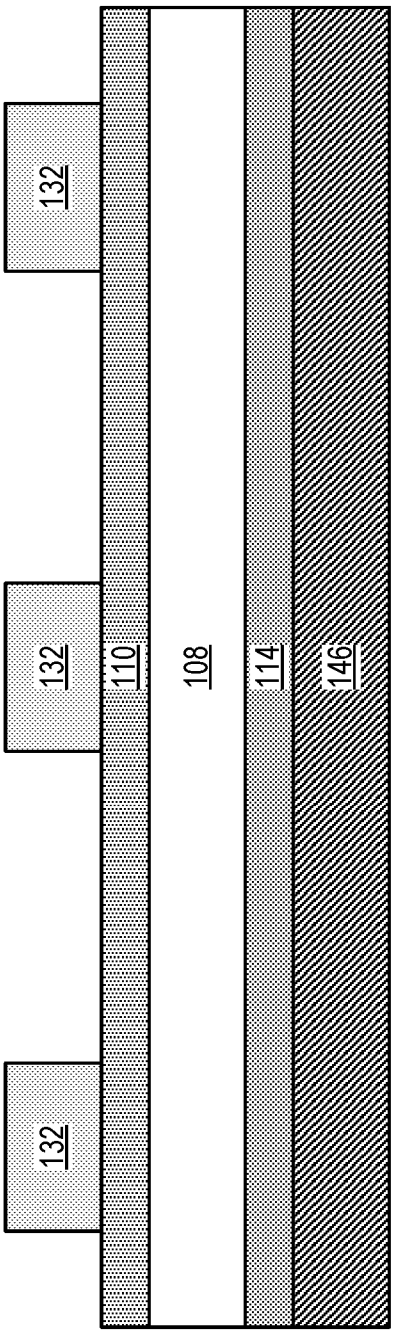


FIG. 2B

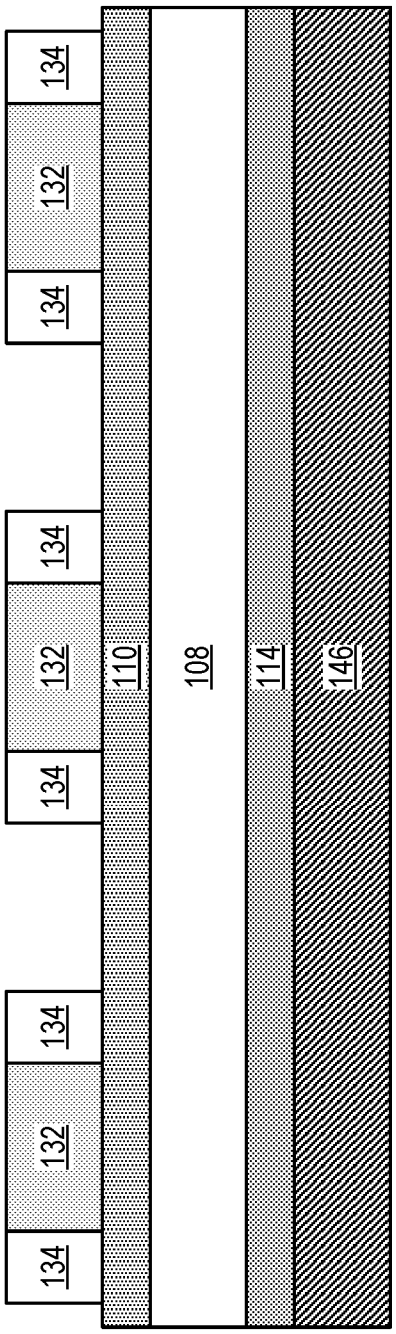

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FIG. 2C

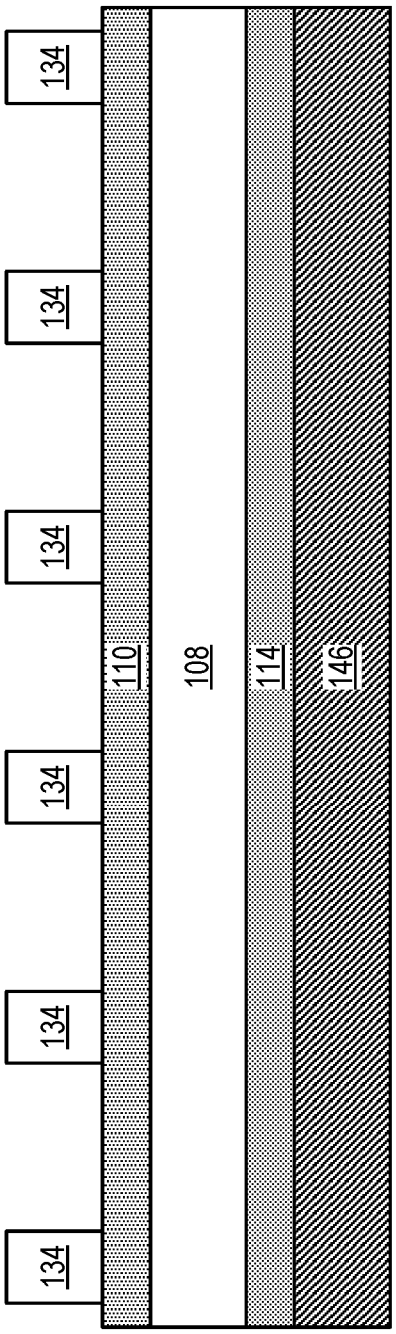

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FIG. 2D

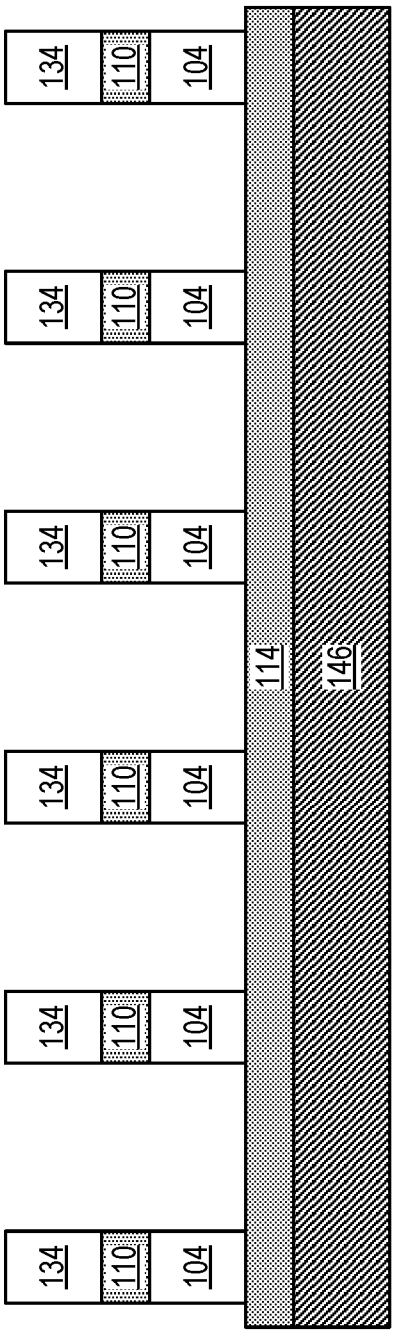


FIG.2E

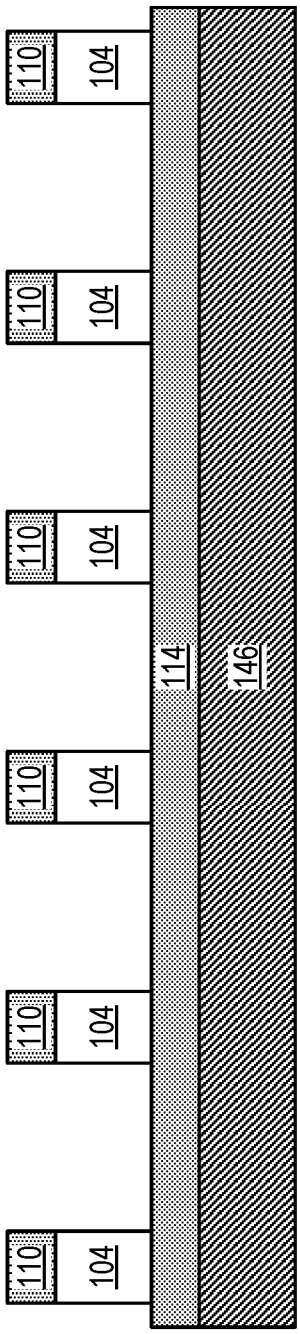


FIG. 2F

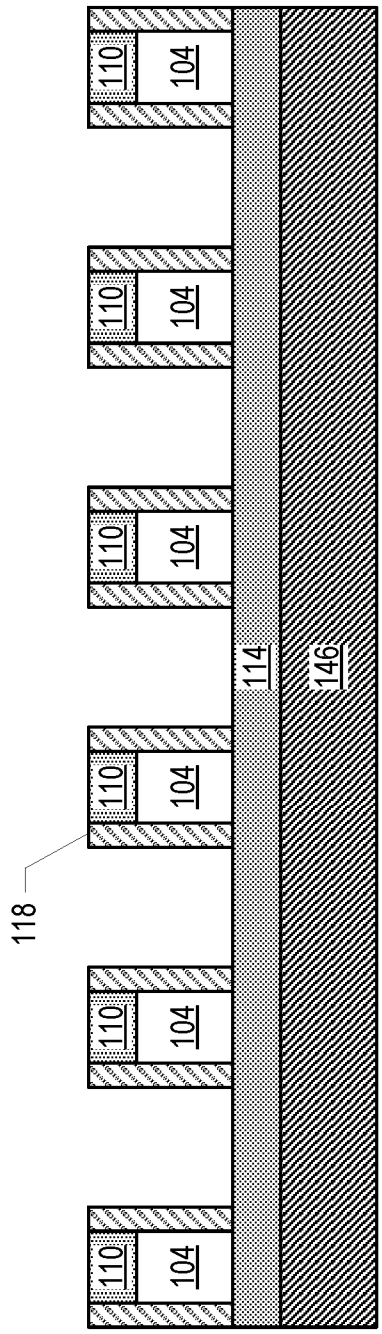


FIG. 2G

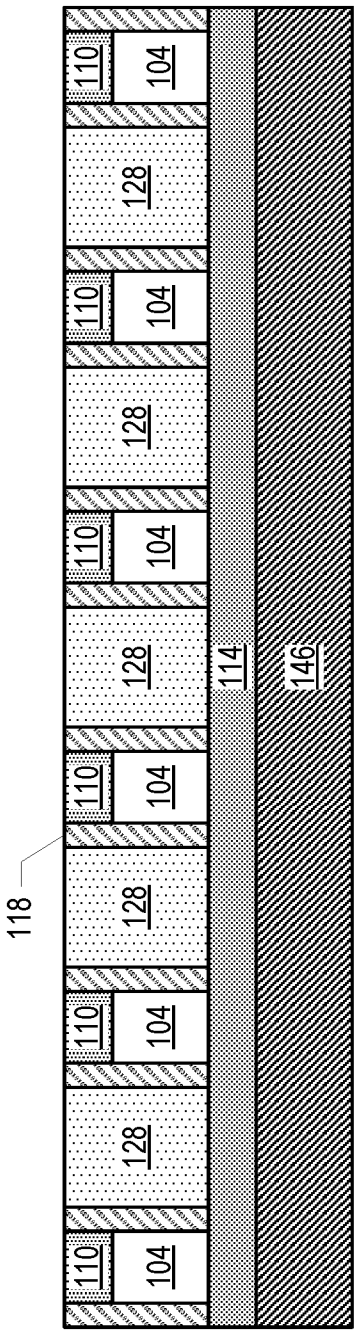


FIG. 2H

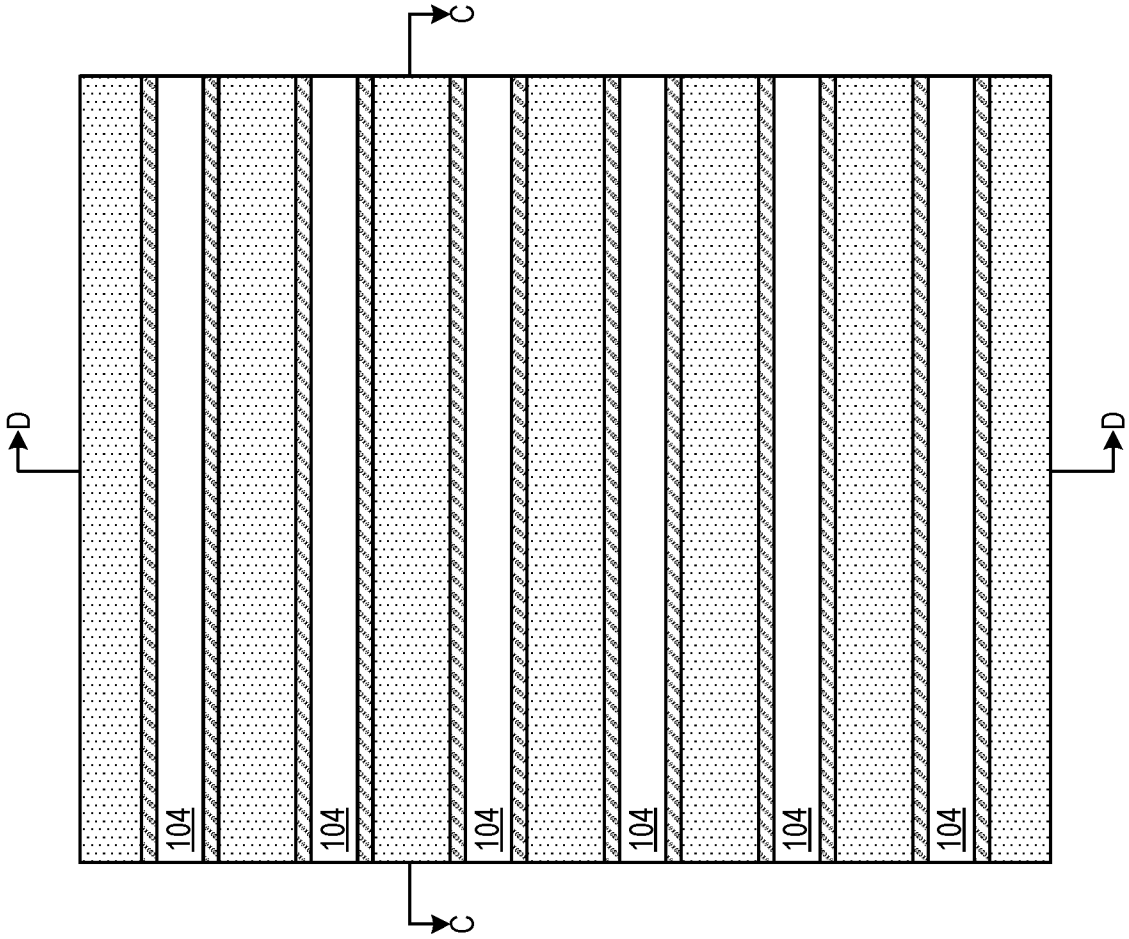


FIG. 2I

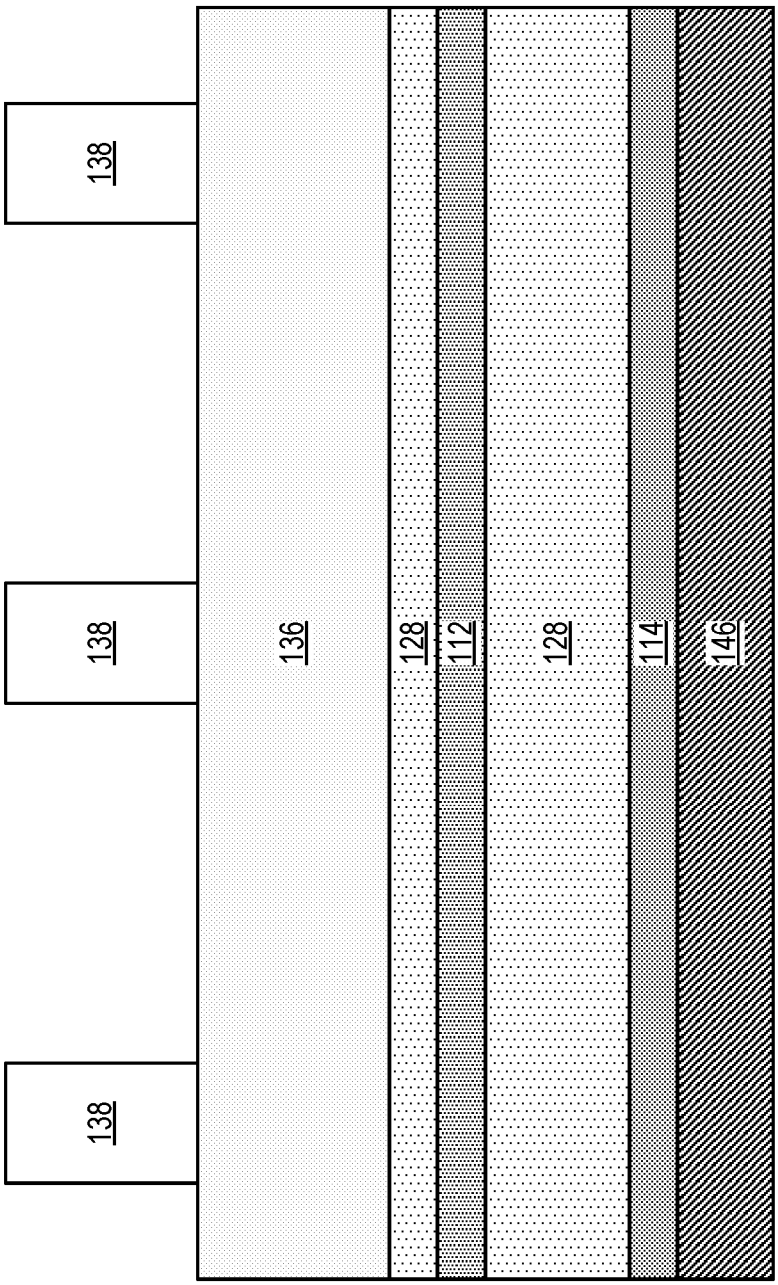


FIG. 2J

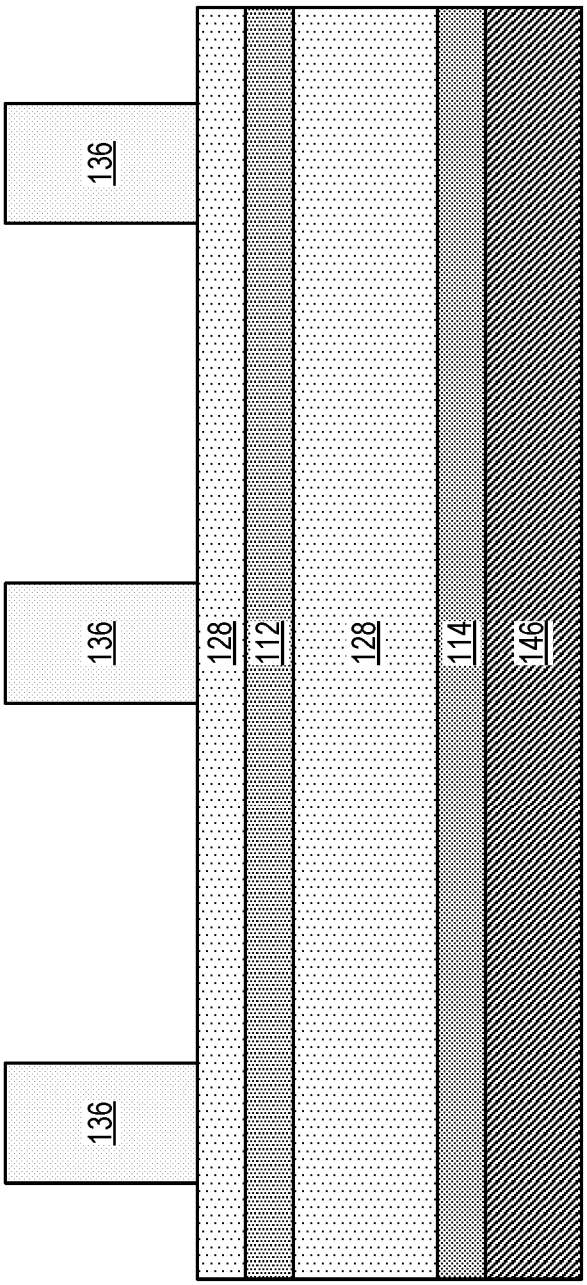


FIG. 2K

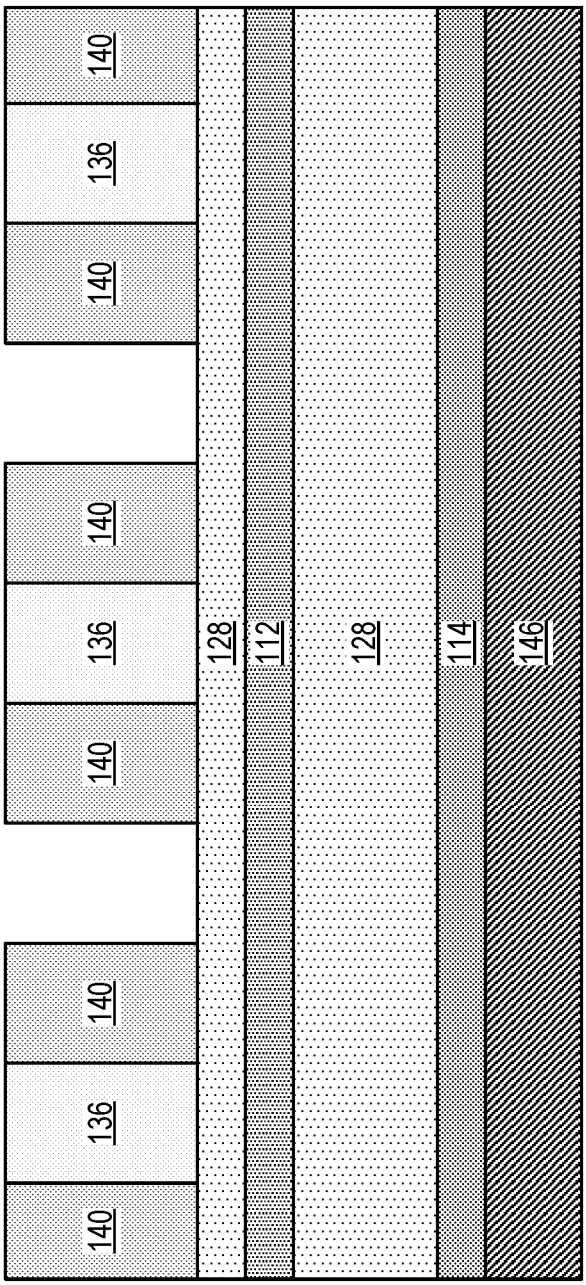


FIG. 2L

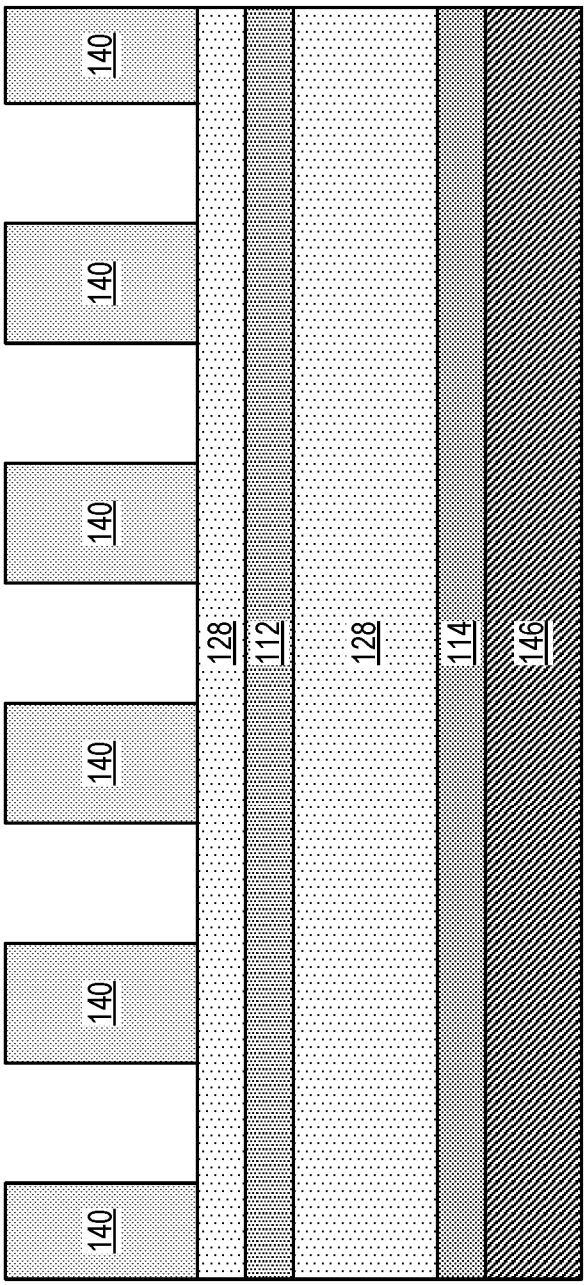


FIG. 2M

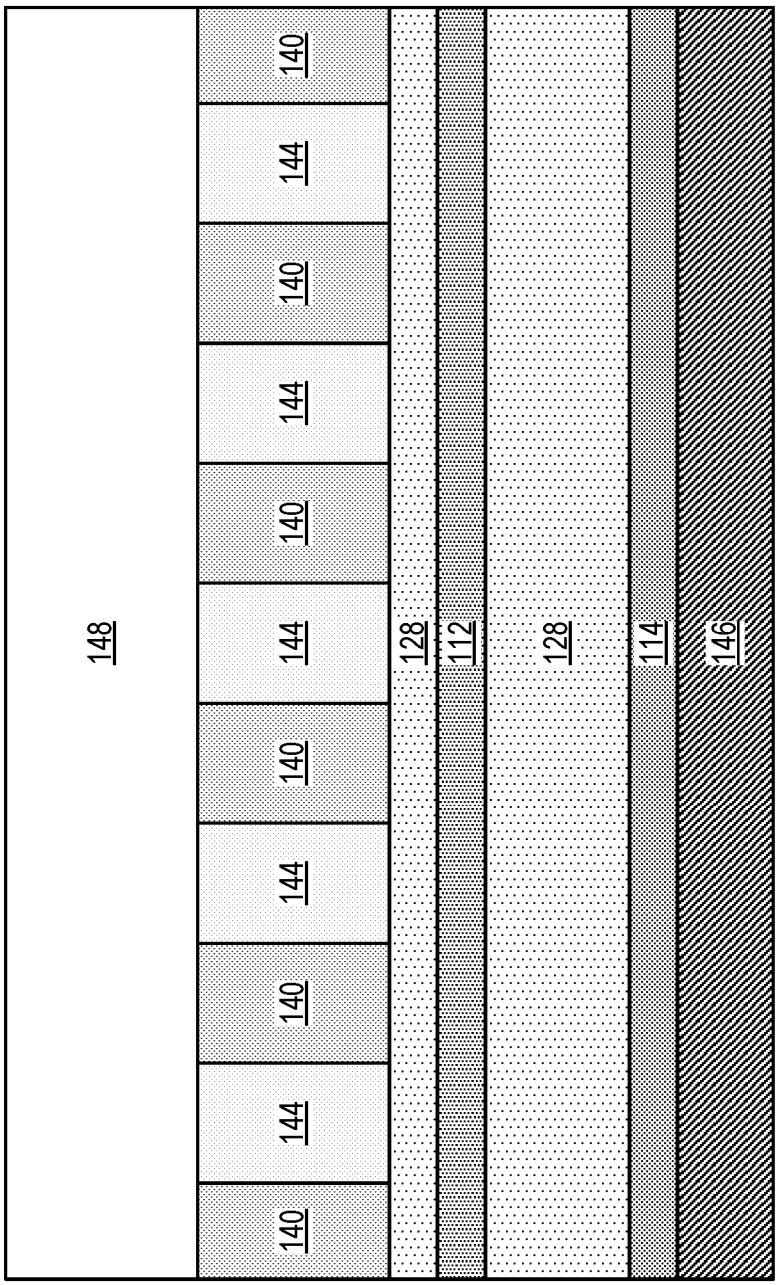

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FIG. 2N

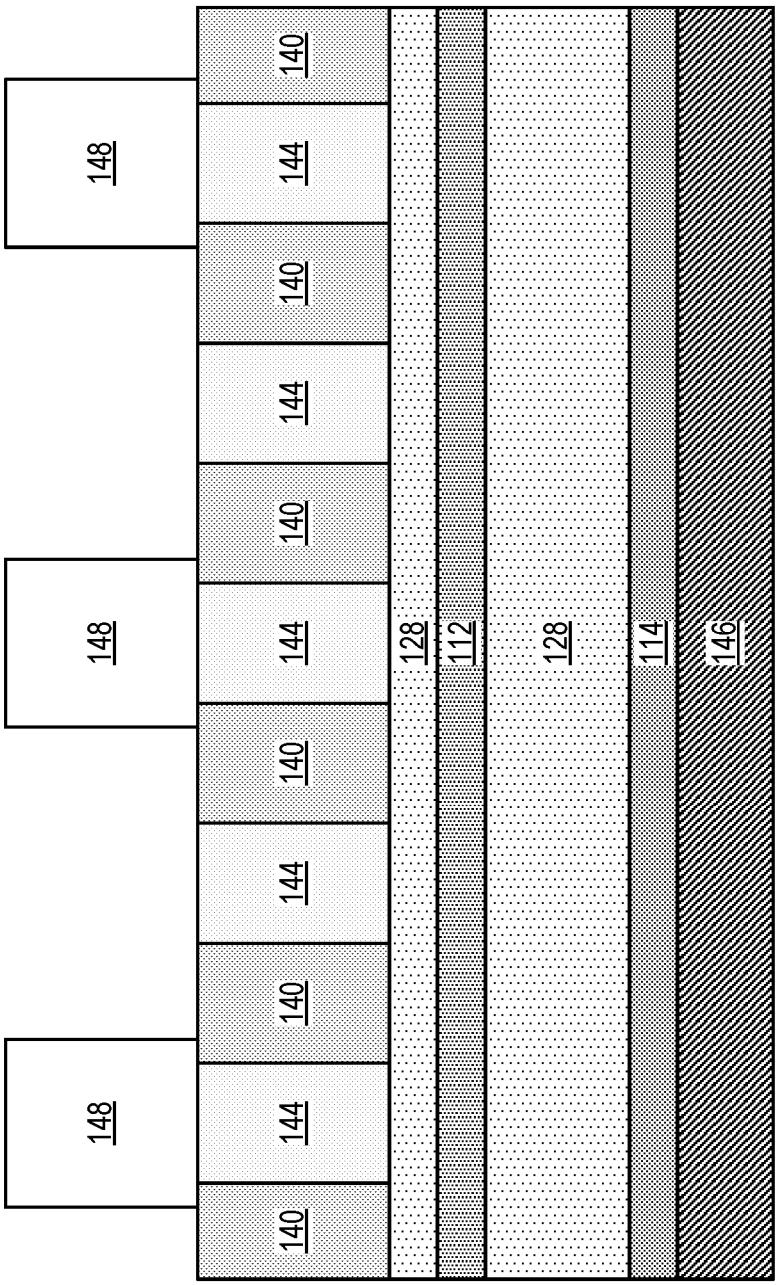

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FIG. 2O

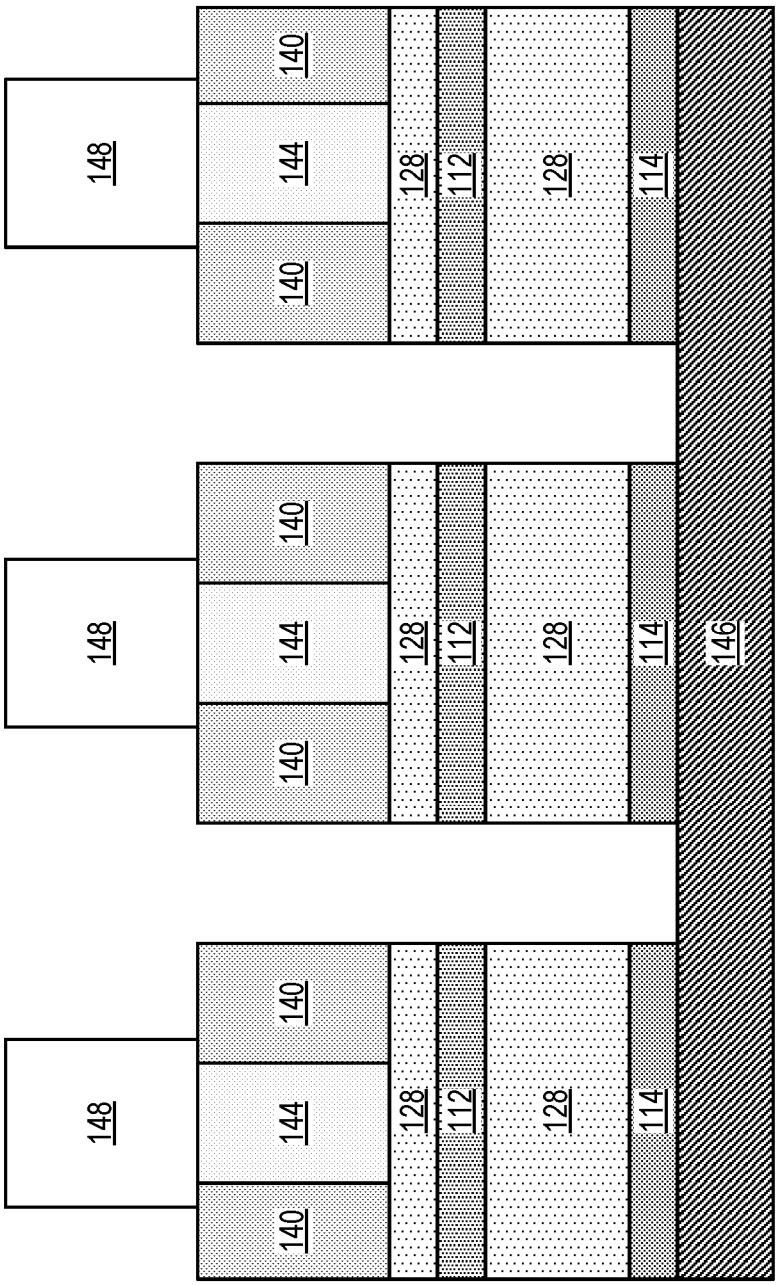


FIG. 2P

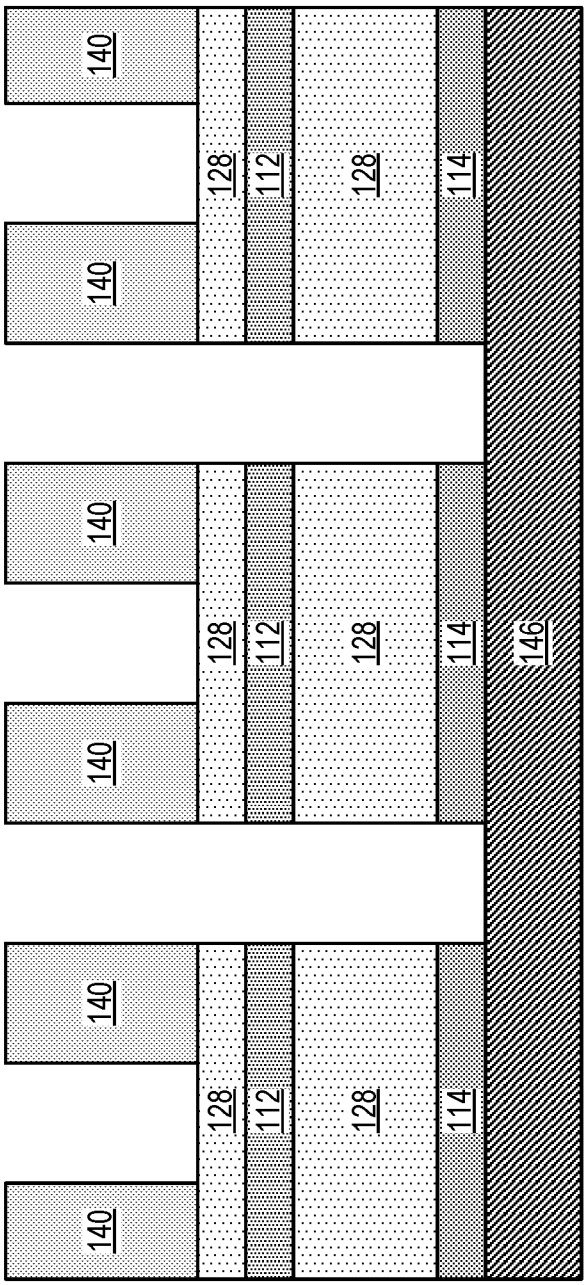


FIG. 2Q

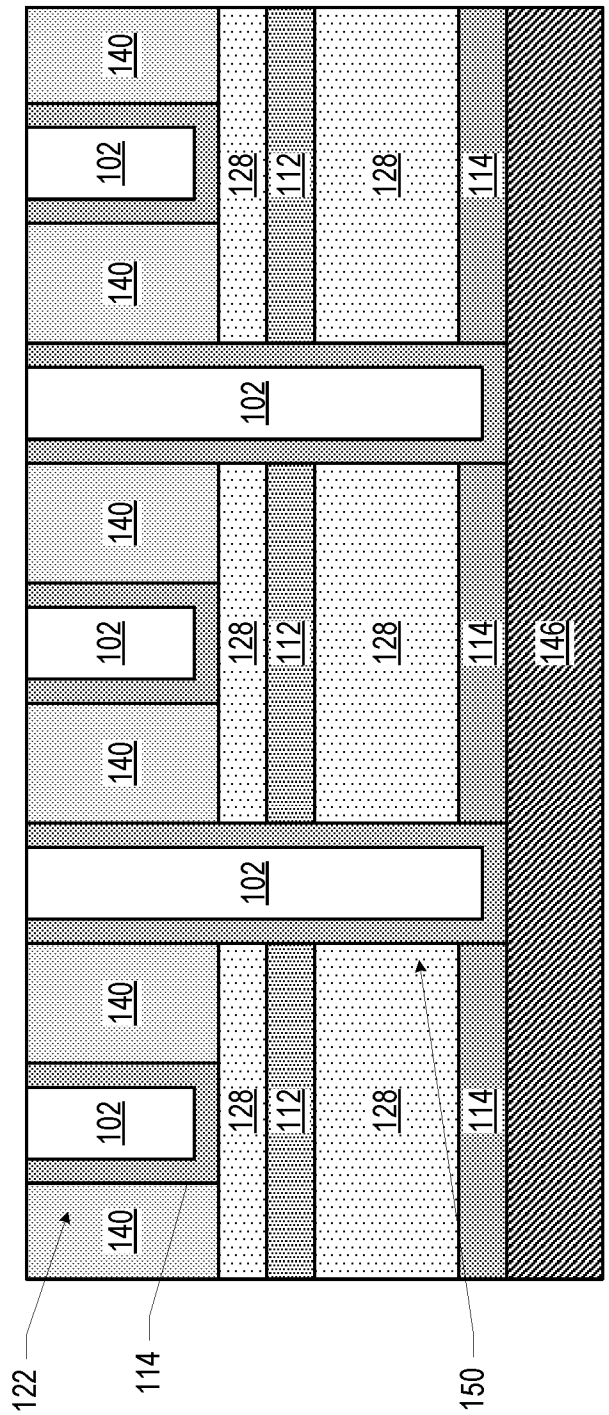

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FIG. 2R

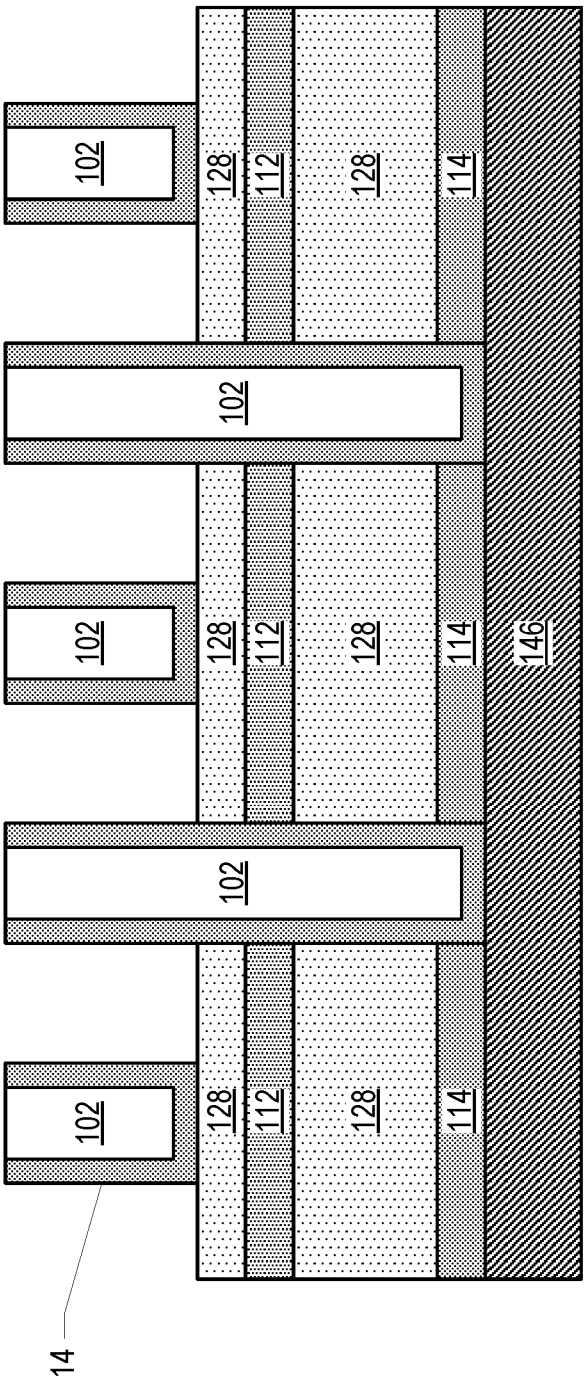

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FIG. 2S

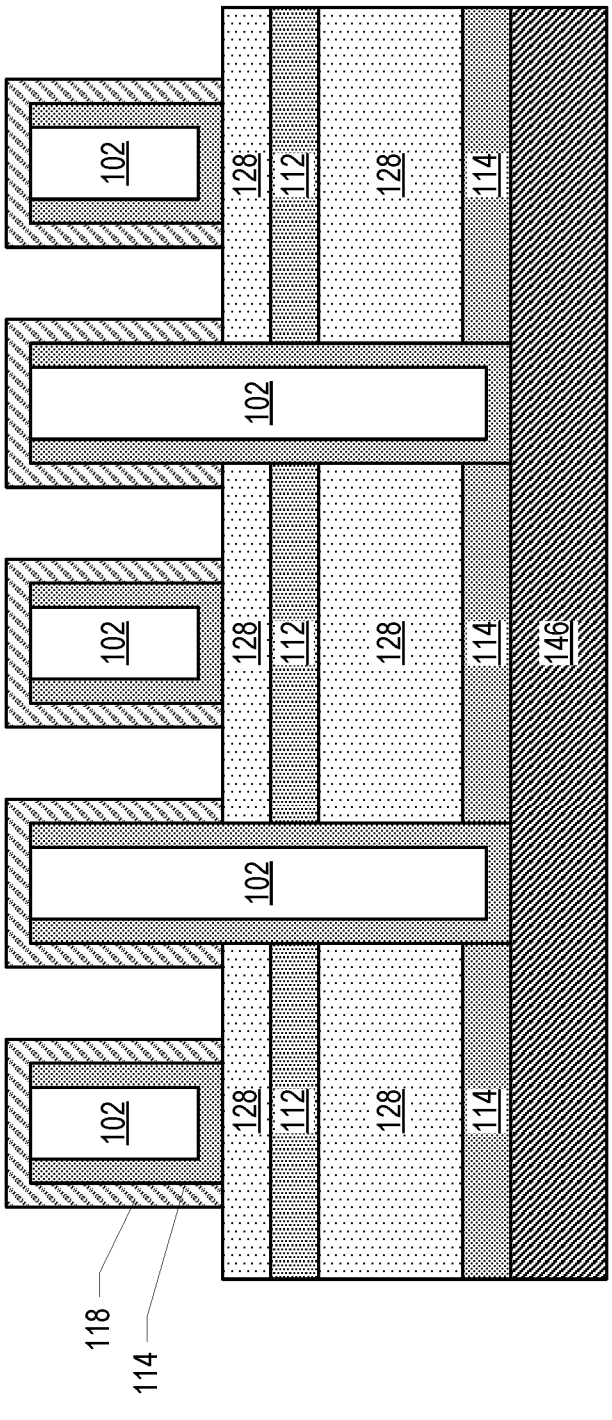


FIG. 2T

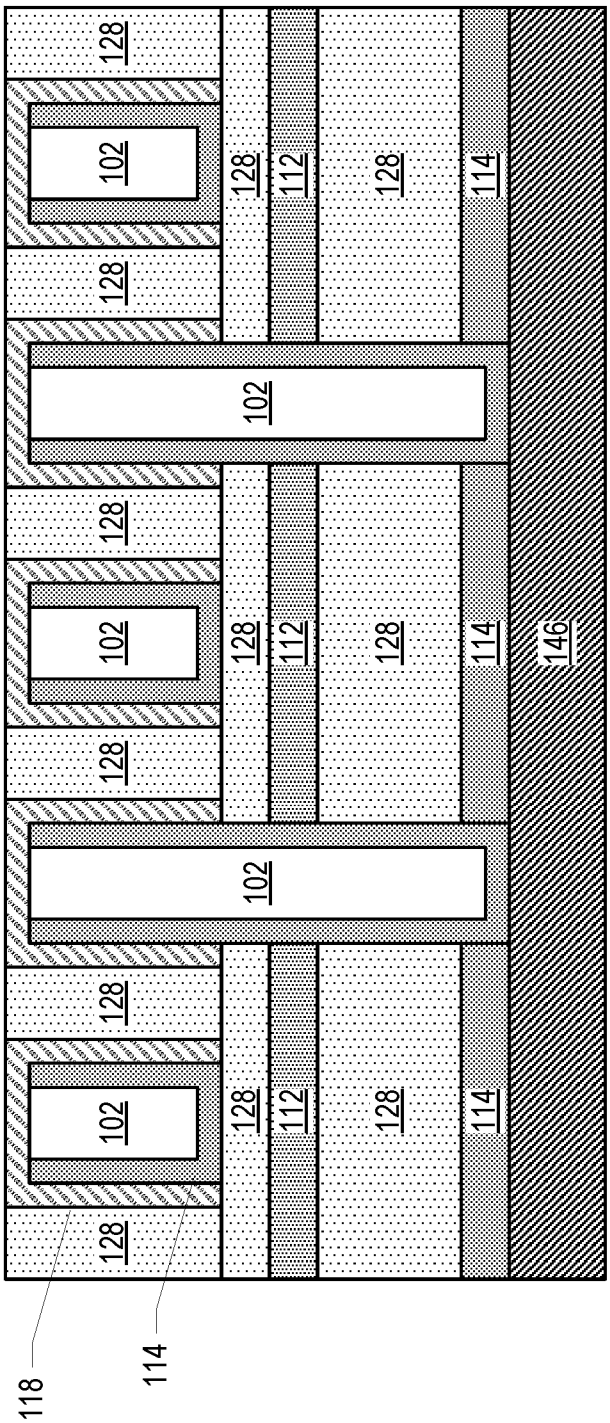


FIG. 2U

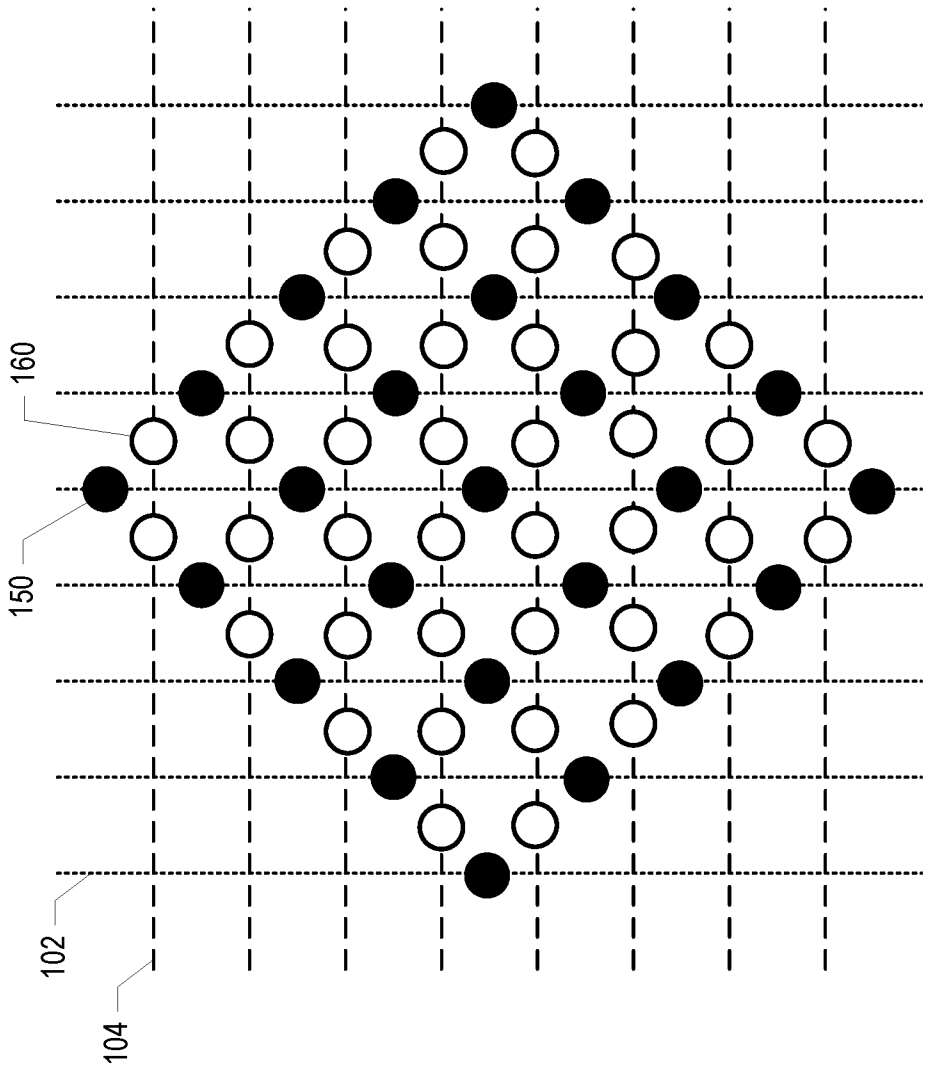


FIG. 3

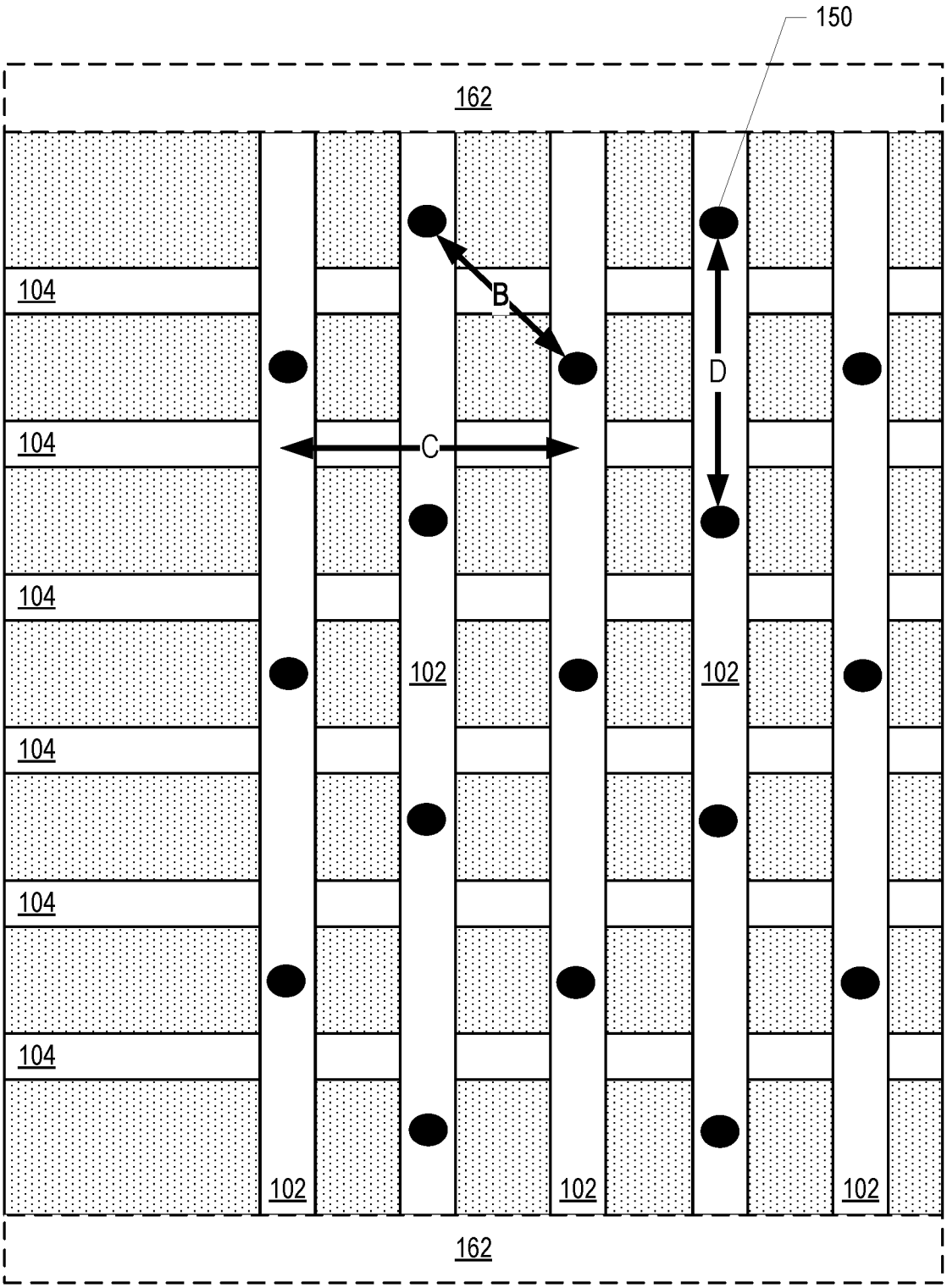


FIG. 4A

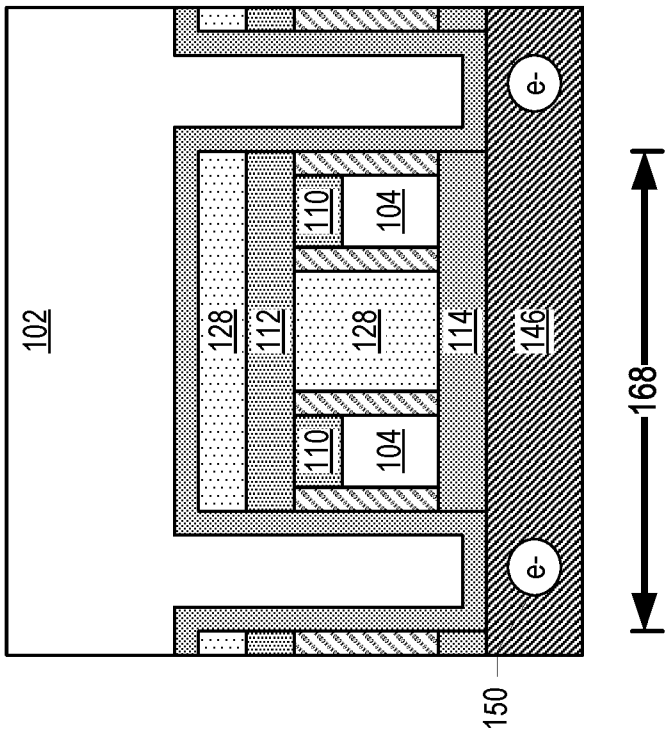


FIG. 4D

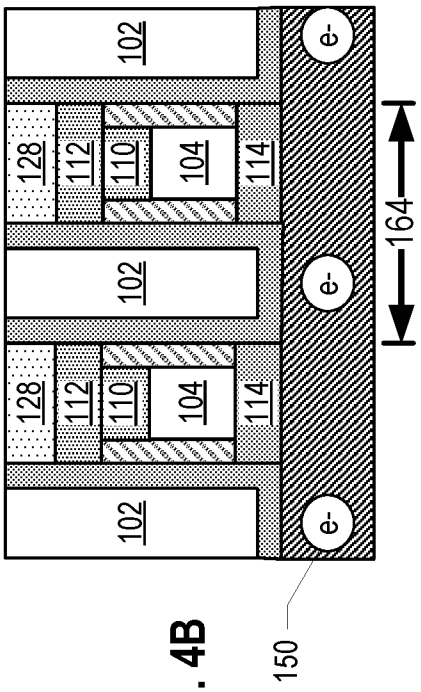


FIG. 4B

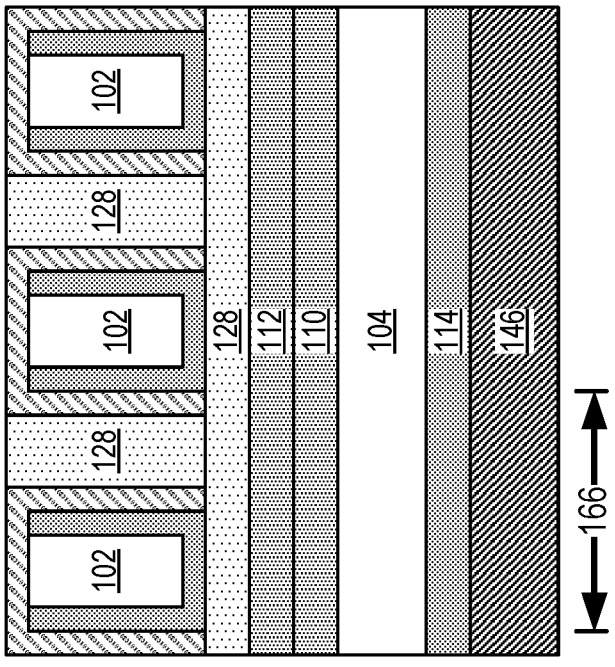


FIG. 4C

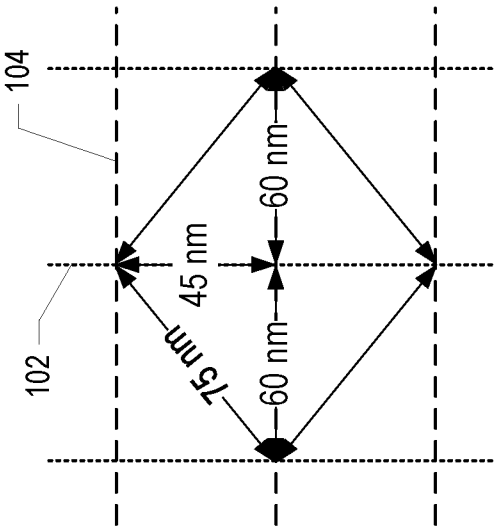


FIG. 5C

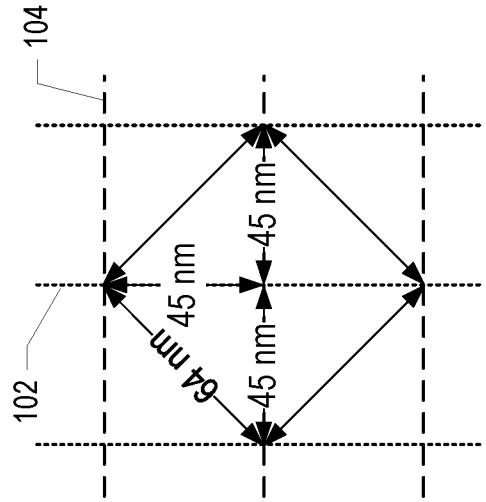


FIG. 5B

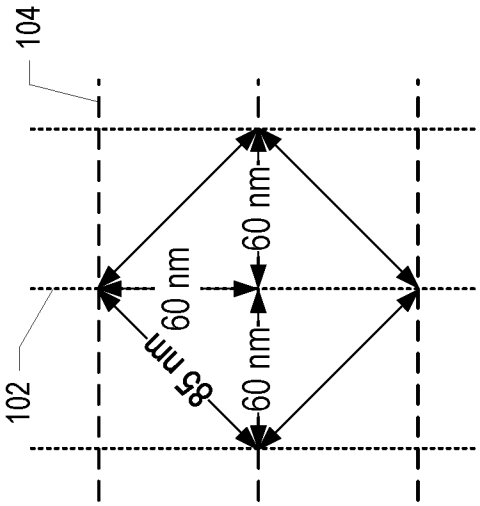


FIG. 5A

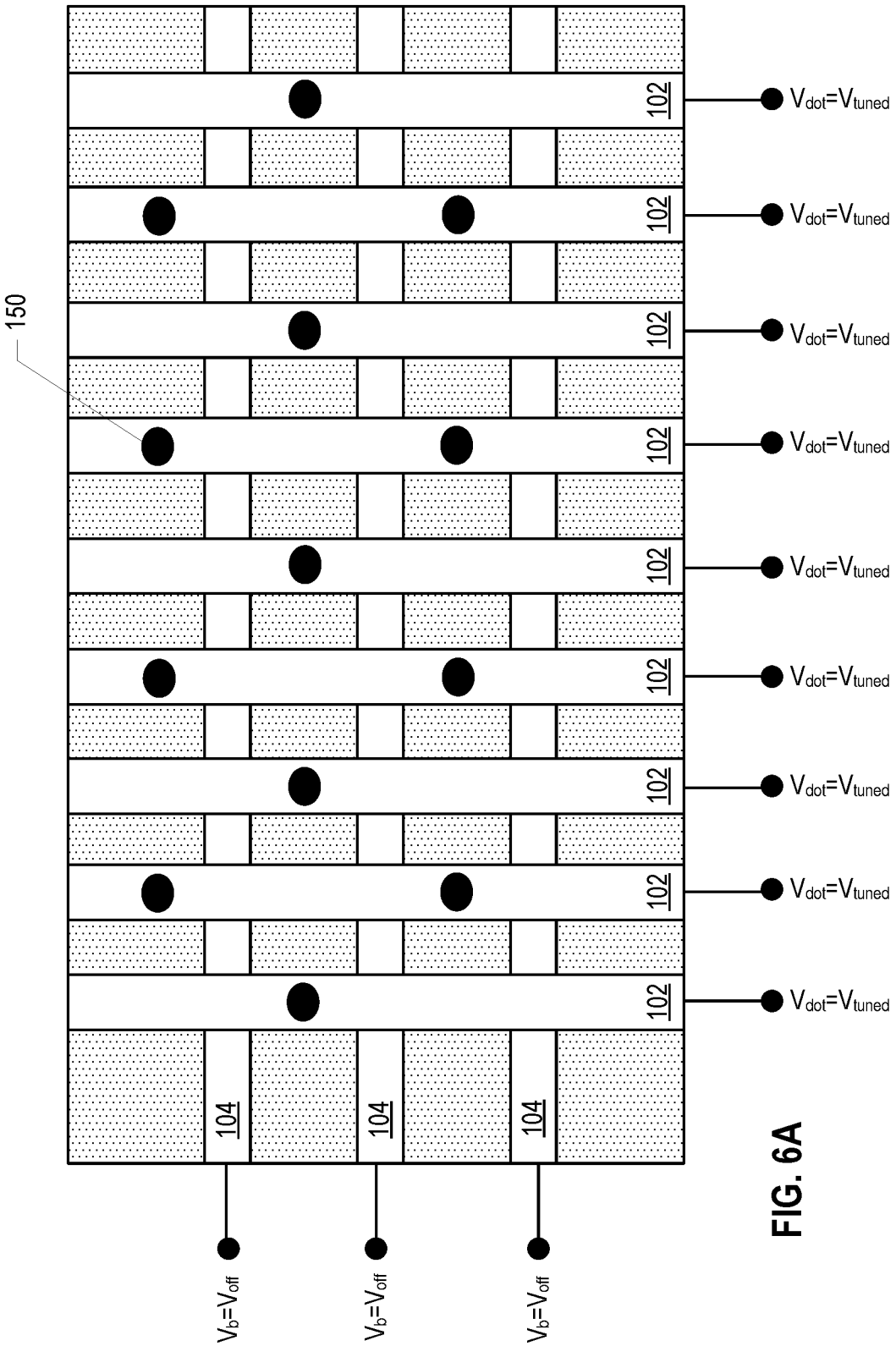

150
102
102
102
102
102
102
102
102
102
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
$V_{dot}=V_{tuned}$
104
104
104
$V_b=V_{off}$
$V_b=V_{off}$
$V_b=V_{off}$

FIG. 6A

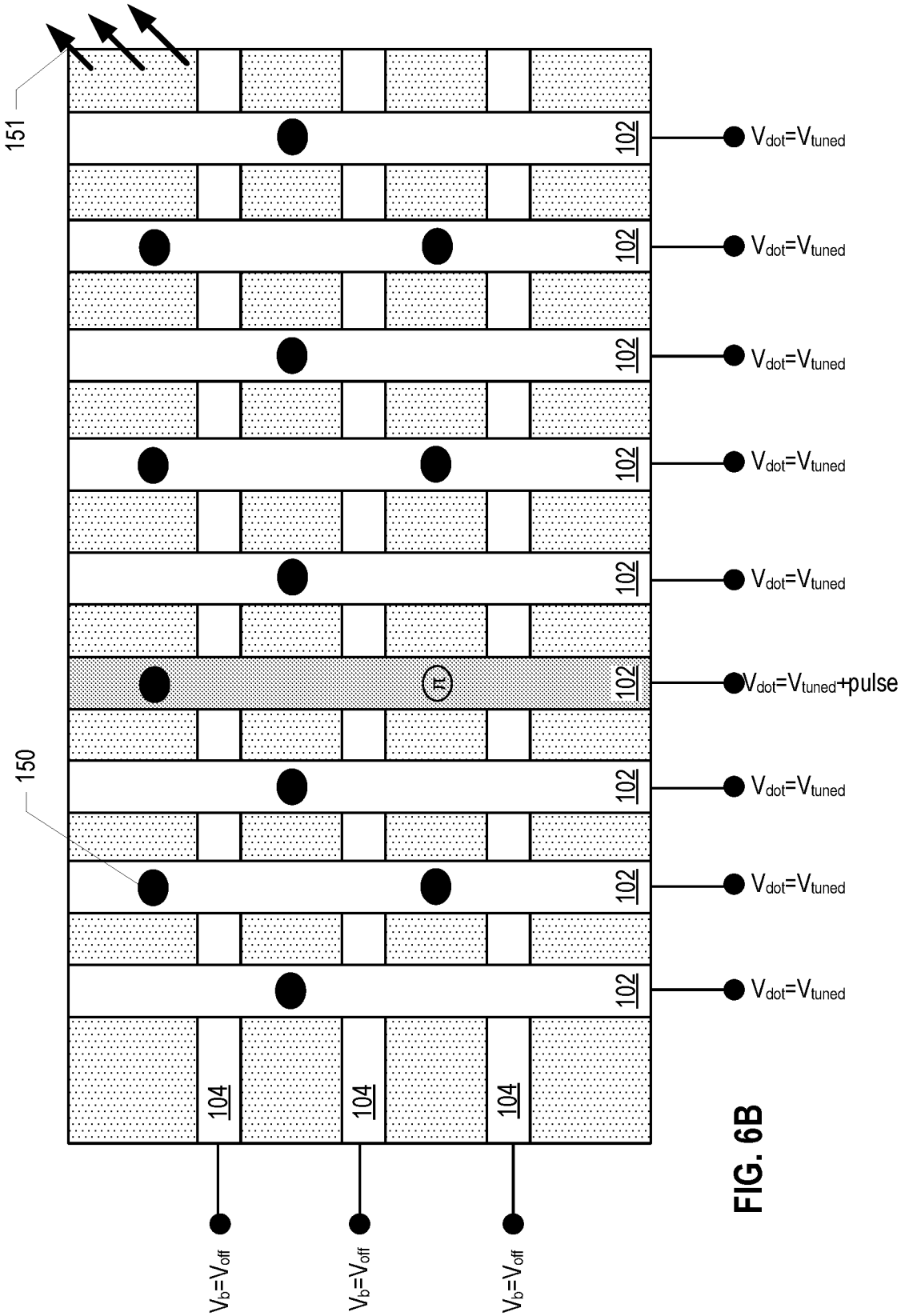


FIG. 6B

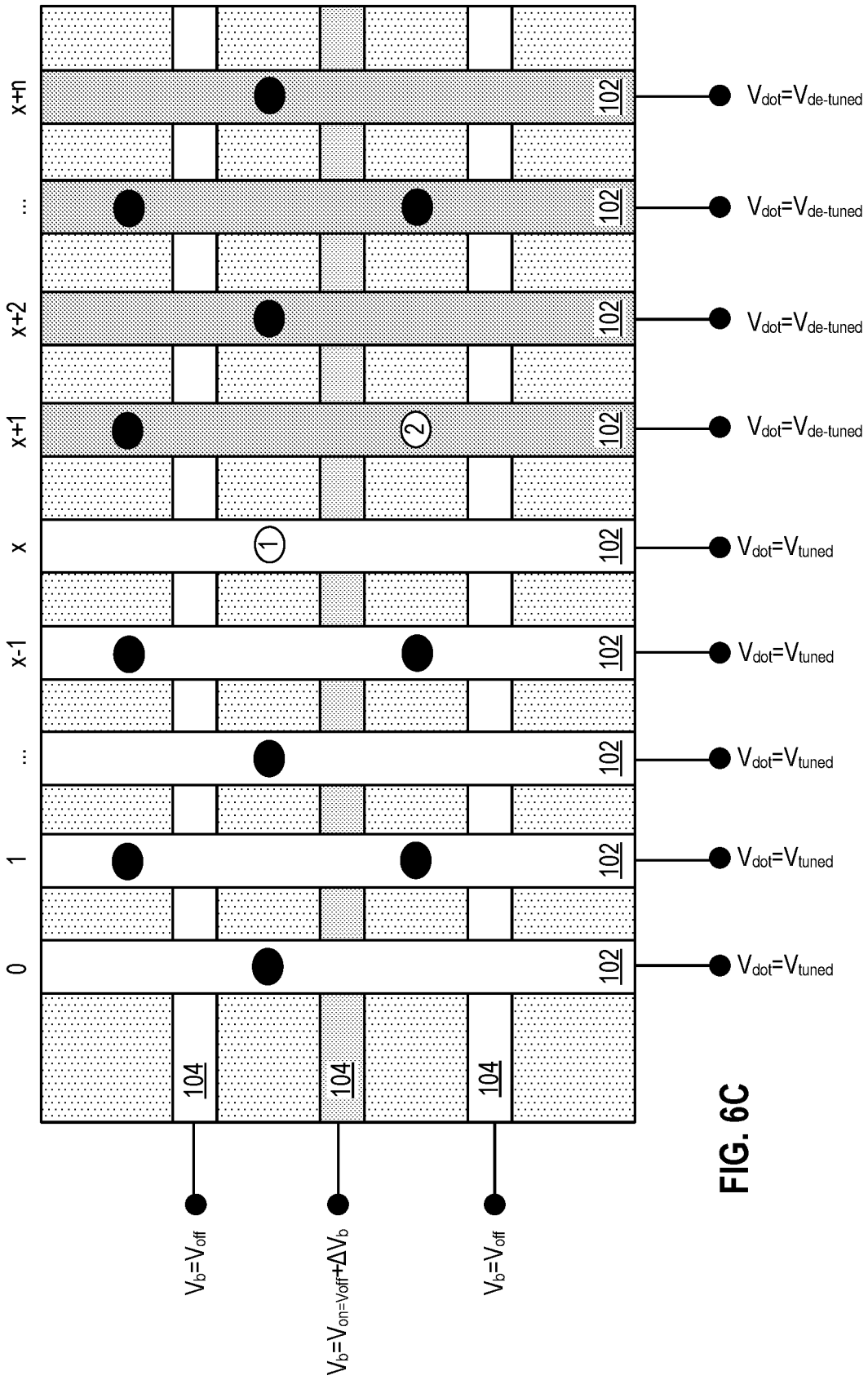

x+n
...
x+2
x+1
x
x-1
...
1
0
102
104
1
2
$V_{dot}=V_{de\text{-}tuned}$
$V_{dot}=V_{tuned}$
$V_b=V_{off}$
$V_b=V_{on=Voff}+\Delta V_b$
$V_b=V_{off}$

FIG. 6C

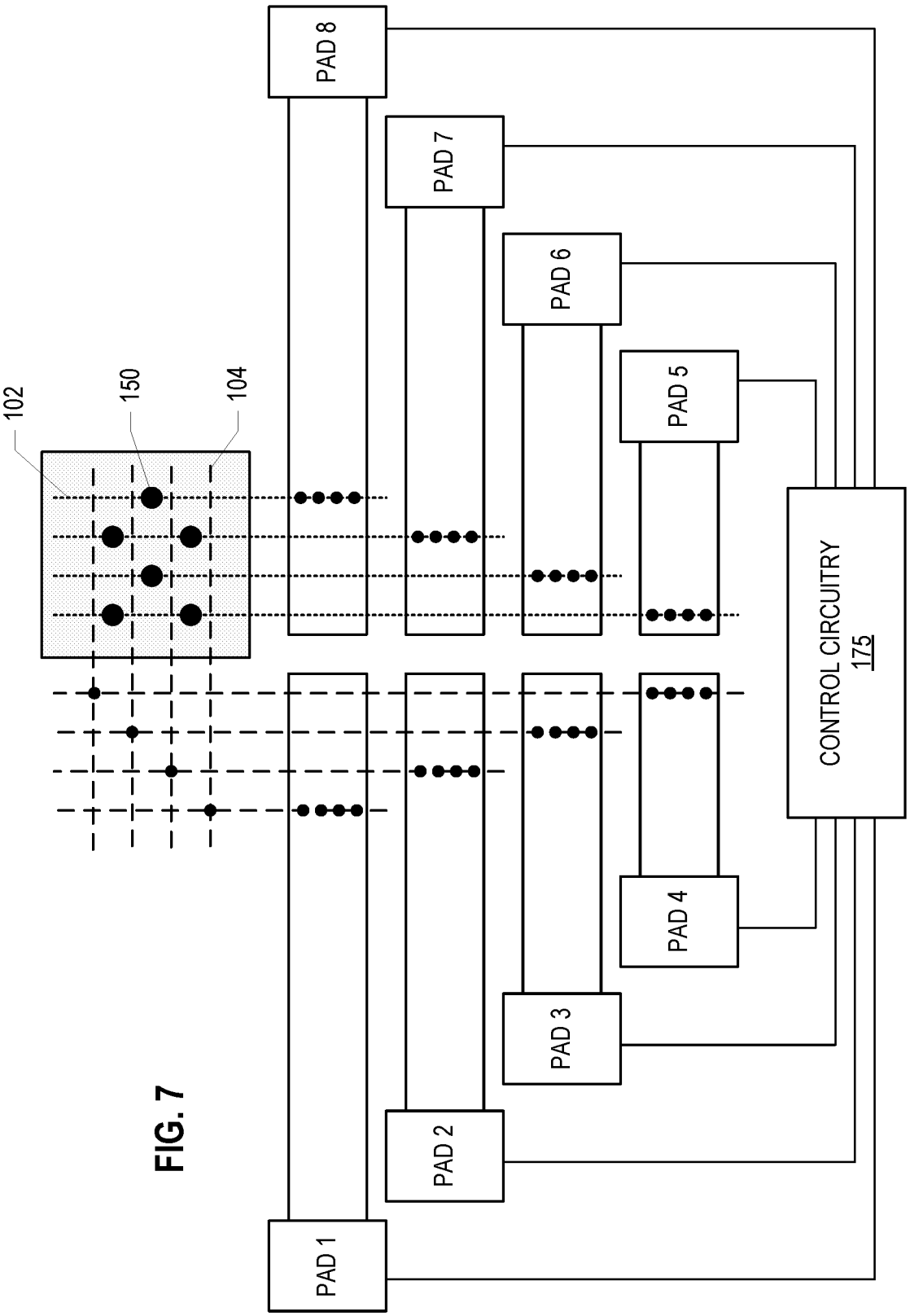

PAD 8
PAD 7
PAD 6
PAD 5
PAD 4
PAD 3
PAD 2
PAD 1
CONTROL CIRCUITRY
175
102
150
104

FIG. 7

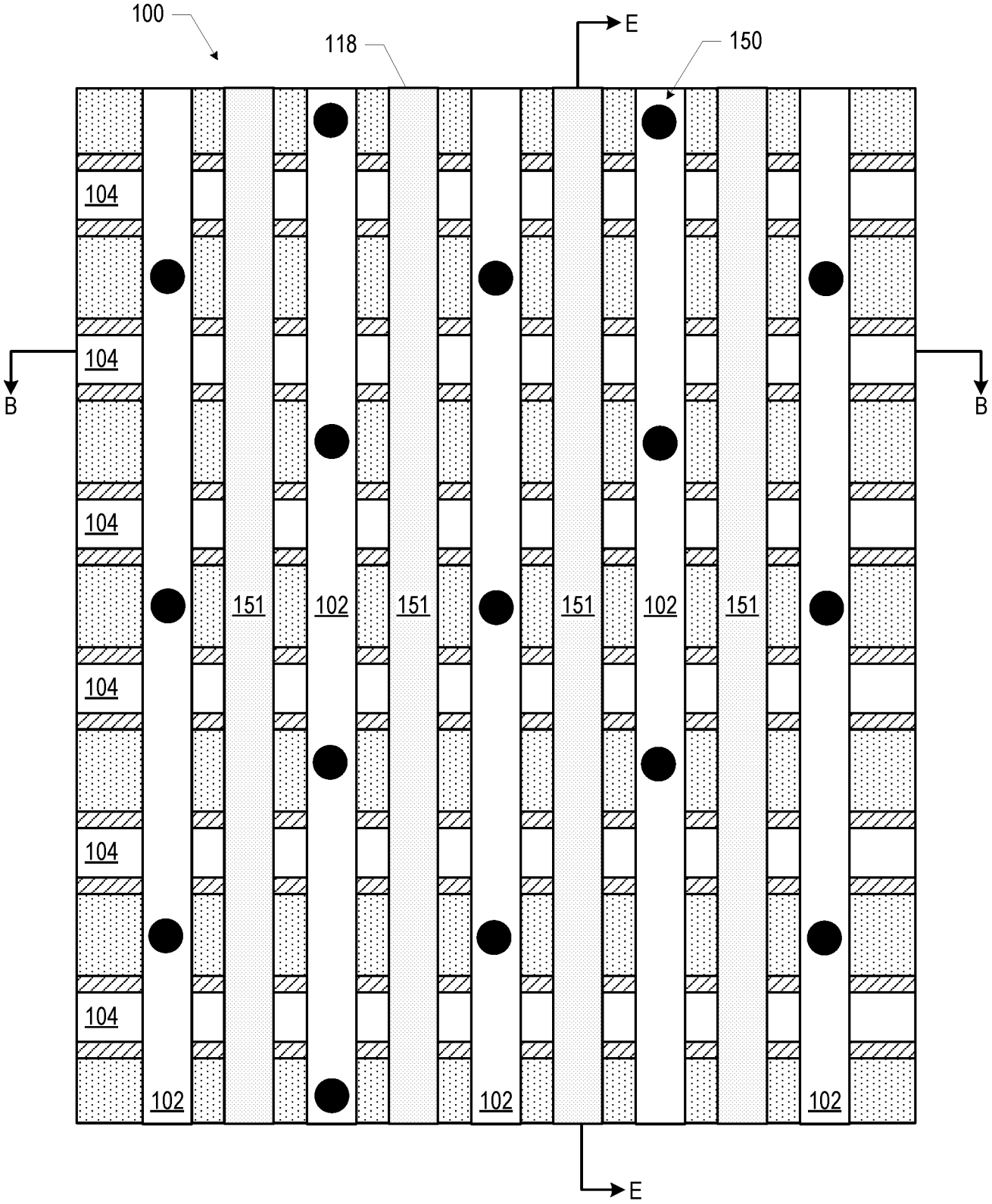

100
118
E
150
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104
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104
104
B
B
151
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102
102
E

FIG. 8A

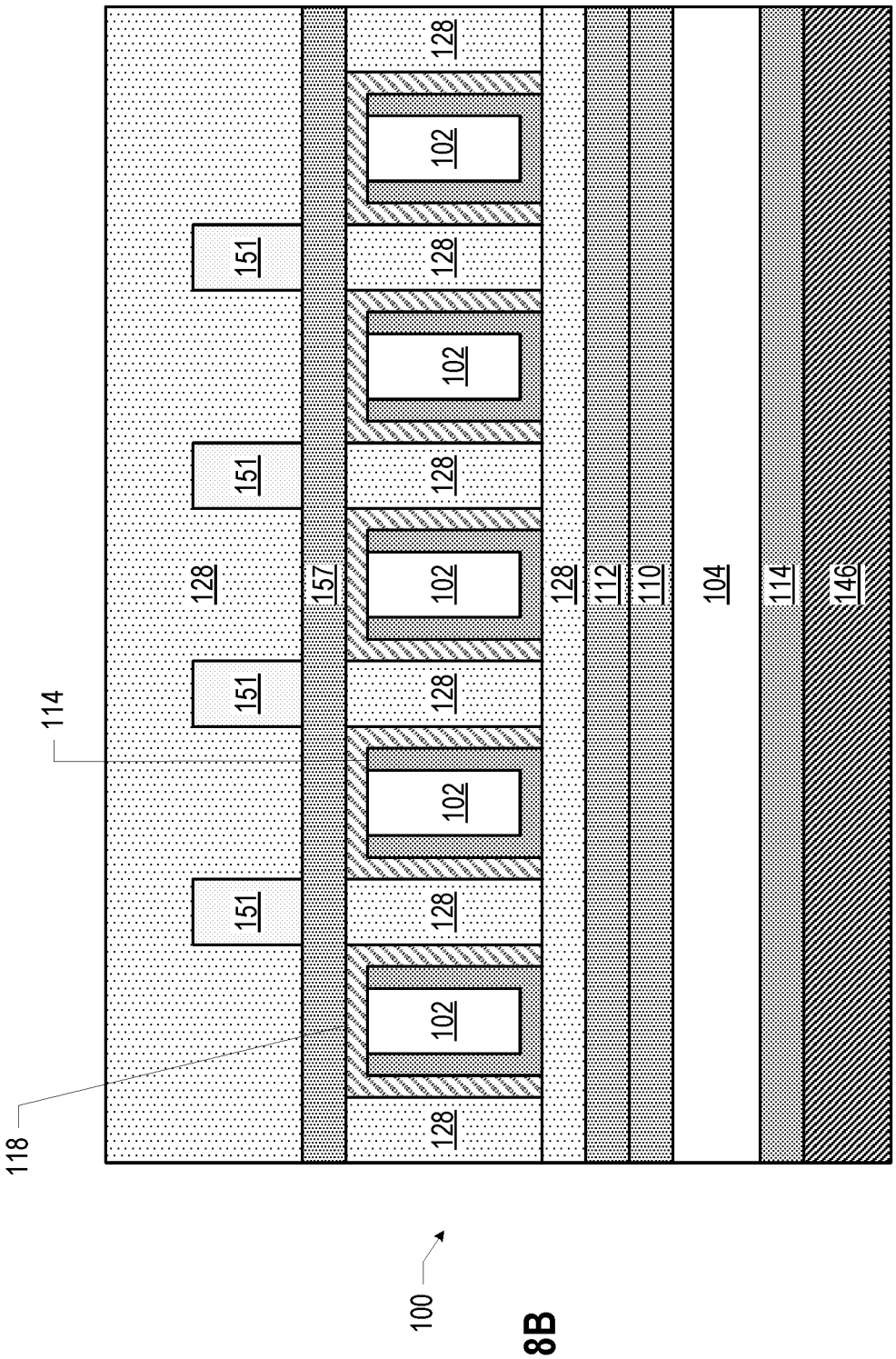

100
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114
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128
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FIG. 8B

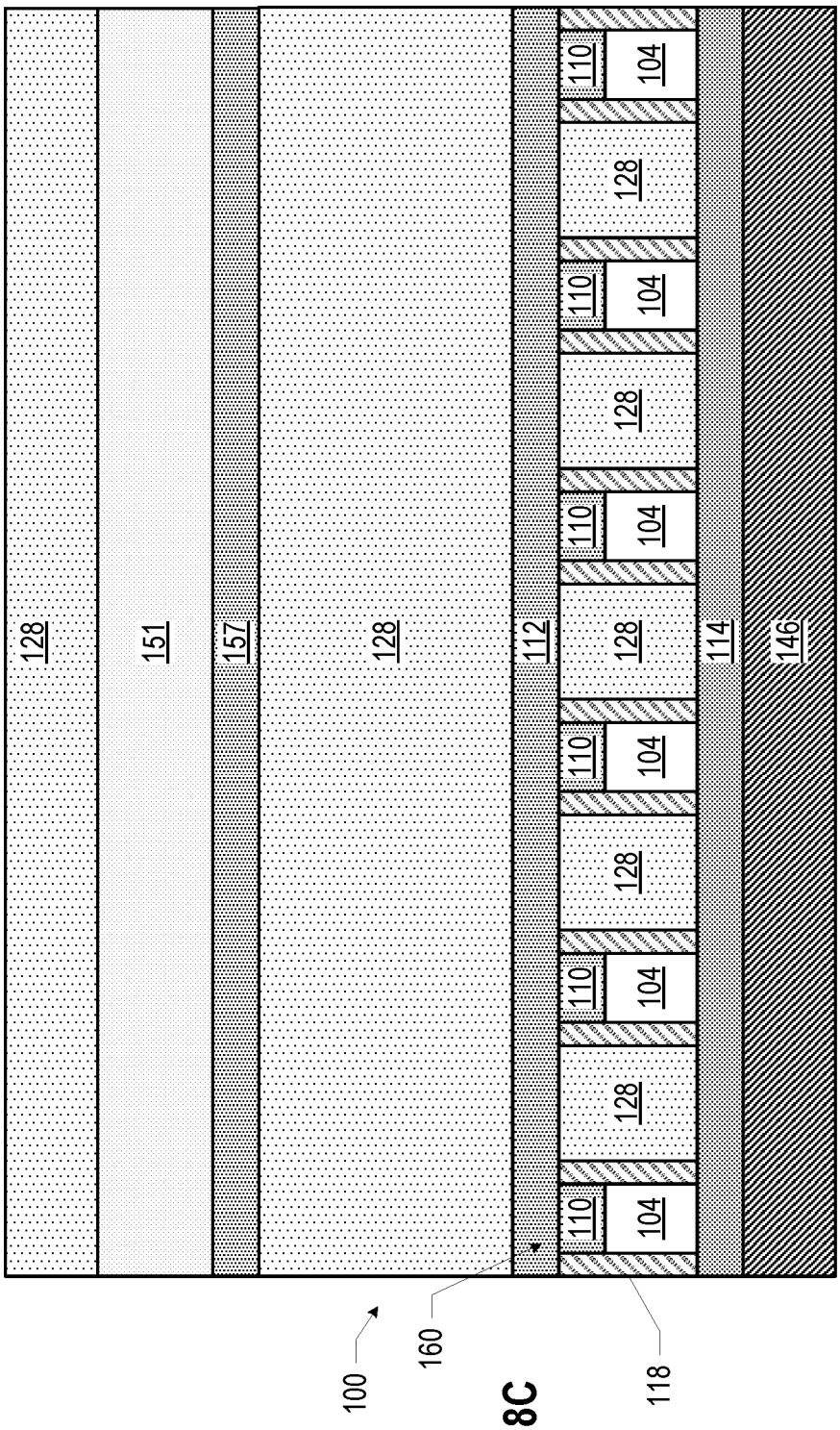

128
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104
128
110
104
128
114
146
100
160
118

FIG. 8C

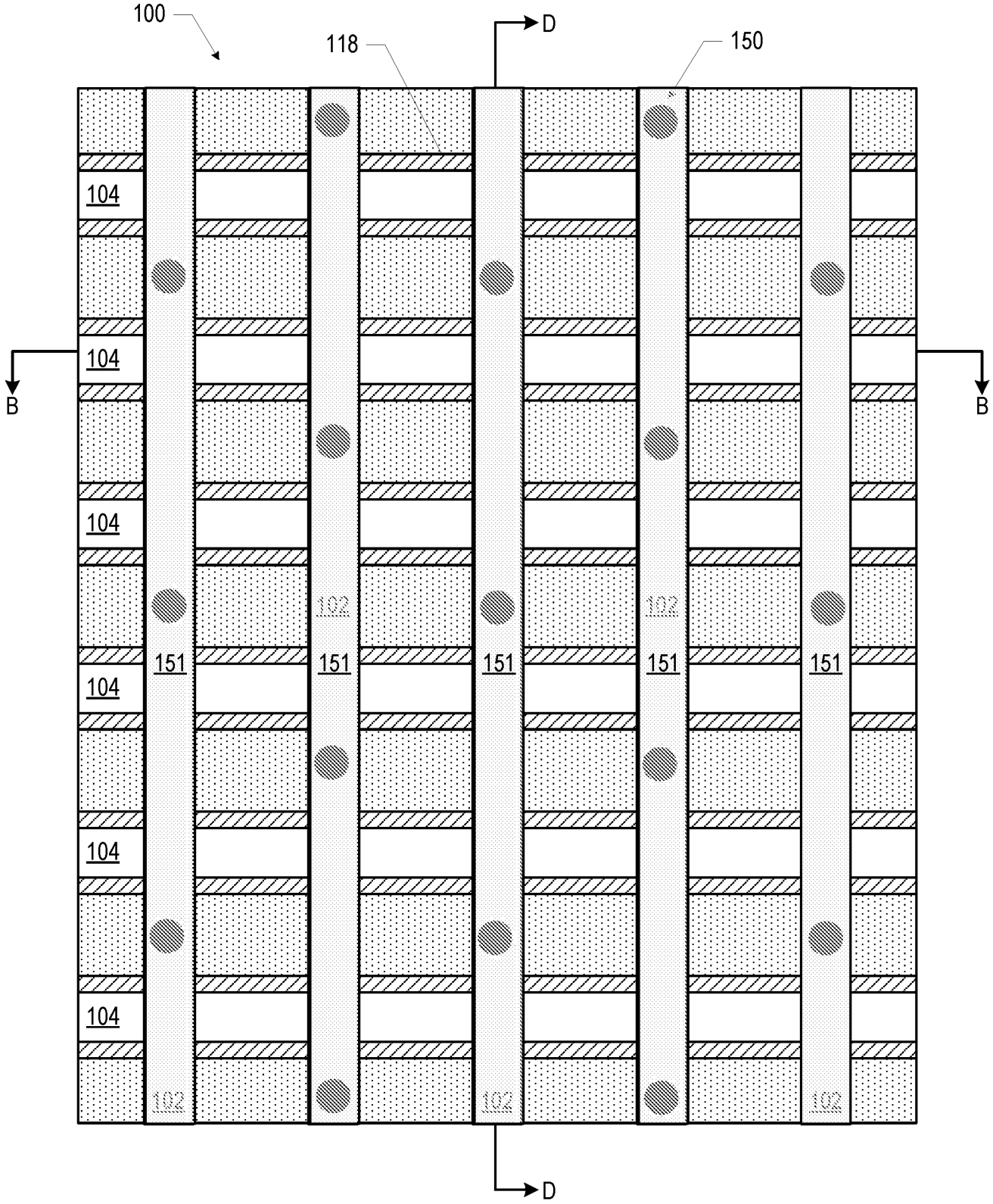

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B
B
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151
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102
D

FIG. 9A

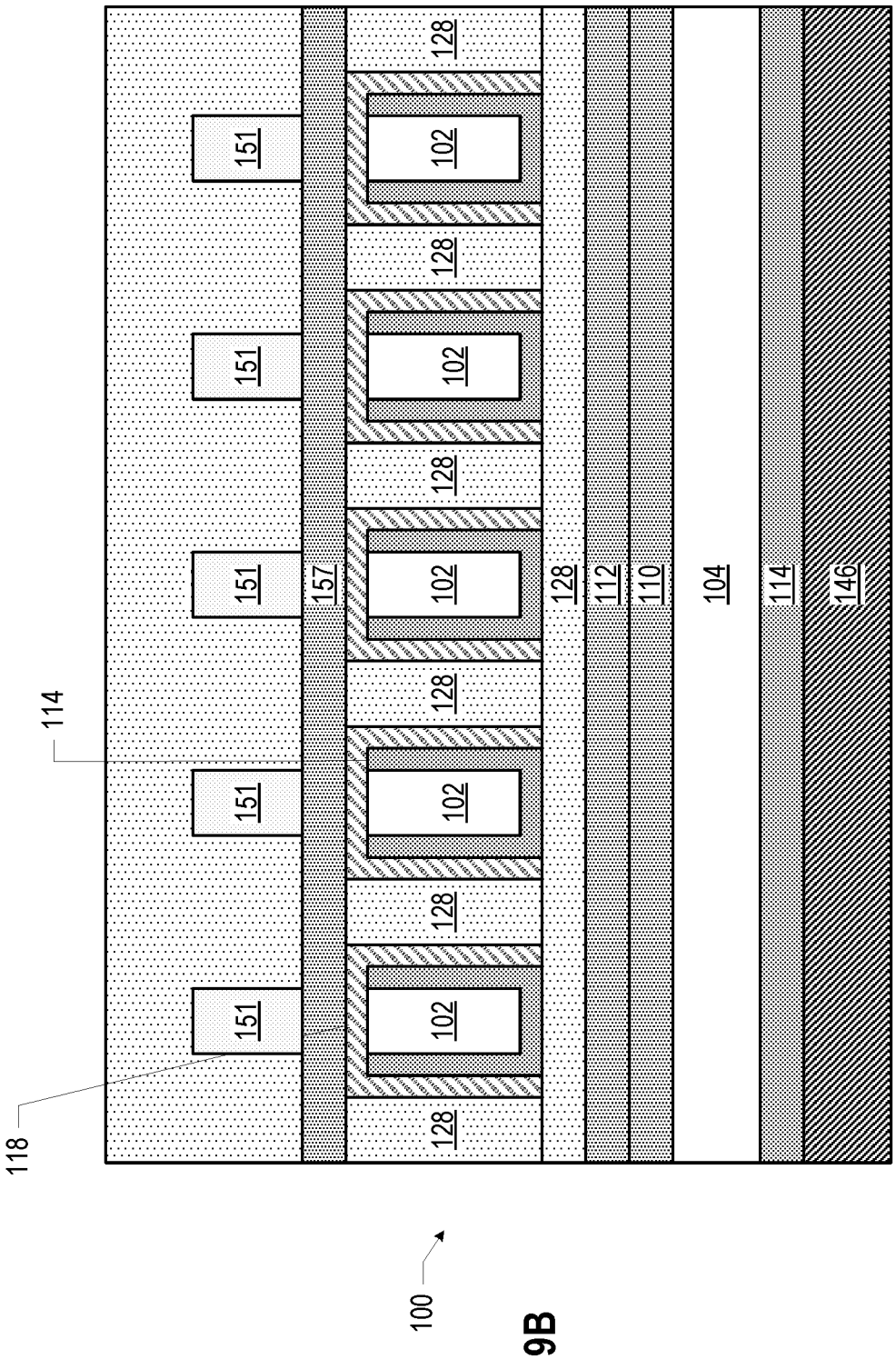

100
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FIG. 9B

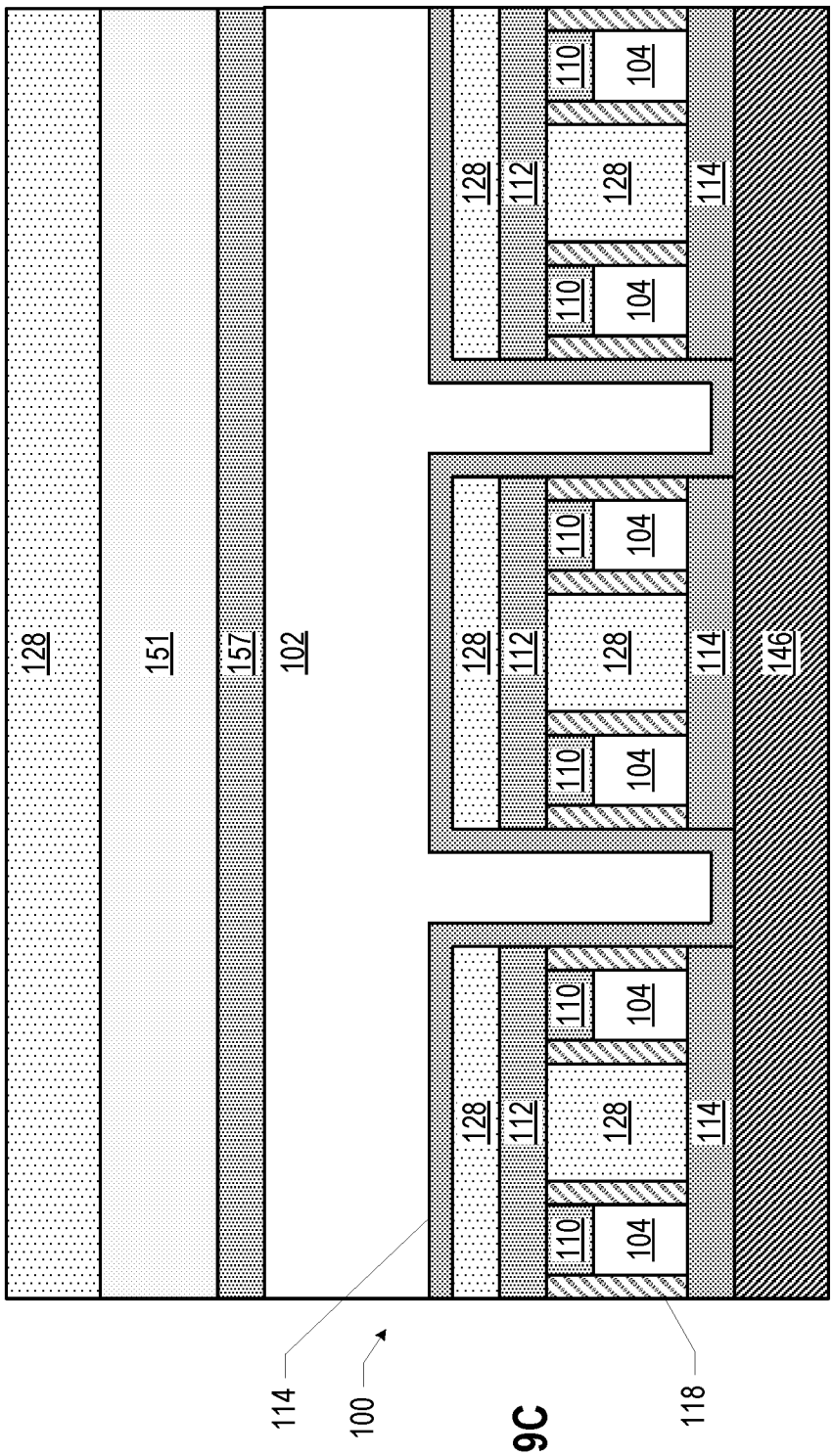


FIG. 9C

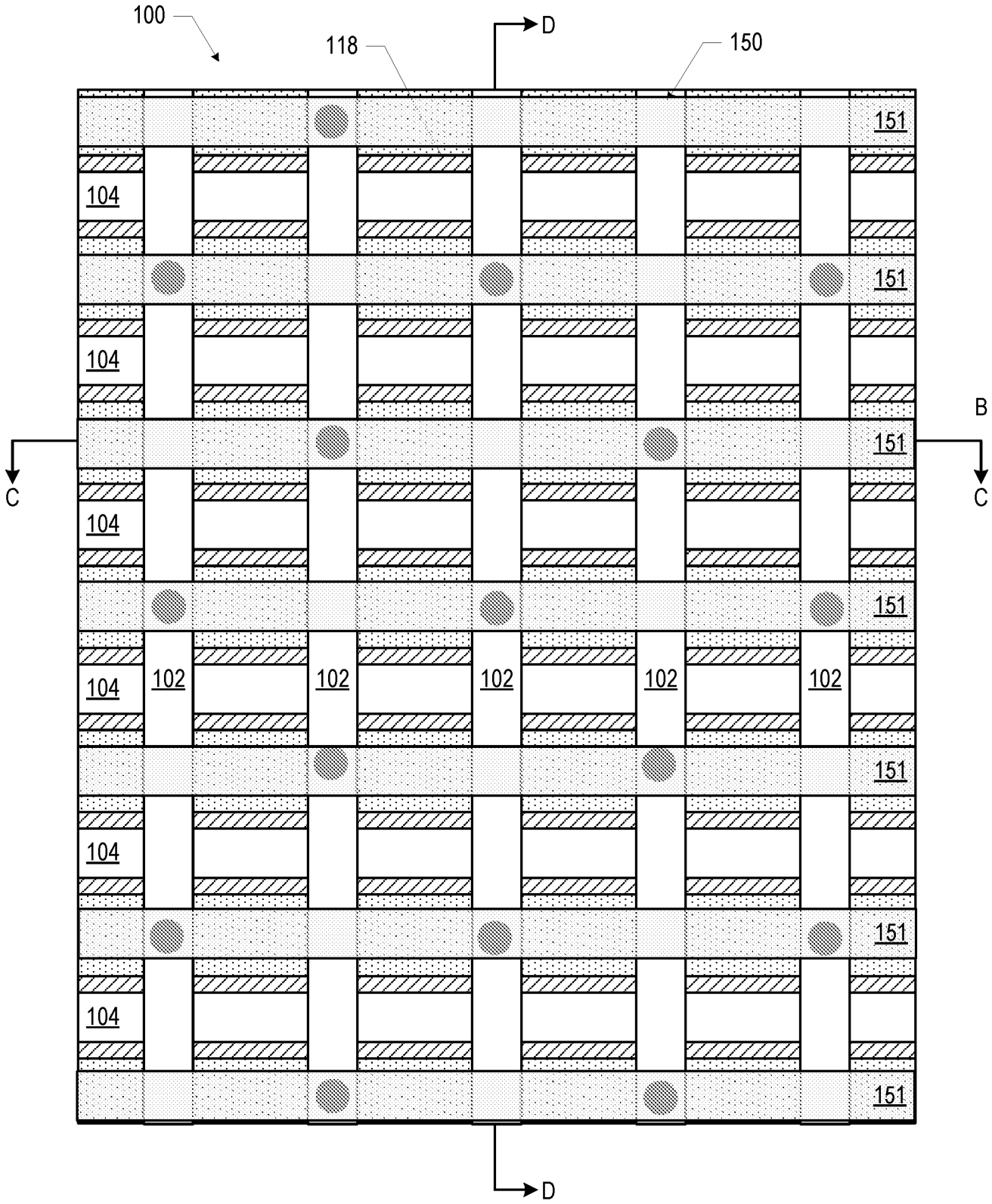

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151
D

FIG. 10A

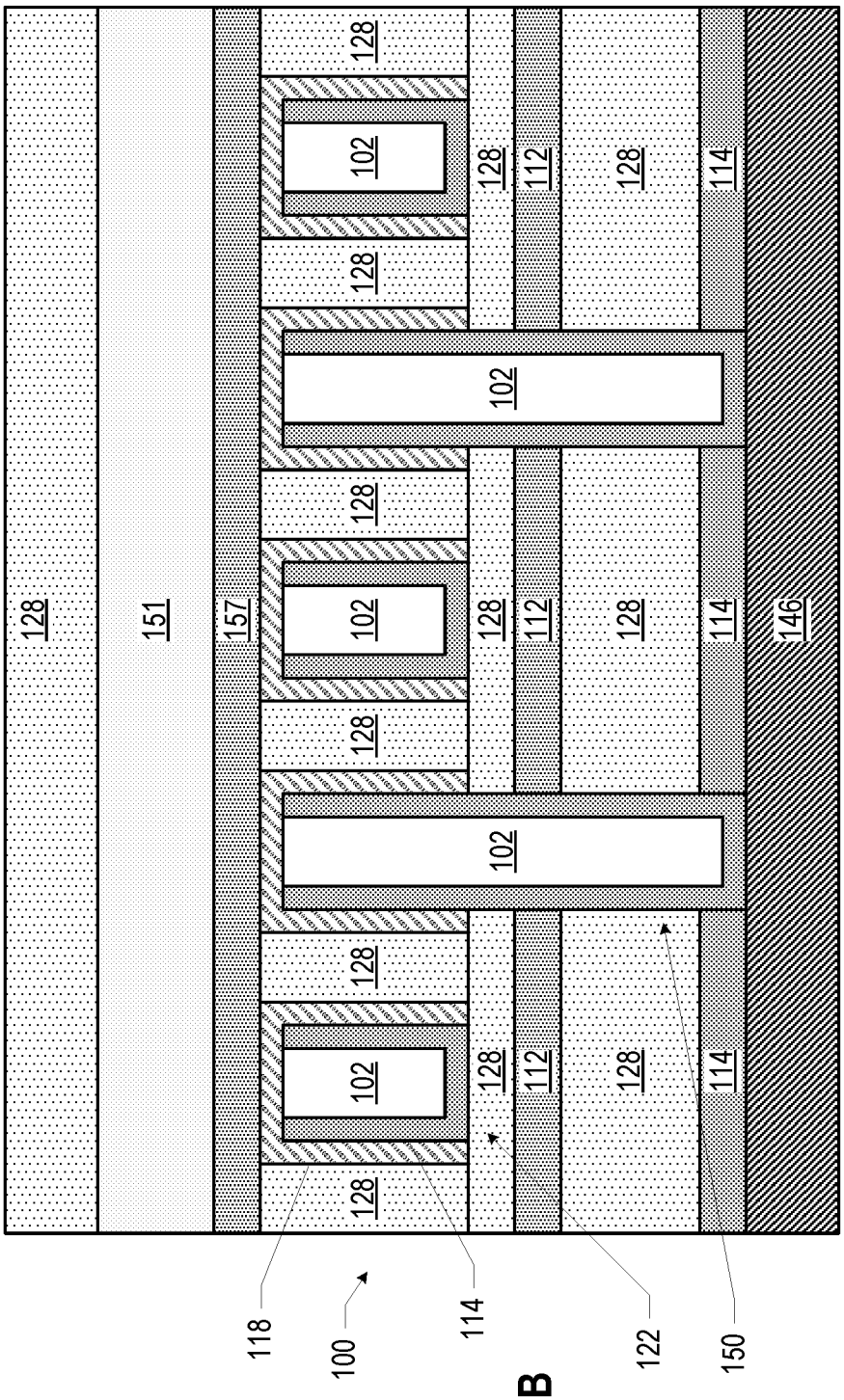


FIG. 10B

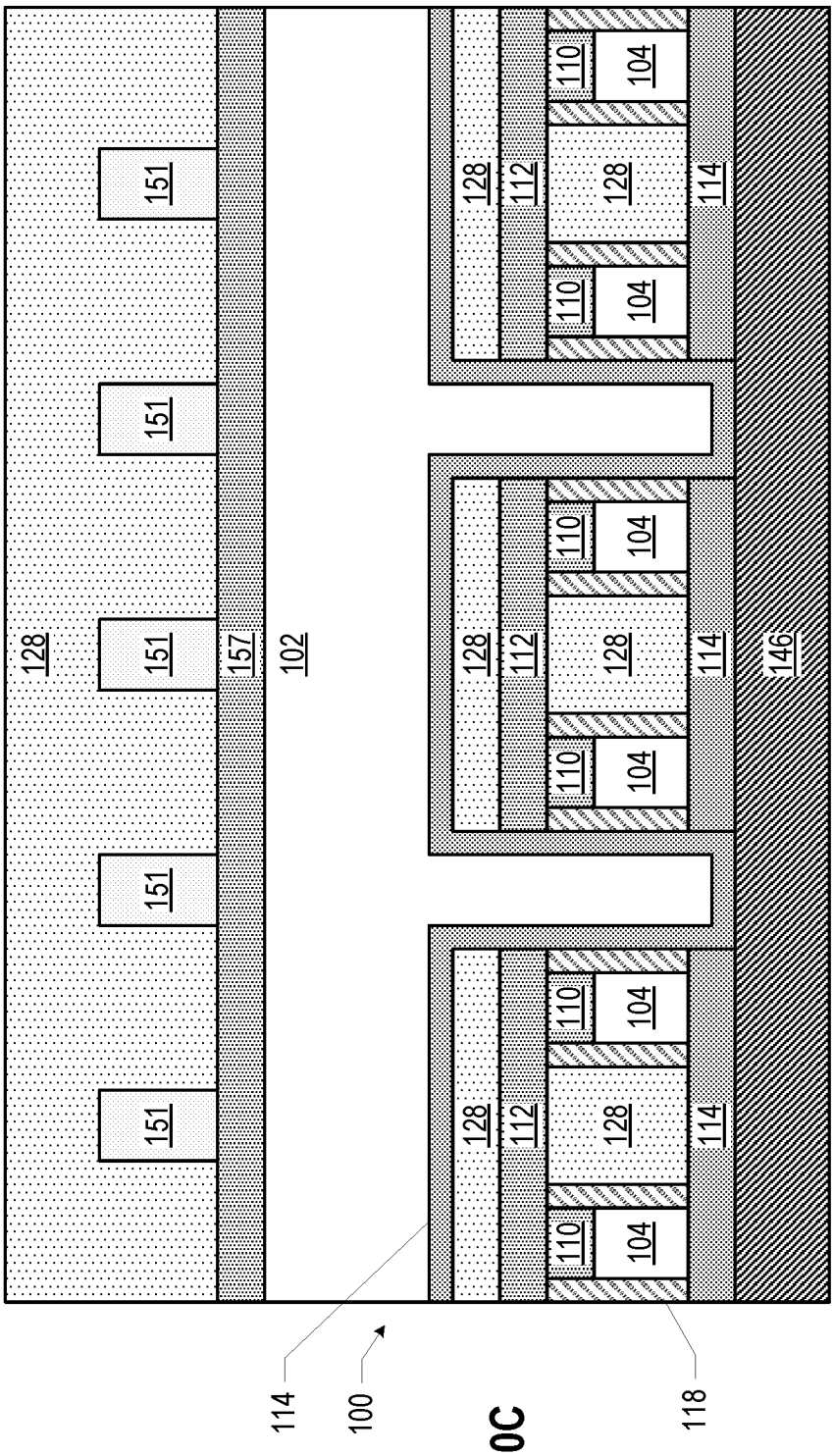

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118

FIG. 10C

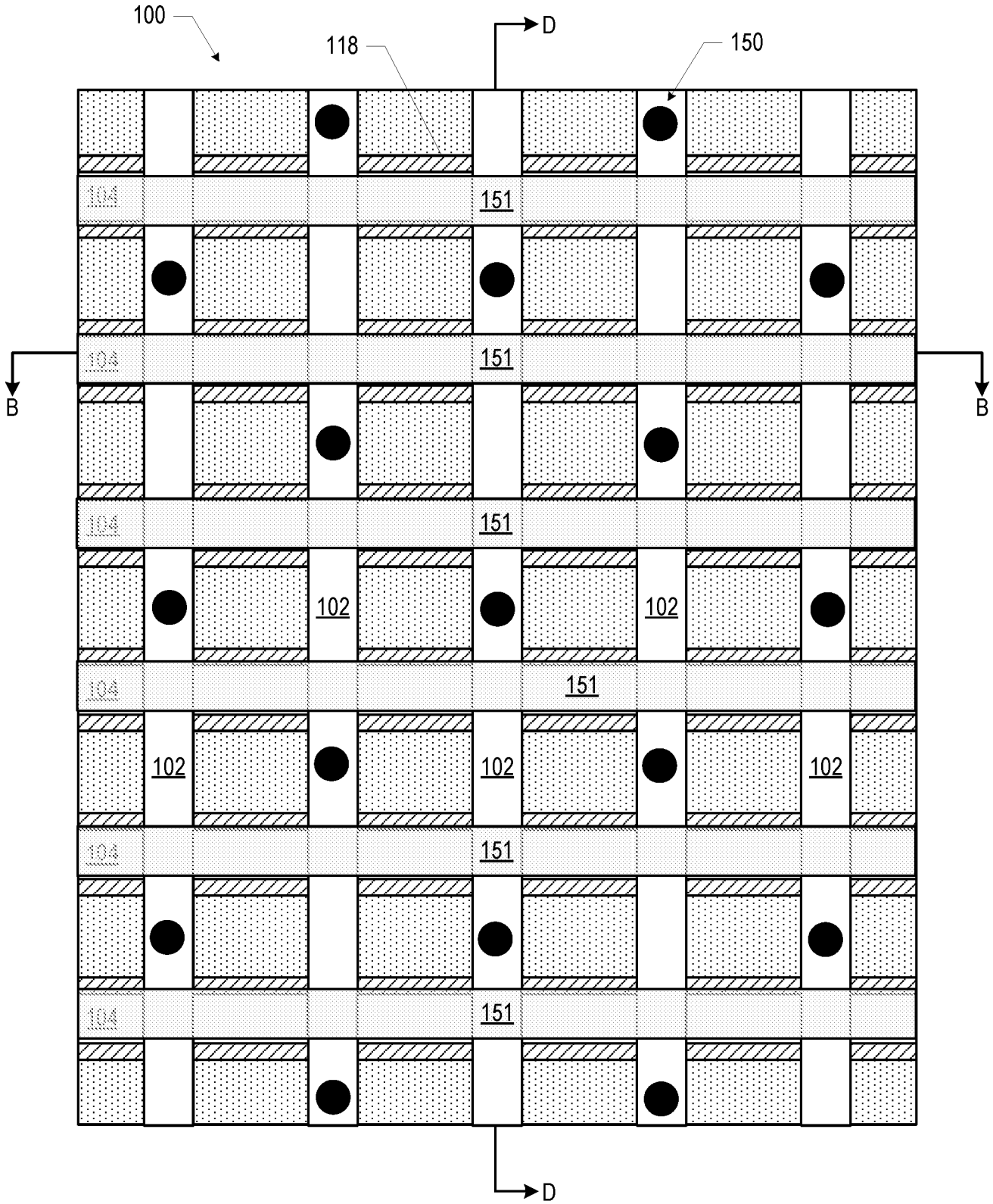


FIG. 11A

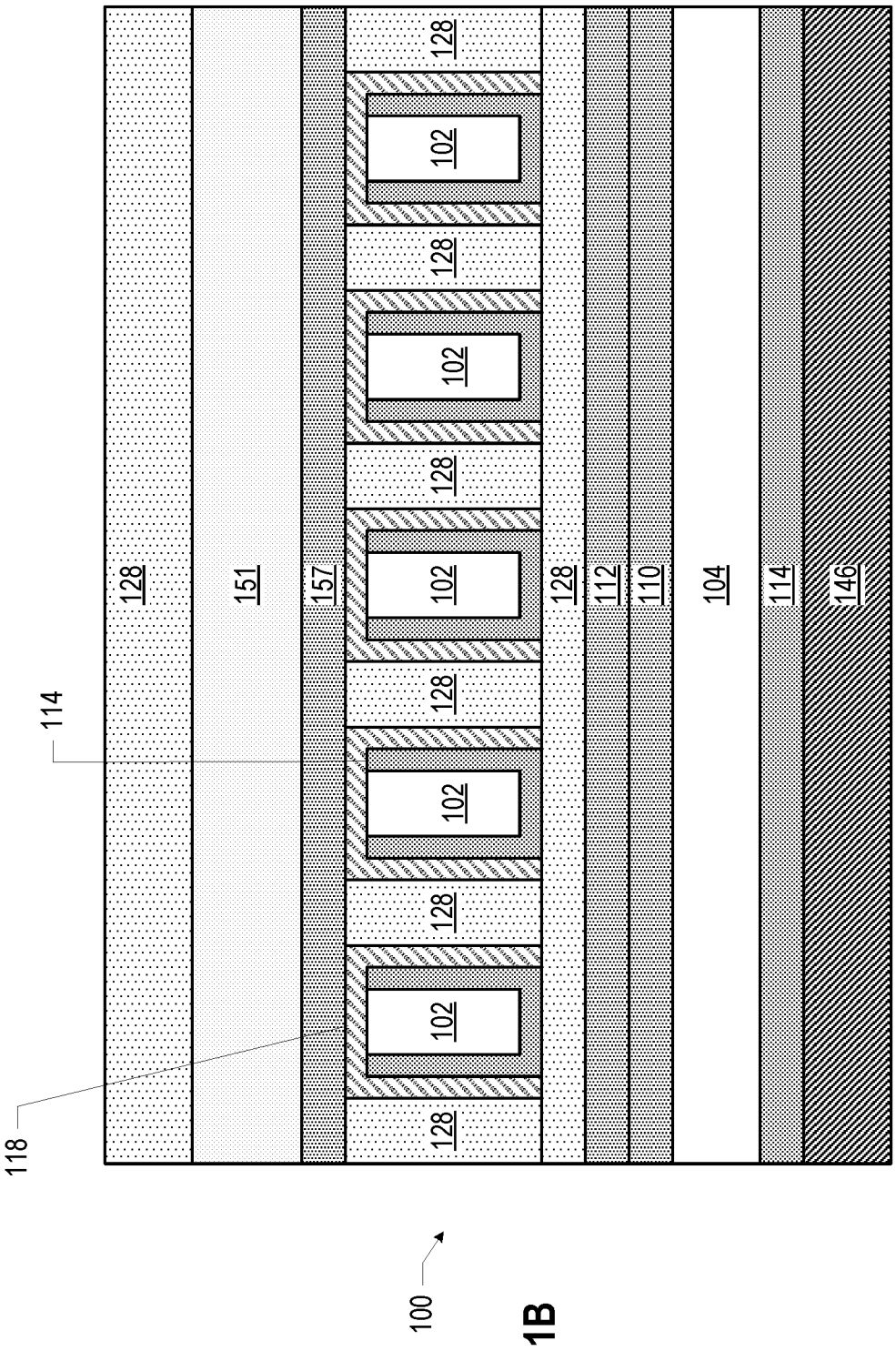

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100

FIG. 11B

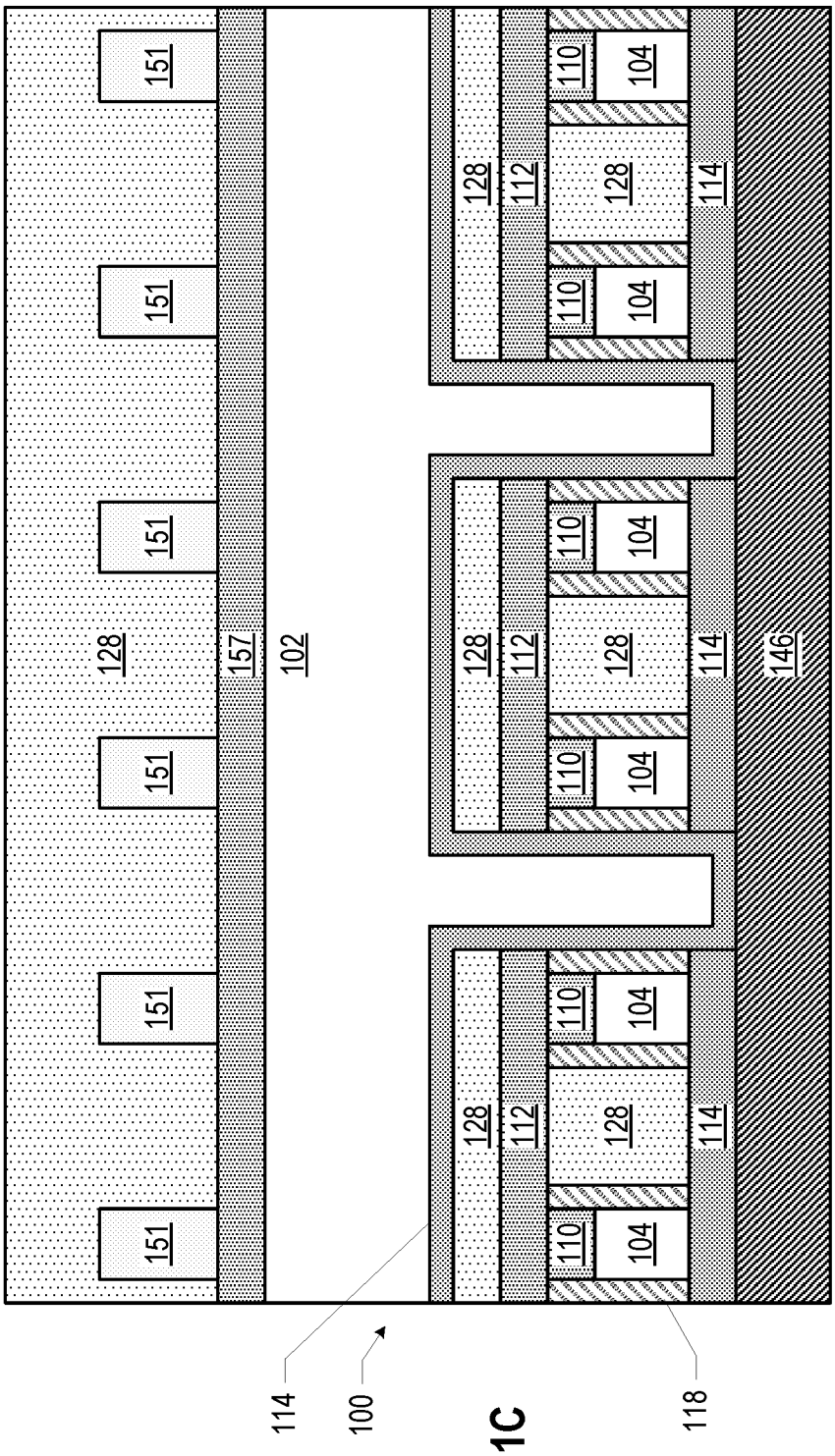


FIG. 11C

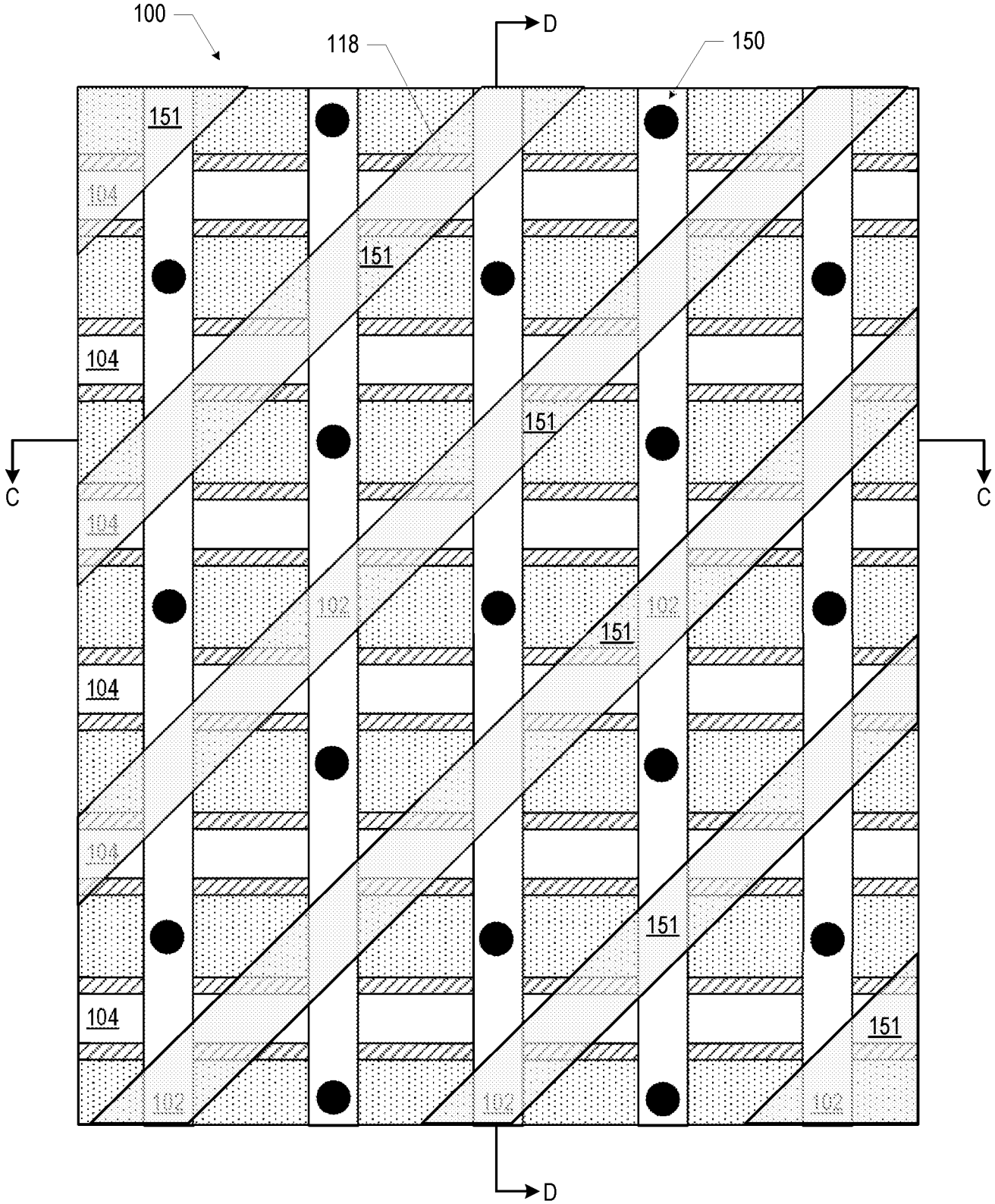

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102
D

FIG. 12A

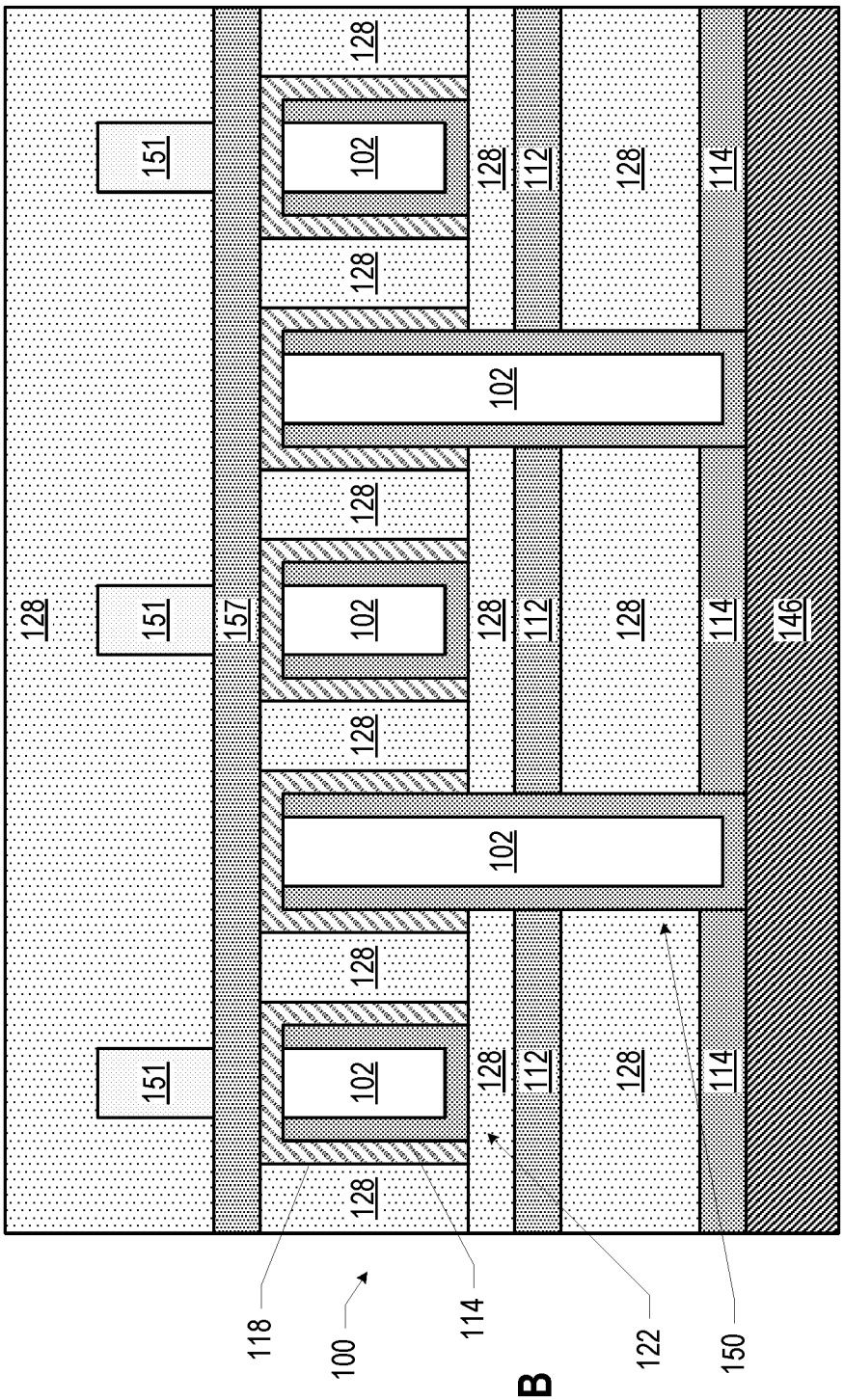


FIG. 12B

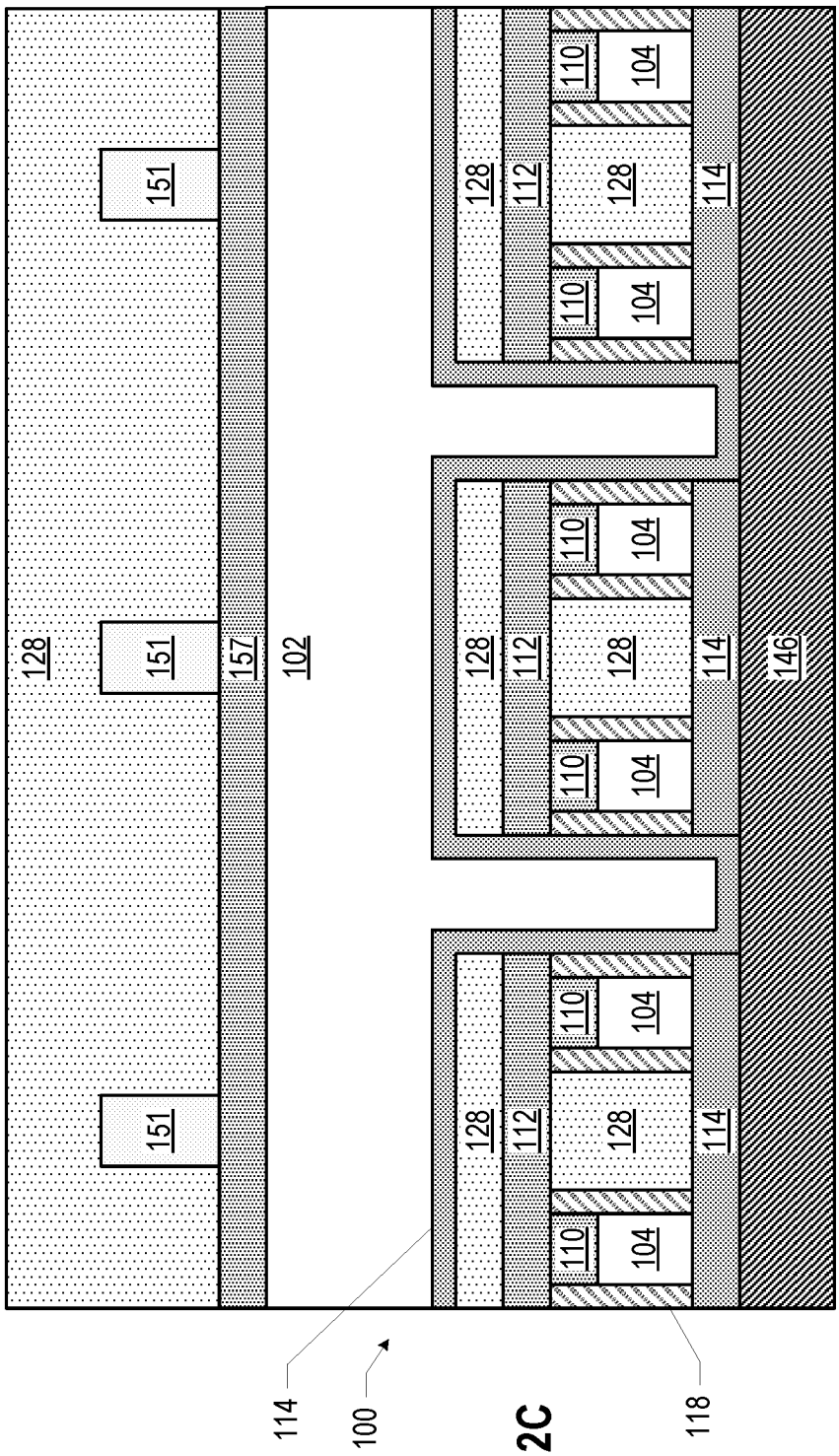


FIG. 12C

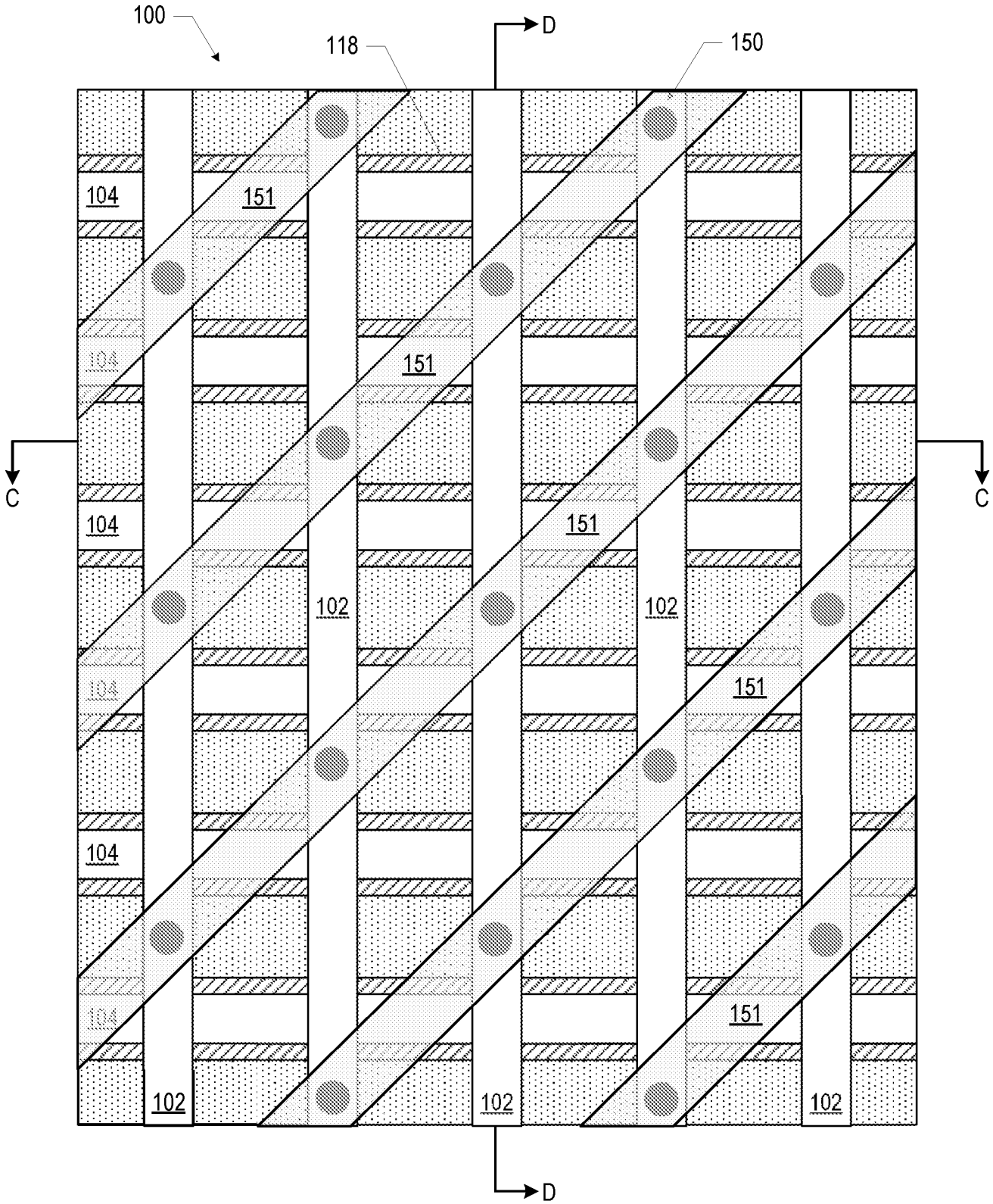

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FIG. 13A

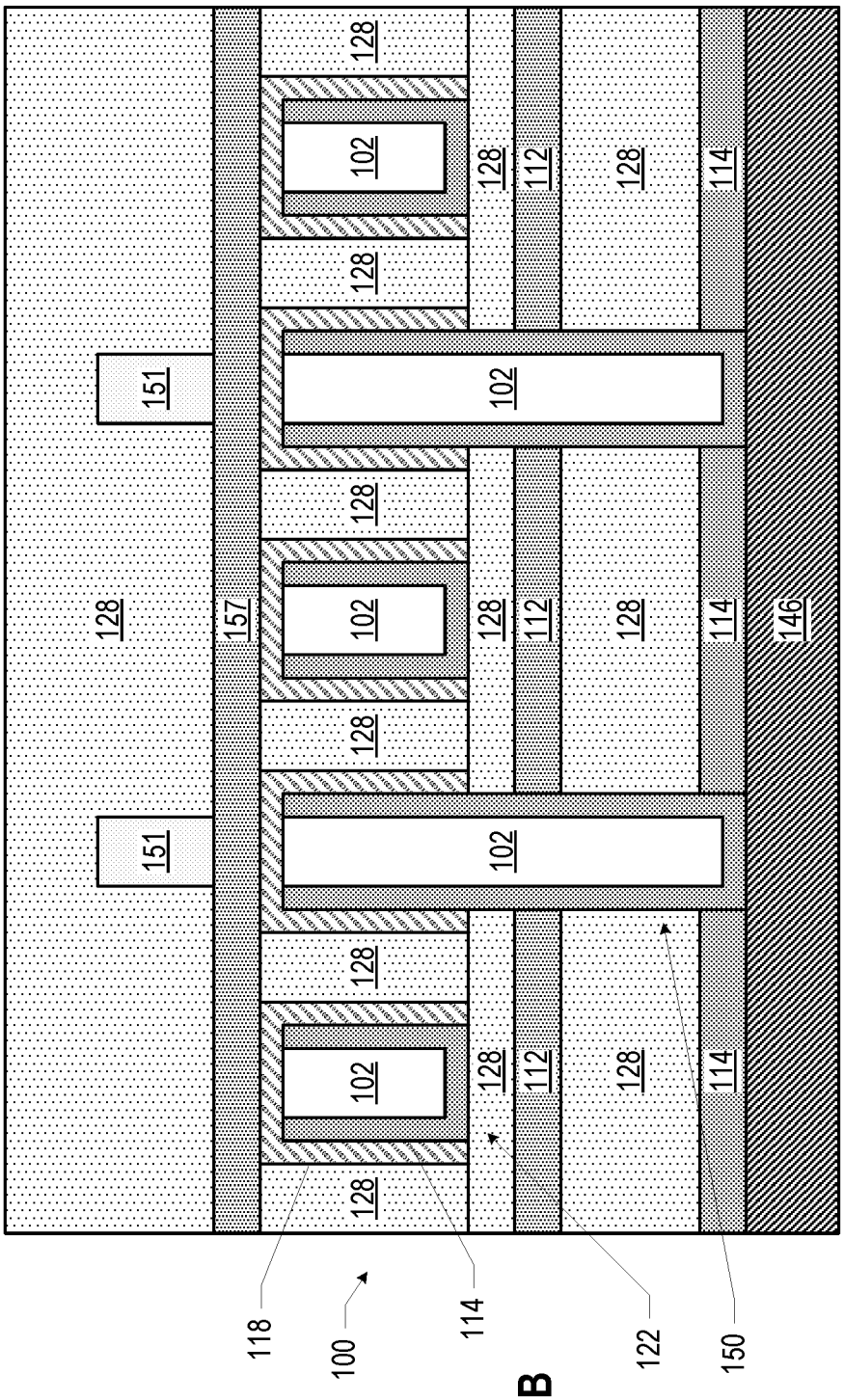


FIG. 13B

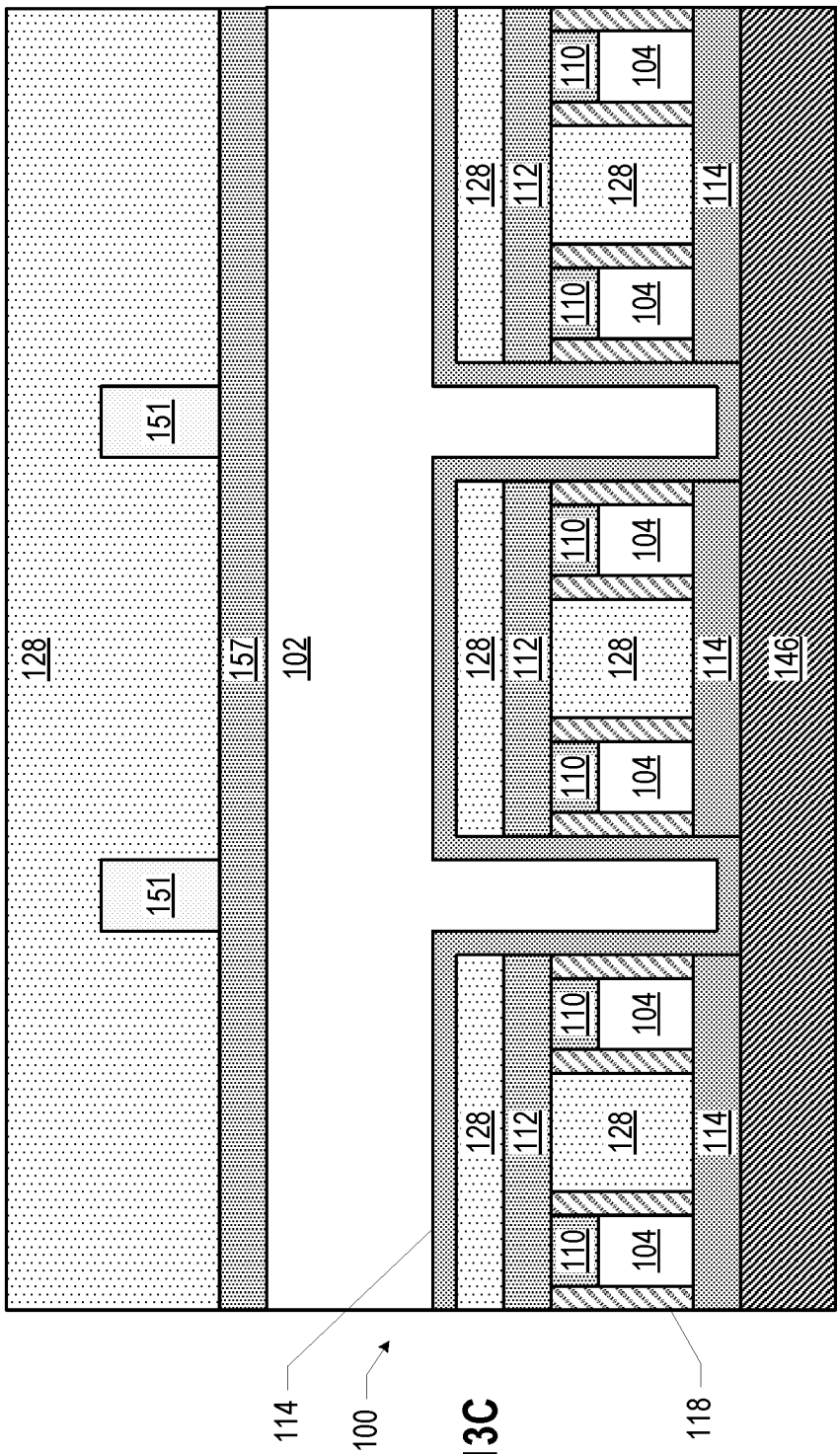


FIG. 13C

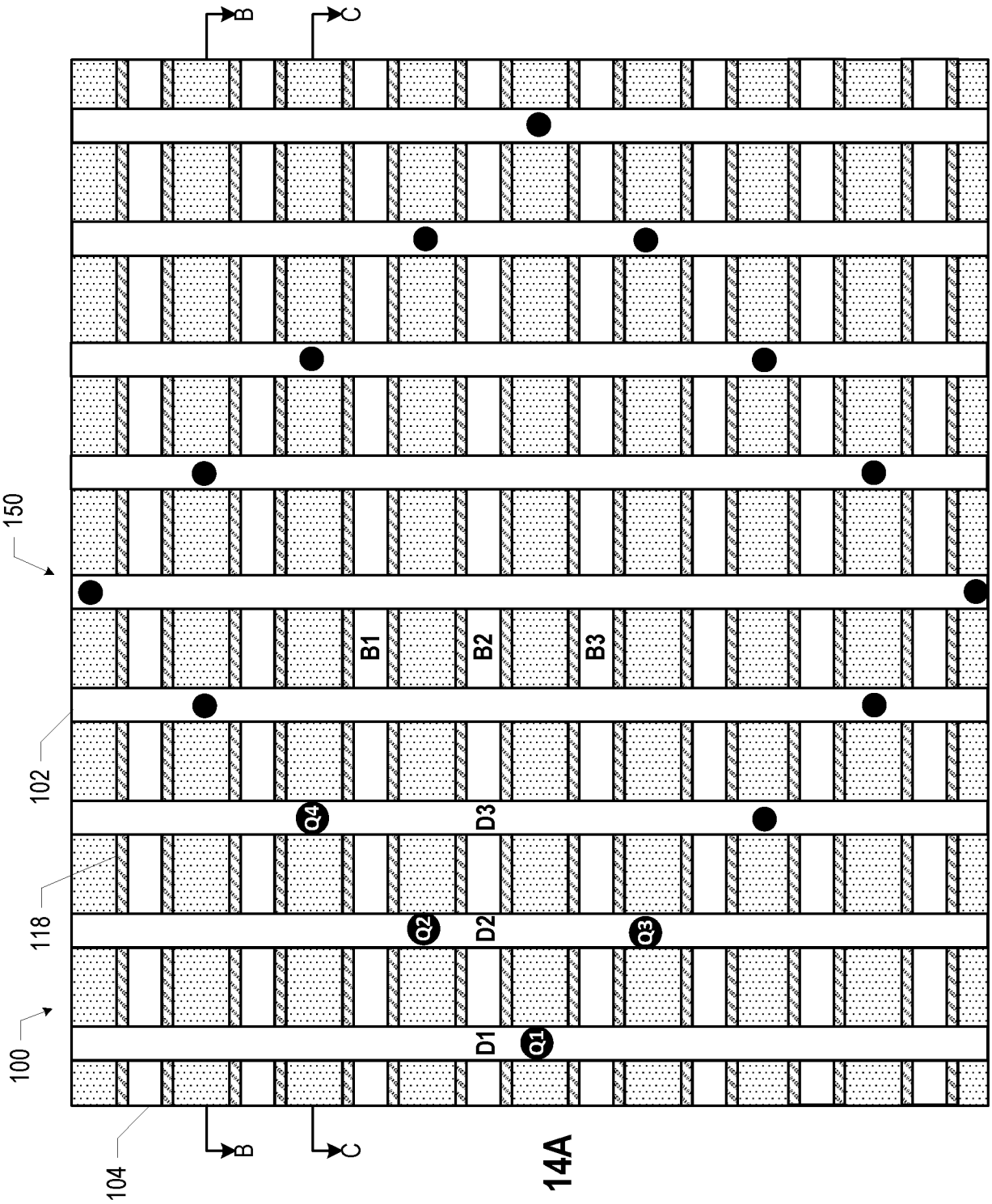


FIG. 14A

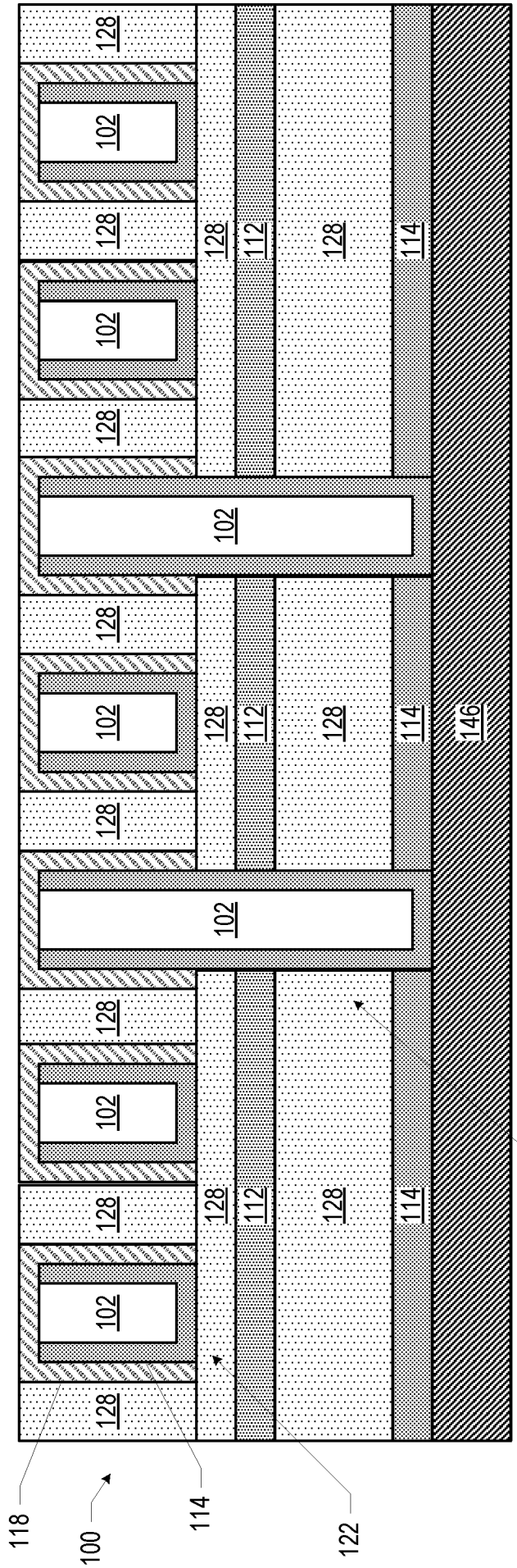


FIG. 14B

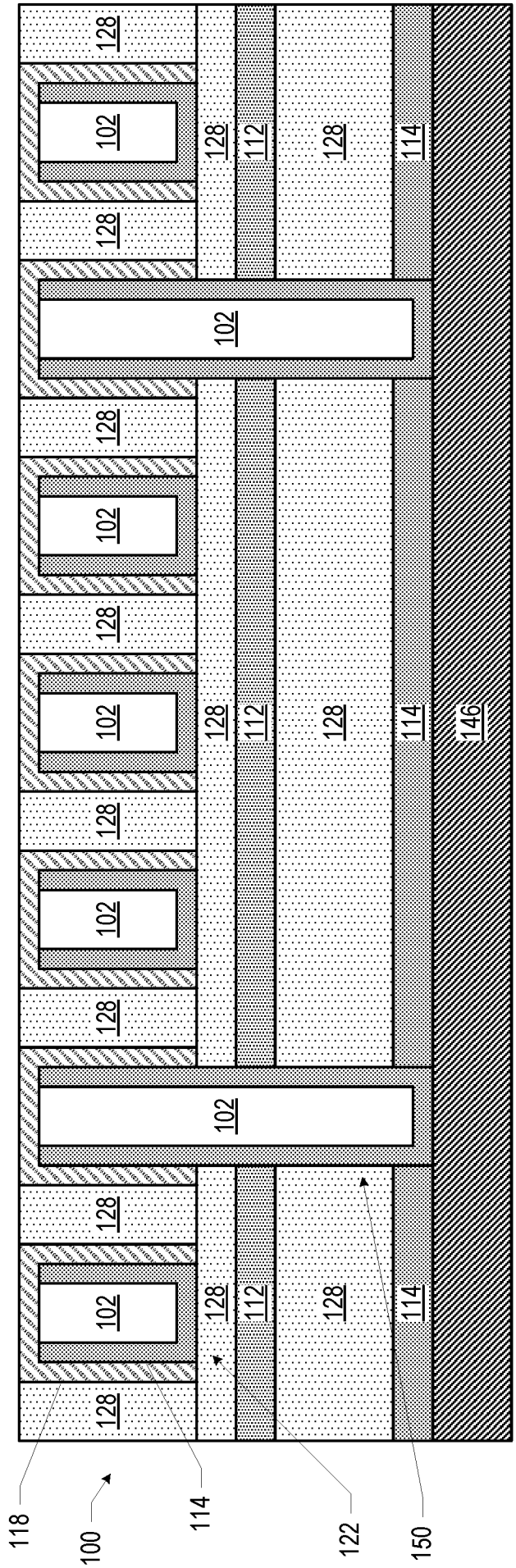


FIG. 14C

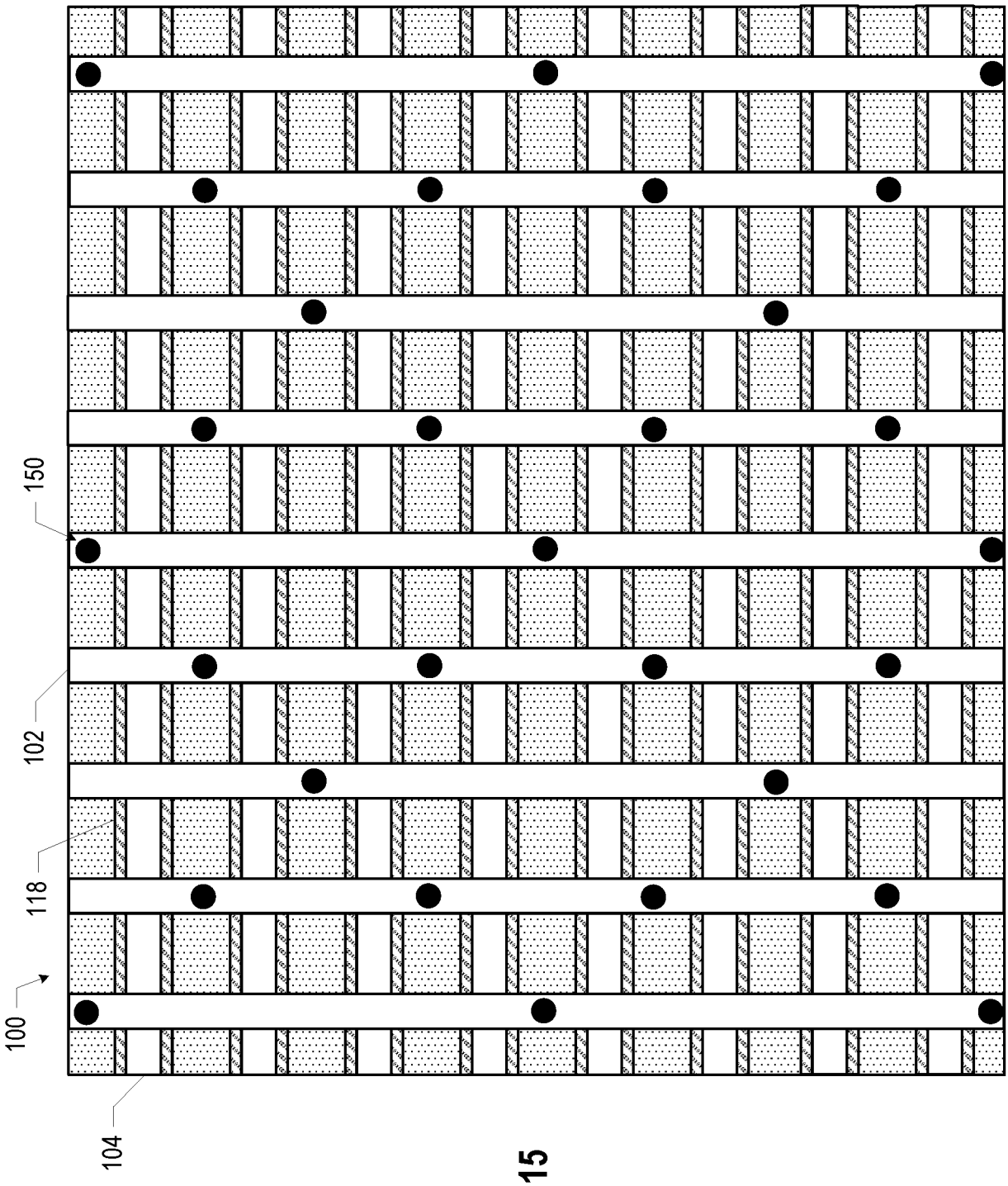


FIG. 15

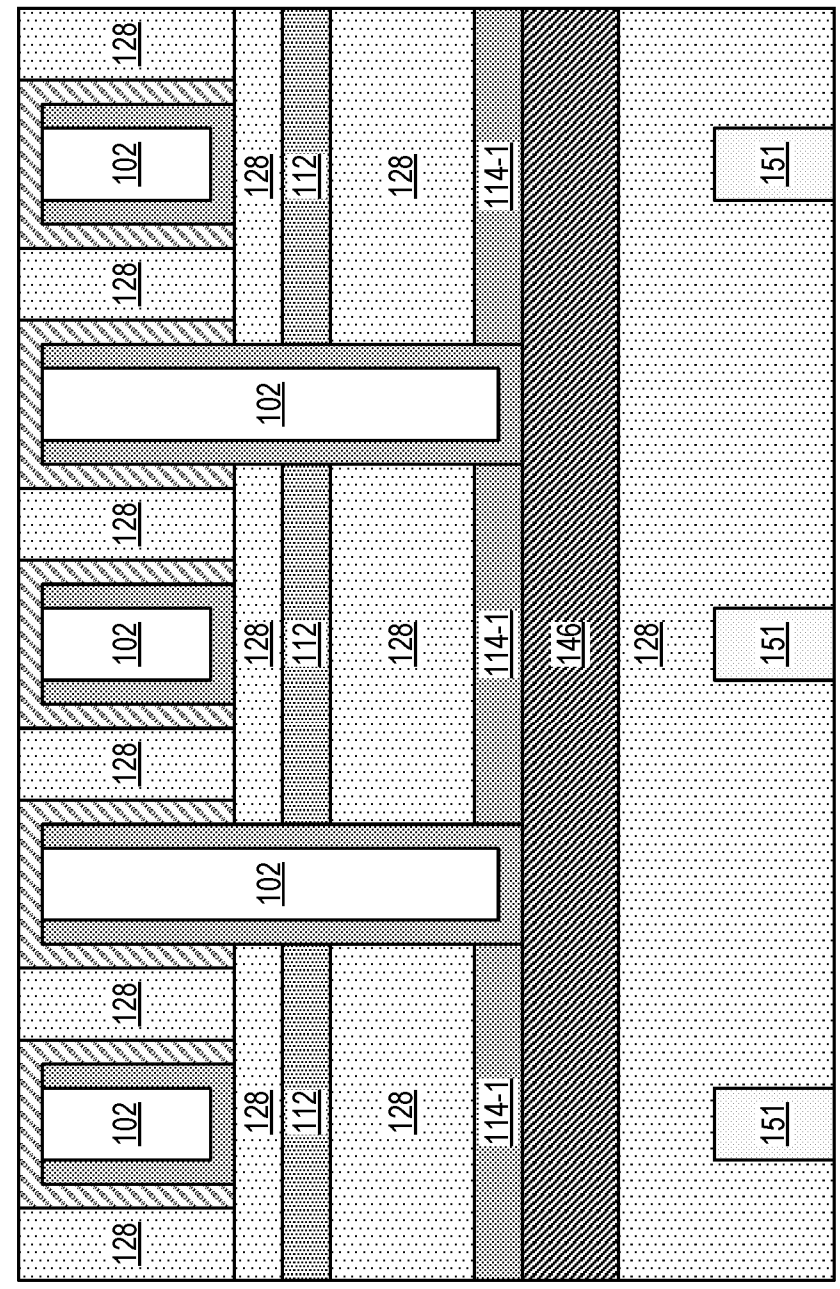


FIG. 16A

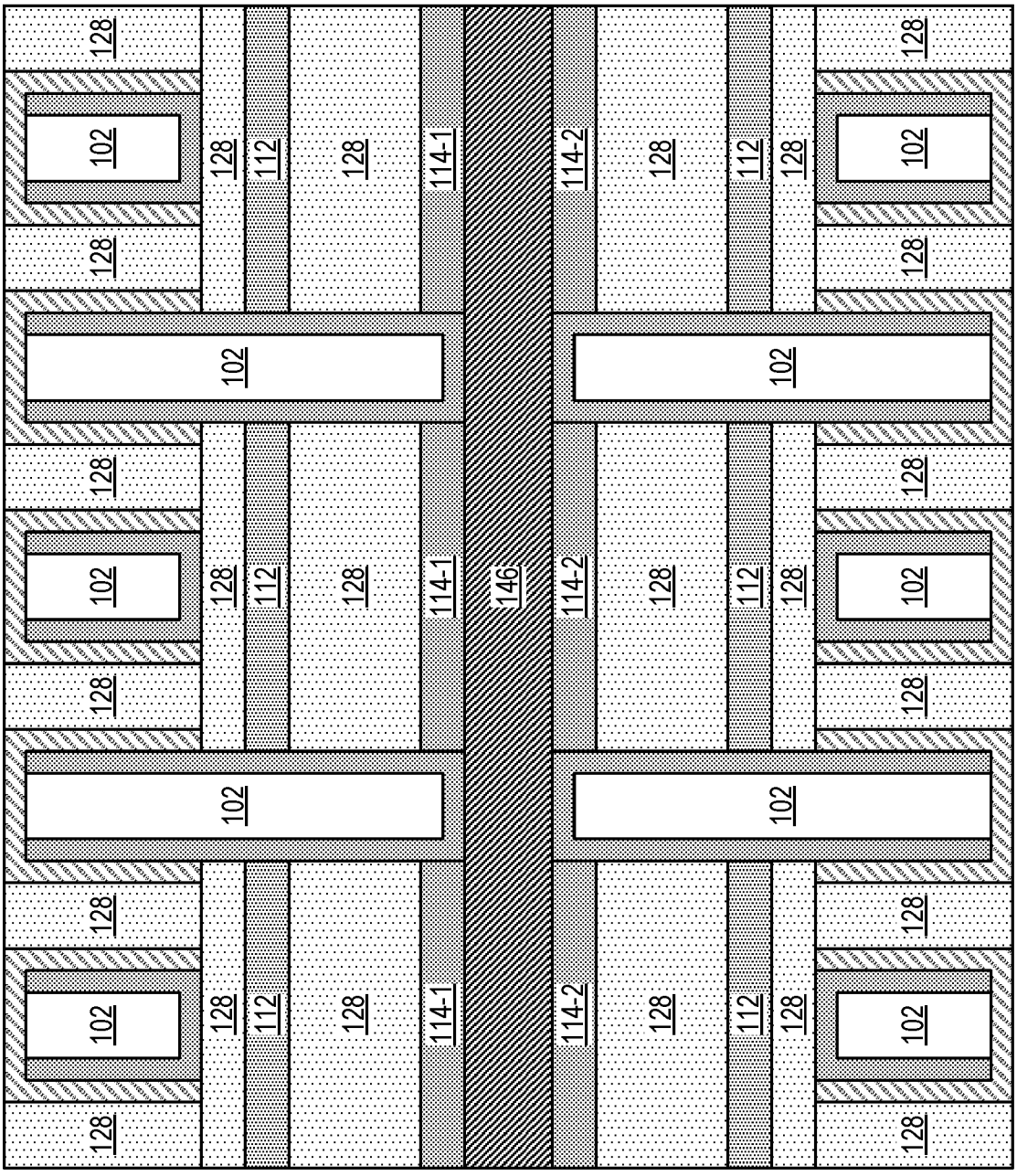


FIG. 16B

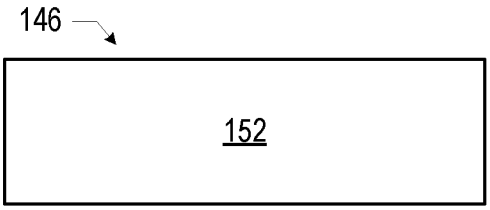


FIG. 17A

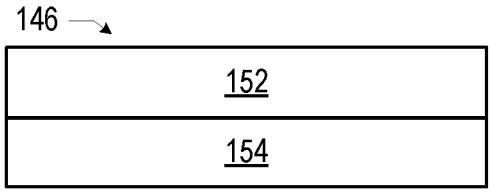


FIG. 17B

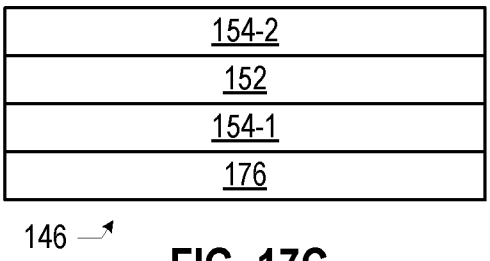


FIG. 17C

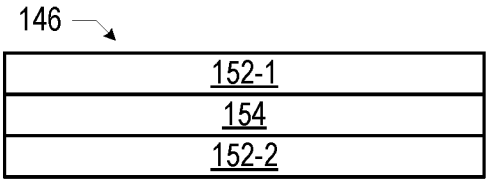


FIG. 17D

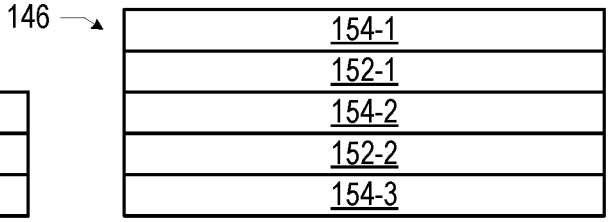


FIG. 17E

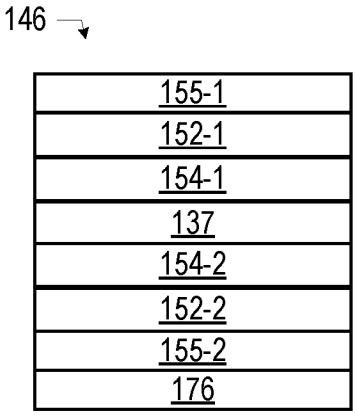


FIG. 17F

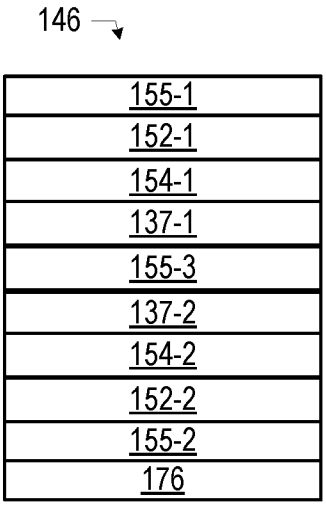


FIG. 17G

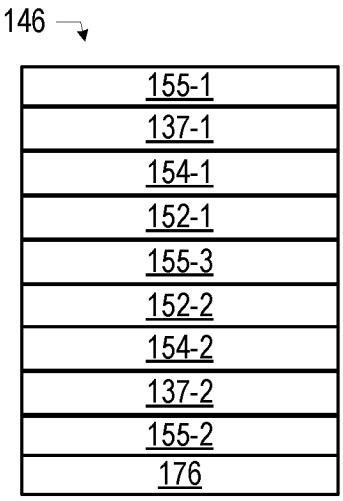


FIG. 17H

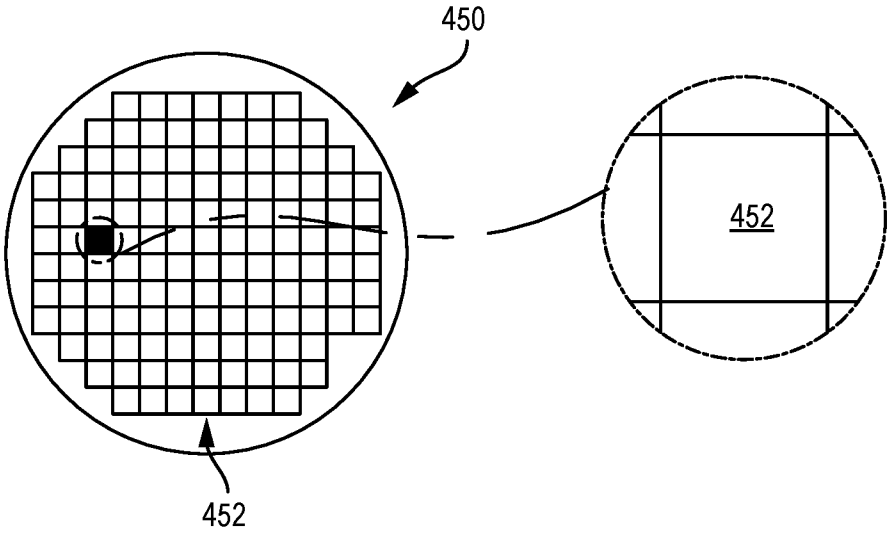

450
452
452

FIG. 18

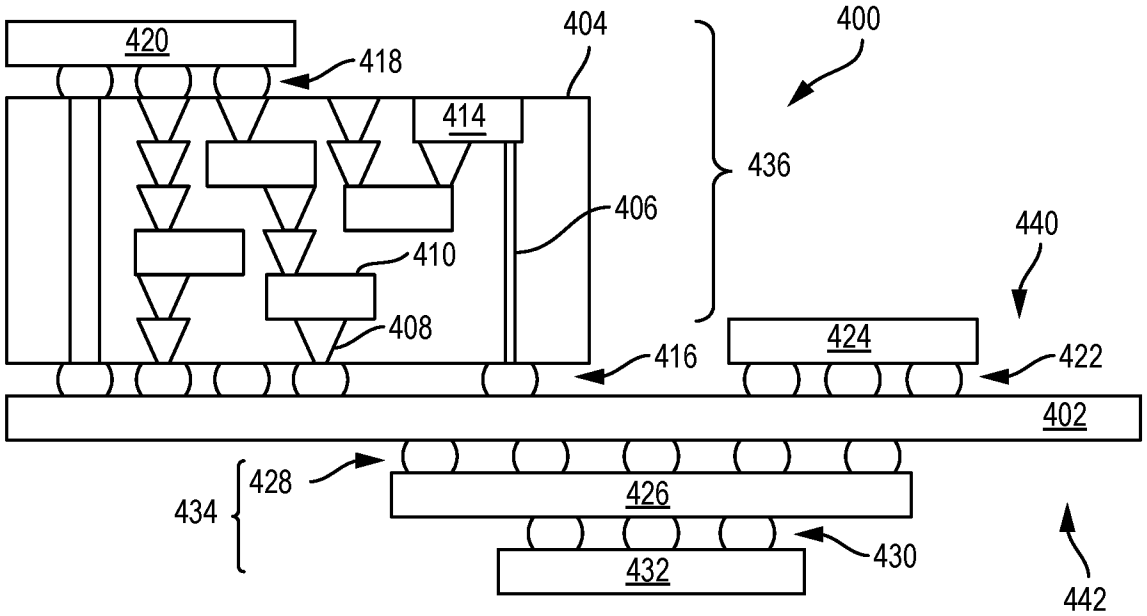

420
418
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422
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428
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430
432
442

FIG. 19

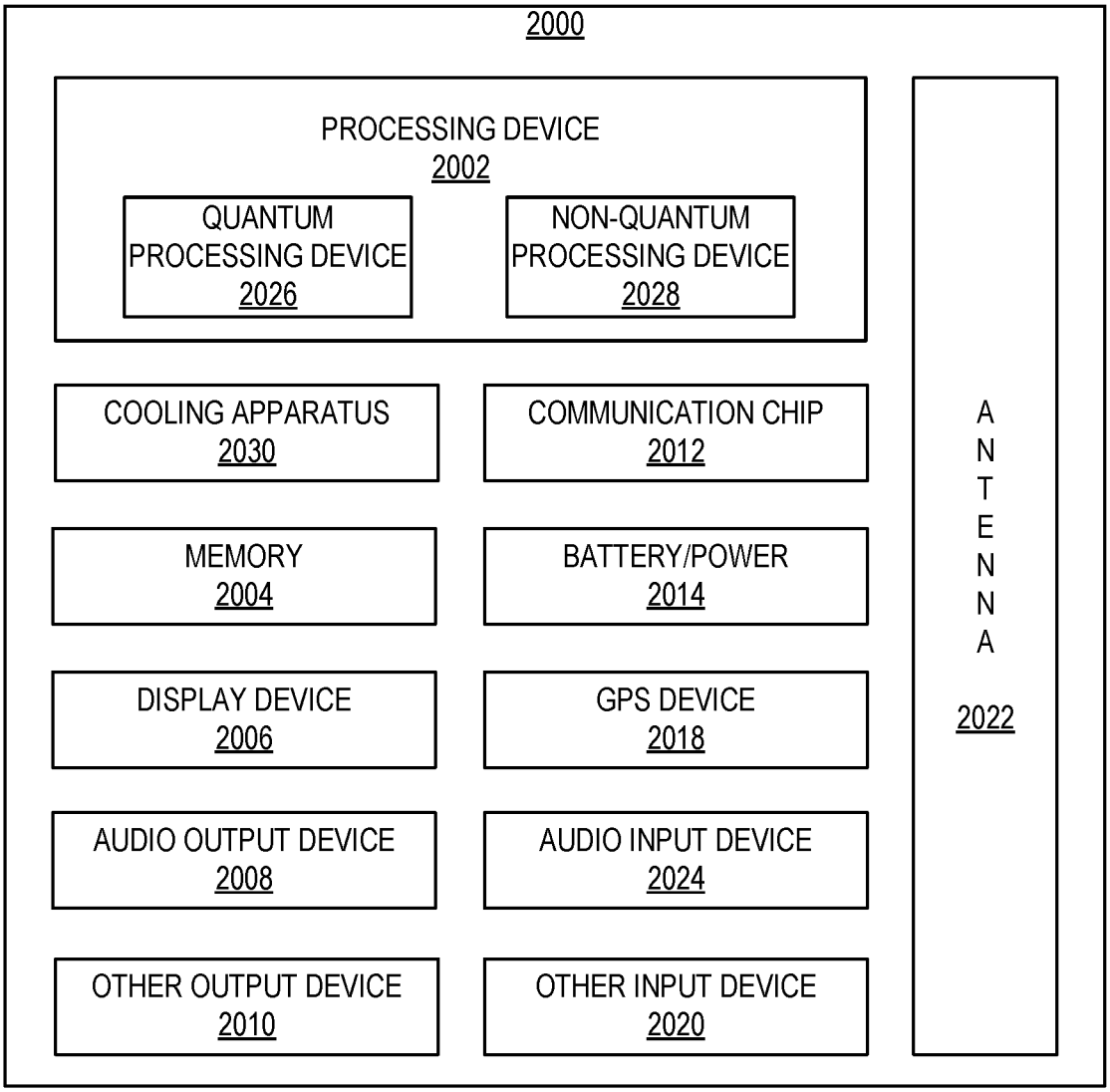

2000
PROCESSING DEVICE
2002
QUANTUM PROCESSING DEVICE
2026
NON-QUANTUM PROCESSING DEVICE
2028
COOLING APPARATUS
2030
COMMUNICATION CHIP
2012
MEMORY
2004
BATTERY/POWER
2014
DISPLAY DEVICE
2006
GPS DEVICE
2018
AUDIO OUTPUT DEVICE
2008
AUDIO INPUT DEVICE
2024
OTHER OUTPUT DEVICE
2010
OTHER INPUT DEVICE
2020
ANTENNA
2022

FIG. 20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/039156

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/12(2006.01)i, H01L 29/06(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/12; H01L 23/52; H01L 29/778; H01L 29/165; H01L 29/06; H01L 29/804; H01L 29/203; H01L 29/20; H01L 21/44; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: quantum well, quantum dot, gate line, perpendicular, magnetic material, superconducting material

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6597010 B2 (ERIKSSON et al.) 22 July 2003 See claims 1, 18 and figure 2.	1-25
A	JP 05-090611 A (SONY CORP.) 09 April 1993 See paragraphs [0017]-[0018], [0041] and figures 1-2, 8.	1-25
A	US 2009-0309229 A1 (ANGUS et al.) 17 December 2009 See paragraphs [0057], [0059], [0061] and figure 1(b).	1-25
A	KR 10-2016-0108585 A (INTEL CORPORATION) 19 September 2016 See claim 1 and figure 1.	1-25
A	US 2015-0279981 A1 (WISCONSIN ALUMNI RESEARCH FOUNDATION) 01 October 2015 See claims 1, 14 and figures 4a-4c.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2018 (19.02.2018)	**20 February 2018 (20.02.2018)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/039156

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