

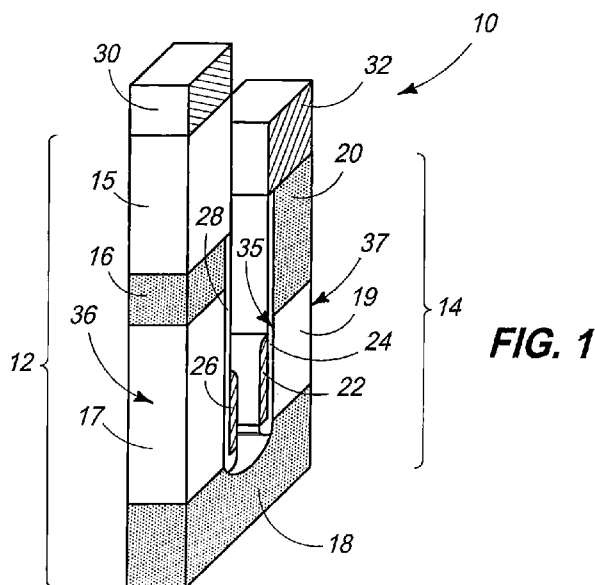


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(54) Title: MEMORY CELLS, MEMORY ARRAYS, METHODS OF FORMING MEMORY CELLS, AND METHODS OF FORMING A SHARED DOPED SEMICONDUCTOR REGION OF A VERTICALLY ORIENTED THYRISTOR AND A VERTICALLY ORIENTED ACCESS TRANSISTOR



(57) Abstract: A memory cell includes a thyristor having a plurality of alternately doped, vertically superposed semiconductor regions; a vertically oriented access transistor having an access gate; and a control gate operatively laterally adjacent one of the alternately doped, vertically superposed semiconductor regions. The control gate is spaced laterally of the access gate. Other embodiments are disclosed, including methods of forming memory cells and methods of forming a shared doped semiconductor region of a vertically oriented thyristor and a vertically oriented access transistor.

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DESCRIPTION

**MEMORY CELLS, MEMORY ARRAYS, METHODS OF FORMING
MEMORY CELLS, AND METHODS OF FORMING A SHARED DOPED
SEMICONDUCTOR REGION OF A VERTICALLY ORIENTED
5 THYRISTOR AND A VERTICALLY ORIENTED ACCESS TRANSISTOR**

TECHNICAL FIELD

Embodiments disclosed herein pertain to memory cells, to memory arrays,
to methods of forming memory cells, and to methods of forming a shared doped
10 semiconductor region of a vertically oriented thyristor and a vertically oriented
access transistor.

BACKGROUND

Many integrated circuit (IC) memory devices conventionally include
15 static random access memory (SRAM). Conventional SRAM is based on
four-transistor memory cells (4T SRAM cells) or six-transistor memory cells
(6T SRAM cells) that are compatible with conventional memory elements, such
as complementary metal-oxide-semiconductor (CMOS) devices, operate at low
voltage levels, and perform at relatively high speeds. However, conventional
20 SRAM consumes a large cell area that limits high-density design of SRAM.

In attempts to reduce the area of IC memory devices, high-density,
low-voltage SRAM cells including four layers of alternating n-and p-type
semiconductive material, often referred to as a “thin capacitively-coupled
thyristor (TCCT)” have been fabricated. As used herein, the term “thyristor,”
25 means and includes a bi-stable, three-terminal device that includes a four layer
structure including a p-type anode region, an n-type base, a p-type base, and an
n-type cathode region arranged in a p-n-p-n configuration. The thyristor may
include two main terminals, an anode and a cathode. Further, a control terminal,
often referred to as the “gate,” may be operatively adjacent to the p-type
30 material nearest the cathode. Thyristor-based random access memory (T-RAM)

cells demonstrate faster switching speeds and lower operating voltages in comparison to conventional SRAM cells.

5 A thyristor in a memory device may be turned on by biasing the gate so that a p-n-p-n channel conducts a current. Once the device is turned on, often referred to as "latched," the thyristor does not require the gate to be biased to maintain the current conducted between the cathode and the anode. Instead, it will continue to conduct until a minimum holding current is no longer maintained between the anode and cathode, or until the voltage between the anode and the cathode is reversed. Accordingly, the thyristor may function as a
10 switch or diode capable of being switched between an "on" state and an "off" state.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic oblique projection view of a memory cell in accordance with an embodiment of the invention.

Fig 2 is a side elevational view of the memory cell of Fig. 1.

5 Fig. 3 is a side elevational view of a memory cell in accordance with an embodiment of the invention.

Fig. 4 is a side elevational view of a memory cell in accordance with an embodiment of the invention.

10 Fig. 5 is a diagrammatic oblique projection view of a portion of a horizontal array of memory cells in accordance with an embodiment of the invention.

Fig. 6 is a diagrammatic oblique projection view of a portion of another horizontal array of memory cells in accordance with an embodiment of the invention.

15 Fig. 7 is a diagrammatic oblique projection view of a portion of another horizontal array of memory cells in accordance with an embodiment of the invention.

Fig. 8 is a diagrammatic oblique projection view of a substrate fragment in process in accordance with an embodiment of the invention.

20 Fig. 9 is a view of the Fig. 8 substrate fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view of the Fig. 9 substrate fragment at a processing step subsequent to that shown by Fig. 9.

25 Fig. 11 is a view of the Fig. 10 substrate fragment at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 11 substrate fragment at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a view of the Fig. 12 substrate fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view of the Fig. 13 substrate fragment at a processing step subsequent to that shown by Fig. 13.

5 Fig. 15 is a view of the Fig. 14 substrate fragment at a processing step subsequent to that shown by Fig. 14.

Fig. 16 is a view of the Fig. 15 substrate fragment at a processing step subsequent to that shown by Fig. 15.

10 Fig. 17 is a view of the Fig. 16 substrate fragment at a processing step subsequent to that shown by Fig. 16.

Fig. 18 is a view of the Fig. 17 substrate fragment at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a view of the Fig. 18 substrate fragment at a processing step subsequent to that shown by Fig. 18.

15 Fig. 20 is a view of the Fig. 19 substrate fragment at a processing step subsequent to that shown by Fig. 19.

Fig. 21 is a view of the Fig. 20 substrate fragment at a processing step subsequent to that shown by Fig. 20.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Some example embodiments of memory cells in accordance with the invention are initially described with respect to a memory cell 10 in Figs. 1 and 2. In one embodiment, such comprises at least one thyristor 12 and at least one vertically oriented access transistor 14.

Memory cell 10 may be fabricated relative to a suitable base substrate (not shown) which may be homogenous or non-homogenous, for example comprising multiple different composition materials and/or layers. As an example, such may comprise bulk monocrystalline silicon and/or a semiconductor-on-insulator substrate. As an additional example, such may comprise dielectric material having conductive contacts or vias formed therein which extend vertically or otherwise into current conductive electrical connection with electronic device components, regions, or material received elevationally inward of the dielectric material. In this document, vertical is a direction generally orthogonal to a primary surface relative to which a substrate is processed during fabrication and which may be considered to define a generally horizontal direction. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative one another independent of orientation of the substrate in three dimensional space. Further in this document, "elevational" and "elevationally" are with reference to the vertical direction from the base substrate upon which the circuitry is fabricated. The base substrate may or may not be a semiconductor substrate. In this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Thyristor 12 may comprise a plurality of alternately doped, vertically superposed semiconductor regions 15, 16, 17, and 18. Vertically oriented access transistor 14 may comprise a plurality of alternately doped, superposed

semiconductor regions 18, 19, and 20. Accordingly in some embodiments, thyristor 12 and access transistor 14 share one of the alternately doped, superposed semiconductor regions, for example region 18 in Figs. 1 and 2. As used herein, the term “vertically superposed” means and includes materials or regions which are disposed elevationally atop or situated one upon another. Lateral perimeters thereof might generally coincide. Further, “alternately doped” means and includes with respect to the stated regions opposite n and p conductivity type disposed in succession one after the other. Material of respective regions 15-20 may be homogenous or non-homogenous, and may comprise any existing or yet-to-be-developed semiconductor material. Crystalline silicon material, silicon germanium material, gallium arsenide material, and/or gallium nitride material are some examples.

Semiconductor regions 15, 18, and 20 may be “highly doped” to the same or different respective n or p dopant concentration(s). Semiconductor regions 16, 17, and 19 may not be highly doped, and may be of the same or different dopant concentration(s). As used herein, the term “highly doped” means and includes a material or region having a higher concentration of a dopant than those which are not highly doped. With respect to thyristor 12, region 15 may be a p-type anode region, region 16 an n-type base region, region 17 a p-type base region, and region 18 an n-type cathode region.

In one embodiment, access transistor 14 has an access gate 22 which is operatively laterally adjacent an unshared of the semiconductor regions of the access transistor, for example region 19 as shown. A suitable gate dielectric 24 is received between at least access gate 24 and region 19, with such also in the example embodiment extending over a portion of shared region 18 and laterally over semiconductor region 20. A control gate 26 is spaced laterally of access gate 22, and is operatively laterally adjacent one of the alternately doped, vertically superposed semiconductor regions, for example unshared region 17 as shown. A suitable gate dielectric 28 is received between at least control gate 26 and semiconductor region 17, with gate dielectric 28 in the example embodiment extending over shared semiconductor region 18 and laterally over semiconductor region 16. Gate dielectrics 24 and 28 may be homogenous or non-homogenous,

and of the same or different composition(s). Gates 22 and 28 comprise current conductive material, and may be homogenous or non-homogenous. In this document, "current conductive material" is a composition where electric current flow would inherently occur therein predominantly by movement by subatomic positive and/or negative charges when such are generated as opposed to predominantly by movement of ions. Example current conductive materials are elemental metals, alloys of elemental metals, current conductive metal compounds, and conductively doped semiconductive material, including any combination thereof.

In one embodiment, the access gate and the control gate elevationally overlap, and in one embodiment, are elevationally coincident. In this document, constructions "elevationally overlap" if some respective portions thereof are elevationally at the same level. Elevationally overlapping constructions are "elevationally coincident" if their elevationally outermost and innermost extents/surfaces are elevationally at the same level.

An electrode 30 may be in current conductive connection with semiconductor region 15, and an electrode 32 may be in current conductive connection with semiconductor region 20. Each may comprise current conductive material, and may be homogenous or non-homogenous.

In one embodiment of the invention, a memory cell comprises a vertically oriented thyristor and a control gate operatively laterally adjacent thereto. Such also includes a vertically oriented access transistor laterally spaced from the vertically oriented thyristor and which shares a doped semiconductor region therewith that extends laterally between the vertically oriented thyristor and the vertically oriented access transistor. That which is depicted in Figs. 1 and 2 is but one such example embodiment.

In one embodiment, a vertically oriented access transistor comprises a channel region having a pair of laterally opposing sides, with the access gate being operatively laterally adjacent only one of such sides. Memory cell 10 is an example such memory cell wherein semiconductor region 19 comprises a channel region having a pair of laterally opposing sides 35 and 37, with access

gate 22 being operatively laterally adjacent only the one side 35. Fig. 3 depicts an alternate example embodiment memory cell 10a wherein access gate 22 and gate dielectric 24 are received operatively laterally adjacent only the one side 37 of semiconductor region 19.

5 In one embodiment, the one of the alternately doped, vertically superposed semiconductor regions which the control gate is operatively laterally adjacent has a pair of laterally opposing sides, with the control gate only being so adjacent one of such sides. For example with respect to memory cell 10 in Fig. 2, semiconductor region 17 has a pair of laterally opposing sides 36 and 38, 10 with control gate 28 being operatively laterally adjacent only the side 38. Fig. 3 depicts an alternate example embodiment wherein control gate 26 is adjacent only the one side 36. Figs. 1-3 depict but two example embodiments wherein gates 28 and 26 are only on one respective side of a channel region. Of course, access gate 22 may alternately be over side 35 in Fig. 3 (not shown), or control 15 gate 26 could be over side 38 in Fig. 3 (not shown).

In one embodiment, the access gate may comprise a pair of such gates with one of each being received operatively laterally adjacent one of the pair of laterally opposing sides of the channel region. Additionally or alternately, the control gate may comprise a pair of such gates with one of each being received 20 operatively laterally adjacent one of the pair of laterally opposing sides of one of the vertically superposed, alternately doped semiconductor regions of the thyristor. For example, Fig. 4 depicts such a memory cell 10b. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being shown with the letter "b". Memory cell 25 10b includes a pair of access gates 22b and a pair of control gates 26b. In one embodiment, access gates 22b may be hard-wired together. In one embodiment, control gates 26b may be hard-wired together. Regardless, any of the Figs. 1 and 2 embodiment and the Fig. 3 embodiment may be combined wherein either the access gate or control gate comprises a pair of such gates on opposing lateral 30 sides with the other comprising only a single gate on only one lateral side.

In one embodiment, a memory cell comprises a plurality of alternately doped, superposed semiconductor regions at least an elevationally inner portion

of which forms an upwardly directed container shape in lateral cross section. The semiconductor regions collectively comprise serially electrically connectable portions of a thyristor and an access transistor of the memory cell and which share one of the doped semiconductor regions. An access gate is
5 operatively laterally adjacent an unshared of the semiconductor regions of the access transistor. A control gate is operatively laterally adjacent an unshared of the semiconductor regions of the thyristor. By way of example only, any of the embodiments of Figs. 1-4 as shown and described are such example memory cells.

10 For example with respect to the depicted memory cells, an elevationally inner upwardly directed container shape in lateral cross section of semiconductor regions 15-20 is indicated generally with reference numeral 40. In one embodiment and as shown, the upwardly directed container shape is in the form of a general U-shape. "V" and/or other upwardly directed container
15 shapes may be used. In one embodiment, the access gate is received laterally within the upwardly directed container shape (i.e., Figs. 1, 2, and 4), and in one embodiment is not received laterally outside of the upwardly directed container shape (i.e., Figs. 1 and 2). In one embodiment, the access gate is received laterally outside of the upwardly directed container shape (i.e., Figs. 3 and 4),
20 and in one embodiment is not received laterally within the upwardly directed container shape (i.e., Fig. 3). In one embodiment, the access gate comprises a pair of access gate portions, one of which is received laterally within the upwardly directed container shape and another of which is received laterally outside the upwardly directed container shape (i.e., Fig. 4). Any one or
25 combination of the just-described lateral orientations with respect to the access gate may additionally or alternately occur with respect to the control gate.

In one embodiment, the container shape as a general U-shape has a pair of vertical stems having a base extending laterally there-between in the lateral cross section, with one of the stems being taller than the other. For example
30 with respect to the embodiments of Figs. 1-4, U-shape 40 may be considered as having vertical stems 41 and 43 having a base 44 extending laterally there-between. Vertical stem 41 is taller than vertical stem 43. Alternately by way of

examples only, the height of the respective stems could be reversed whereby a stem 43 of the access transistor is taller (not shown) than a stem 41 of the thyristor, or such stems may be of equal height/tallness (not shown). Regardless, other attributes as described above may be used.

5 Embodiments of the invention encompass a memory array comprising a horizontal array of memory cells, with one such example memory array 50 that includes memory cells 10 being shown and described with reference to Fig. 5. Like numerals from Figs. 1 and 2 have been used in Fig. 5 where appropriate, with some construction differences and additions being indicated with different
10 numerals. Array 50 is received over some suitable base substrate 51, and comprises a plurality of thyristors 12 substantially aligned in a plurality of rows 52 in a first direction "x" and in a plurality of columns 54 in a second direction "y" that angles relative to the first direction "x". In one embodiment as shown, "x" and "y" are perpendicular. Individual of the thyristors comprise a plurality
15 of alternately doped, vertically superposed semiconductor regions, for example regions 15-18.

 Array 50 includes a plurality of vertically oriented access transistors 14 substantially aligned in a plurality of rows 56 in first direction "x" and in a plurality of columns 54 in second direction "y". Accordingly in one
20 embodiment, thyristor columns 54 and access transistor columns 54 may be the same. Individual of the access transistors have an access gate which comprises a portion of individual conductive access gate lines 58 oriented in a plurality of rows in first direction "x". A control gate is operatively laterally adjacent one of the plurality of vertically superposed, alternately doped semiconductor
25 regions of individual of the plurality of thyristors 12, for example control gates 26 which are operatively laterally adjacent respective semiconductor regions 17. Individual of the control gates comprise a portion of individual conductive control gate lines 60 oriented in a plurality of rows in first direction "x". In one embodiment, the thyristors are vertically taller than the access transistors. In
30 one embodiment, the access gate lines are spaced laterally of the control gate lines, and in one embodiment alternate one after the other across the horizontal array in second direction "y". In one embodiment, the access gate lines and

control gate lines elevationally overlap, and in one embodiment are elevationally coincident. Regardless, the rows, columns, and/or lines therein may be straight linear as shown or curvilinear (not shown).

5 A plurality of cathode lines 62 are substantially aligned in a plurality of rows in first direction "x" elevationally outward of access gate lines 58 and elevationally outward of control gate lines 60. Cathode lines 62 may be homogenous or non-homogenous, and comprise current conductive material. A plurality of anode lines 64 are substantially aligned in a plurality of columns in second direction "y" elevationally outward of control gate lines 60 and
10 elevationally outward of access gate lines 58. Regardless, lines 62 and/or 64 may be straight linear as shown or curvilinear (not shown).

Fig. 5 depicts an example embodiment wherein anode lines 64 are elevationally outward of cathode lines 62. Alternately, the cathode lines may be elevationally outward of the anode lines (not shown). In one embodiment, the
15 cathode lines are elevationally outward of the vertically oriented access transistors. In one embodiment, the anode lines are elevationally outward of the thyristors. Any other attribute as described above with respect to the Figs. 1 and 2, or other embodiments, may be used.

Fig. 6 by way of example only, depicts another example memory
20 array 50a comprising a horizontal array of the example memory cells 10a of the Fig. 3 embodiment. Like numerals from the Figs. 3 and 5 embodiments have been used where appropriate. Any of the above just-described attributes with respect to the memory array embodiment of Fig. 5 may also be used in the Fig. 6 embodiment.

25 Fig. 7 depicts another alternate embodiment memory array 50b incorporating memory cells 10b of Fig. 4. Like numerals from the Figs. 4 and 5 embodiments have been used where appropriate. As an example, control gate lines 60/26b and access gate lines 58/22b are respectively shown as being hard-wired relative each other. Fig. 7 also depicts an example embodiment wherein
30 access gate lines and control gate lines are spaced laterally apart, with the access gate lines and control gate lines alternating in pairs across the horizontal

array in second direction “y”. Other attributes as described above with respect to the array embodiments of Figs. 5 and 6 might additionally or alternately be used in connection with the Fig. 7 array 50b.

5 The above embodiments of memory cells and memory arrays may be fabricated by any existing or yet-to-be-developed manner(s). Nevertheless, embodiments of the invention encompass methods of forming one or more memory cells which may or may not encompass some of the structural attributes described above. Accordingly, the method subject matter provided herein is not necessarily limited by the structure subject matter, nor is the structure subject
10 matter as just-described necessarily limited by the method by which such structure(s) may be fabricated.

An embodiment of the invention encompasses a method of forming a memory cell comprising a vertically oriented thyristor and a control gate operatively laterally adjacent thereto. Such memory cell also comprises a
15 vertically oriented access transistor which shares a doped semiconductor region with the thyristor. One such method is described by way of example only with reference to Figs. 8-21 with respect to fabricating array 50 of Fig. 5. Accordingly, like numerals from the Figs. 1, 2 and 5 embodiments have been used where appropriate, with some construction differences or construction
20 precursors being indicated with different numerals. Fig. 8 depicts a substrate fragment 70 comprising, for example, a base 51 having semiconductor material 72 formed thereover. Trenches 73 have been etched through semiconductor material 72, whereby material 72 remains as plates or fins oriented in the “y” direction. Such are shown as being straight rectangular, although other shapes
25 including curved or arcuate shapes might alternately or additionally be used.

Referring to Fig. 9, gaps 73 have been filled with dielectric material 74 which has then been planarized back. Any suitable dielectric material may be used, with doped or undoped silicon dioxide, silicon nitride, etc. being examples. Any masking material (not shown) which may have been used to
30 produce the structure of Fig. 8 may be received over semiconductor material 72 in the structure of Fig. 9.

Referring to Fig. 10, substrate 70 has been patterned orthogonally to the pattern depicted by Fig. 8, thereby forming blocks 71 of alternating semiconductor material and dielectric material having trenches 75 (only one being shown) formed between blocks 71.

5 Referring to Fig. 11, trench 75 has been filled with dielectric material 76. Examples include those described above with respect to dielectric material 74. In one embodiment, materials 74 and 76 may be of the same composition or at least be capable of being etched at substantially the same rate relative one another. Regardless, the processing through Fig. 11 depicts but one example of
10 forming a block 78 of semiconductor material 72 over a substrate, with multiple such blocks 78 being shown.

Referring to Fig. 12, blocks 78 have been etched into to form an upwardly directed container shape (in the depicted embodiment a general U-shape) of semiconductor material 72 in lateral cross section with respect to individual
15 blocks. In one embodiment where the container shape is of a general U-shape, such has a pair of vertical stems 80 having a base 82 extending laterally there-between in such lateral cross section. As an example, suitable masking material (not shown) may be provided over the outer surfaces of the structure of Fig. 12. Openings may be formed there-through which correspond in lateral and
20 longitudinal dimensions to the trenches formed in Fig. 12, for example by etching, to produce the depicted cross-sectional upwardly directed container shape. Etching may be conducted, for example, to leave a thickness of base 82 of from about 20 nanometers to 50 nanometers. Materials 72 and 74 may be etched simultaneously and/or sequentially.

25 Referring to Fig. 13, base 82 between stems 80 has been ion implanted with a conductivity modifying impurity of a first type to a first impurity concentration, for example to comprise region 18. The depicted laterally inner facing sidewalls within the container shape and the elevationally outer surfaces of the Fig. 13 structure may be masked (not shown) during such ion implanting.
30 During or after such ion implanting, the conductivity modifying impurity may spread laterally, for example as shown. In one embodiment, the first type is n, with example dopant implant species being phosphorous and/or arsenic.

Alternately, the first type may be p, with an example dopant implant species being boron.

Referring to Fig. 14, gate dielectric 24, 28 has been deposited over inner facing sidewalls of at least semiconductor material 72. Such may be of the same composition or of different compositions. The gate dielectric may be formed by one or both of depositing a layer over the substrate, or as another example and as shown by thermally oxidizing the exposed surfaces of semiconductor material 72 including for example the uppermost surface of the depicted region 18. Subsequently, a current conductive material may be deposited to line the depicted openings, and subsequently subjected to an anisotropic spacer etch to form control gate lines 26/60 and access gate lines 22/58. Thus, a control gate is provided operatively laterally adjacent an intermediate portion of one stem 80, and an access gate of an access transistor is provided operatively laterally adjacent an intermediate portion of the other stem 80. Gate dielectric 24, 28 may be exposed and etched through between gate lines 26/60 and 22/58. Further as shown, semiconductor material 72 of region 18 there-beneath may be etched elevationally inwardly and/or undercut laterally.

Referring to Fig. 15, dielectric 86 has been deposited to fill remaining center volume of the container shapes, and subsequently planarized back.

Referring to Fig. 16, a suitable conductivity modifying impurity implant of the first type has been conducted into elevationally outermost portions of pair of stems 80, thereby forming example semiconductor regions 16. Referring to Fig. 17, at least such regions 16 have been masked and an implant of the first type conducted into the respective opposing stems to form semiconductor regions 20 of access transistors 14. Accordingly, elevationally outermost portions of one of the pair of stems 80 (namely the left-illustrated of such pairs of stems) is provided at a second impurity concentration of the first type (regions 16) that is lower than the first type impurity concentration within region 18.

Intermediate portions of stems 80 between elevationally outermost portions 16, 20 and base 82/18 are doped with a conductivity modifying

impurity of a second type different from the first type and to a third impurity concentration, for example to form semiconductor regions 17 and 19. In one embodiment and as an example, semiconductive material 72 of blocks 78 (Fig. 11) may be provided in Fig. 11 and before to be entirely doped with

5 conductivity modifying impurity of the second type to the third impurity concentration. Regions 16, 18 and 20 may be provided at other impurity concentrations of the second type by the processing described above with respect to Figs. 15, 16 and 17. Regardless, regions 16 and/or 20 may be doped with their respective conductivity modifying impurity concentrations before or
10 after the implanting to produce regions 18.

Referring to Fig. 18, cathode lines 62 have been formed. Such may be provided by any suitable existing or yet-to-be-developed manner(s), with subtractive patterning and etch and/or damascene-like processing being examples. The respective cathode lines 62 may be hard-wired together as-
15 shown.

Referring to Fig. 19, semiconductor material doped with a conductivity impurity of the second type to a fourth impurity concentration has been formed elevationally outward of and directly against elevationally outermost portion 16 of the left-illustrated stems, thereby forming semiconductor region 15. In this
20 document, a material or structure is “directly against” another when there is at least some physical touching contact of the stated materials or structures relative one another. In contrast, “over” encompasses “directly against” as well as constructions where intervening material(s) or structure(s) result(s) in no physical touching contact of the stated materials or structures relative one
25 another. The fourth impurity concentration is greater than the third impurity concentration. Semiconductor regions 15 may also be formed by any suitable existing or yet-to-be-developed manner(s), including for example epitaxial silicon growth. As another example, dielectric material could be deposited and contact openings subsequently etched there-through in the shape of regions 15.
30 Such openings may be subsequently filled or provided with suitable semiconductor material doped with conductivity impurity of the second type to a desired fourth impurity concentration.

Referring to Fig. 20, anode lines 64 may be formed in current conductive connection with semiconductor regions 15. Dielectric material elevationally outward of regions 16, 20 and material there-between is not shown in Fig. 20 for clarity in the drawing.

5 Referring to Fig. 21, substrate 70 has been subjected to a suitable anneal to impart lateral diffusion of the dopant within shared region 18 laterally outward. In one embodiment and as shown, such diffusing is to laterally outermost surfaces of stems 80. The processing depicted by Fig. 21 may inherently occur with respect to the above processing associated with Figs. 14-
10 20 such that a dedicated annealing step may not be conducted. Alternately, no such laterally diffusion may occur such that the finished memory cell construction may have little or no lateral diffusion, for example as depicted in Fig. 14.

Processing may be alternately conducted to produce any of the memory
15 cell or array constructions as described above with respect to Figs. 3-7, for example to provide any of the control gates and/or access gates as shown and described above.

An embodiment of the invention includes a method of forming a shared doped semiconductor region of a vertically oriented thyristor and a vertically
20 oriented access transistor. Such method comprises forming a general U-shape of semiconductor material in lateral cross section, with such shape having a pair of vertical stems and a base extending laterally there-between in such lateral cross section. The base is doped between the stems with a conductivity modifying impurity of at least one of n-type and p-type, with the shared doped
25 semiconductor region being formed there-from. Such doping may be by ion implanting or other technique.

In one embodiment, the laterally inner facing sidewalls of the stems may be masked from such doping during such doping. In one embodiment, the shared doped semiconductor region may be annealed to diffuse the conductivity
30 modifying impurity laterally outward into the stems, and in one embodiment to a

degree to the laterally outermost surfaces of the stems. The above-described processing with respect to Figs. 13-21 is but one example of such embodiments.

CLAIMS

The invention claimed is:

1. A memory cell, comprising:
a thyristor comprising a plurality of alternately doped, vertically
5 superposed semiconductor regions;
a vertically oriented access transistor having an access gate; and
a control gate operatively laterally adjacent one of the alternately doped,
vertically superposed semiconductor regions; the control gate being spaced
laterally of the access gate.
- 10 2. The memory cell of claim 1 wherein the access gate and the control
gate elevationally overlap.
3. The memory cell of claim 2 wherein the access gate and the control
gate are elevationally coincident.
4. A memory cell, comprising:
15 a vertically oriented thyristor and a control gate operatively laterally
adjacent thereto; and
a vertically oriented access transistor laterally spaced from the vertically
oriented thyristor and sharing a doped semiconductor region therewith which
extends laterally between the vertically oriented thyristor and the vertically
20 oriented access transistor.
5. The memory cell of claim 4, wherein the thyristor comprises a
cathode region, a p base region, an n base region, and an anode region vertically
superimposed one over another.

6. A memory cell, comprising:

a plurality of alternately doped, superposed semiconductor regions at least an elevationally inner portion of which forms an upwardly directed container shape in lateral cross section, the semiconductor regions collectively comprising serially electrically connectable portions of a thyristor and an access transistor of the memory cell which share one of the doped semiconductor regions;

an access gate operatively laterally adjacent an unshared of the semiconductor regions of the access transistor; and

a control gate operatively laterally adjacent an unshared of the semiconductor regions of the thyristor.

7. The memory cell of claim 6 wherein the access gate is received laterally within the upwardly directed container shape.

8. The memory cell of claim 6 wherein the access gate is received laterally within the upwardly directed container shape and not laterally outside of the upwardly directed container shape.

9. The memory cell of claim 6 wherein the access gate is received laterally outside of the upwardly directed container shape.

10. The memory cell of claim 6 wherein the access gate is received laterally outside of the upwardly directed container shape and not laterally within the upwardly directed container shape.

11. The memory cell of claim 6 wherein the access gate comprises a pair of access gate portions one of which is received laterally within the upwardly directed container shape and another of which is received laterally outside the upwardly directed container shape.

12. The memory cell of claim 6 wherein the control gate is received laterally within the upwardly directed container shape.

13. The memory cell of claim 6 wherein the control gate is received laterally within the upwardly directed container shape and not laterally outside of the upwardly directed container shape.

14. The memory cell of claim 6 wherein the control gate is received
5 laterally outside of the upwardly directed container shape.

15. The memory cell of claim 6 wherein the control gate is received laterally outside of the upwardly directed container shape and not laterally within the upwardly directed container shape.

16. The memory cell of claim 6 wherein the control gate comprises a
10 pair of control gate portions one of which is received laterally within the upwardly directed container shape and another of which is received laterally outside the upwardly directed container shape.

17. The memory cell of claim 6 wherein the control gate and the access
15 gate are received laterally outside of the upwardly directed container shape and not laterally within the upwardly directed container shape.

18. The memory cell of claim 6 wherein the upwardly directed container shape comprises a general U-shape having a pair of vertical stems having a base extending laterally there-between in the lateral cross section, one of the stems being taller than the other.

19. A memory array, comprising:

a horizontal array of memory cells comprising:

a plurality of thyristors substantially aligned in a plurality of rows in a first direction and in a plurality of columns in a second direction angled relative to the first direction; individual of the thyristors comprising a plurality of alternately doped, vertically superposed semiconductor regions;

a plurality of vertically oriented access transistors substantially aligned in a plurality of rows in the first direction and in a plurality of columns in the second direction, individual of the access transistors having an access gate which comprises a portion of individual conductive access gate lines oriented in a plurality of rows in the first direction;

a control gate operatively laterally adjacent one of the plurality of vertically superposed, alternately doped semiconductor regions of individual of the plurality of thyristors; individual of the control gates comprising a portion of individual conductive control gate lines oriented in a plurality of rows in the first direction;

a plurality of cathode lines substantially aligned in a plurality of rows in the first direction elevationally outward of the access gate lines; and

a plurality of anode lines substantially aligned in a plurality of columns in the second direction elevationally outward of the control gate lines.

20. The memory array of claim 19 wherein the access gate lines are spaced laterally of the control gate lines.

21. The memory array of claim 20 wherein the access gate lines and the control gate lines elevationally overlap.

22. The memory array of claim 21 wherein the access gate lines and the control gate lines are elevationally coincident.

23. The memory array of claim 20 wherein the access gate lines and the control gate lines alternate one after the other across the horizontal array in the second direction.

24. The memory array of claim 20 wherein the access gate lines and the control gate lines alternate in pairs across the horizontal array in the second direction.

25. The memory array of claim 20 wherein individual of the vertically oriented access transistors comprise a respective channel region having a pair of laterally opposing sides, the access gate of individual of the vertically oriented access transistors being operatively laterally adjacent only one of the pair of laterally opposing sides of the respective channel region.

26. The memory array of claim 20 wherein individual of the vertically oriented access transistors comprise a respective channel region having a pair of laterally opposing sides, the access gate of individual of the vertically oriented access transistors comprising a pair of access gates, one of the pair of access gates being operatively laterally adjacent one of the pair of laterally opposing sides of the respective channel region, another of the pair of access gates being operatively laterally adjacent the other of the pair of laterally opposing sides of the respective channel region.

27. The memory array of claim 26 wherein the one and another access gates are hardwired together.

28. The memory array of claim 20 wherein individual of the one of the plurality of vertically superposed, alternately doped semiconductor regions of individual thyristors have a pair of laterally opposing sides; individual of the control gates being operatively laterally adjacent only one of the pair of laterally opposing sides.

29. The memory array of claim 20 wherein individual of the one of the plurality of vertically superposed, alternately doped semiconductor regions of individual thyristors have a pair of laterally opposing sides; individual of the control gates comprising a pair of control gates for individual of the thyristors, one of the pair of control gates being operatively laterally adjacent one of the pair of laterally opposing sides, another of the pair of control gates being operatively laterally adjacent the other of the pair of laterally opposing sides.

30. The memory array of claim 29 wherein the one and another control gates are hardwired together.

31. The memory array of claim 19 wherein the thyristors are vertically taller than the access transistors.

32. The memory array of claim 19 wherein the anode lines are elevationally outward of the cathode lines.

33. The memory array of claim 19 wherein the cathode lines are elevationally outward of the anode lines.

34. The memory array of claim 19 wherein the cathode lines are elevationally outward of the vertically oriented access transistors.

35. The memory array of claim 19 wherein the anode lines are elevationally outward of the thyristors.

36. The memory array of claim 19 wherein the cathode lines are elevationally outward of the vertically oriented access transistors and the anode lines are elevationally outward of the thyristors.

37. The memory array of claim 36 wherein the access gate lines are spaced laterally of the control gate lines.

38. The memory array of claim 36 wherein the anode lines are elevationally outward of the cathode lines.

39. The memory array of claim 36 wherein the access gate lines are spaced laterally of the control gate lines, and the anode lines are elevationally outward of the cathode lines.

5 40. A method of forming a shared doped semiconductor region of a vertically oriented thyristor and a vertically oriented access transistor, the method comprising:

forming a general U-shape of semiconductor material in lateral cross section, the general U-shape having a pair of vertical stems having a base extending laterally there-between in the lateral cross section; and

10 doping the base between the stems with a conductivity modifying impurity of at least one of n type and p type and forming the shared doped semiconductor region there-from.

41. The method of claim 40 wherein laterally inner facing sidewalls of the stems are masked from such doping during the doping.

15 42. The method of claim 40 wherein forming the shared doped semiconductor region there-from comprises annealing to diffuse the conductivity modifying impurity laterally outward into the stems.

43. The method of claim 42 wherein the diffusing is to laterally outermost surfaces of the stems.

44. A method of forming a memory cell comprising a vertically oriented thyristor and a control gate operatively laterally adjacent thereto, the memory cell comprising a vertically oriented access transistor which shares a doped semiconductor region with the thyristor, the method comprising:

- 5 forming a block of semiconductor material relative to a substrate;
 etching into the block to form a general U-shape of the semiconductor material in lateral cross section, the general U-shape having a pair of vertical stems having a base extending laterally there-between in the lateral cross section;
- 10 after the etching, ion implanting the base between the stems with a conductivity modifying impurity of a first type to a first impurity concentration;
 providing elevationally outermost portions of the pair of stems to be doped with a conductivity modifying impurity of the first type, providing the elevationally outermost portion of one of the pair of stems to be at a second
- 15 impurity concentration that is lower than the first impurity concentration;
 providing respective intermediate portions of the stems between the elevationally outermost portions and the base to be doped with a conductivity modifying impurity of a second type different from the first type and to a third impurity concentration;
- 20 forming semiconductor material doped with a conductivity impurity of the second type to a fourth impurity concentration elevationally outward of and directly against the elevationally outermost portion of the one stem, the fourth impurity concentration being greater than the third impurity concentration;
 providing a control gate operatively laterally adjacent the intermediate
- 25 portion of the one stem;
 providing an access gate of an access transistor operatively laterally adjacent the intermediate portion of the other of the pair of stems.

45. The method of claim 44 wherein the elevationally outermost portions of the pair of stems are doped with a conductivity modifying impurity
- 30 of the first type after the ion implanting.

46. The method of claim 44 wherein the elevationally outermost portion of the one stems is doped with a conductivity modifying impurity of the first type before the ion implanting.

47. The method of claim 44 comprising providing the control gate
5 laterally within the U-shape.

48. The method of claim 44 comprising providing the control gate laterally outside of the U-shape.

49. The method of claim 44 comprising providing the control gate both laterally within and laterally outside of the U-shape.

10 50. The method of claim 44 comprising providing the access gate laterally within the U-shape.

51. The method of claim 44 comprising providing the access gate laterally outside of the U-shape.

15 52. The method of claim 44 comprising providing the access gate both laterally within and laterally outside of the U-shape.

53. The method of claim 44 comprising providing the control gate and the access gate only laterally outside of the U-shape.

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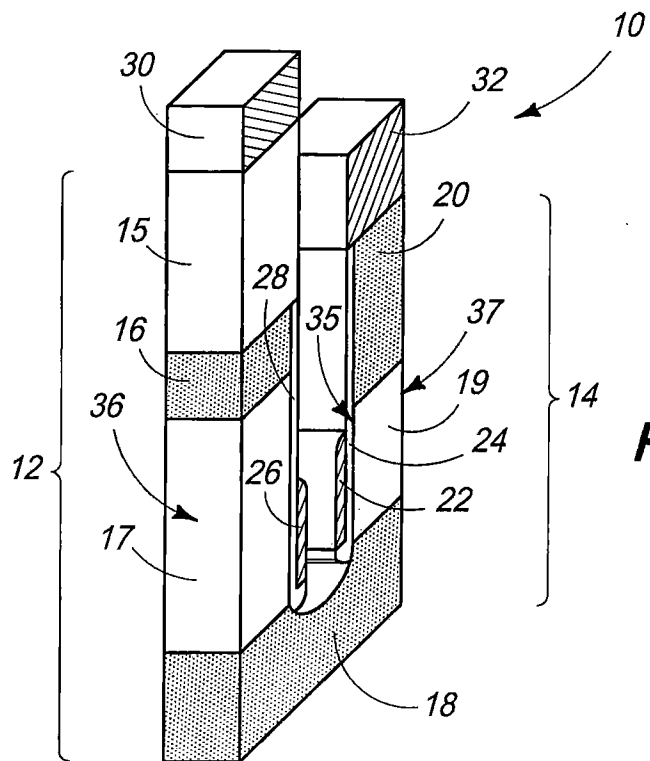
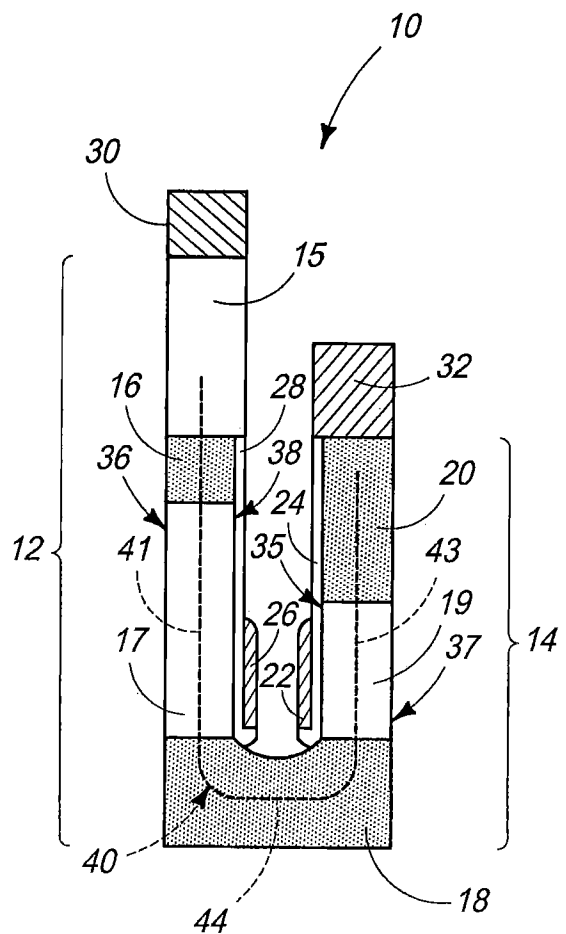


FIG. 1

FIG. 2



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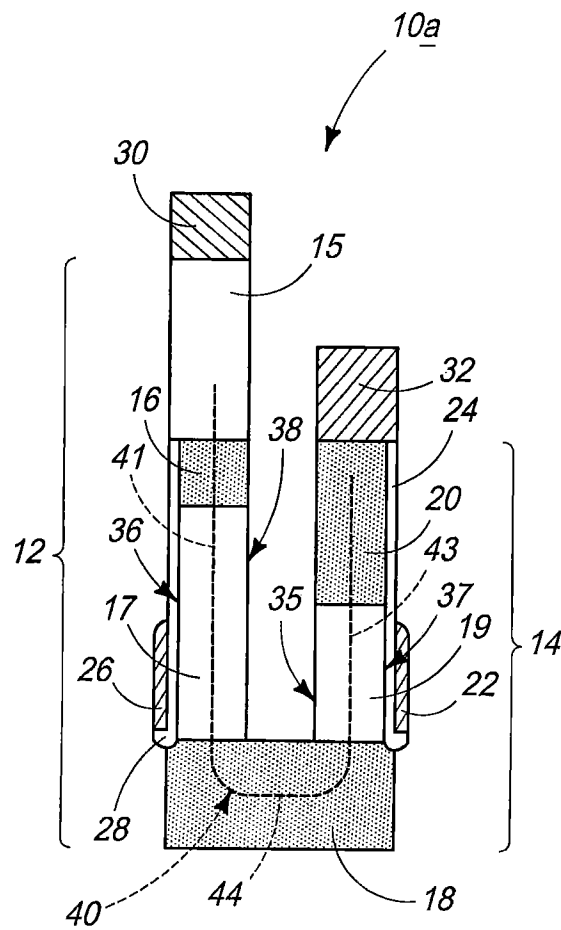
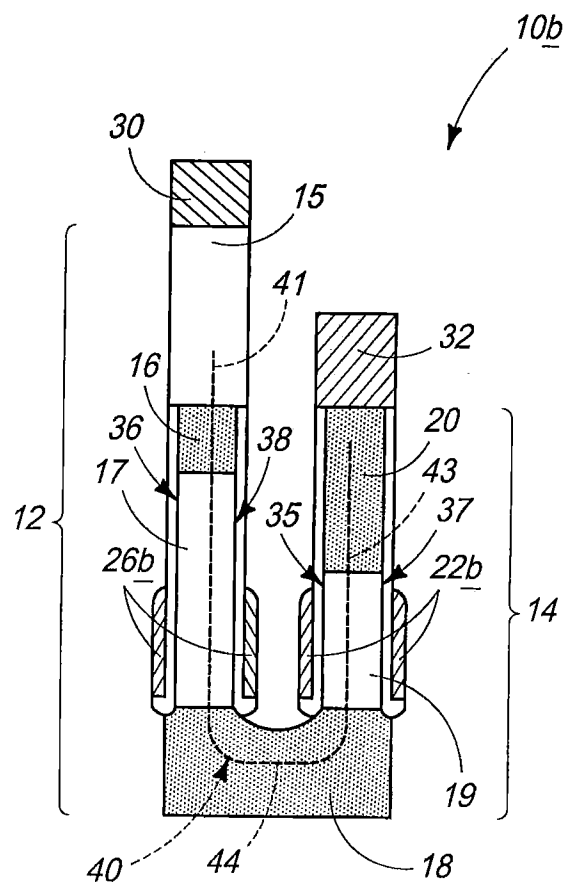


FIG. 3

FIG. 4



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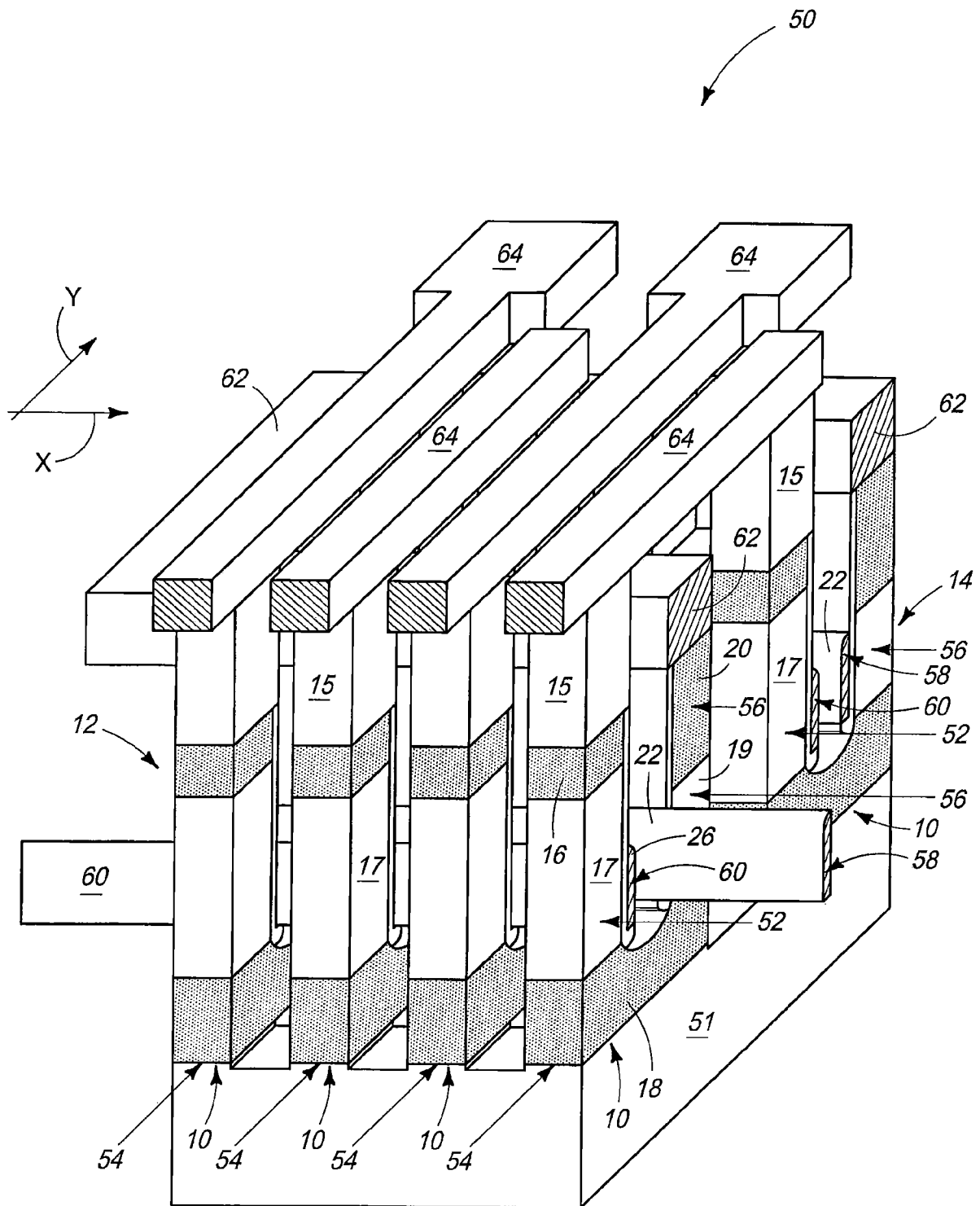


FIG. 5

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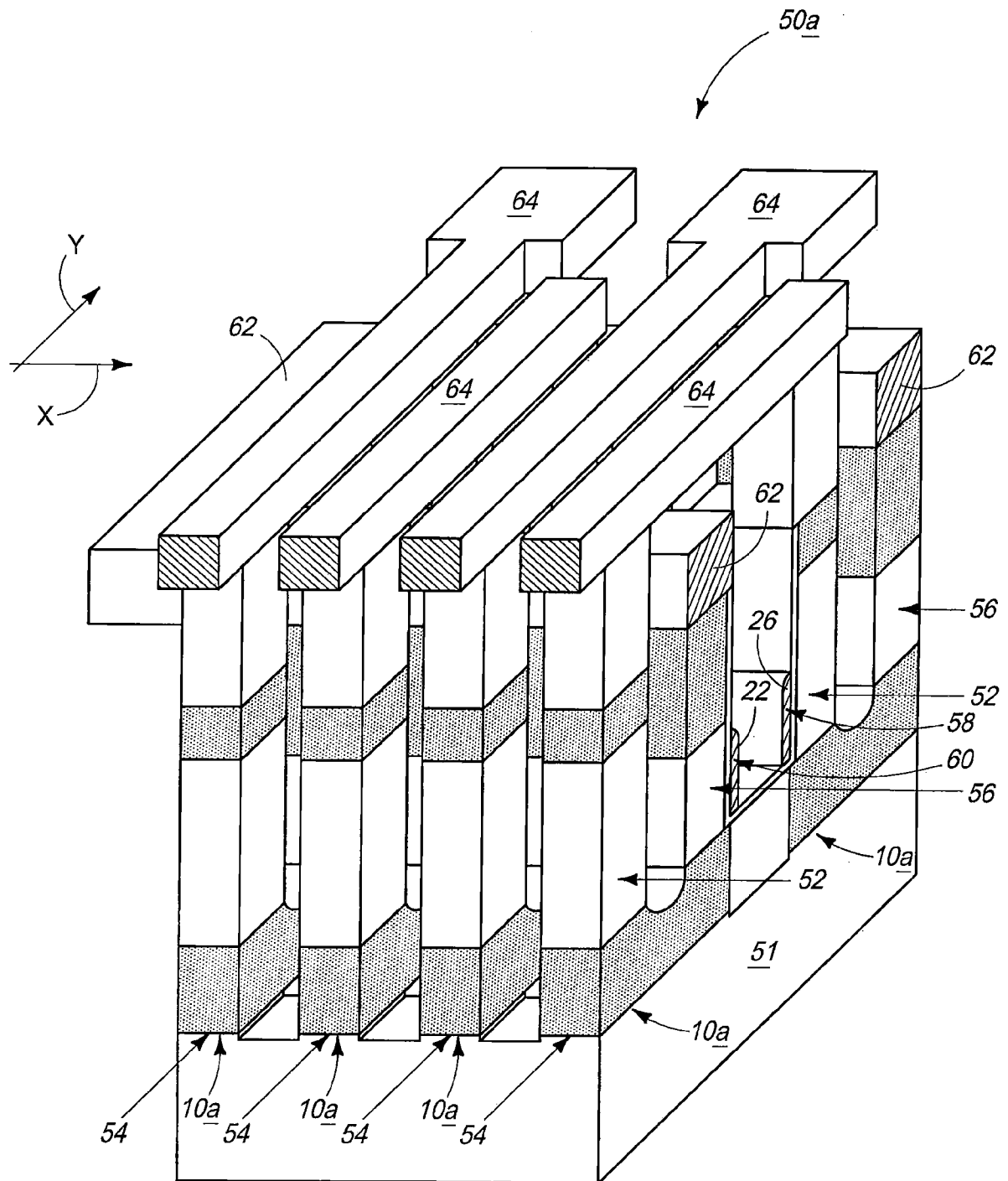


FIG. 6

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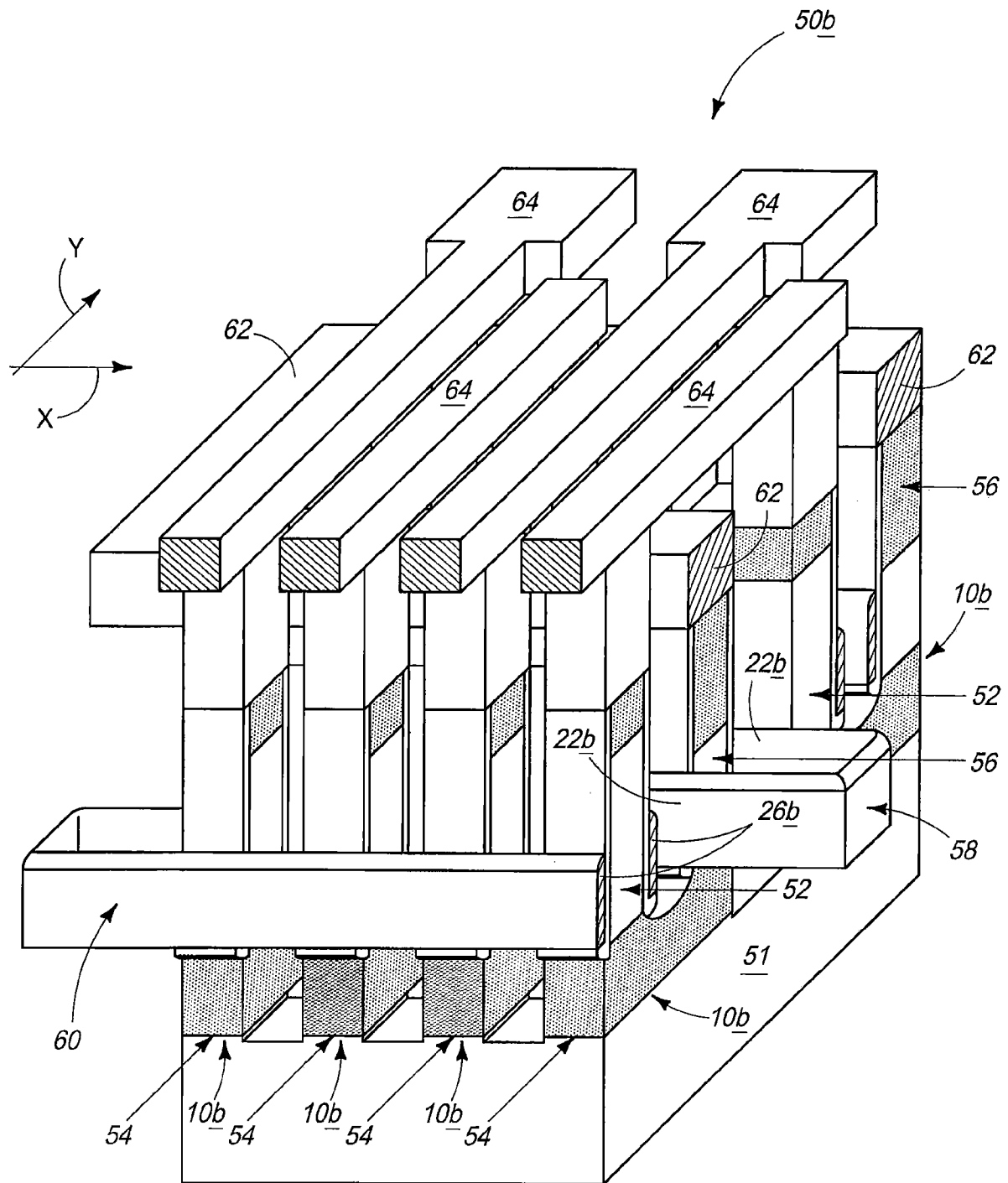
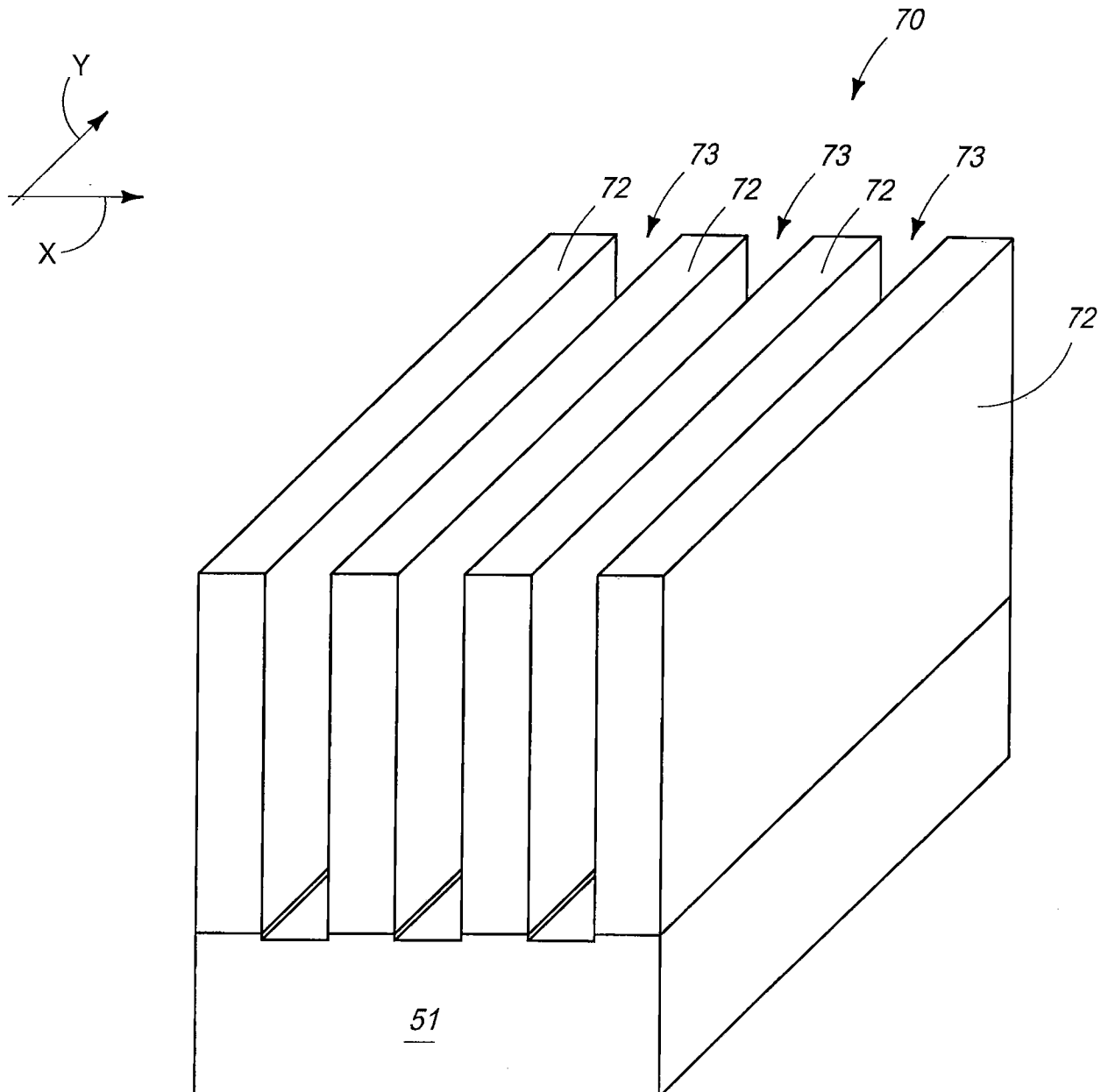


FIG. 7

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**FIG. 8**

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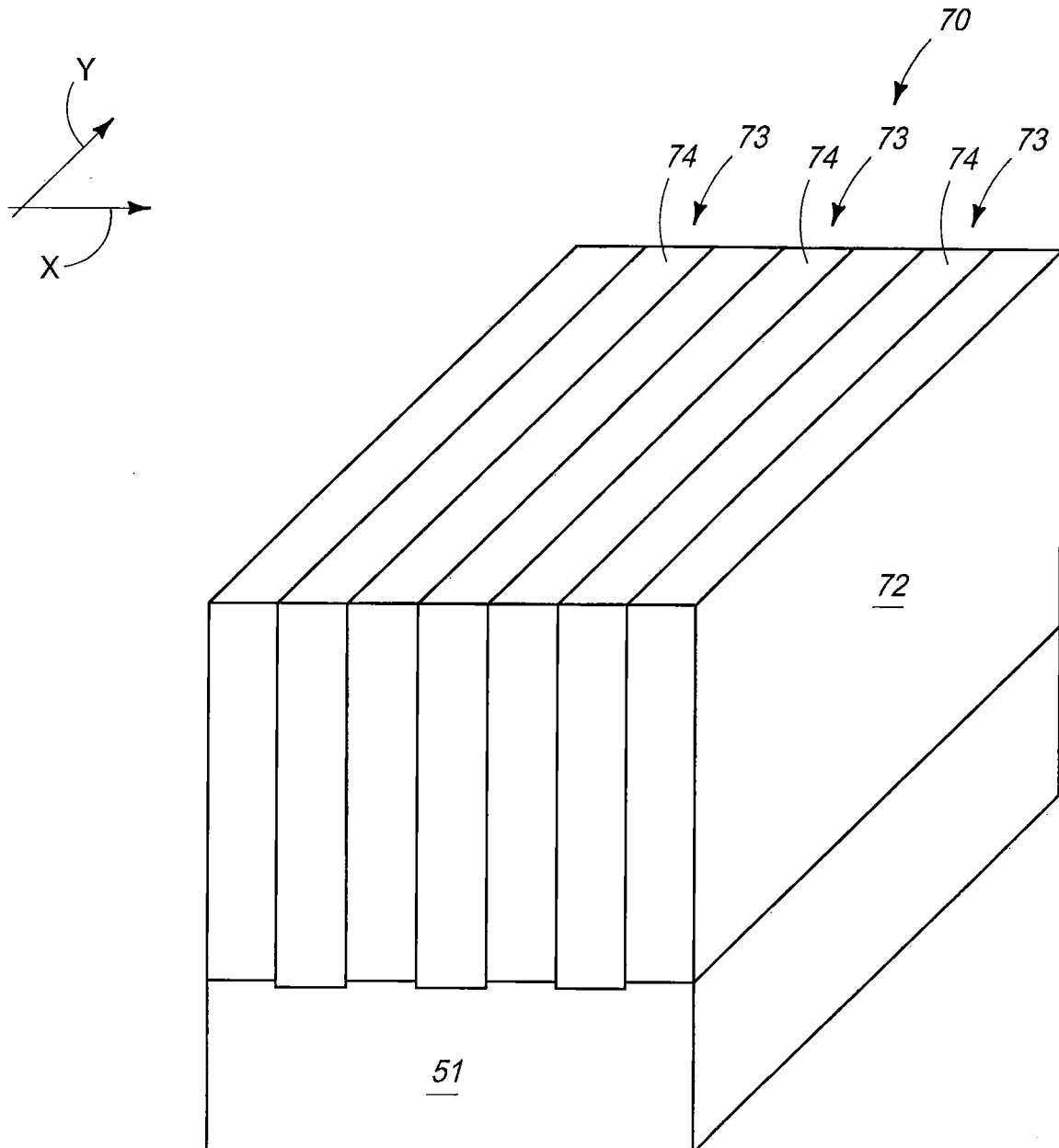


FIG. 9

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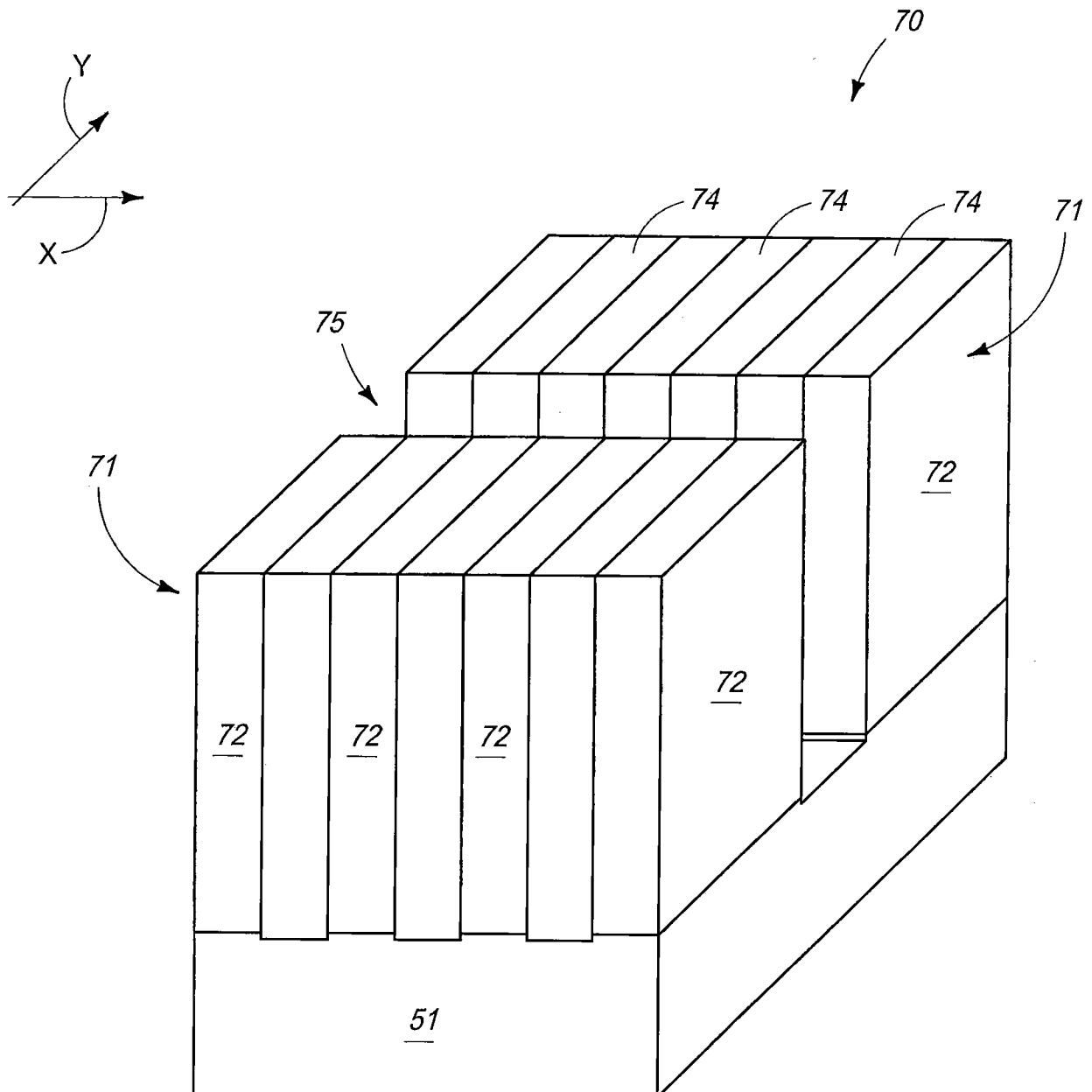
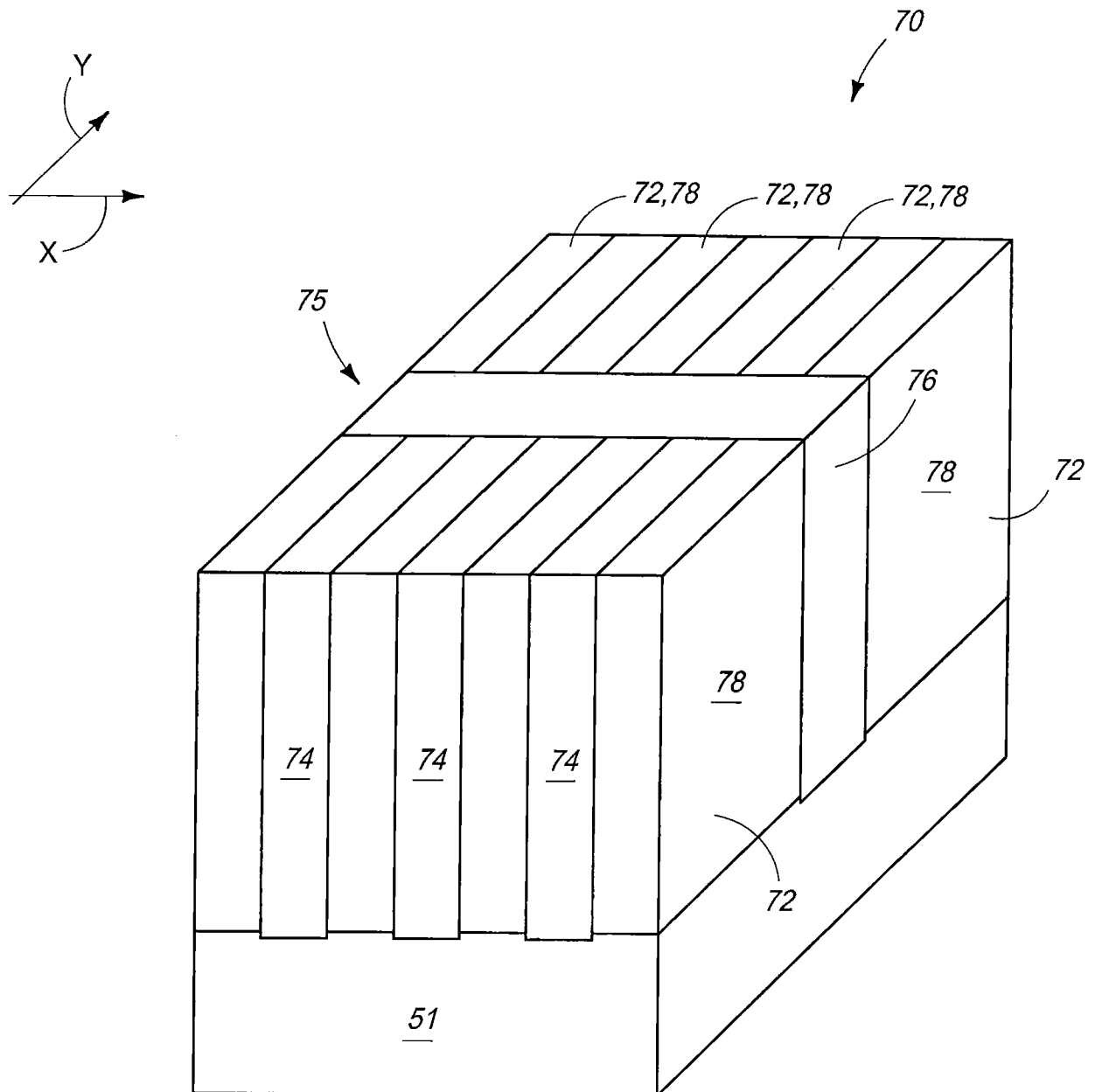


FIG. 10

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**FIG. 11**

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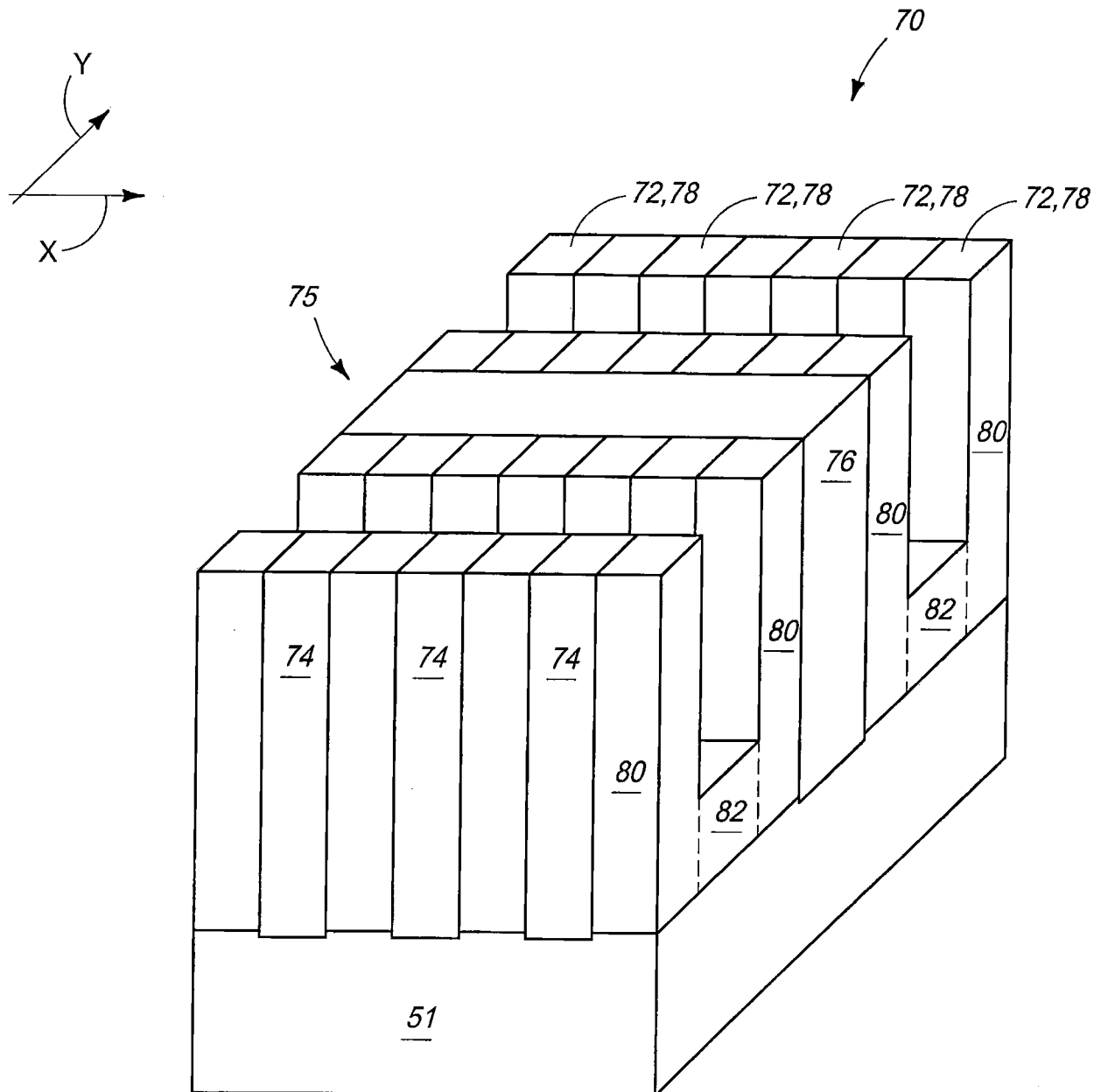
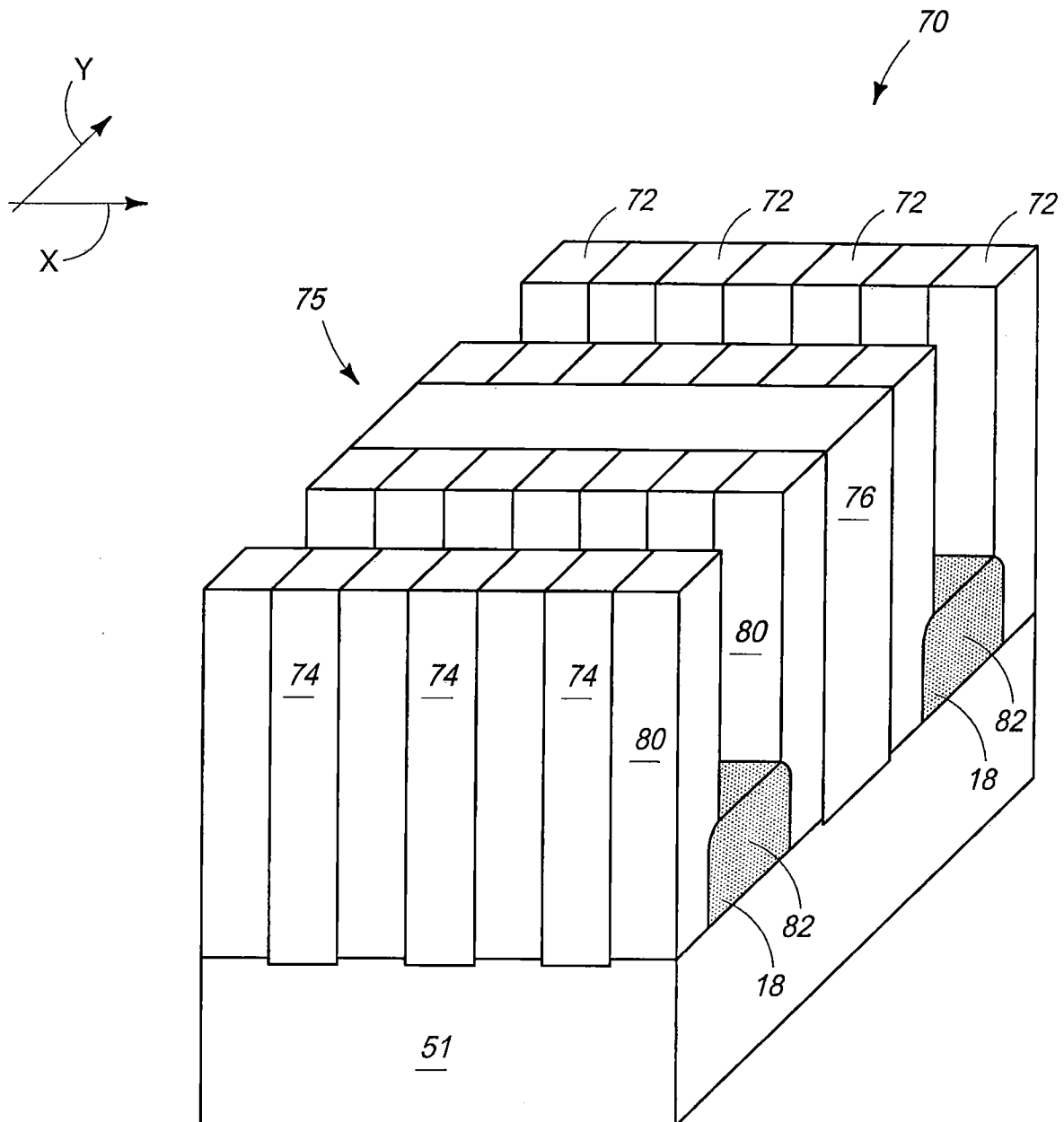


FIG. 12

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**FIG. 13**

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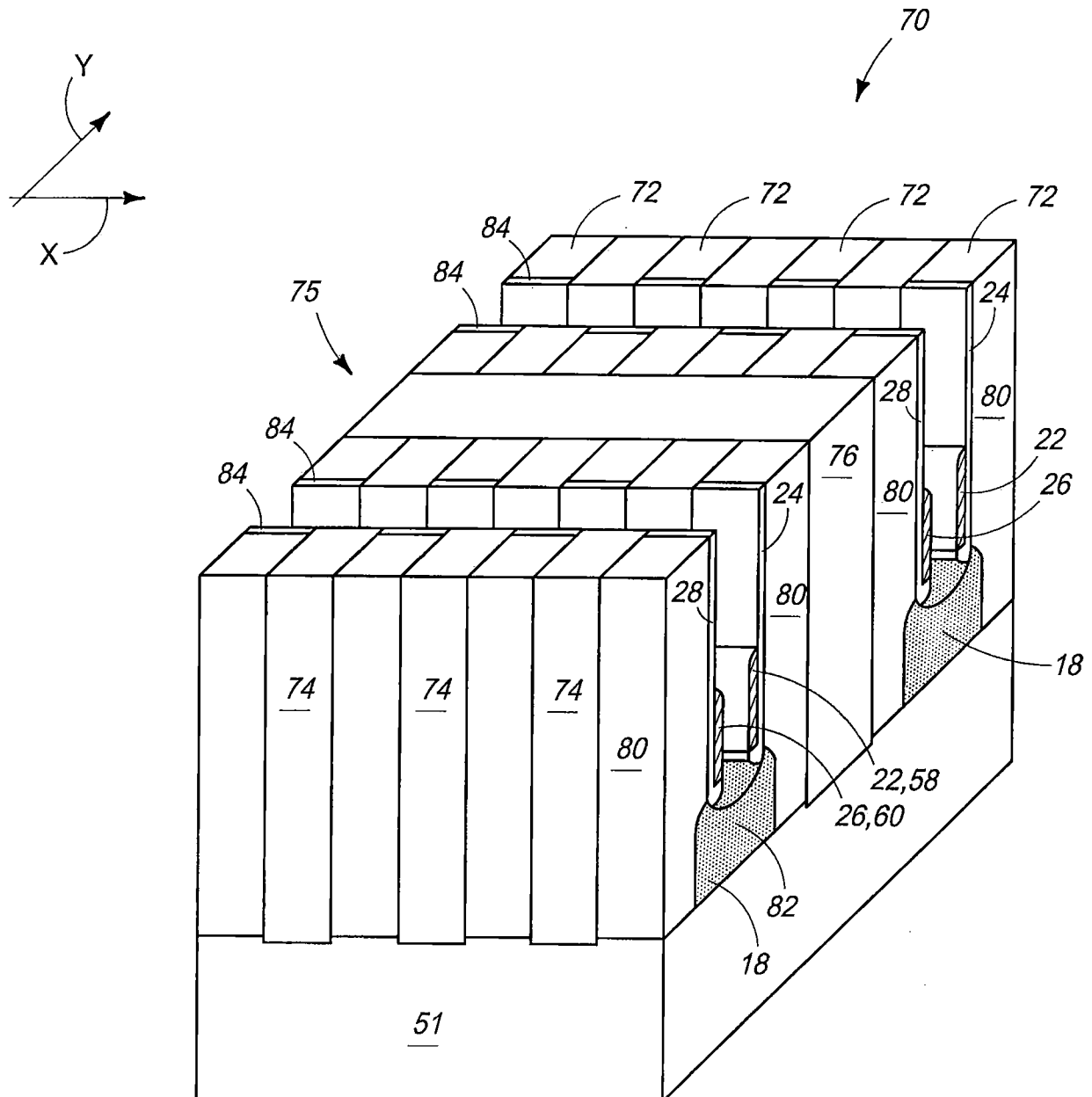


FIG. 14

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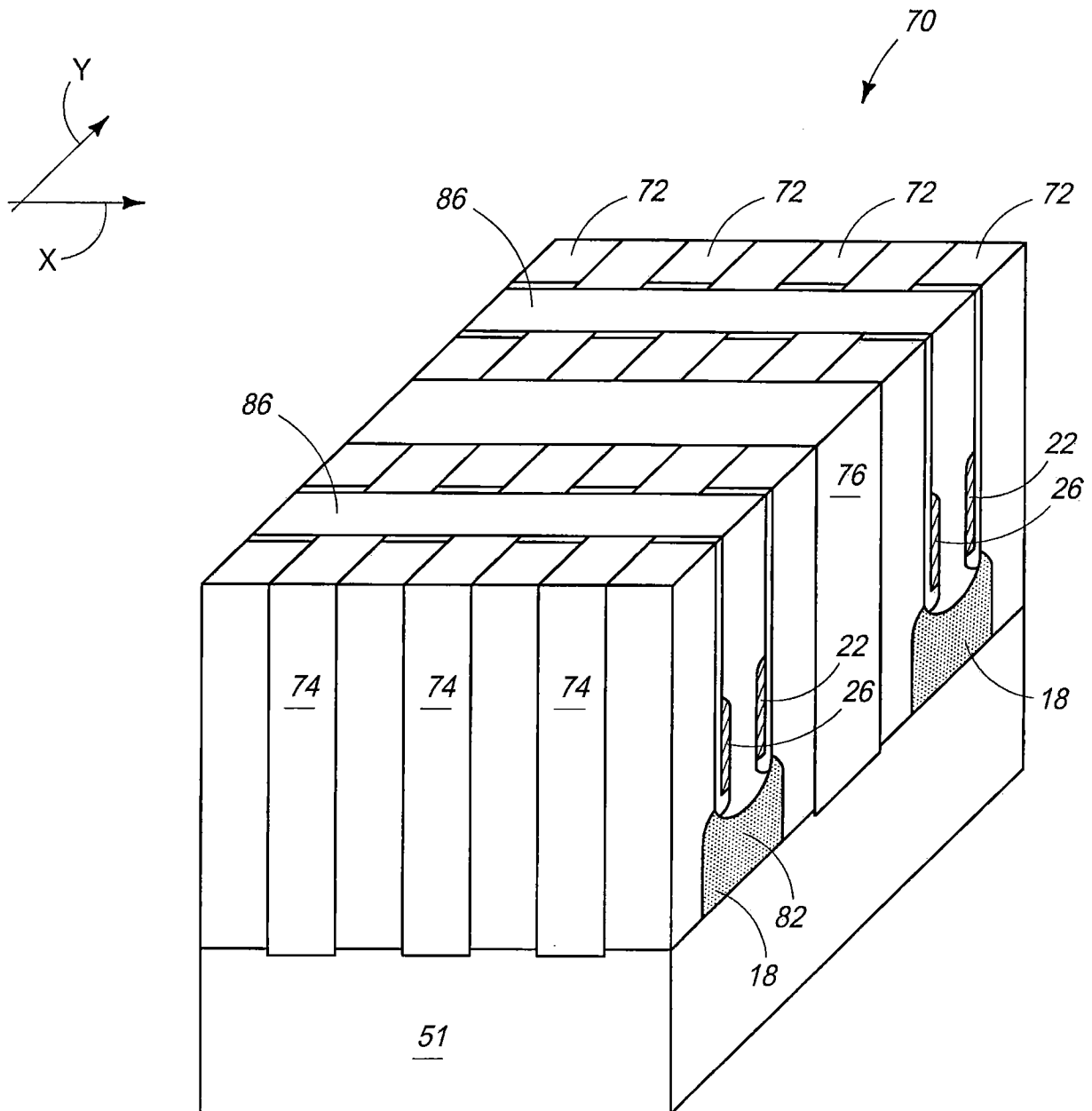


FIG. 15

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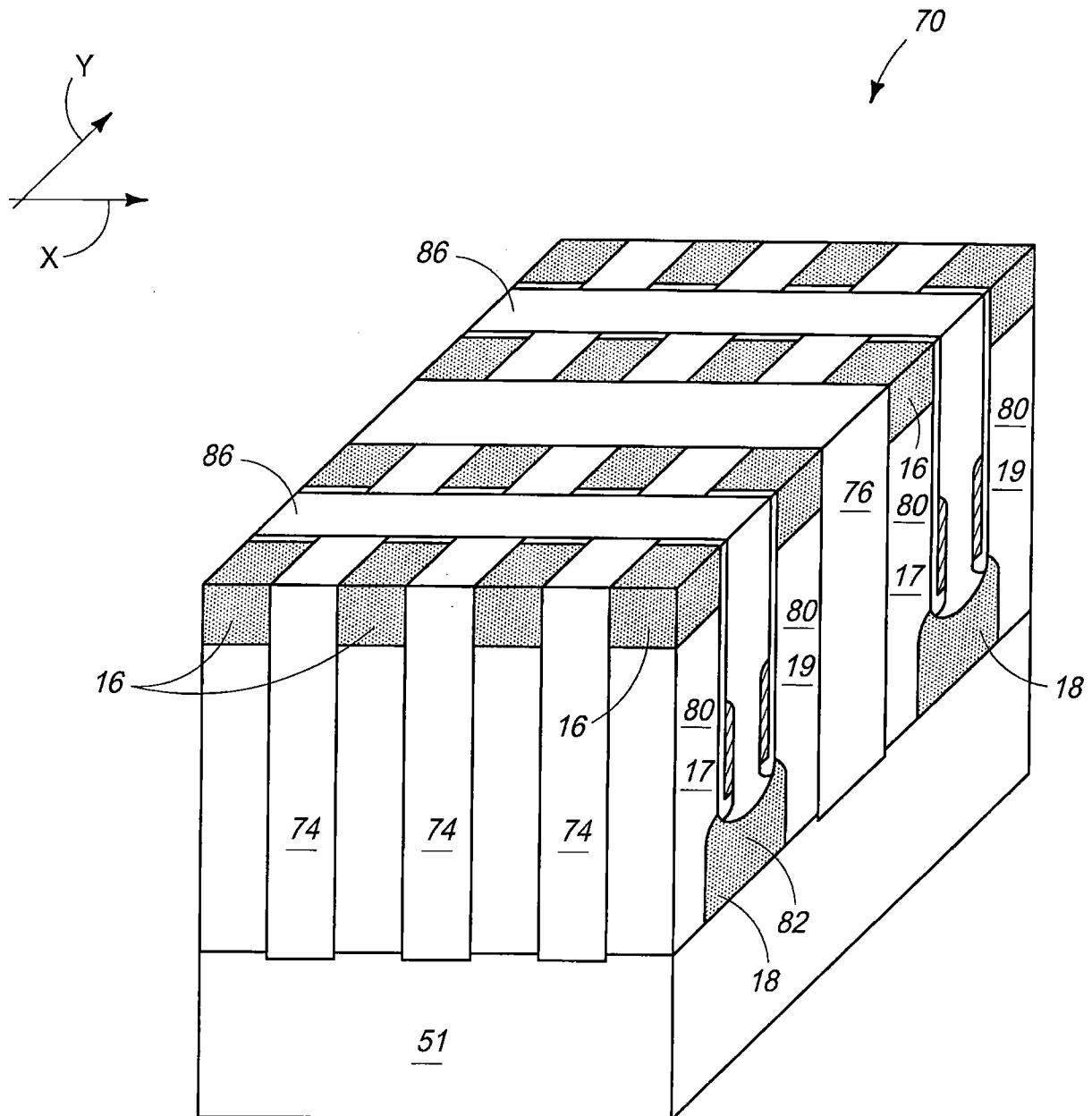


FIG. 16

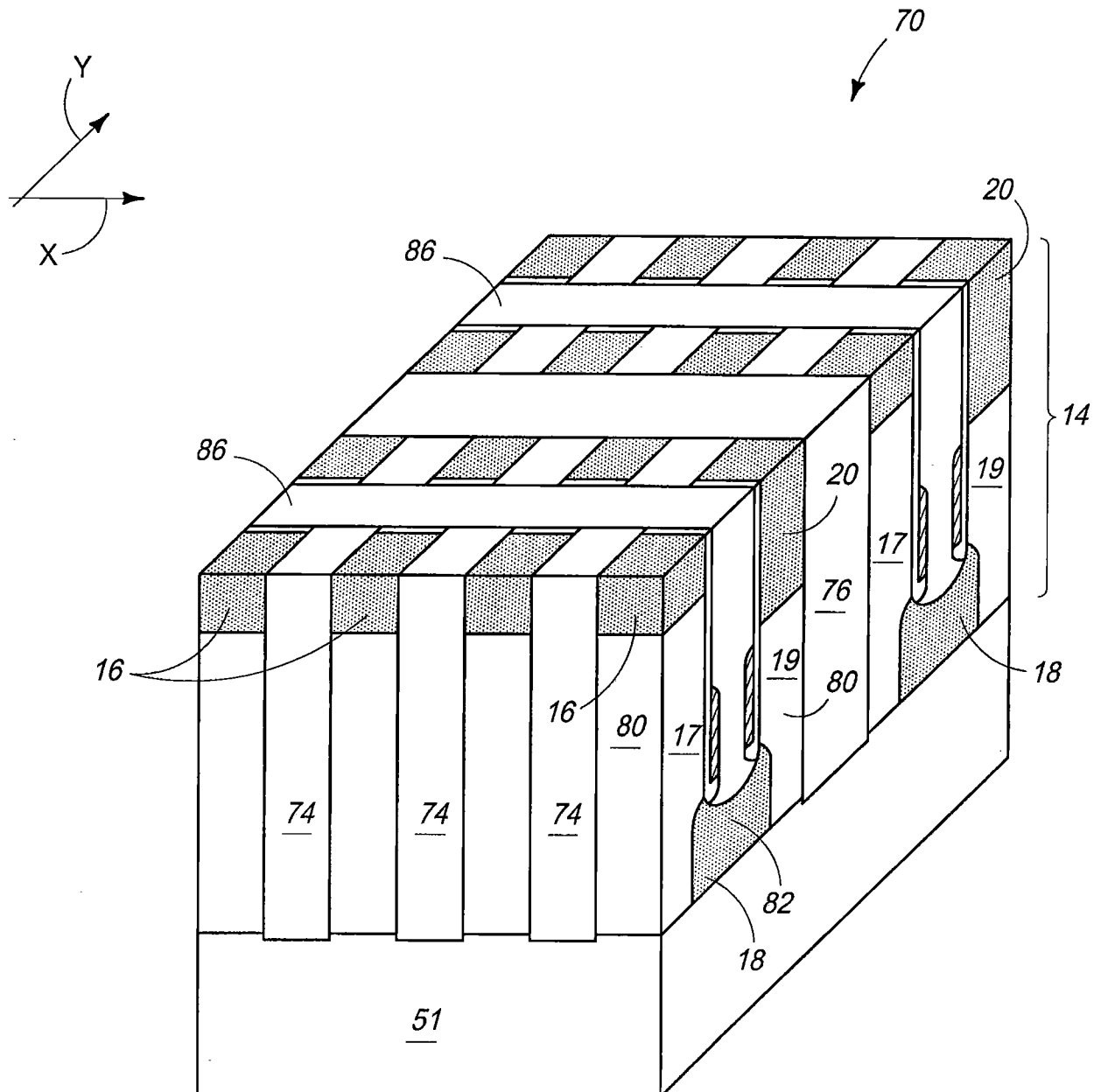


FIG. 17

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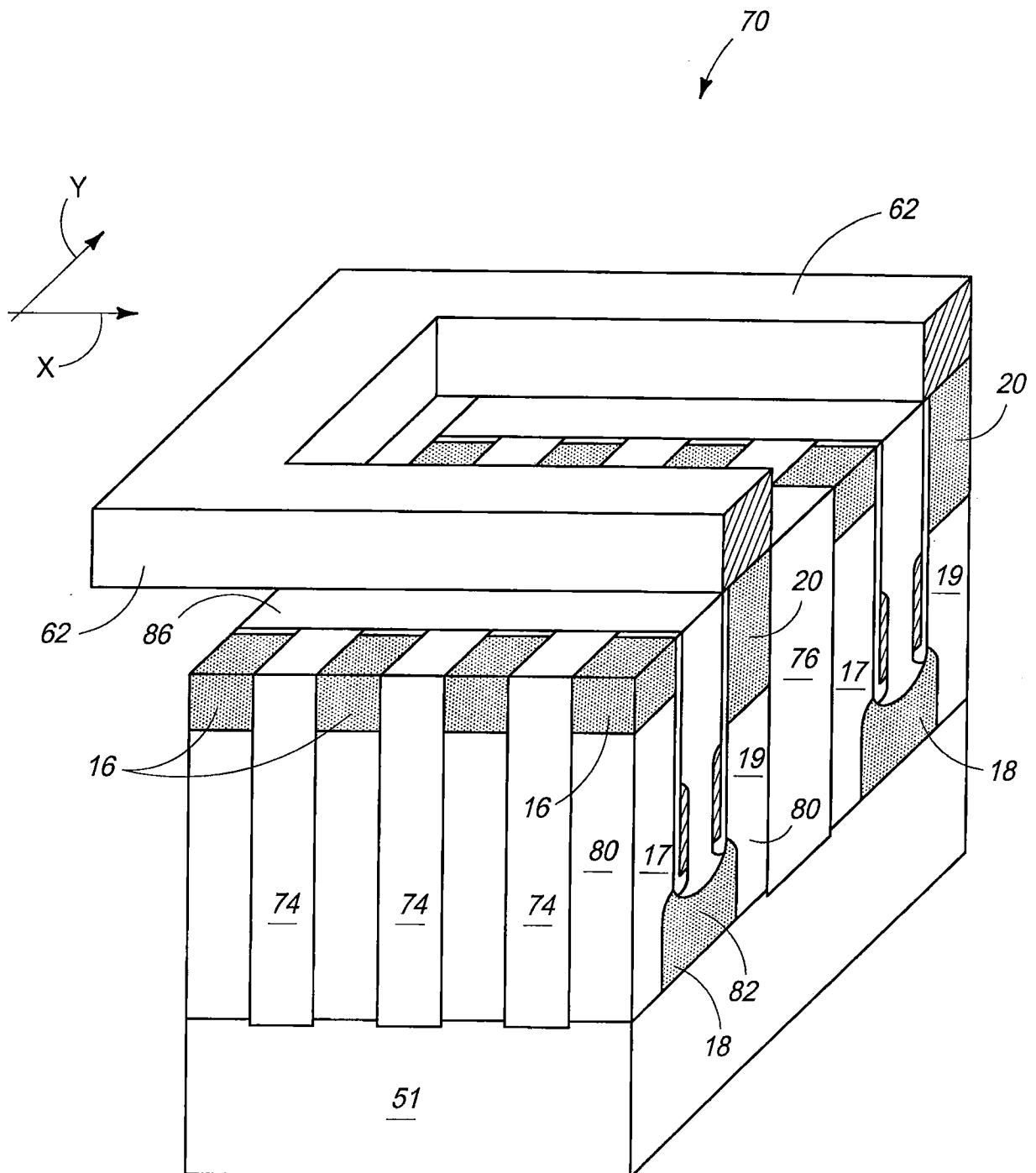
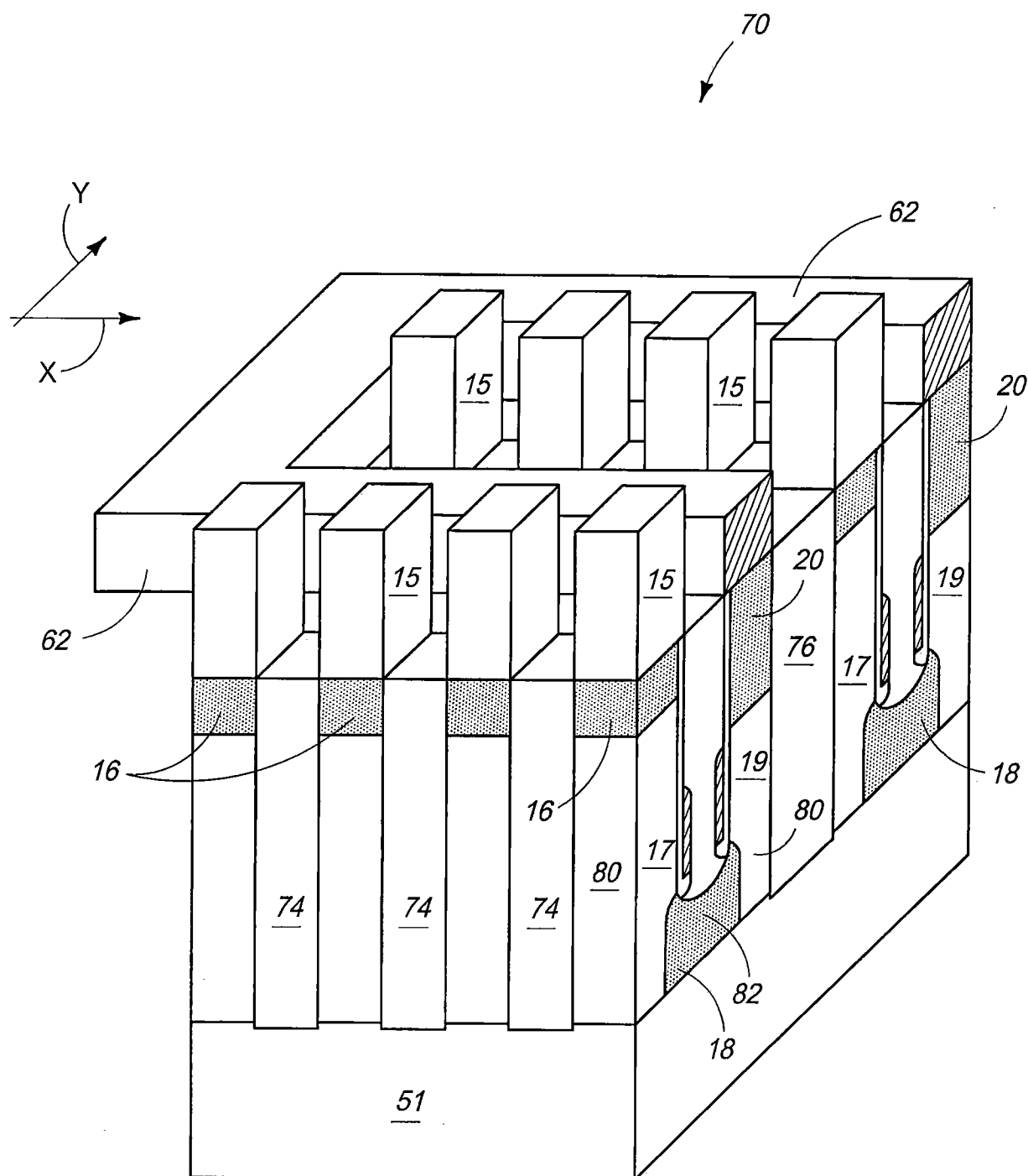
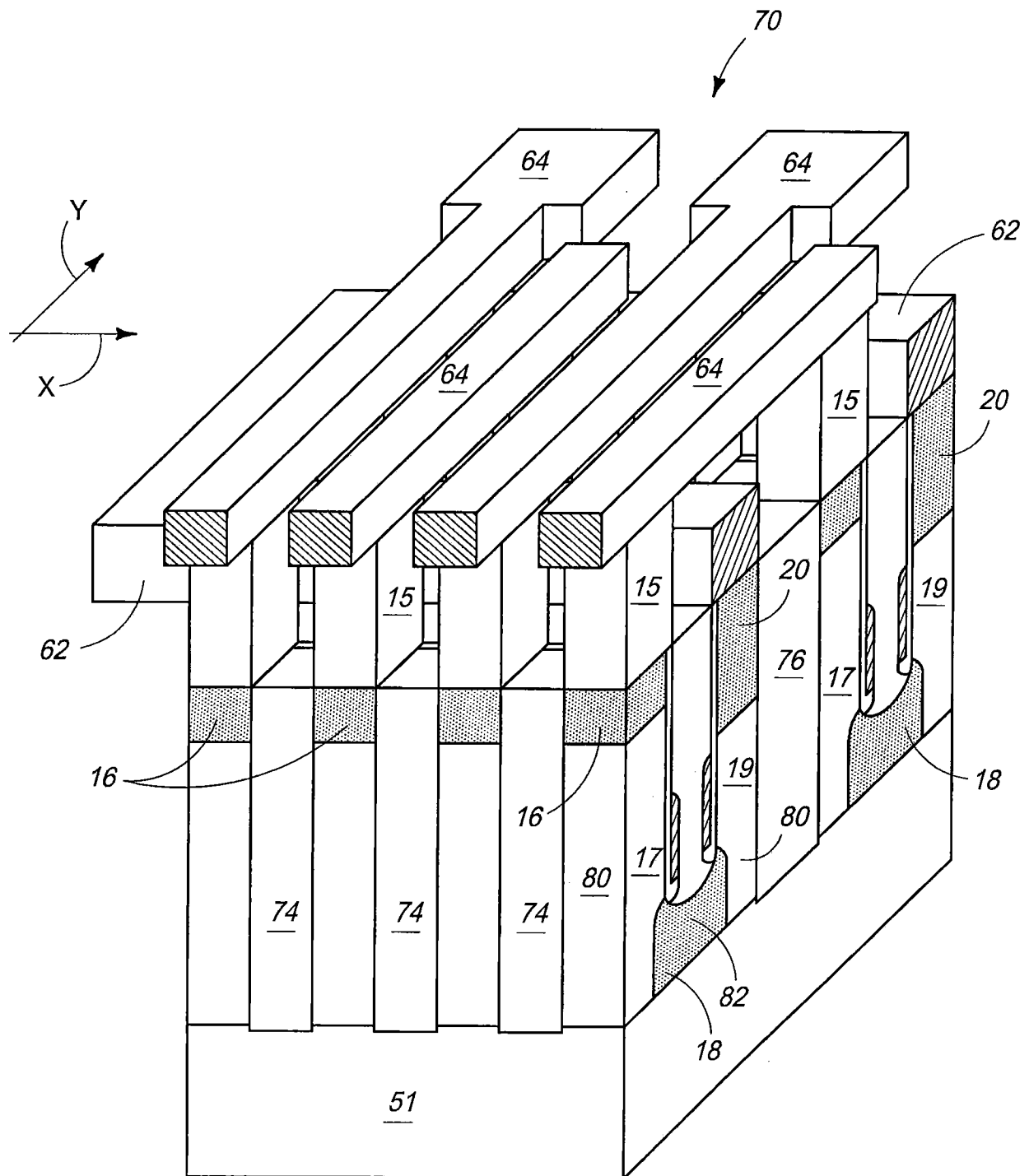


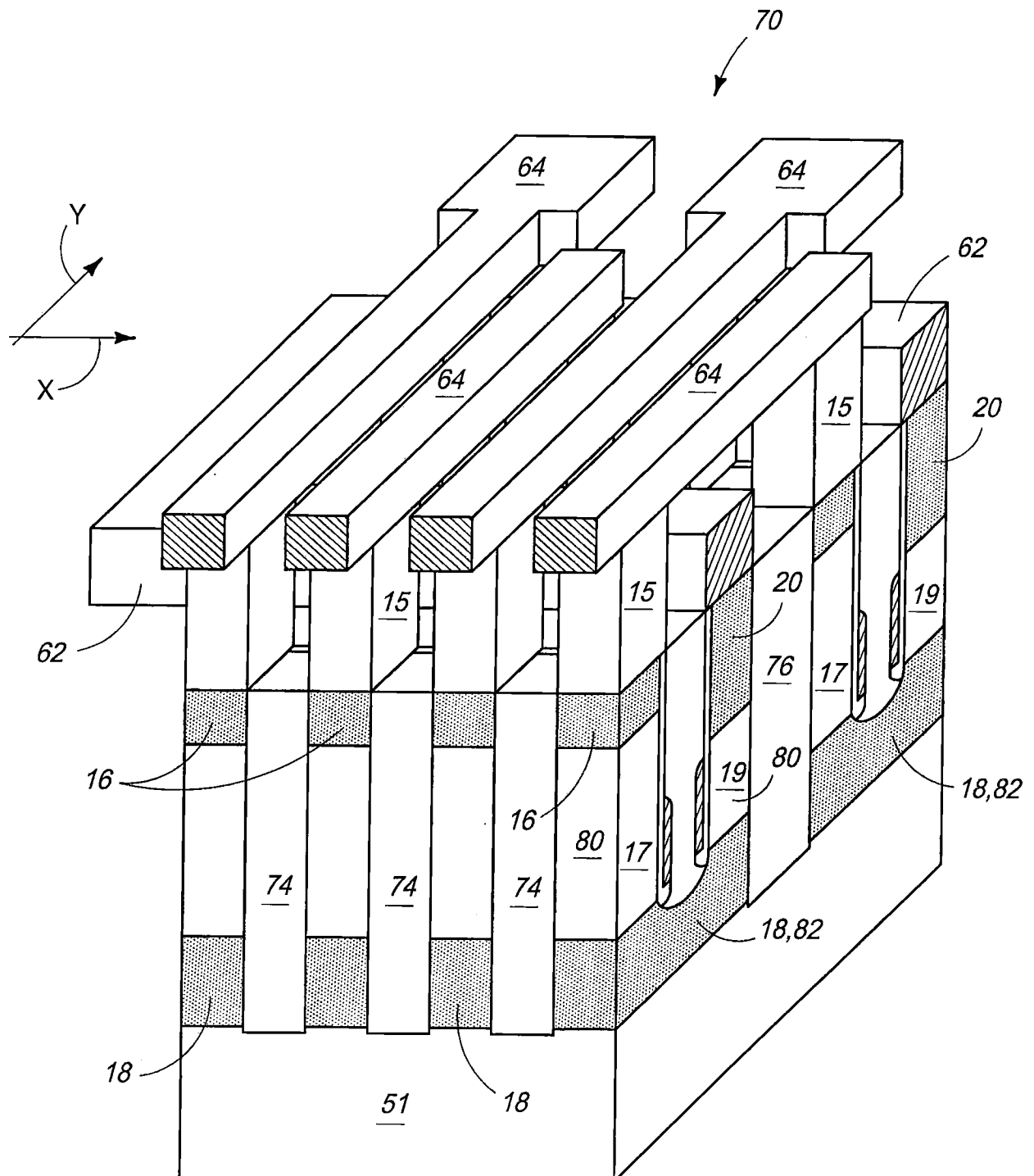
FIG. 18

**FIG. 19**

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**FIG. 20**

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**FIG. 21**