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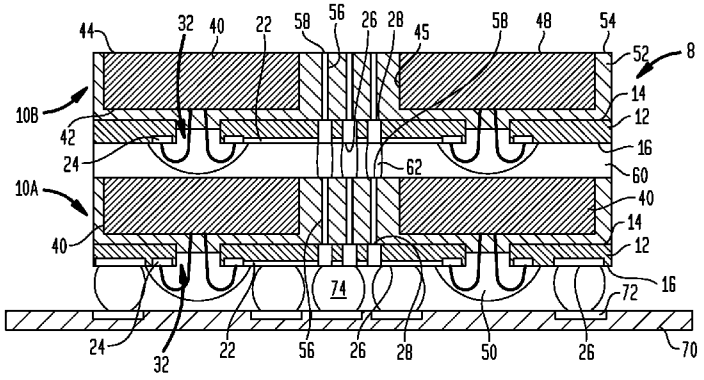
(54) Title: STACKABLE MICROELECTRONIC PACKAGE STRUCTURES

FIG. 1



(57) Abstract: A microelectronic assembly (8) includes a first microelectronic package (10A) having a substrate (12) with first (14) and second (16) surfaces and substrate contacts (24). The first package further includes first and second microelectronic elements (40) having element contacts electrically connected with the substrate contacts (24) and spaced apart from one another on the first surface to provide an interconnect area between the first and second microelectronic elements. A plurality of package terminals (74) at the second surface are interconnected with the substrate contacts for connecting the package with an external component. A plurality of stack terminals (28) are exposed at the first surface in the interconnect area for connecting the package with a component overlying the first surface of the substrate. The assembly further includes a second microelectronic package (10B) overlying the first microelectronic package and having terminals (62) joined to the stack terminals of the first microelectronic package.

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STACKABLE MICROELECTRONIC PACKAGE STRUCTURES

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Patent Application No. 13/346,167, filed on January 9, 2012, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to improved microelectronic packages and to methods of making such packages.

[0003] Microelectronic elements generally comprise a thin slab of a semiconductor material, such as silicon or gallium arsenide, commonly called a die or a semiconductor chip. Semiconductor chips typically embody large numbers of active or passive devices which can be electrically connected together internally to perform circuit function, e.g., as an integrated circuit. Semiconductor chips are commonly provided as individual, prepackaged units. In some unit designs, the semiconductor chip is mounted to a substrate or chip carrier.

[0004] Despite the advances that have been made in semiconductor packaging, there is still a need for improvements which may help to reduce the overall size of the package, while enhancing electrical interconnection reliability. These attributes of the present invention are achieved by the construction of the microelectronic packages and methods of making the microelectronic packages as described hereinafter.

BRIEF SUMMARY OF THE INVENTION

[0005] An aspect of the present disclosure relates to a microelectronic assembly including a first microelectronic package having a substrate with first and second opposed

surfaces and substrate contacts thereon. The first package further includes first and second microelectronic elements, each having element contacts electrically connected with the substrate contacts, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements. A plurality of package terminals at the second surface are electrically interconnected with the substrate contacts for connecting the package with a component external to the package. A plurality of stack terminals are exposed at the first surface in the interconnect area for connecting the package with a component overlying the first surface of the substrate. The assembly further includes a second microelectronic package overlying the first microelectronic package and having terminals joined to the stack terminals of the first microelectronic package.

[0006] The package terminals and the stack terminals can overlie each other in respective electrically connected pairs. In an example, the package terminals and the stack terminals can be opposite ends of conductive vias through the substrate.

[0007] Additional ones of the stack terminals can be at the first surface of the substrate in a portion thereof that is outside of the interconnect area. In an embodiment, the first microelectronic package can further include third and fourth microelectronic elements spaced on opposite sides of the interconnect area between the first and second microelectronic elements. In such an embodiment, the additional ones of the stack terminals can be in a corner region of the substrate bounded by adjacent ones of the microelectronic elements. Additionally or alternatively, at least some of the stack terminals can be connected with both of the first and second microelectronic elements. In such an example, at least some of the stack terminals that are connected with both of the

first and second microelectronic elements can be configured to carry at least one of command, address, and timing signals.

[0008] The first microelectronic package can further include a molded encapsulant layer overlying at least a portion of the first surface of the substrate, and at least portions of the first conductive interconnects can comprise first conductive vias extending through the molded encapsulant layer to exposed ends. In an embodiment, contact-bearing faces of the first and second microelectronic elements can face the substrate, the substrate contacts including substrate contacts exposed at the second surface, and the element contacts can be connected with the substrate contacts by wire bonds.

[0009] The microelectronic assembly can include substrate contacts exposed at the first surface. In such an embodiment, the element contacts of the first and second first microelectronic elements can face the substrate contacts exposed at the first surface and can be joined thereto.

[0010] The second microelectronic package can include a third microelectronic element mounted on a second substrate. In such an embodiment, the terminals of the second package can be on the second substrate and electrically connected with the third microelectronic element. In an example, the second microelectronic package can include a substrate having first and second spaced apart surfaces and third and fourth microelectronic elements mounted on the second surface thereof. The third and fourth microelectronic elements can be spaced apart on the substrate of the second package to define an interconnect area therein, and the terminals can be exposed at the second surface of the substrate of the second package within the interconnect area. The substrate of the second package can further include a window extending therethrough between the first and second surfaces thereof, and the terminals of the second package can be joined to the stack

terminals of the first package by wire bonds that extend through the window. In a further embodiment, the substrate of the first package can define a peripheral area surrounding at least one of the first and second microelectronic elements, additional stack terminals being located in the peripheral area. The peripheral area can surround at least one of the third and fourth microelectronic elements and a peripheral edge can bound the peripheral area. Additional terminals can be located in the peripheral area thereof, and at least some of the additional stack terminals of the first package can be joined with at least some of the additional terminals of the second package by wire bonds that extend past the peripheral edge of the substrate of the second package.

[0011] A third microelectronic package can overlie the first microelectronic package and can have terminals joined to the stack terminals of the first microelectronic package. Further, the microelectronic assembly can include a circuit panel with circuit contacts exposed at a surface thereof. The package terminals of the first microelectronic package can be electrically connected with the circuit contacts. The second microelectronic package terminals can be at least one of package terminals or stack terminals. The stack terminals of the first package can be electrically connected with the package terminals of the second package. Further, the stack terminals of the first and second packages can be electrically connected.

[0012] The microelectronic assembly can further include a heat spreader between the first and second microelectronic packages. The heat spreader can have an aperture formed therethrough that overlies at least a portion of the interconnect area. The stack terminals of the second microelectronic package can be connected with the stack terminals of the first microelectronic package through the aperture. The heat spreader can be a first heat spreader, in

an embodiment of an assembly that further includes a second heat spreader, the first heat spreader being disposed on a first side of the interconnect area and the second heat spreader being disposed on a second side of the interconnect area. A gap can be defined between the first and second heat spreaders, and the stack terminals of the second microelectronic package can be connected with the stack terminals of the first microelectronic package through the gap.

[0013] Another aspect of the present disclosure relates to a microelectronic assembly including a first microelectronic package having first and second microelectronic elements. Each microelectronic element has front faces and back faces thereof and element contacts exposed at the respective front faces. The first and second microelectronic elements are laterally spaced apart from one another so as to provide an interconnect area therebetween. The first package further has a dielectric layer having a surface overlying the front faces of the first and second microelectronic elements and facing away from the front faces of the microelectronic elements. The dielectric layer further has a second surface opposite the first surface. A plurality of package terminals are exposed at the first surface of the dielectric layer and are electrically connected with the element contacts through traces extending along the dielectric layer and first metallized vias extending from the traces and contacting the element contacts. A plurality of stack terminals are exposed at the second surface of the dielectric layer and electrically connected with the package terminals for connecting the package with a component overlying the second surface of the dielectric layer. The assembly further includes a second microelectronic package overlying the first microelectronic package and having terminals joined to the stack terminals of the first microelectronic package.

[0014] In an example, the first package can further include a molded encapsulation layer at least partially surrounding the first and second microelectronic elements within the interconnect area and defining a surface thereof overlying the second surface of the dielectric layer. Conductive interconnects can be electrically connected with the stack terminals and having end surfaces exposed at the surface of the molded encapsulation layer.

[0015] Yet another aspect of the present disclosure relates to a microelectronic assembly including a first package, having a substrate with first and second opposed surfaces. The first package further includes first and second microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface. The first and second microelectronic elements are spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements. A plurality of package terminals at the second surface are electrically interconnected with the substrate contacts for connecting the package with a component external to the package. A plurality of stack terminals exposed at the first surface of the substrate in the interconnect area are electrically connected with at least some of the package terminals. The assembly further includes a second microelectronic package overlying the first microelectronic package and having terminals. A plurality of conductive interconnects are joined between the stack terminals of the first microelectronic package and the terminals of the second microelectronic package.

[0016] The second microelectronic package can further have a second dielectric layer having first and second opposed surfaces and at least one microelectronic element mounted on the first surface of the dielectric layer.

[0017] A microelectronic assembly according to another embodiment of the present disclosure includes a first package having a substrate having first and second opposed surfaces and four microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface. The microelectronic elements are arranged on the first surface so as to define an interconnect area of the first surface surrounded by the microelectronic elements. A plurality of package terminals at the second surface are electrically interconnected with the substrate contacts for connecting the package with a component external to the package. A plurality of stack terminals at the first surface in the interconnect area are electrically connected with the package terminals. The assembly further includes second microelectronic package overlying the first microelectronic package and having terminals. Conductive interconnects are joined between the stack terminals of the first microelectronic package and the terminals of the second microelectronic package. Each of the microelectronic elements can include a peripheral edge adjacent to the interconnect area such that the interior interconnect area is defined as a rectangular area. At least some of the first conductive elements can be electrically connected with at least two of the first microelectronic elements.

[0018] Another aspect of the present disclosure relates to a microelectronic assembly including a first package, having a substrate with first and second opposed surfaces. The first package also includes first and second microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements. A plurality of contact

pads have surfaces exposed at the second surface of the substrate, the surfaces of the contact pads defining package terminals electrically interconnected with the substrate contacts for connecting the package with a component external to the package. A molded encapsulant layer overlies at least a portion of the first surface of the substrate and defines an encapsulant surface. The assembly further includes a second microelectronic package bonded to the encapsulant surface and having terminals facing the encapsulant surface. A plurality of conductive vias extend at least through the molded encapsulant layer and connect the contact pads of the first microelectronic package and the terminals of the second microelectronic package.

[0019] The conductive vias can further extend through the contact pads of the first package in electrical contact therewith. The second microelectronic package can further include a substrate having first and second spaced apart surfaces. The second surface can be bonded to the encapsulant surface, and the terminals of the second package can be surfaces of conductive pads exposed at the second surface of the substrate. The conductive vias can further extend through the conductive pads of the second package in electrical contact therewith.

[0020] A system according to another aspect of the present disclosure can include a microelectronic assembly according to any of the embodiments discussed above and one or more other electronic components electrically connected to the microelectronic assembly.

[0021] A further aspect of the present disclosure relates to a method for making a microelectronic assembly. The method includes assembling a first microelectronic package with a second microelectronic package, the second microelectronic package overlying the first microelectronic package and having terminals thereon. The first microelectronic package includes

a substrate having first and second opposed surfaces and substrate contacts thereon. The first package further includes first and second microelectronic elements, each having element contacts electrically connected with the substrate contacts. The first and second microelectronic elements are spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements. A plurality of package terminals at the second surface electrically interconnect with the substrate contacts for connecting the package with a component external to the package. A plurality of stack terminals are exposed at the first surface in the interconnect area for connecting the package with a component overlying the first surface of the substrate. The method further includes connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package to form an electrical connection therebetween.

[0022] In an embodiment, the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package includes joining the package terminals to exposed ends of interconnects on an encapsulant layer of the first microelectronic package overlying the first surface of the substrate at least in the interconnect area thereof. In such an example, the interconnects can be joined to the stack terminals opposite the exposed ends thereof. In another embodiment, the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package can includes depositing conductive bond material masses into holes within an encapsulant layer of the first microelectronic package overlying the first surface of the substrate at least in the interconnect area. In such an embodiment, the stack terminals can be exposed at a surface of the encapsulant layer

within the holes, and the conductive bond material masses can be joined to the terminals of the second package and the stack terminals of the first package.

[0023] In a further embodiment, the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package can includes forming a plurality of holes through at least an encapsulant of the first microelectronic package overlying the first surface of the substrate in at least the interconnect area thereof. The plurality of holes can be aligned with respective ones of the stack terminals at first ends thereof and with corresponding ones of the terminals of the second package at second ends thereof. Such a method can further include filling the holes with a conductive material in contact with the stack terminals of the first microelectronic package and the package terminals of the second package. The holes can be further formed through the substrate of the first package and through the respective stack terminals thereof. Alternatively, the holes can be further formed through a substrate of the second package and through the corresponding terminals thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Various embodiments of the present invention will be now described with reference to the appended drawings. It is appreciated that these drawings depict only some embodiments of the invention and are therefore not to be considered limiting of its scope.

[0025] Fig. 1 is a sectional view of an assembly including microelectronic packages according to an embodiment of the present disclosure;

[0026] Fig. 1A is a detail view of a portion of an alternative assembly ;

[0027] Fig. 2 is a sectional view of a further assembly including additional microelectronic packages as shown in Fig. 1;

[0028] Figs 3A-3C are sectional views of alternative assemblies incorporating alternative microelectronic packages;

[0029] Fig. 4 is a sectional view of an alternative assembly of alternative microelectronic packages;

[0030] Figs. 5A and 5B are sectional views of further alternative assemblies of alternative microelectronic packages;

[0031] Fig. 6 is an alternative assembly including microelectronic packages of the type shown in Fig. 1;

[0032] Fig. 7 is a further alternative assembly including microelectronic packages of the type shown in Fig. 1;

[0033] Figs. 8-10 are sectional views of various assemblies of further alternative microelectronic packages according to further embodiments of the present disclosure;

[0034] Fig. 11 is an assembly of the type shown in Fig. 6 incorporating microelectronic packages as shown in Fig. 8;

[0035] Fig. 12 is an assembly of the type shown in Fig. 7 incorporating microelectronic packages as shown in Fig. 8;

[0036] Fig. 13 is a section view of an assembly including additional microelectronic elements of the type shown in Fig. 8;

[0037] Fig. 14 is a sectional view of an assembly of further alternative microelectronic packages;

[0038] Fig. 15 is a top plan view of a microelectronic package as used in the assembly shown in Fig. 14;

[0039] Figs. 16 and 17 are top plan views of alternative microelectronic packages that can be used in the assembly shown in Fig. 14; and

[0040] Fig. 18 shows a system including a microelectronic assembly according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0041] Turning now to the figures, where like reference numbers are used to indicate similar features, Fig. 1 shows a microelectronic assembly 8 of microelectronic packages 10A and 10B on a circuit panel 70. In the embodiment shown, packages 10A and 10B are substantially identical and each includes a plurality of microelectronic elements 40 mounted on the front face 14 of a substrate 12. In one example, each microelectronic element may be or include a semiconductor chip embodying a plurality of active circuit elements, e.g. semiconductor devices, which can be electrically configured as an integrated circuit, for example. In another example, each microelectronic element can include a plurality of passive circuit elements such as capacitors, inductors or resistors, which in some cases may be embodied in a semiconductor chip, either as only passibe devices, or together with active circuit elements, i.e. active devices. In the embodiment shown, each package 10A and 10B includes two microelectronic elements 40, but in other embodiments a package (such as those discussed below) can include more than two microelectronic elements such as three, four, or more.

[0042] In the exemplary embodiment of Fig. 1, the microelectronic elements 40 are mounted on respective substrates in a face-down wire bond configuration. In this configuration, the microelectronic elements 40 are mounted with their front faces 42 facing the front face 14 of substrate 12. Element contacts 46 are exposed at front face 42 of the microelectronic element 40 and are electrically connected with substrate wiring 22 that can include traces or contact pads either formed on or at least partially embedded in substrate 12. In the embodiment shown, the element contacts 46 are connected with the substrate wiring 22 by wire bonds 48 that pass through a window 32 in substrate 12. Although only a pair of wire bonds 48 is shown in Fig. 1, a

plurality of wire bond pairs can extend along a row (See Fig. 15) and can pass through a window that is elongated to accept the multiple wire bond pairs. An encapsulant 50 can surround and protect wire bonds 48 in the area of window 32 and along portions thereof that extend outside of substrate 12 beyond the back surface 16 thereof. A molded dielectric layer 52 can at least partially surround microelectronic elements 40 including the edges 45 thereof and, in the face-down arrangement of Fig. 1, front face 42. Molded dielectric layer 52 can further bond microelectronic elements 40 to front face 14 of substrate 12. Molded dielectric layer 52 can define a surface 54 that can be substantially flush with back faces 44 of microelectronic elements 40 or can overlie back faces 44 to fully encapsulate microelectronic elements 40. Alternatively, as seen in Fig. 1A, some or all of the leads may be beam leads 137 which extend in a direction parallel to a surface 123 or 124 of the second substrate 120 and have portions aligned with aperture 126 and are joined to the contacts 112 of the first microelectronic element 102.

[0043] Substrate wiring 22 can include a plurality of package terminals 26 exposed at the back surface 16 of substrate 12. Package terminals 26 can be electrically connected with either or both microelectronic elements 40 of the package 10A or 10B and can further be interconnected with each other. Package terminals 26 can be available for use in connecting package 10A or 10B with a component external to that package 10A,10B. For example, package terminals 26 in package 10A can be used to connect package 10A with circuit contacts 72 exposed at a surface of a circuit panel 70 that can be a printed circuit board ("PCB") or the like. The package terminals 26 of package 10B illustrate another example, in which package terminals 26 can be used to electrically connect with another package such as package 10A

through structures of the package 10A, 10B that are discussed in greater detail below.

[0044] Microelectronic elements 40 are arranged along their respective substrates 12 in package 10A,10B such that they are spaced apart on the first surface 14 to define an interconnect area 18 therebetween. In the embodiment shown in Fig. 1, the microelectronic elements 40 are arranged such that respective edge surfaces 45 thereof face and are substantially parallel to each other in a spaced-apart manner to define interconnect area 18 therebetwen. It is not necessary, however for edge surfaces 45 to be parallel. In the embodiment shown interconnect area 18 can be bounded on two sides by the edges 45 of the microelectronic elements 40 and on the remaining two sides by edges of substrate 12. In other embodiments, interconnect area 18 can be considered bounded by an imaginary boundary extending between the outsides of the microelectronic elements 40. In embodiments with, for example, four microelectronic elements 40, the interconnect area 18 can be bounded on four sides by edges 45 of the individual microelectronic elements 40. In embodiments with more than four microelectronic elements, the interconnect area can be fully enclosed by the microelectronic elements, for example, on as many sides as there are microelectronic elements.

[0045] A plurality of stack terminals 28 are arranged within interconnect area 18 exposed as front surface 14 of substrate 12. The term "exposed at", as used herein does not refer to any specific means of attachment for stack terminals 28 onto substrate 12 or any relative position therebetween. Rather, it indicates that the electrically conductive structure is available for contact with a theoretical point moving in a direction perpendicular to the surface of the dielectric structure toward the surface of the dielectric structure from outside the dielectric structure. Thus, a terminal or other conductive structure which is exposed at a

surface of a dielectric structure may project from such surface; may be flush with such surface; or may be recessed relative to such surface and exposed through a hole or depression in the dielectric. Stack terminals 28 can be an array of individual terminals 28 that can include various rows or columns thereof. Other alternative arrangements of terminals 28 are also possible, including those with only two stack terminals 28 or with more than two terminals in various locations selected based on connection with other elements of package 10A or 10B. Stack terminals 28 can be a part of or can otherwise be connected with substrate wiring 22 such that stack terminals 28 can be interconnected with the microelectronic elements 40 of the same package 10A or 10B, with other stack terminals 28 or with package terminals 26.

[0046] Stack terminals 28 can be used to connect the associated package 10A or 10B with an external component that overlies front surface 14 of substrate 12. In one example, a plurality of interconnect elements 56 can be connected with stack terminals 28 and extend upwardly therefrom to end surfaces 58 thereof that can be exposed at surface 54 of molded dielectric layer 52. Interconnects 56 can be pins, posts, masses of bond metal or other conductive material, such as may include solder or a metal such as copper, gold, silver, tin, bismuth, indium, aluminum, nickel, etc. In the embodiment shown interconnects 56 are in the form of pins that extend away from front surface 14 of substrate 12 and extend through the molded dielectric layer 52. In such an embodiment, end surfaces 58 can form terminals exposed at surface 54 for interconnection with another component. In other embodiments, end surfaces 58 can be covered by contacts that are connected therewith to provide a terminal with a larger surface area than that of end surfaces 58 themselves.

[0047] As shown in Fig. 1, package 10B is mounted over package 10A, which can be done for example, using adhesive

layer 60 that can be formed from a dielectric material such as epoxy or another curable material that can be positioned between surface 54 of package 10A and second surface 16 of the substrate 12 of package 10B. Masses of conductive material or a bond metal such as solder or the like, as described above, can connect the end surfaces 58 of the interconnects 56 of package 10A with the package terminals 26 of package 10B. This arrangement, thusly, provides a connection between stack terminals 28 of package 10A with package terminals 26 of package 10B, which can facilitate a number of further connections throughout the assembly 8. For example, this arrangement can provide a connection between either or both of the microelectronic elements 40 of package 10B with circuit panel 70 and, accordingly, any other components connected therewith. In another example, either or both of the microelectronic components 40 of package 10B with either or both of the microelectronic components of package 10A. The particular connections facilitated by such a connection can be made by adapting the substrate wiring 22 within each package 10A and 10B, including the particular connection made to the individual stack terminals 28.

[0048] A method for making a microelectronic assembly 8 such as that shown in Fig. 1 can include making or forming microelectronic packages 10A and 10B in the configurations described above separately. Packages 10A and 10B can then be aligned with each other, such that the corresponding package terminals 26 of package 10B align with the corresponding interconnects 56 of package 10A. The corresponding package terminals 26 of package 10B can then be electrically connected with the ends 58 of their respective interconnects 56 by joining together using, for example a conductive bonding material such as solder or the like in the form of masses 62. Adhesive layer 60 can then be injected or otherwise deposited

between facing surfaces 16 and 54 and around the bonding metal masses 62 to secure packages 10A and 10B together.

[0049] In package 10A, some package terminals 26 and stack terminals 28 may directly overlie one another and can be electrically connected by a via 30 that extends through substrate 12. In the specific embodiment shown, a via 30 can be exposed at ends thereof on front surface 14 and back surface 16 such that the respective ends thereof are, respectively, the stack terminals 28 and the package terminals 26. Other embodiments are possible, including those in which contact pads overlie via 30 to form stack terminals 28 and package terminals 26. As illustrated by package 10A, vias 30 can be connected with substrate wiring 22 that extends along back surface 16 and includes package terminals that are displaced in one or more lateral directions from vias 30. A similar arrangement is possible wherein the substrate wiring 22 extends along front surface 14 and includes stack terminals 28 that are displaced from vias 30. Embodiments of a package such as package 10A that includes displaced package terminals 26 can also overlie another package (such as in the place of package 10B) and such displacement can compensate for different spatial placement of interconnects 56 in different packages or can redistribute the particular connections.

[0050] As shown in Fig. 2, additional microelectronic packages, such as packages 10C and 10D can be included in an assembly 8. In the embodiment shown, packages 10C and 10D are similar in structure to package 10B such that the package terminals 26 of package 10C can be connected with the interconnect 56 end surfaces 58 of package 10B. Similarly, the package terminals 26 of package 10D can be connected with the interconnect 56 end surfaces 58 of package 10C. In both instances the packages are bonded together using adhesive layers 62 and the package terminals 26 can be connected with the end surfaces 58 of interconnects 56 using bonding metal

masses 62. As in the embodiment of Fig. 1, the interconnection between packages 10A,10B,10C,10D can achieve a number of different interconnections between assembly elements. For example, the microelectronic elements 40 of packages 10C and 10D can connect through packages 10A and 10B to circuit panel 70. Further, any of the microelectronic elements 40 within assembly 8 can connect with any of the remaining microelectronic elements 40 through the interconnects 56 of any intervening packages.

[0051] A method for making a package 8 as shown in Fig. 2 can be similar to the method described above for making the package 8 of Fig. 1 with additional, similar steps included to attach additional packages 10C and 10D therewith.

[0052] A number of other types of packages can be connected in such a manner using stack terminals in an interconnect area between microelectronic elements. Further a number of different connections to such stack terminals to external package terminals are also possible. In the examples shown in Figs. 3A-3C, packages 110A and 110B are similar in structure to packages 10A and 10B, respectively, as shown in Fig. 1. In the embodiments of Figs. 3A-3C, however, interconnects 156 are in the form of conductive masses, e.g. of a bonding metal, e.g. solder, tin, indium, gold, or combinations thereof, or other conductive bond material such as conductive paste, a conductive matrix material, amont others. In the example shown in Fig. 3C, the bond metal interconnects 156 extend all the way from stack terminals 128 of package 110A to package terminals 126 of package 110B. In such an embodiment, holes can be made in the molded dielectric layer 152 of package 110A to expose stack terminals 128 on surface 154. These holes can also extend through adhesive layer 160 in cases where adhesive layer 160 is formed before assembly with package 110B. Otherwise bonding metal, such as solder, can be deposited in such holes in contact with stack terminals 128 and package

110B can be assembled with package 110A and can interconnects 156 can be connected with package terminals 126 by reflowing the bonding metal. in one example, the adhesive layer 160 can then be injected between packages 110A and 110B and around exposed portions of the interconnects 156.

[0053] In the example of Fig. 3B, which is a variation of Fig. 3A, the stack terminals 128 and package terminals 126 are opposing surfaces of a contact pad 134 that is positioned adjacent the second surface 116 of substrate 112 in package 110A. As shown, the stack terminals 128 are exposed at first surface 114 of substrate 112 by openings 136 in substrate 112. In such an embodiment the bond metal interconnects 156 can further extend into the openings 136 in substrate 112 to join with stack terminals 128. Fig. 3C shows a further variation of the example of fig 3B in which the contact pads 134 are adjacent to first surface 114 of substrate 112 of package 110A. Package terminals 126 are exposed at second surface 116 by openings 136 in substrate 112. Solder balls 174 extend into openings 136 to connect with package terminals 126 for connection with an external component, as discussed above. Package 110B in Fig. 3C includes similar terminal structures as in package 110A. Bond metal interconnects 156 extend through openings 136 in substrate 112 of package 110B to connect with package terminals 126 thereof. In a method for making microelectronic packages 108, as shown in Figs. 3A-3C, openings 136 can be included in package 110A prior to assembly with package 110B. Interconnect masses 156 can be included in openings 136 when package 110A is provided for assembly with package 110B. Masses 156 can then be heated to re-flow the bonding material for joining with package terminals 126 of package 110B. Alternatively, openings 136 can be left unfilled prior to assembly, at which point bonding metal can be deposited therein in a flowable state and can be further joined with package terminals 126 of package 10B. In a

further alternative, openings 136 can be filled with bond metal interconnects 136 that are substantially even with surface 154 of molded dielectric 152. At assembly additional bonding metal can be added thereto and joined with package terminals 126 of package 110B.

[0054] Fig. 4 shows a further alternative arrangement wherein a window 219 is formed through substrate 212 of package 210B such that the interconnects 256 can be in the form of wire bonds that connect stack terminals 228 of package 210A directly to stack terminals 228 of package 210B. In such an embodiment, the substrate wiring 222 of package 210B can connect between stack terminals 228 and the wire bonds 248 that are on the opposite face 216 from stack terminals 228. In some cases a single molded dielectric 250 can be formed at once which encapsulates the microelectronic elements 240 and the wire bonds 248 that connect microelectronic elements 240 to substrate wiring 222 and the interconnect wire bonds 256. As further shown in Fig. 4 additional stack terminals 226 can be exposed at first surface 214 of substrate 212 of package 210A in a peripheral area outside of the microelectronic elements 240. Similarly, additional stack terminals 228 can be exposed at the first surface 214 of substrate 212 of package 210B such that additional wire bond interconnects 256 can connect between the stack terminals 228 of packages 210A and 210B in the peripheral areas thereof. Additional examples of assemblies incorporating wire bonds through substrate windows to interconnect packages are described in co-pending, commonly-owned U.S. Patent Application Nos. 11/666,975 and 13/216/415, the disclosures of which are incorporated by reference herein in their entireties.

[0055] In further variations shown in Figs. 5A and 5B, packages 310A and 310B can include microelectronic elements 340 that include element contacts 346 on the front face 342 thereof. Such microelectronic elements 340 are flip-chip

bonded on substrates 312 such that element contacts 346 are connected to substrate wiring 322, including substrate contacts on the first surface 314 of substrate 312 by solder balls 348. The example of Fig. 5B further shows interconnects 356 in the form of metalized vias that extend through the vias 330 (or other similar structures) that define package terminals 326 and stack terminals 328 of package 310B to electrically connect therewith. The vias 356 further extend through molded dielectric 352 of package 310A and adhesive layer 360 to connect with stack terminals 328 of package 310A. In the example shown in Fig. 5B, vias further extend through molded dielectric 352 of package 310B such that vias 356 can be made by first forming corresponding openings through package 310B, including molded dielectric 352, stack terminals 328, package terminals 326 and any structure (such as the remainder of vias 330 or any portion of substrate 312) therebetween. Such openings are further formed through adhesive layer 360 and through molded dielectric 352 of package 310A. In some embodiments, the openings can also extend through stack terminals 328 and any associated structure such as vias 330. The openings are then filled with a conductive material such as copper or another wiring metal discussed herein. Such conductive metals can be deposited in openings by plating or the like. Alternatively, depending on the size of the openings and other factors including the thicknesses of the respective packages 310A and 310B, a conductive paste or bonding metal can be deposited in the openings to achieve the desired electrical connection. The vias 356 discussed with respect to Fig. 5B for connection between packages 310A and 310B can be used to form similar connections in the other examples of packages and assemblies thereof discussed herein.

[0056] Packages of the types described herein can be assembled with additional packages of similar types by

connecting with either the package terminals or the stack terminals of such additional packages. In an example, packages of any of the types described herein can be mounted to each other in a face-to-face arrangement such as those shown in Figs. 6 and 7. For example, in Fig. 6, packages 410A and 410B are positioned such that their respective dielectric surfaces 454 face each other and such that interconnect 456 end surfaces 458 are mutually aligned. Solder balls 462 can electronically connect the aligning interconnect 456 end surfaces 458 and an adhesive layer 460 can affix the two packages 410A and 410B. In a similar example, two packages can be attached back-to-back with solder balls connecting facing and aligning package terminals with an adhesive layer between facing back surfaces of respective package substrates. These examples can further be combined to assemble two sets of face-to-face bonded packages, such as packages 410A and 410B in Fig. 6 together. Fig. 7 shows a variation of the embodiment of Fig. 6 wherein a heat spreader 464 is disposed between packages 410A and 410B. Heat spreader 464 includes a window 466 therein through which interconnects 456 can pass. In anther example, heat spreader 464 can be two discrete heat spreaders 464, with one being disposed on each side of interconnect area 418. In such an embodiment, window 466 can be in the form of a gap defined between the two separate heat spreaders 464.

[0057] Similar stack terminal arrangements can also be incorporated into multiple die arrangements in wafer-level packages. As shown in Fig. 8, packages 510A and 510B are both wafer level packages including two microelectronic elements 540. In this case, the substrate can be omitted such that the microelectronic packages 510A and 510B can be in form of a microelectronic elements 540 having packaging structure which includes an electrically conductive redistribution layer overlying the front faces 542 of the microelectronic elements

540. The redistribution layer has electrically conductive metallized vias 530 extending through a dielectric layer 538 of the package to contacts 546 of the microelectronic elements The redistribution layer includes package terminals 526 and traces electrically connected with the terminals 526, such that the terminals are electrically connected with the contacts 546, such as through the metallized vias 536 or through metallized vias 536 and electrically conductive traces. In the particular embodiment of Fig. 8, where package terminals 526 and stack terminals 528 are disposed on areas of the dielectric layer 538 which extend beyond one or more edges of the microelectronic elements 540, such as in interconnect area 518, the packages 510A and 510B can further be referred to as "fan-out wafer-level packages". Stack terminals 528 and package terminals 526 can be opposing surfaces of contact pads 534 that are incorporated in the redistribution circuitry 522 of each wafer level package 510A,510B within dielectric layer 538.

[0058] As in the embodiment of Fig. 1, interconnects 556 such as pins or the like can extend through molded dielectric 552 and, if necessary through dielectric layer 538, to end surfaces 558 thereof that are exposed on surface 554. This structure allows package 510B to be assembled over package 510A with the package terminals of package 510B connected with interconnect end surfaces 558. As described above, this connection configuration facilitates a number of different particular connections between the components of the packages 510A and 510B and connection therewith to external components, such as by connection of package terminals 526 of package 510A to circuit contacts of a PCB or the like. Such a connection can be achieved, as shown in Fig. 8 by bonding package terminals 526 of package 510A, for example, directly to circuit contacts 572. Alternatively, as shown in Fig. 9, a package substrate 576 can be included in assembly 508 that

connects to package terminals 526 of package 510A via solder balls 562. Package substrate 576 can then connect to circuit contacts 572 by solder balls 574 connected to package contacts 576. In an alternative example, shown in Fig. 10, package terminals 526 of package 510A can be wire bonded to wiring within package substrate 576 that connects to package contacts 578.

[0059] Figs. 11 and 12 show examples of assemblies 508 that include wafer level packages 510A and 510B in arrangements that are similar to those shown in Figs. 6 and 7. In particular packages 510A and 510B are assembled face-to-face with solder balls 562 connecting facing and mutually aligned interconnect 556 end surfaces 558. A adhesive layer 560 can attach between facing surfaces 554 of the respective packages 510A and 510B. The embodiment of Fig. 500 incorporates a heat spreader 564 in a similar manner to that of Fig. 7. Multiple sub-assemblies of face-to-face bonded packages can be assembled together, as discussed above.

[0060] As shown in Fig. 13, assemblies with additional packages 510C and 510D by continuing to assemble packages on top of each other and connecting adjacent pairs of package terminals 526 and interconnect 556 end surfaces 558 in a similar manner to that discussed with respect to Fig. 2. Even more than the four packages shown in Fig. 13 can be included in such an assembly.

[0061] As previously discussed, any of the assemblies discussed above in Figs. 1-13 can be adapted to include more than two microelectronic elements in each package. Figs. 14-17 show further examples of an assembly of the type shown in Fig. 8 having four microelectronic elements 640 in each package 610. In particular, Fig. 15 shows a top schematic view of a package 610 that can be used in the assembly of Fig. 14. In this embodiment, microelectronic elements 640 are arranged such that edges 645 are arranged in

a square along surface 614 of substrate 612. This arrangement defines interconnect area 618 in the square area defined by edges 645. As in previously-discussed embodiments, stack terminals 628 are arranged in an array on front surface 614 of substrate 612 within interconnect area 618. As discussed previously, package terminals 626 are exposed on back surface 616 of substrate 612 and can directly align with stack terminals 628 or be offset therefrom.

[0062] In addition to the interconnect area 618 defined within the four microelectronic elements 640, as shown in Fig. 15, adjacent pairs of microelectronic elements 640 define outer interconnect areas 620 between edges 645 thereof and the boundary of substrate 612. Additional stack terminals 628 can be exposed on front surface 614 of substrate 612 in these outer interconnect areas 620 as well. In the example shown in Fig. 15, four such outer interconnect areas 620 are defined on substrate 612; however, more of fewer outer interconnect areas can be present, depending on the number of microelectronic elements included in a given package.

[0063] In an assembly 608 of packages 610 of the type shown in Figs. 14 and 15, the stack terminals 628 within different interconnect areas 618 and 620 can be used to carry different signals, depending on their location or can be interconnected with different combinations of microelectronic elements 640. For example, the stack terminals 628 within interconnect area 618 can be interconnected with more than one of the microelectronic elements 640 to carry common signals to two, three or all of the microelectronic elements 640. As shown in Fig. 15, one such stack terminal 628A can connect with all microelectronic elements 640. In a further example, the stack terminals within outer interconnect area 620 can connect with only one of the microelectronic elements 640 that bound it or with both of the microelectronic elements that bound that particular outer interconnect area 640. In an embodiment, the

stack terminals 628C within an outer interconnect area 640 can connect with only the closest one of the microelectronic elements 640C to carry a signal that is specific to that microelectronic element. The remaining stack terminals can be connected with the various microelectronic elements 640 according to this scheme. To do so may be advantageous due to the relative distances between the stack terminals 628 and the microelectronic elements 640 because the stack terminals 628 in the outer interconnect areas 620 can be at too disparate a distance between opposite microelectronic elements (such as microelectronic elements 640A and 640B) to carry common signals. This can be due to the additional time required for such signals to reach the farther of the microelectronic elements 640. Conversely, the stack terminals 628 within interconnect area 618 can be close enough in distance to all microelectronic elements 640 to reliably carry common signals.

[0064] In certain embodiments of the invention, the microelectronic elements in the package include microelectronic elements configured to provide memory storage array function. For example, the microelectronic elements can provide dynamic random access memory ("DRAM") function, and may in some cases include or be dedicated DRAM chips. In such case, the stack terminals 628 in the interconnect area may be configured to carry all of a group of command-address bus signals to the second microelectronic package 601B. Packages that have centrally located terminals configured to carry command, address, and timing signals can be as further described in commonly owned U.S. Provisional Patent Application No. 61/506,889 filed July 12, 2011 (the "'889 Application"), U.S. Provisional Patent Application No. 61/542,488 filed October 3, 2011 (the "'488 Application"), and U.S. Provisional Patent Application No. 61/542,553 filed October 3, 2011 (the "'553 Application"), the disclosures of said '889, '488, and '553 Applications being incorporated by

reference herein. Typically, the command-address bus signals can be bussed on a circuit panel such as a printed circuit board or module card to multiple microelectronic packages in parallel, particularly to microelectronic packages mounted to the same or to opposite surfaces of the circuit panel. In one example, such a circuit panel can be a motherboard or single-inline memory module or "SIMM" or dual-inline memory module or "DIMM" module board. In a particular example, the command-address bus signal terminals of the interconnect area can be configured to carry all of a group of command signals, address signals, bank address signals and clock signals, wherein the command signals are write enable, row address strobe, and column address strobe, and the clock signals are sampling clocks used for sampling the address signals. While the clock signals can be of various types, in one embodiment, the clock signals carried by these terminals can be one or more pairs of differential clock signals which are received as differential or true and complement clock signals. In yet another example, package terminals aligned with the stack terminals or disposed on the outwardly-facing surface of the substrate will also include command-address bus signal terminals for mating with a circuit panel, or for mating with the stack terminals of a like package.

[0065] In one embodiment, the microelectronic package can be functionally equivalent to a SIMM or a DIMM, and the stack terminals in the interconnect area of the package, and the package terminals connected thereto, may be configured to carry all of a group of command-address bus terminals; i.e., all of the command signals, address signals, bank address signals, and clock signals transferred to the package, the command signals being write enable, row address strobe, and column address strobe signals, and the clock signals being sampling clocks used for sampling the address signals. In a particular embodiment, the package may incorporate a buffer

element, e.g., an integrated circuit therefor, which is configured to regenerate the command-address bus signals received at the package terminals and transmit the regenerated signals on the stack terminals to additional packages which may be assembled therewith, as also described in the '488 Application. In such case, the microelectronic package may be functionally equivalent to a registered DIMM or "RDIMM". In another example, the microelectronic package may be functionally equivalent to a load-reduced DIMM ("LRDIMM") in which case, the buffer element can be configured to regenerate all of the data signals received by the microelectronic package and transmit the same to one or more additional microelectronic packages assembled therewith.

[0066] In a particular example, the microelectronic package can be configured to transfer, i.e., receive by the package, or transmit from the package thirty-two data bits in parallel in a clock cycle. In another example, the microelectronic package can be configured to transfer sixty-four data bits in parallel in a clock cycle. A number of other data transfer quantities are possible, among which only a few such transfer quantities will be mentioned without limitation. For example, the package can be configured to transfer 72 data bits per clock cycle which may include a set of 64 underlying bits which represent data and 8 bits which are error-correction code ("ECC") bits for the 64 underlying bits. Ninety-six data bits, 108 bits (data and ECC bits), 128 data bits and 144 bits (data and ECC bits) are other examples of data transfer widths per cycle that the microelectronic package may be configured to support.

[0067] Figs. 16 and 17 show additional examples of how microelectronic elements 640 can be arranged in a four microelectronic element package 610. In Fig. 16, the microelectronic elements 640 are staggered and do not overlap (as they do in Fig. 15), which eliminates the outer

interconnect areas 620. In particular, the microelectronic elements 640 in the arrangement of Fig. 16 can be described as having inside edge surfaces 645A extending along a plane that intersects an adjacent inside edge surface 645A of another microelectronic element 640. In this an embodiment, stack terminals 628 within interconnect area 618 can carry both common and specific signals. As shown in Fig. 16, substrate 612 can extend outside of the areas that microelectronic elements 640 overlie to define a continuous outer interconnect area 620 surrounding the microelectronic elements 640 and including stack terminals 628 therein. These stack terminals 628 can connect with adjacent microelectronic elements to carry signals specific to that element with common signals carried by stack terminals 628 within the interconnect area 618 surrounded by the microelectronic elements 640.

[0068] In Fig. 17 a non-overlapping arrangement of microelectronic elements 640 is shown that, as in the embodiment of Fig. 15, defines outer interconnect areas 620 having stack terminals 628 therein. In such an arrangement, inside edge surfaces 645A extend along planes such that each microelectronic element 640 is positioned between two such planes defined by inside edge surfaces 645A of adjacent microelectronic elements 640. As used herein, "between" can include an arrangement where a microelectronic element is tangent to such a plane.

[0069] Various embodiments of the connection components described herein can be used in connection with various diverse electronic systems. The interconnection components described above can be utilized in construction of diverse electronic systems, as shown in Fig. 18. For example, a system 1 in accordance with a further embodiment of the invention can include a microelectronic assembly 8, being a unit formed by assembly of microelectronic packages 10A and 10B, similar to the microelectronic assembly 8 shown in Fig.

1. The embodiment shown, as well as other variations of microelectronic assemblies, as described above can be used in conjunction with other electronic components 6 and 3. In the example depicted, component 6 can be a semiconductor chip or package or other assembly including a semiconductor chip, whereas component 3 is a display screen, but any other components can be used. Of course, although only two additional components are depicted in Fig. 18 for clarity of illustration, the system may include any number of such components. In a further variant, any number of microelectronic assemblies including a microelectronic element and an interconnection component can be used. The microelectronic assembly and components 6 and 3 are mounted in a common housing 4, schematically depicted in broken lines, and are electrically interconnected with one another as necessary to form the desired circuit. In the exemplary system shown, the system includes a circuit panel 70 such as a flexible printed circuit board, and the circuit panel includes numerous conductors 72 interconnecting the components with one another. However, this is merely exemplary; any suitable structure for making electrical connections can be used, including a number of traces that can be connected to or integral with contact pads or the like. Further, circuit panel 70 can connect to assembly 8 using solder balls 74 or the like. The housing 4 is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen 3 is exposed at the surface of the housing. Where system 1 includes a light-sensitive element such as an imaging chip, a lens 5 or other optical device also may be provided for routing light to the structure. Again, the simplified system 1 shown in Fig. 18 is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop

computers, routers and the like can be made using the structures discussed above.

[0070] Although the description herein has been made with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present disclosure. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present disclosure as defined by the appended claims.

CLAIMS

1. A microelectronic assembly, comprising:

a first microelectronic package, including:

a substrate having first and second opposed surfaces and substrate contacts thereon;

first and second microelectronic elements each having element contacts electrically connected with the substrate contacts, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements;

a plurality of package terminals at the second surface electrically interconnected with the substrate contacts for connecting the package with a component external to the package; and

a plurality of stack terminals exposed at the first surface in the interconnect area for connecting the package with a component overlying the first surface of the substrate; and

a second microelectronic package overlying the first microelectronic package and having terminals joined to the stack terminals of the first microelectronic package.

2. The microelectronic assembly of claim 1, wherein the package terminals and the stack terminals overlie each other in respective electrically connected pairs.

3. The microelectronic assembly of claim 2, wherein the package terminals and the stack terminals are opposite ends of conductive vias through the substrate.

4. The microelectronic assembly of claim 1, wherein additional ones of the stack terminals are at the first

surface of the substrate in a portion thereof that is outside of the interconnect area.

5. The microelectronic assembly of claim 4, wherein at least some of the stack terminals are connected with both of the first and second microelectronic elements.

6. The microelectronic assembly of claim 5, wherein at least some of the stack terminals that are connected with both of the first and second microelectronic elements are configured to carry at least one of command, address, and timing signals.

7. The microelectronic assembly of claim 1, wherein the first microelectronic package further includes third and fourth microelectronic elements spaced on opposite sides of the interconnect area between the first and second microelectronic elements.

8. The microelectronic assembly of claim 7, wherein additional ones of the stack terminals are positioned in a corner region of the substrate bounded by adjacent ones of the microelectronic elements.

9. The microelectronic assembly of claim 7, wherein the third and fourth microelectronic elements respectively overlap with the first and second microelectronic elements in corner regions thereof adjacent to corners of the interconnect area defined thereby.

10. The microelectronic assembly of claim 7, wherein each of the first, second, third, and fourth microelectronic elements has an edge that defines a side of the interconnect area, and wherein each of the edge surfaces extends along a

plane that interests the edge surface of an adjacent microelectronic element.

11. The microelectronic assembly of claim 7, wherein each of the first, second, third, and fourth microelectronic elements has an edge surface that defines at least a portion of a side of the interconnect area, and wherein each of the edge surfaces extends along a plane with each of the microelectronic elements positioned between two adjacent planes.

12. The microelectronic assembly of claim 1, wherein the first microelectronic package further includes a molded encapsulant layer overlying at least a portion of the first surface of the substrate, and wherein at least portions of the first conductive interconnects comprise first conductive vias extending through the molded encapsulant layer to exposed ends.

13. The microelectronic assembly of claim 1, wherein contact-bearing faces of the first and second microelectronic elements face the substrate, the substrate contacts including substrate contacts exposed at the second surface, and wherein the element contacts are connected with the substrate contacts by wire bonds.

14. The microelectronic assembly of claim 1, including substrate contacts exposed at the first surface and wherein the element contacts of the first and second first microelectronic elements face the substrate contacts exposed at the first surface and are joined thereto.

15. The microelectronic assembly of claim 1, wherein the second microelectronic package includes a third

microelectronic element mounted on a second substrate, the terminals being on the second substrate and electrically connected with the third microelectronic element.

16. The microelectronic assembly of claim 1, wherein the second microelectronic package includes a substrate having first and second spaced apart surfaces and third and fourth microelectronic elements mounted on the second surface thereof, the third and fourth microelectronic elements being spaced apart on the substrate of the second package to define an interconnect area therein, and the terminals being exposed at the second surface of the substrate of the second package within the interconnect area, the substrate of the second package further including a window extending therethrough between the first and second surfaces thereof, and wherein the terminals of the second package are joined to the stack terminals of the first package by wire bonds that extend through the window.

17. The microelectronic assembly of claim 16, wherein the substrate of the first package defines a peripheral area surrounding at least one of the first and second microelectronic elements, additional stack terminals being located in the peripheral area, wherein the substrate of the second package defines a peripheral area surrounding at least one of the third and fourth microelectronic elements and a peripheral edge bounding the peripheral area, additional terminals being located in the peripheral area thereof, and wherein at least some of the additional stack terminals of the first package are joined with at least some of the additional terminals of the second package by wire bonds that extend past the peripheral edge of the substrate of the second package.

18. The microelectronic assembly of claim 1, further including a third microelectronic package underlying the first microelectronic package and having terminals joined to the package terminals of the first microelectronic package.

19. The microelectronic assembly of claim 1, further including a circuit panel with circuit contacts exposed at a surface thereof, wherein the package terminals of the first microelectronic package are electrically connected with the circuit contacts.

20. The microelectronic assembly of claim 1, wherein the second microelectronic package terminals are at least one of package terminals or stack terminals.

21. The microelectronic assembly of claim 20, wherein the stack terminals of the first package are electrically connected with the package terminals of the second package.

22. The microelectronic assembly of claim 20, wherein stack terminals of the first and second packages are electrically connected.

23. The microelectronic assembly of claim 22, further including a heat spreader between the first and second microelectronic packages.

24. The microelectronic assembly of claim 23, wherein the heat spreader includes an aperture formed therethrough that overlies at least a portion of the interconnect area, the stack terminals of the second microelectronic package being connected with the stack terminals of the first microelectronic package through the aperture.

25. The microelectronic assembly of claim 23, wherein the heat spreader is a first heat spreader, the assembly further including a second heat spreader, the first heat spreader being disposed on a first side of the interconnect area and the second heat spreader being disposed on a second side of the interconnect area with a gap being defined between the first and second heat spreaders, the stack terminals of the second microelectronic package being connected with the stack terminals of the first microelectronic package through the gap.

26. A microelectronic assembly, comprising:

a first microelectronic package, including:

first and second microelectronic elements each having front faces and back faces thereof and element contacts exposed at the respective front faces, the first and second microelectronic elements being laterally spaced apart from one another so as to provide an interconnect area therebetween;

a dielectric layer having a surface overlying the front faces of the first and second microelectronic elements and facing away from the front faces of the microelectronic elements, the dielectric layer further having a second surface opposite the first surface;

a plurality of package terminals exposed at the first surface of the dielectric layer and electrically connected with the element contacts through traces extending along the dielectric layer and first metallized vias extending from the traces and contacting the element contacts; and

a plurality of stack terminals exposed at the second surface of the dielectric layer and electrically connected with the package terminals for connecting the package with a component overlying the second surface of the dielectric layer; and

a second microelectronic package overlying the first microelectronic package and having terminals joined to the stack terminals of the first microelectronic package.

27. The assembly of claim 26, wherein the first package further includes:

a molded encapsulation layer at least partially surrounding the first and second microelectronic elements within the interconnect area and defining a surface thereof overlying the second surface of the dielectric layer; and

conductive interconnects electrically connected with the stack terminals and having end surfaces exposed at the surface of the molded encapsulation layer.

28. A microelectronic assembly, comprising:

a first package, including:

a substrate having first and second opposed surfaces;

first and second microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements;

a plurality of package terminals at the second surface electrically interconnected with the substrate contacts for connecting the package with a component external to the package;

a plurality of stack terminals exposed at the first surface of the substrate in the interconnect area and electrically connected with at least some of the package terminals;

a second microelectronic package overlying the first microelectronic package and having terminals;

a plurality of conductive interconnects joined between the stack terminals of the first microelectronic package and the terminals of the second microelectronic package.

29. The microelectronic assembly of claim 28, wherein the second microelectronic package further includes a second dielectric layer having first and second opposed surfaces and at least one microelectronic element mounted on the first surface of the dielectric layer.

30. A microelectronic assembly, comprising:

a first package, including:

a substrate having first and second opposed surfaces;

four microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface, the microelectronic elements being arranged on the first surface so as to define an interconnect area of the first surface surrounded by the microelectronic elements;

a plurality of package terminals at the second surface electrically interconnected with the substrate contacts for connecting the package with a component external to the package; and

a plurality of stack terminals at the first surface in the interconnect area electrically connected with the package terminals

a second microelectronic package overlying the first microelectronic package and having terminals;

conductive interconnects joined between the stack terminals of the first microelectronic package and the terminals of the second microelectronic package.

31. The microelectronic assembly of claim 30, wherein each of the microelectronic elements includes a peripheral edge adjacent to the interconnect area such that the interior interconnect area is defined as a rectangular area.

32. The microelectronic assembly of claim 30, wherein at least some of the first stack terminals are electrically connected with at least two of the first microelectronic elements.

33. A microelectronic assembly, comprising:

a first package, including:

a substrate having first and second opposed surfaces;

first and second microelectronic elements each having element contacts electrically connected with corresponding substrate contacts on the first surface, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements;

a plurality of contact pads having surfaces exposed at the second surface of the substrate, the surfaces of the contact pads defining package terminals electrically interconnected with the substrate contacts for connecting the package with a component external to the package; and

a molded encapsulant layer overlying at least a portion of the first surface of the substrate and defining an encapsulant surface; and

a second microelectronic package bonded to the encapsulant surface and having terminals facing the encapsulant surface;

a plurality of conductive vias extending at least through the molded encapsulant layer and connecting the contact pads of the first microelectronic package and the terminals of the second microelectronic package.

34. The assembly of claim 33, wherein the conductive vias further extend through the contact pads of the first package in electrical contact therewith.

35. The assembly of claim 33, wherein the second microelectronic package further includes a substrate having first and second spaced apart surfaces, the second surface being bonded to the encapsulant surface, wherein the terminals of the second package are surfaces of conductive pads exposed at the second surface of the substrate, and wherein the conductive vias further extend through the conductive pads of the second package in electrical contact therewith.

36. A system comprising a microelectronic assembly according to claim 1 and one or more other electronic components electrically connected to the microelectronic assembly.

37. A method for making a microelectronic assembly, comprising:

assembling a first microelectronic package with a second microelectronic package, the second microelectronic package overlying the first microelectronic package and having terminals thereon, the first microelectronic package including:

a substrate having first and second opposed surfaces and substrate contacts thereon;

first and second microelectronic elements each having element contacts electrically connected with the

substrate contacts, the first and second microelectronic elements being spaced apart from one another on the first surface so as to provide an interconnect area of the first surface between the first and second microelectronic elements;

a plurality of package terminals at the second surface electrically interconnected with the substrate contacts for connecting the package with a component external to the package; and

a plurality of stack terminals exposed at the first surface in the interconnect area for connecting the package with a component overlying the first surface of the substrate; and

connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package to form an electrical connection therebetween.

38. The method of claim 37, wherein the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package includes joining the package terminals to exposed ends of interconnects on an encapsulant layer of the first microelectronic package overlying the first surface of the substrate at least in the interconnect area thereof, the interconnects being joined to the stack terminals opposite the exposed ends thereof.

39. The method of claim 37, wherein the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package includes depositing conductive bond material masses into holes within an encapsulant layer of the first microelectronic package overlying the first surface of the substrate at least in the interconnect area, the stack terminals being exposed at a surface of the encapsulant layer within the holes, and

wherein the conductive bond material masses are joined to the terminals of the second package and the stack terminals of the first package.

40. The method of claim 37, wherein the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package includes:

forming a plurality of holes through at least an encapsulant of the first microelectronic package overlying the first surface of the substrate in at least the interconnect area thereof, the plurality of holes being aligned with respective ones of the stack terminals at first ends thereof and with corresponding ones of the terminals of the second package at second ends thereof; and

filling the holes with a conductive material in contact with the stack terminals of the first microelectronic package and the package terminals of the second package.

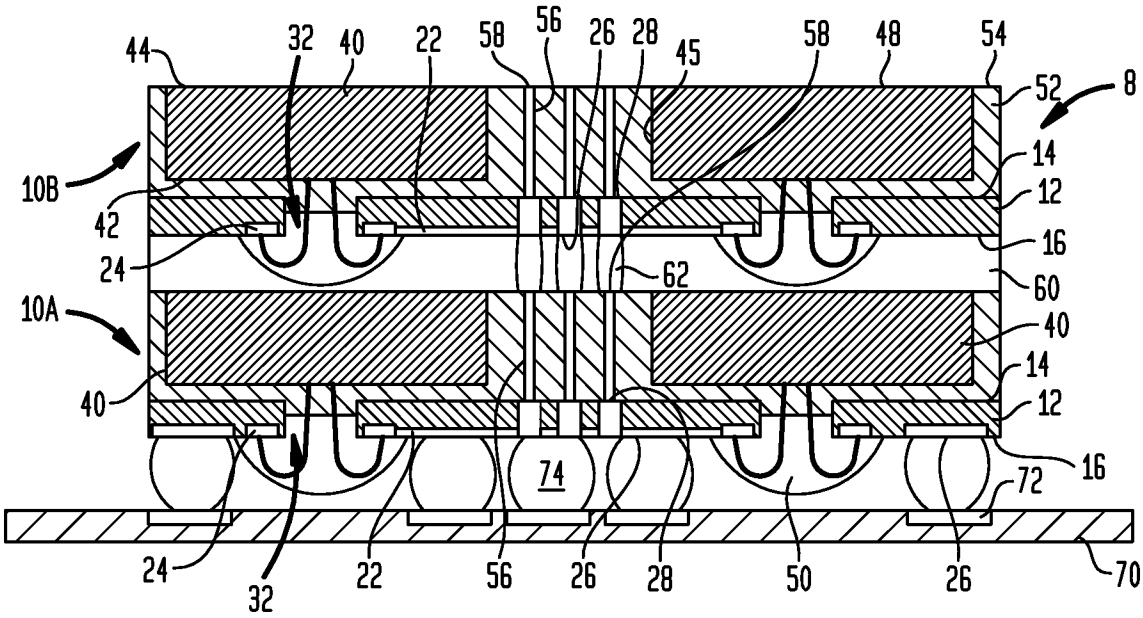
41. The method of claim 40, wherein the holes are further formed through the substrate of the first package and through the respective stack terminals thereof.

42. The method of claim 40, wherein the holes are further formed through a substrate of the second package and through the corresponding terminals thereof.

43. The method of claim 37, wherein the first microelectronic package further includes third and fourth microelectronic elements spaced on opposite sides of the interconnect area between the first and second microelectronic elements, and wherein the step of connecting the terminals of the second microelectronic package with the stack terminals of the first microelectronic package facilitates a connection

between the first, second, third, and fourth microelectronic elements of the first package to the second package.

FIG. 1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10A
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FIG. 1A

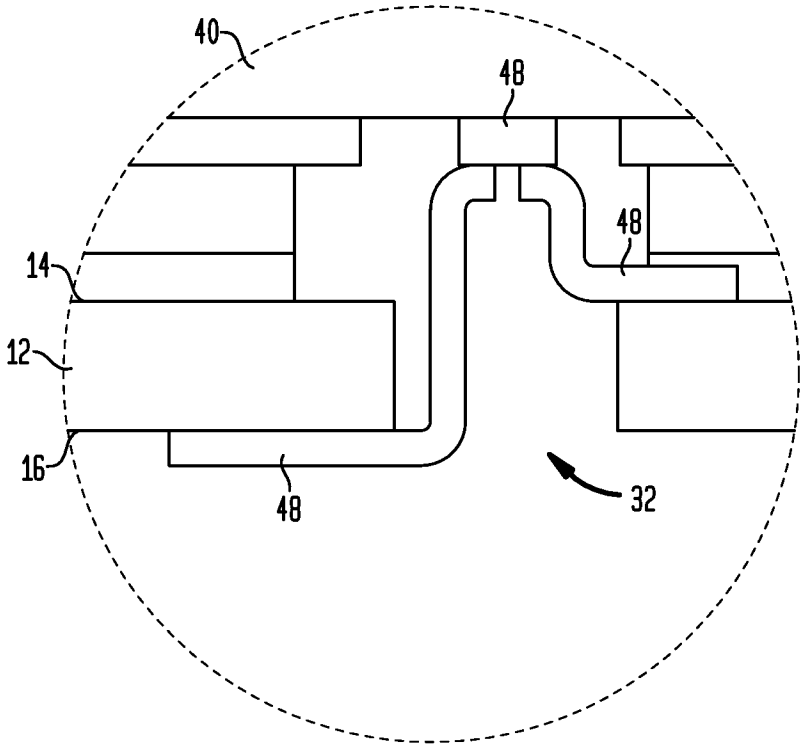
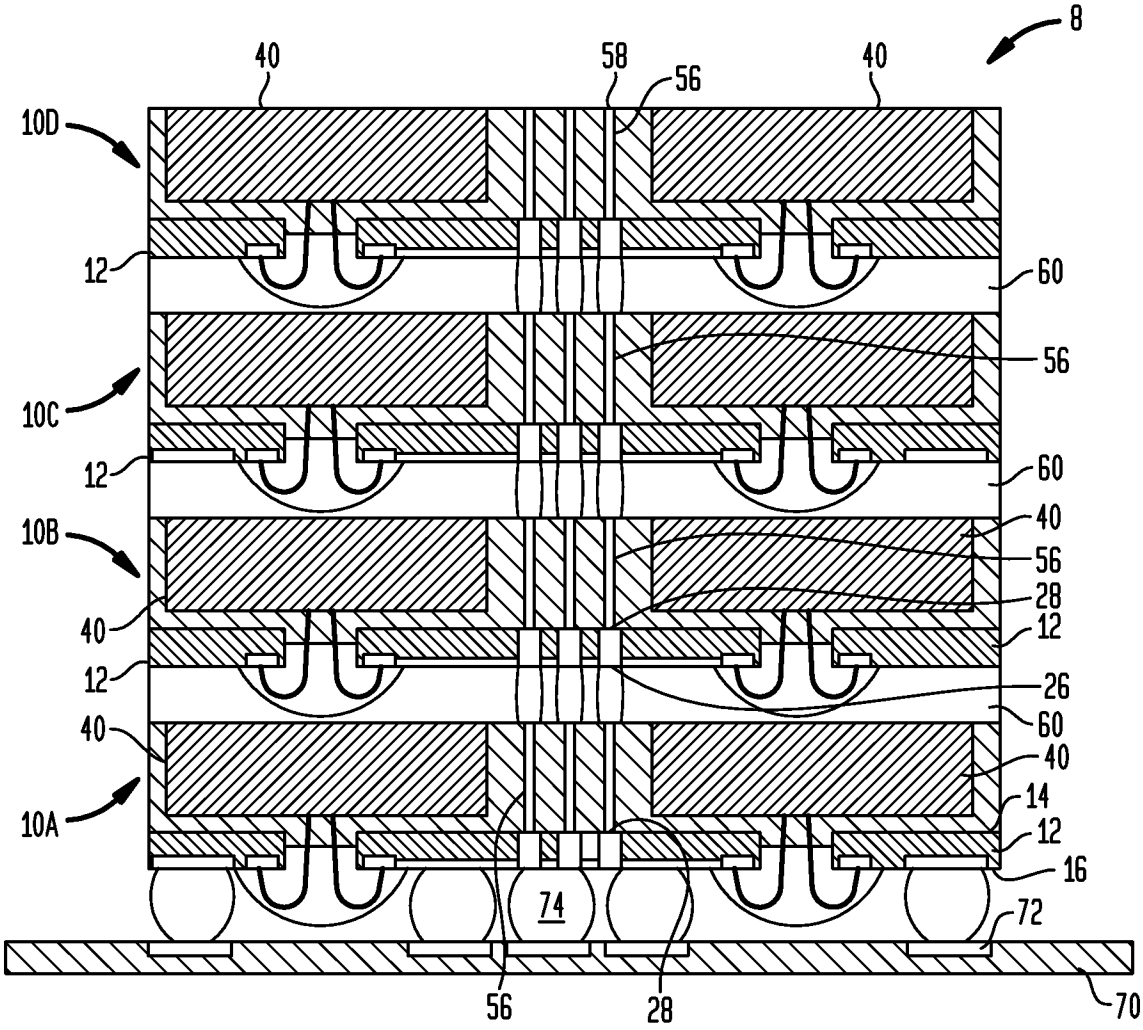


FIG. 2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10C
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FIG. 3A

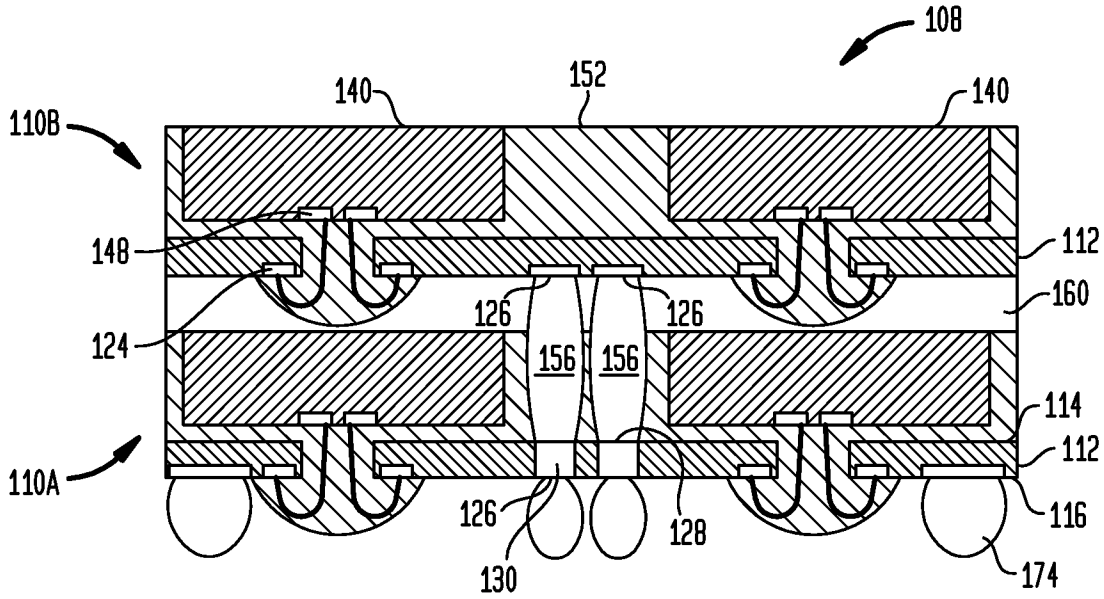
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FIG. 3B

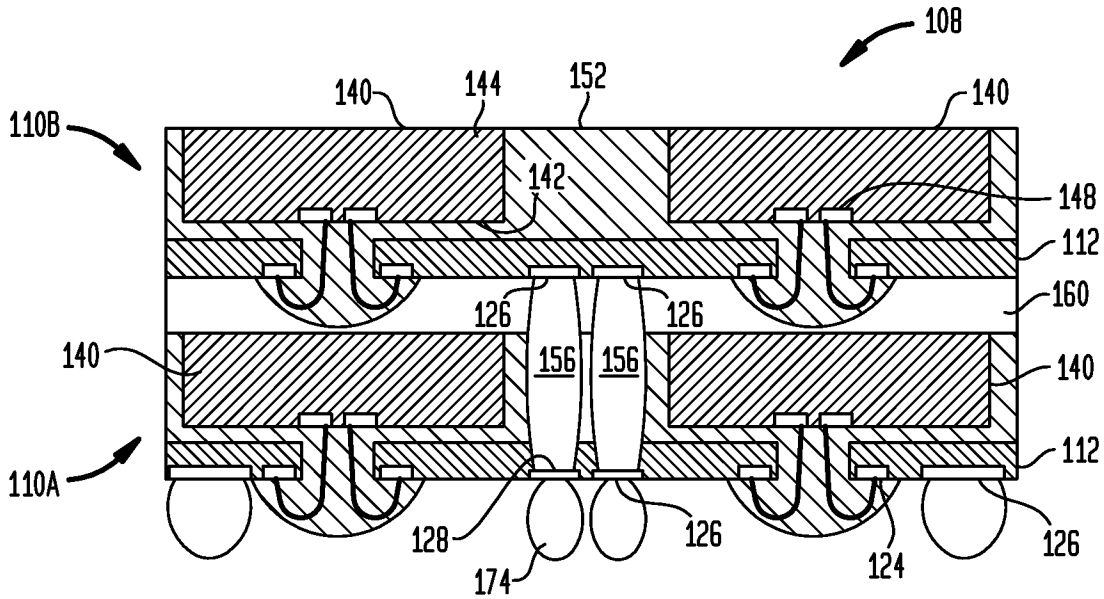
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FIG. 3C

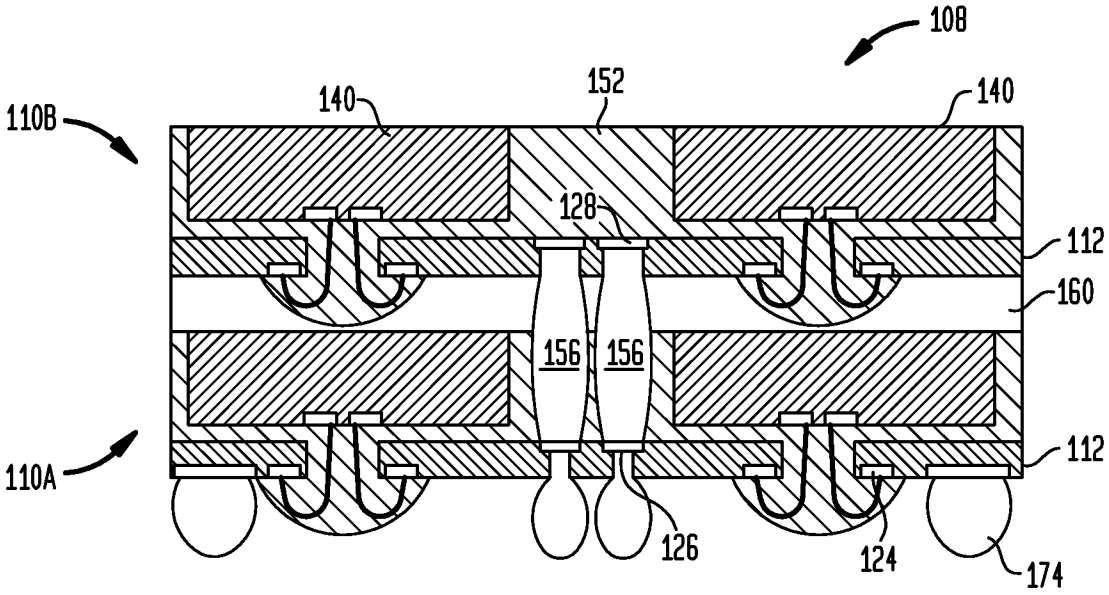
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FIG. 4

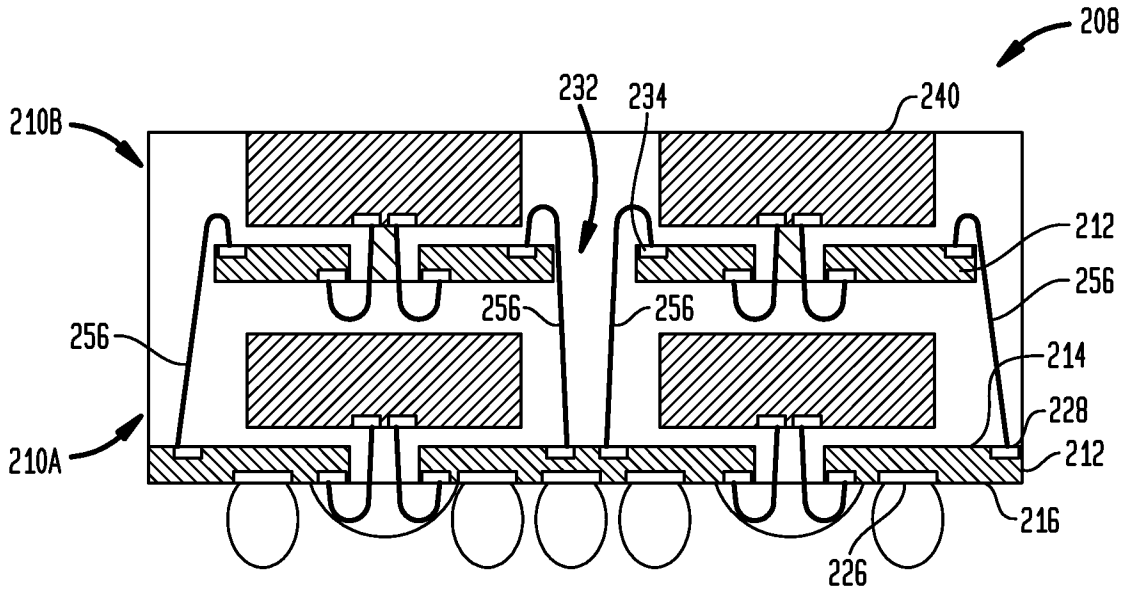
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FIG. 5A

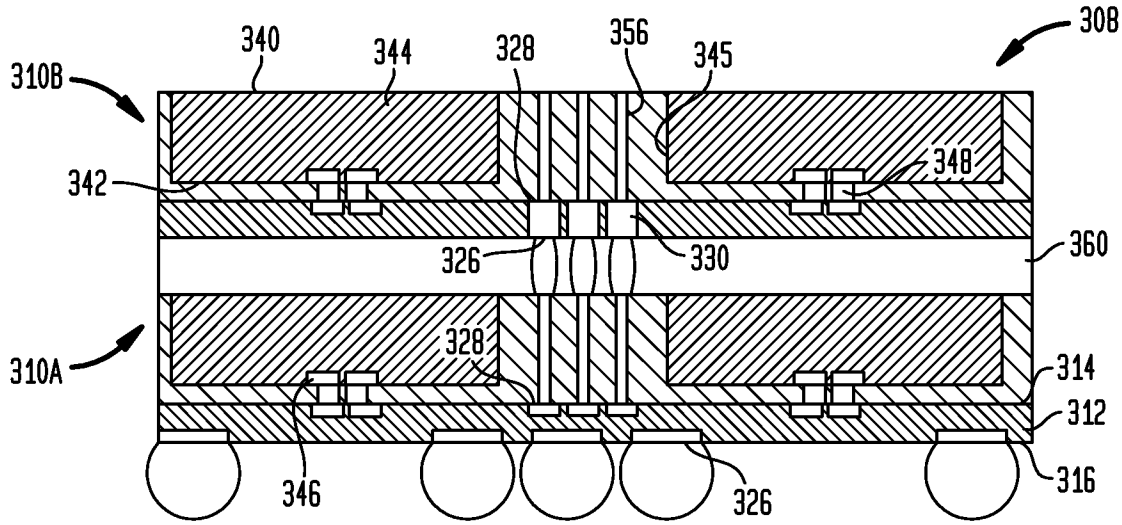
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FIG. 5B

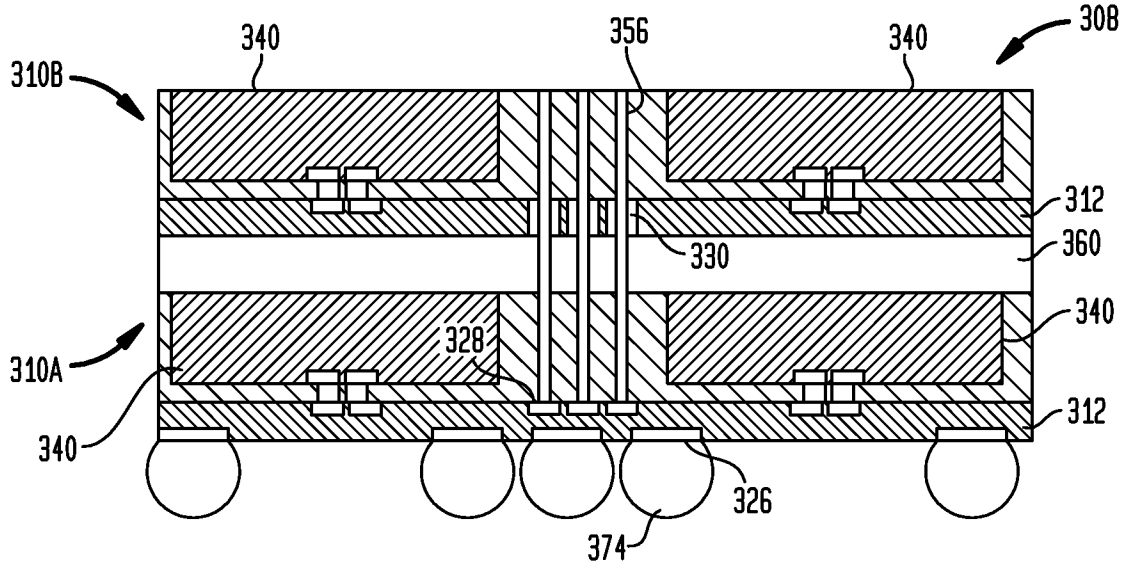
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FIG. 6

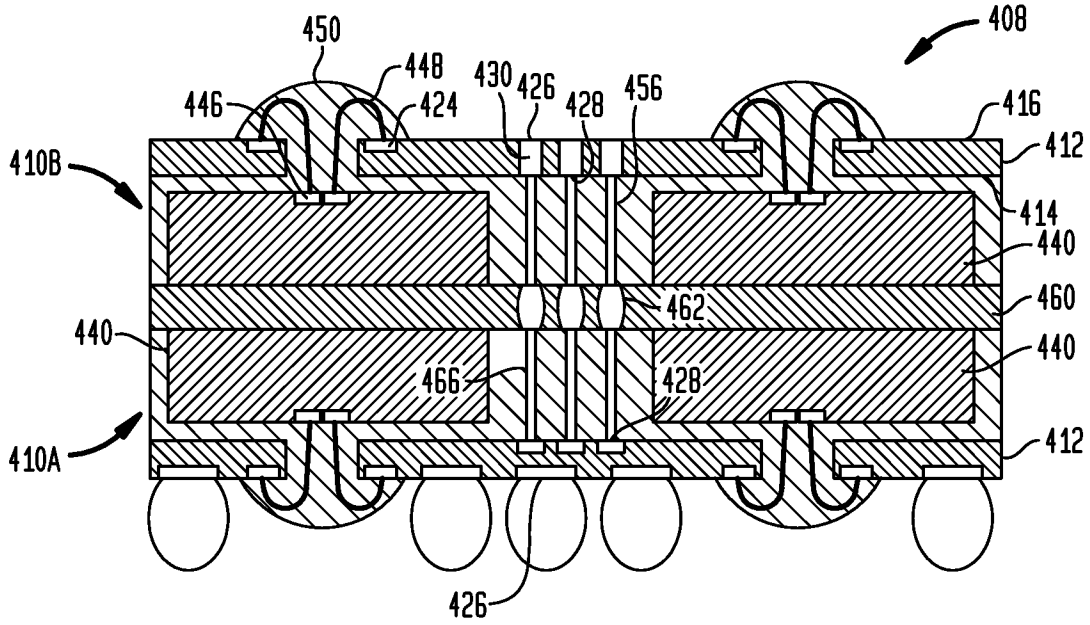
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FIG. 7

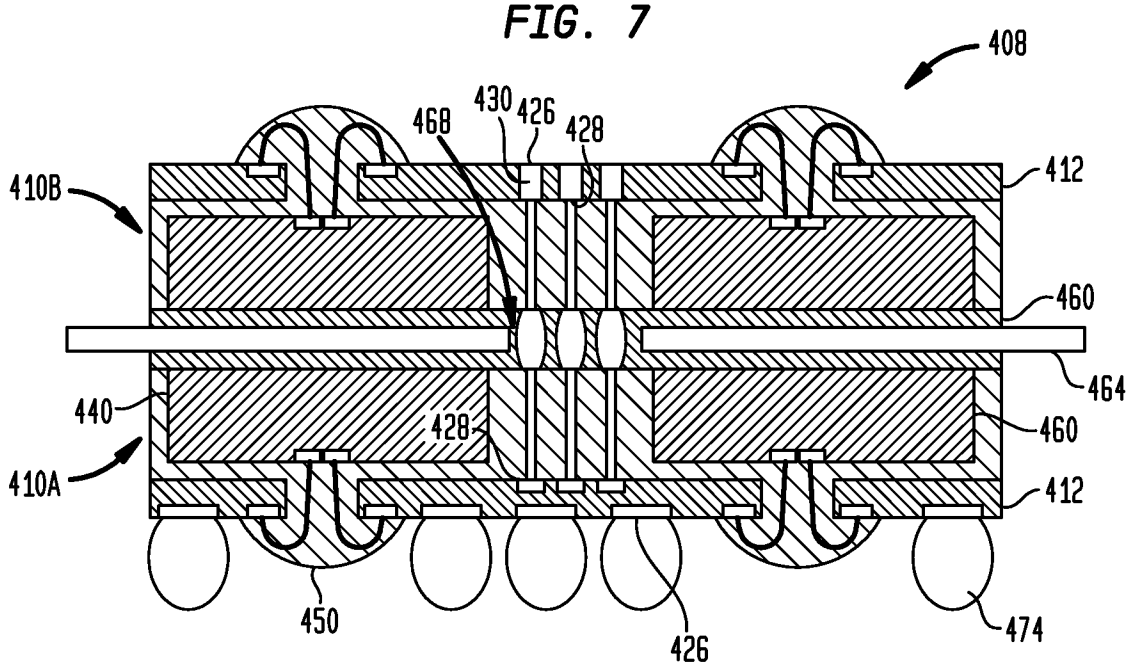
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FIG. 8

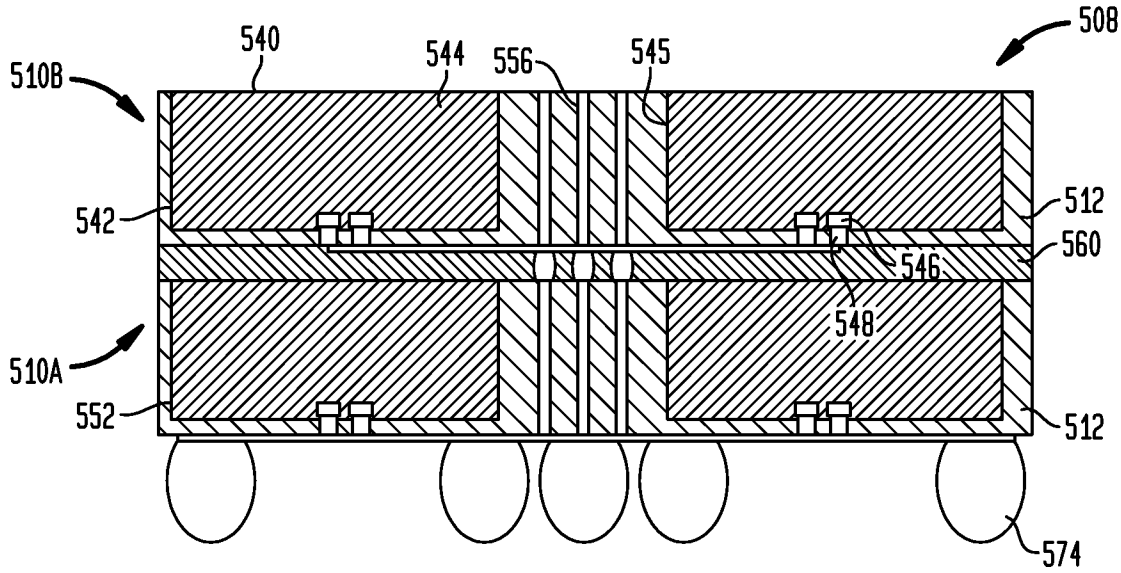
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FIG. 9

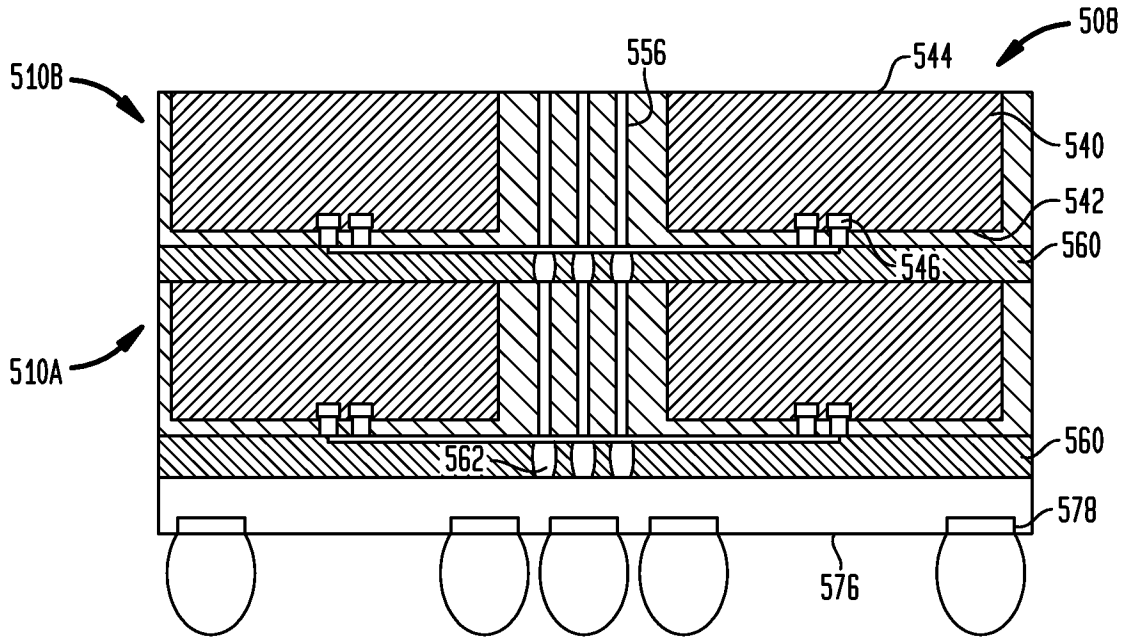
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FIG. 10

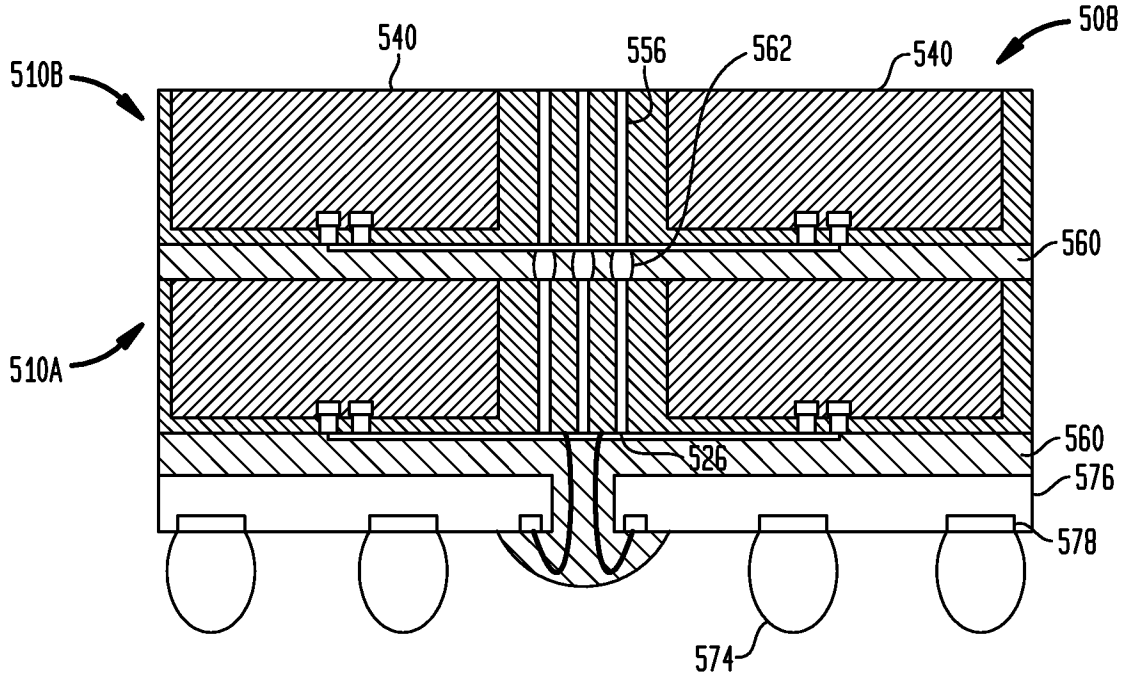
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FIG. 11

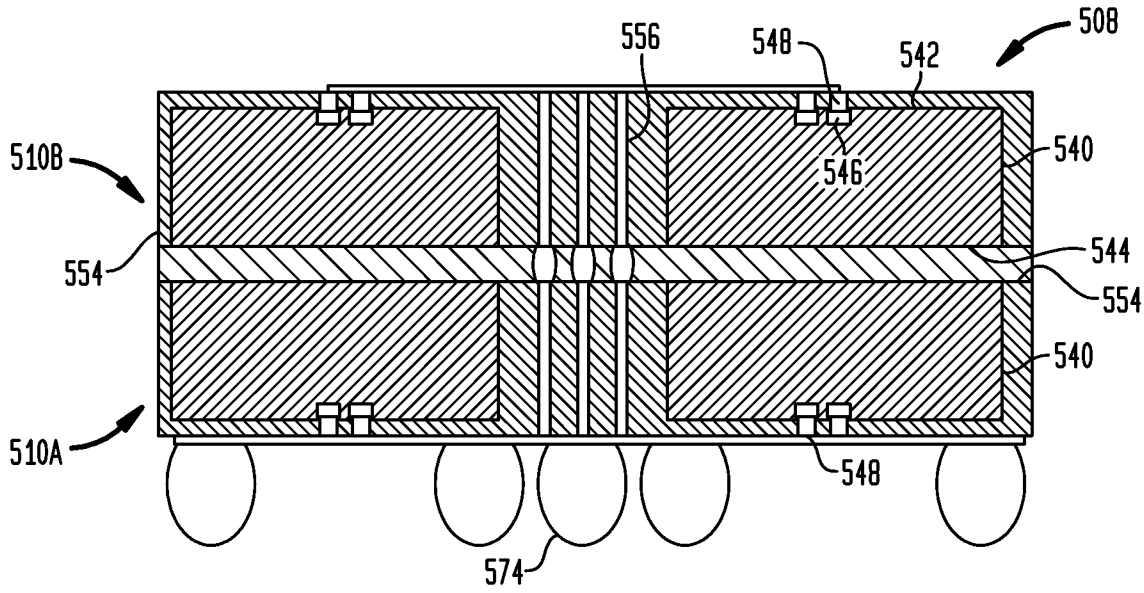
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FIG. 12

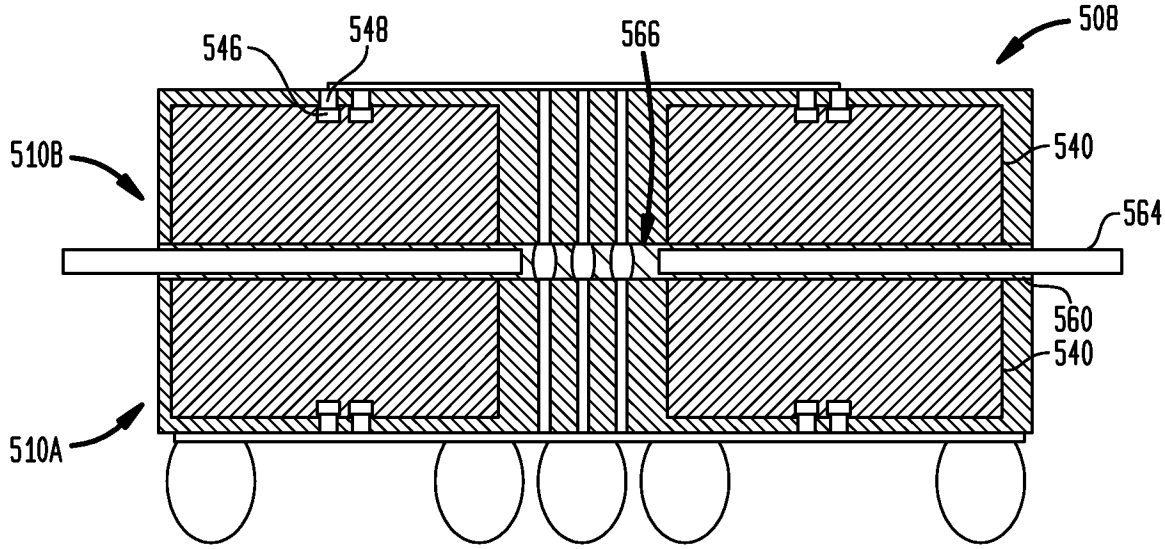
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FIG. 13

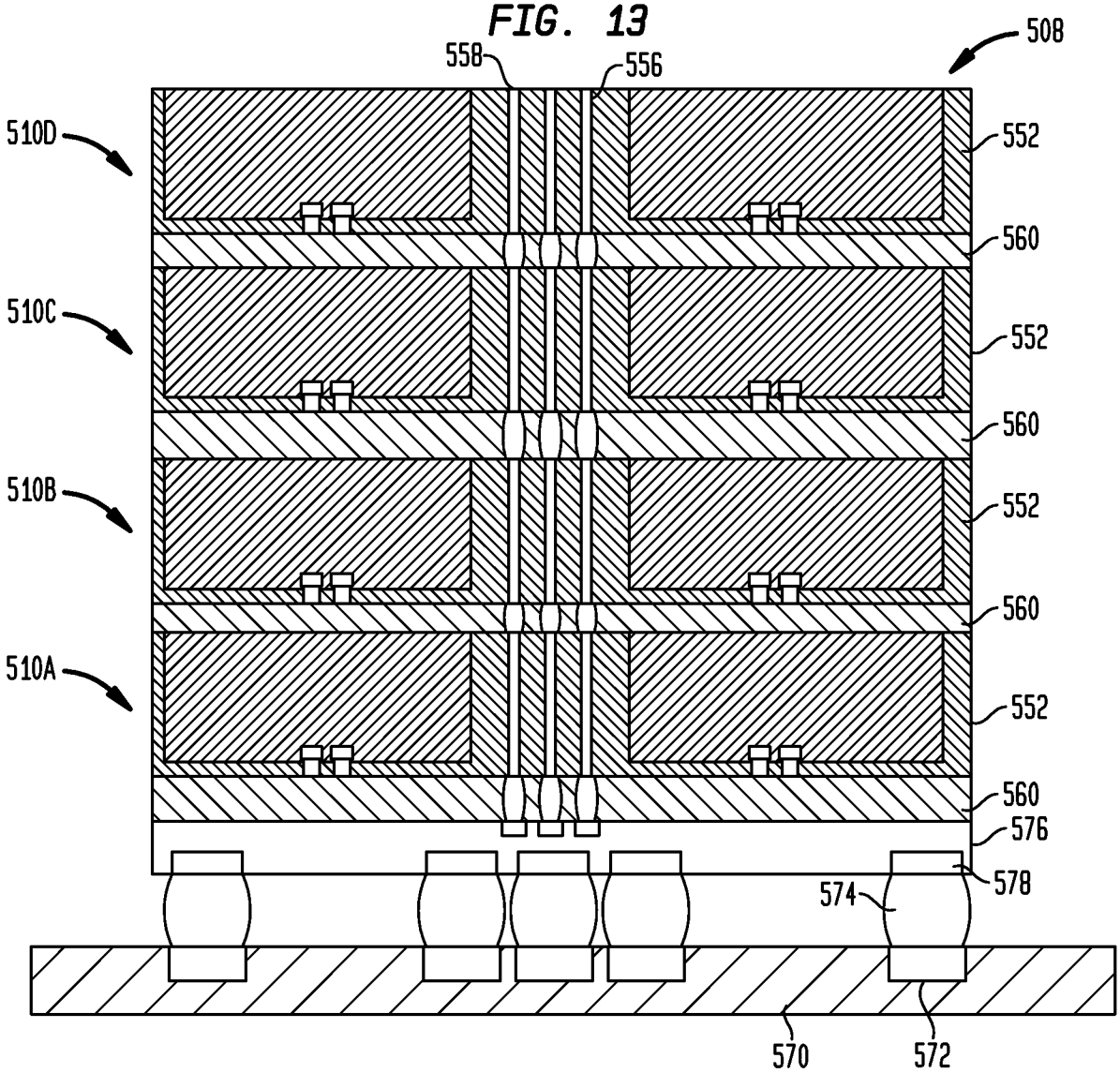
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FIG. 14

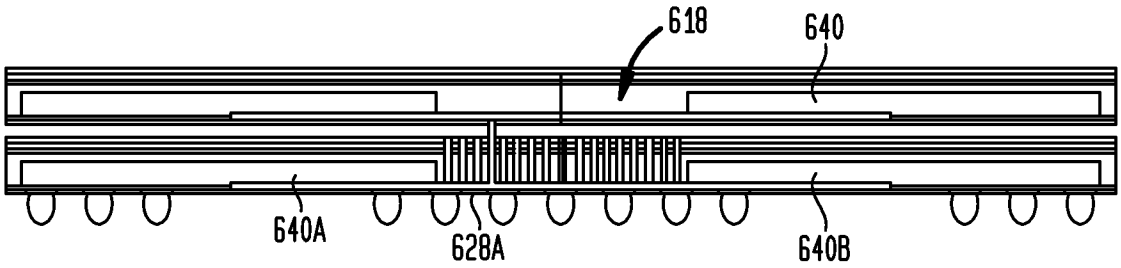
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FIG. 15

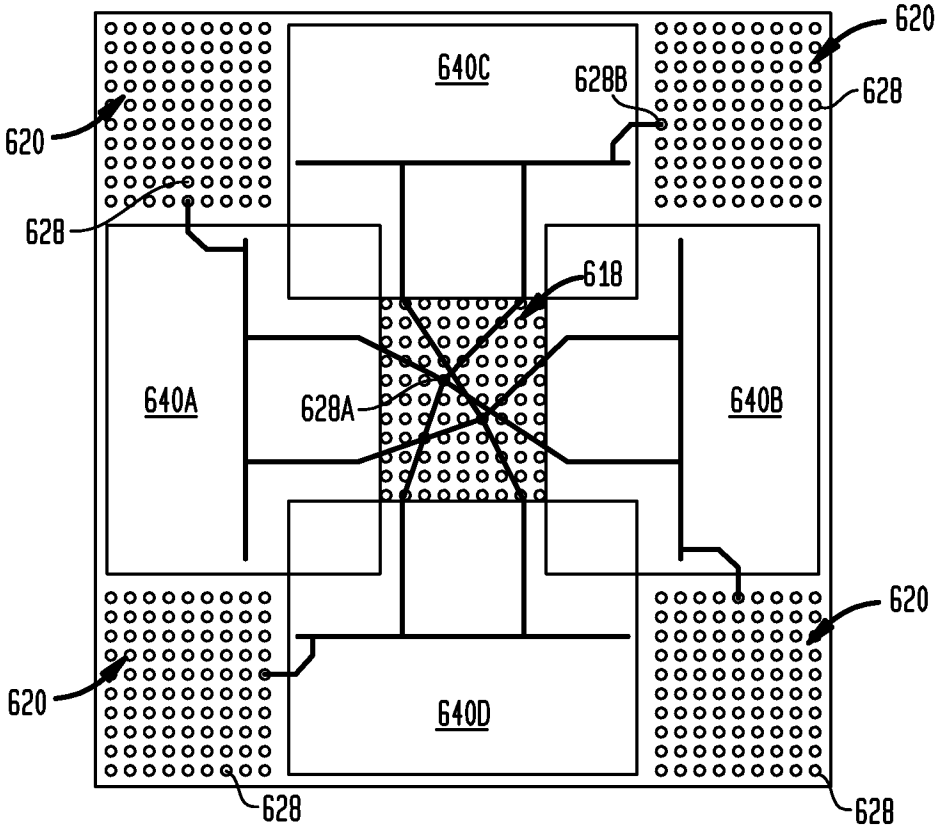
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FIG. 16

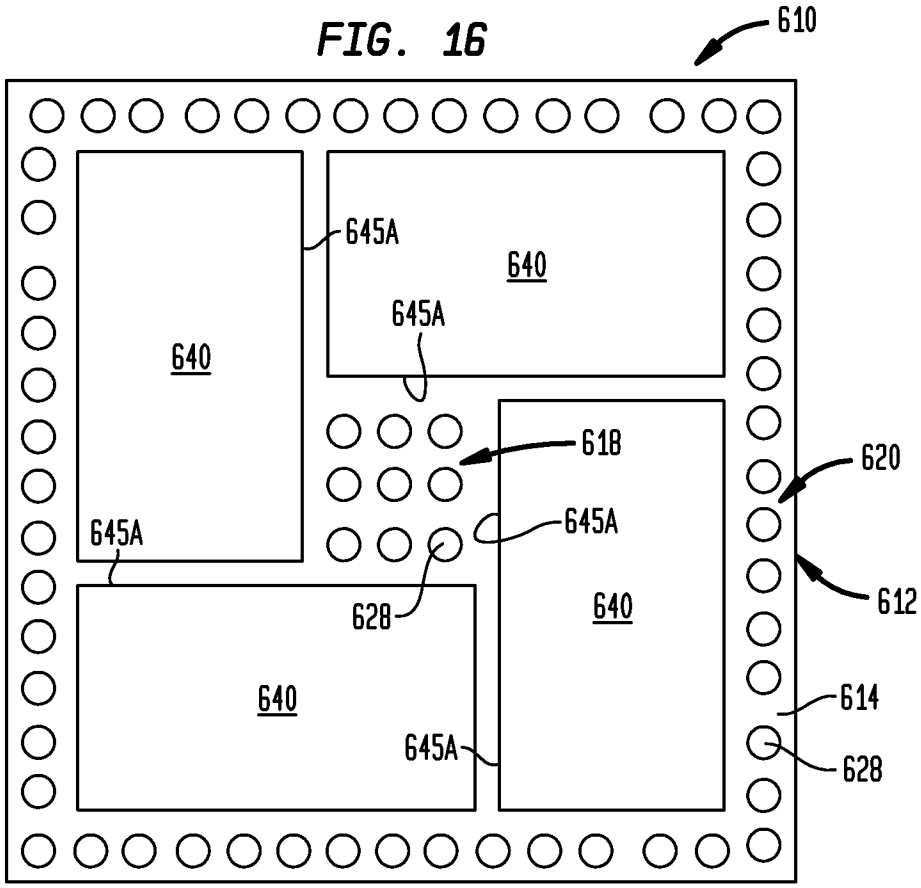
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FIG. 17

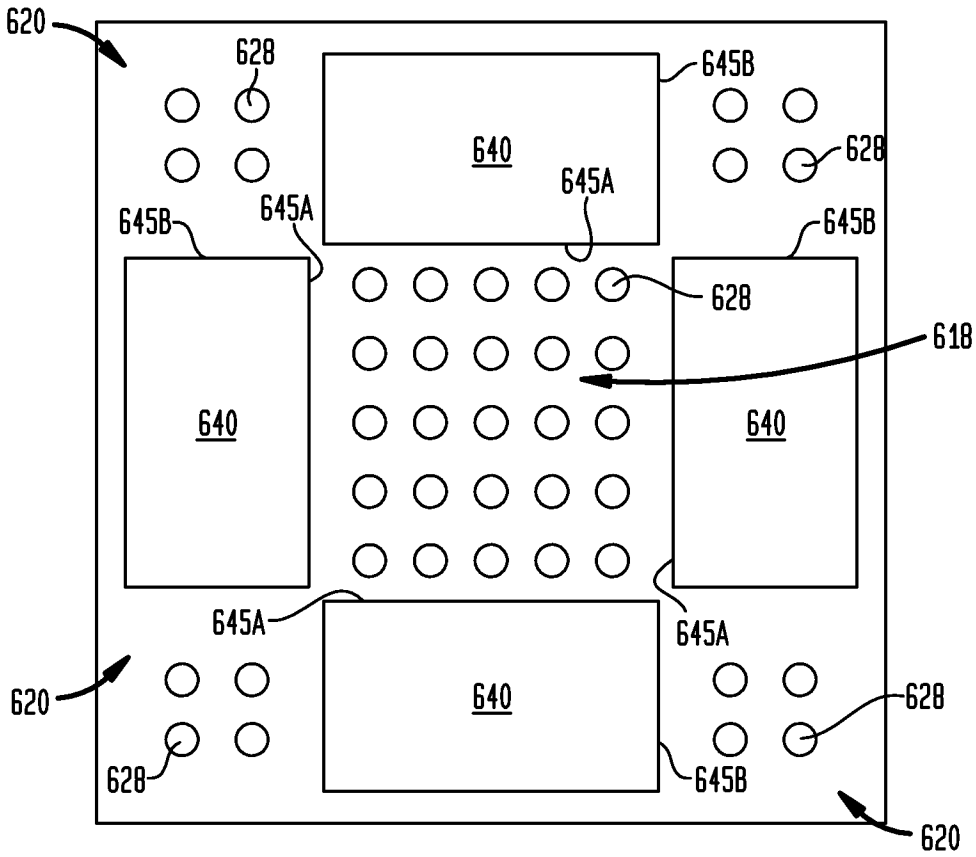
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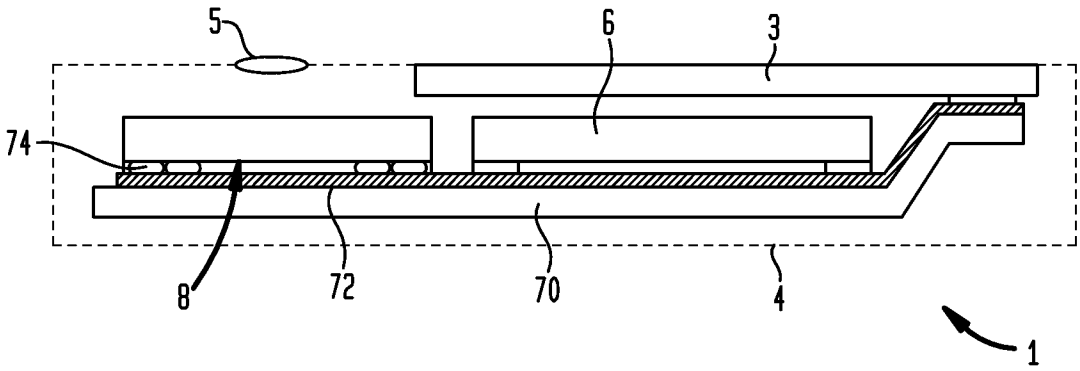
FIG. 18



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/070477

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/10 H01L23/538 H01L25/065 H01L23/34
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/155960 A1 (CHOW SENG GUAN [SG] ET AL) 18 June 2009 (2009-06-18) figure 2 -----	1-3,28, 36,37

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 April 2013	03/06/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Manook, Rhoda

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/070477

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-3, 28, 36, 37

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-3, 28, 36, 37

See invention groups 10,11 and 12 for the non-unity reasoning between independent claims 1,26,30 and 33.
A further non-unity objection arises for the cls. within group I (cls. 1-25, 28-29 & 36-43):
The subject matter of independent product cl. 1 & corresponding independent method cl. 37 & independent product cl. 28 is not new compared to the teaching of document US2009/155960 (D1) & cannot therefore serve as a common concept for the directly dependent cls. 2,4,7,12,13,14,15,16,18,19,20,29,38,39,40 & 43.
See the written non-unity reasoning (section 1.5.1 in the written non-unity reasoning) for the lack of novelty of the subject matter of independent claims 1,28 and 37 in view of document D1.
As a consequence of the above, the following claimed separate sub-invention groups within group I have been identified in the sense of Rule 13(2) PCT:
Group Ia: cls. 1,2,3 (c.f. cl. 2), 28, 36 & 37
Re. cl. 2 the stf with respect to (wrt) the known cl. 1 is that the package terminals & the stack terminals overlie each other in respective electrically connected pairs.
As all of the features of cl. 2 are known from D1 none of them can form a contribution over the known prior art.
Although the stf of the dependent cl. 36 are not the same, they could be searched without any additional effort & thus they form the basis of the 1st searched invention.

---

2. claims: 4-6

Group Ib: cls. 4-6
Re. cl. 4 the stf wrt the known cl. 1 is additional ones of the stack terminals are at the 1st surface of the substrate in a portion thereof that is outside of the interconnect area.
The problem to be solved by cl. 4 is how to minimise re-routing.

---

3. claims: 7-11, 43

Group Ic: cls. 7-11 & 43 (c.f. cls. 7 & 43)
Re. cl. 7 the stf wrt the known cl. 1 is that the 1st microelectronic package further includes 3rd & 4th microelectronic elements spaced on opposite sides of the interconnect area between the 1st & 2nd microelectronic elements.
Re. cl. 43 the stf wrt the known cl. 37 is that the 1st microelectronic package further includes 3rd & 4th microelectronic elements spaced on opposite sides of the

interconnect area between the 1st & 2nd microelectronic elements, & wherein the step of connecting the terminals of the 2nd microelectronic package with the stack terminals of the 1st microelectronic package facilitates a connection between the 1st, 2nd, 3rd, & 4th microelectronic elements of the 1st package to the 2nd package.
The problem to be solved by cls. 7 & 43 is ensuring designing the 1st microelectronic package for higher density operation.

---

4. claims: 12, 38-42

Group Id: cl. 12, 38, 39 & 40-42 (c.f. cls. 12, 38,39,40)
Re. cl. 12 the stf wrt the known cl. 1 is that the 1st microelectronic package further includes a molded encapsulant layer overlying at least a portion of the 1st surface of the substrate, & wherein at least portions of the 1st conductive interconnects comprise 1st conductive vias extending through the molded encapsulant layer to exposed ends.
Re. cl. 38 the stf wrt the known cl. 37 is that the step of connecting the terminals of the 2nd microelectronic package with the stack terminals of the 1st microelectronic package includes joining the package terminals to exposed ends of interconnects on an encapsulant layer of the 1st microelectronic package overlying the 1st surface of the substrate at least in the interconnect area thereof, the interconnects being joined to the stack terminals opposite the exposed ends thereof.
Re. cl. 39 the stf wrt the known cl. 37 is that the step of connecting the terminals of the 2nd microelectronic package with the stack terminals of the 1st microelectronic package includes depositing conductive bond material masses into holes within an encapsulant layer of the 1st microelectronic package overlying the 1st surface of the substrate at least in the interconnect area, the stack terminals being exposed at a surface of the encapsulant layer within the holes, & wherein the conductive bond material masses are joined to the terminals of the 2nd package & the stack terminals of the 1st package.
Re. cl. 40 the stf wrt the known cl. 37 is that the step of connecting the terminals of the 2nd microelectronic package with the stack terminals of the 1st microelectronic package includes: forming a plurality of holes through at least an encapsulant of the 1st microelectronic package overlying the 1st surface of the substrate in at least the interconnect area thereof, the plurality of holes being aligned with respective ones of the stack terminals at 1st ends thereof & with corresponding ones of the terminals of the 2nd package at 2nd ends thereof; & filling the holes with a conductive material in contact with the stack terminals of the 1st microelectronic package & the package terminals of the 2nd package.
The problem to be solved by cls. 12, 38, 39 or 40 is

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

providing electrical paths through mold material.

---

5. claims: 13, 14

Group Ie: cls. 13 & 14
Re. cl. 13 the stf wrt the known cl. 1 is that contact-bearing faces of the 1st & 2nd microelectronic elements face the substrate, the substrate contacts including substrate contacts exposed at the 2nd surface, & wherein the element contacts are connected with the substrate contacts by wire bonds.
Re. cl. 14 the stf wrt the known cl. 1 is that substrate contacts are exposed at the 1st surface & wherein the element contacts of the 1st & 2nd 1st microelectronic elements face the substrate contacts exposed at the 1st surface & are joined thereto.
The problem to be solved by cls. 13 & 14 is selecting the connection between the microelectronic elements & the substrate such that electrical resistance is kept to a minimum.

---

6. claims: 15-17, 29

Group If: cls. 15,16-17 & 29
Re. cl. 15 the stf wrt the known cl. 1 is that the 2nd microelectronic package includes a 3rd microelectronic element mounted on a 2nd substrate, the terminals being on the 2nd substrate & electrically connected with the 3rd microelectronic element.
Re. cl. 16 the stf wrt the known cl. 1 is that the 2nd microelectronic package includes a substrate having 1st & 2nd spaced apart surfaces & 3rd & 4th microelectronic elements mounted on the 2nd surface thereof, the 3rd & 4th microelectronic elements being spaced apart on the substrate of the 2nd package to define an interconnect area therein, & the terminals being exposed at the 2nd surface of the substrate of the 2nd package within the interconnect area, the substrate of the 2nd package further including a window extending therethrough between the 1st & 2nd surfaces thereof, & wherein the terminals of the 2nd package are joined to the stack terminals of the 1st package by wire bonds that extend through the window.
Re. cl. 29 the stf wrt the known cl. 28 the 2nd microelectronic package further includes a 2nd dielectric layer having 1st & 2nd opposed surfaces & at least one microelectronic element mounted on the 1st surface of the dielectric layer.
The problem to be solved by cls. 15 & 16 & 29 is designing the 2nd microelectronic package for high density.

---

7. claim: 18

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Group Ig: cl. 18
Re. cl. 18 the stf wrt the known cl. 1 is that it further includes a 3rd microelectronic package underlying the 1st microelectronic package & having terminals joined to the package terminals of the 1st microelectronic package.
The problem to be solved by cl. 18 is designing the assembly for high density performance whilst ensuring the assembly footprint is kept small.

---

8. claim: 19

Group Ih: cl. 19
Re. cl. 19 the stf wrt the known cl. 1 is that it further includes a circuit panel with circuit contacts exposed at a surface thereof, wherein the package terminals of the 1st microelectronic package are electrically connected with the circuit contacts.
The problem to be solved by cl. 19 is providing means for connecting a multitude of microelectronic assemblies.

---

9. claims: 20-25

Group Ii: cls. 20-25
Re. cl. 20 the stf wrt the known cl. 1 is that the 2nd microelectronic package terminals are at least one of package terminals or stack terminals.
The problem to be solved by cl. 20 is providing electrical connection to other parts of the package or the outside world.

---

10. claims: 26, 27

The common concept between the subject-matter of independent product claims (cls.) 1 & 26 is already known in view of document US2009/155960 (D1) & cannot therefore serve as a common concept (Rule 13(1) PCT) between these cls.
see section 1.1.1 of the written non-unity objection attached to this partial search report which discloses the common concept between the claims and its lack of novelty with respect to document D1 (fig. 2).
The surplus technical features (stf) of cl. 1 are that there is a substrate having 1st & 2nd opposed surfaces & substrate contacts thereon; the element contacts of the microelectronic elements are electrically connected with the substrate contacts & the microelectronic elements are on the 1st surface, the plurality of package terminals are located at the 2nd surface of the substrate & electrically connected with the substrate contacts, the plurality of stack terminals are exposed at the 1st surface of the substrate.
Thus the problem of cl. 1 to be solved can be construed as: defining a microelectronic package for enhanced mechanical stability.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

The stf of cl. 26 are that the microelectronic elements have front faces & back faces & the element contacts are exposed at the front faces, there is a dielectric layer which has a surface overlying the front faces of the microelectronic elements & facing away from the front faces of the microelectronic elements, the dielectric layer further having a 2nd surface opposite the 1st surface, the plurality of package terminals are exposed at the 1st surface of the dielectric layer & electrically connected with the element contacts through traces extending along the dielectric layer & 1st metallized vias extending from the traces & contacts the element contacts, & the stack terminals are exposed at the 2nd surface of the dielectric layer & connect the package with a component overlying the 2nd surface of the dielectric layer,
Thus the problem of cl. 26 to be solved can be construed as: Use of a HDI-type connection to ensure the microelectronic elements have a shorter electrical connection to the outside.
Neither does cl. 1 refer to the dielectric layer & its traces & vias nor does cl. 26 refer to the details of the substrate. The problems solved by independent cls. 1 & 26 refer to different features which solve different problems.

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11. claims: 30-32

The features common to cls. 1 & 30 (see section referring to claim 26) are known from document D1 (D1 also shows the substrate (fig. 2 (108) having 1st & 2nd opposed surfaces) & cannot therefore serve as a common inventive concept for these cls..
The stf of cl. 1 are that the plurality of stack terminals for connecting the package with a component overlying the 1st surface of the substrate.
Thus the objective problem of cl. 1 to be solved can be construed as defining a microelectronic package for higher densities whilst maintaining the same package footprint.
The stf of cl. 30 are that there are four microelectronic elements arranged so as to define the interconnect area of the 1st surface surrounded by the microelectronic components, the plurality of stack terminals are electrically connected with the package terminals.
Thus the objective problem of cl. 30 to be solved can be construed as: defining a microelectronic package for higher densities whilst minimising the thickness of the package.
The problems solved by independent cls. 1 & 30 refer to different features which solve different problems.

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12. claims: 33-35

The features common to cls. 1 & 33 (see section referring to claim 26) are known from document D1 (D1 also shows the substrate (fig. 2 (108) having 1st & 2nd opposed surfaces &

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that there are a plurality of contact pads having surfaces exposed at the 2nd surface of the substrate, the surfaces of the contact pads defining package terminals electrically interconnected with the substrate contacts for connecting the package with a component external to the package) & cannot therefore serve as a common inventive concept for these cls..

The stf of cl. 1 are that the plurality of stack terminals are exposed at the 1st surface in the interconnect area (for connecting the package with a component overlying the 1st surface of the substrate).

Thus the objective problem of cl. 1 to be solved can be construed as defining a microelectronic package for higher densities whilst maintaining the same package footprint.

The stf of cl. 33 are that a molded encapsulant layer overlying at least a portion of the 1st surface of the substrate & defining an encapsulant surface,

the 2nd microelectronic package bonding to the encapsulant surface & having terminals facing the encapsulant surface

a plurality of conductive vias extending at least through the molded encapsulant layer & connecting the contact pads of the 1st microeletronic package & the terminals of the 2nd microelectronic package.

Thus the objective problem of cl. 33 to be solved can be construed as protecting the microelectronic elements against environmental damage.

Neither does cl. 1 refer to the detail of the encapsulant layer & conductive vias nor does cl. 33 refers to the existence of stack terminals. The problems solved by independent cls. 1 & 33 refer to different features which solve different problems.

INTERNATIONAL SEARCH REPORT

Information on patent family members

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