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Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

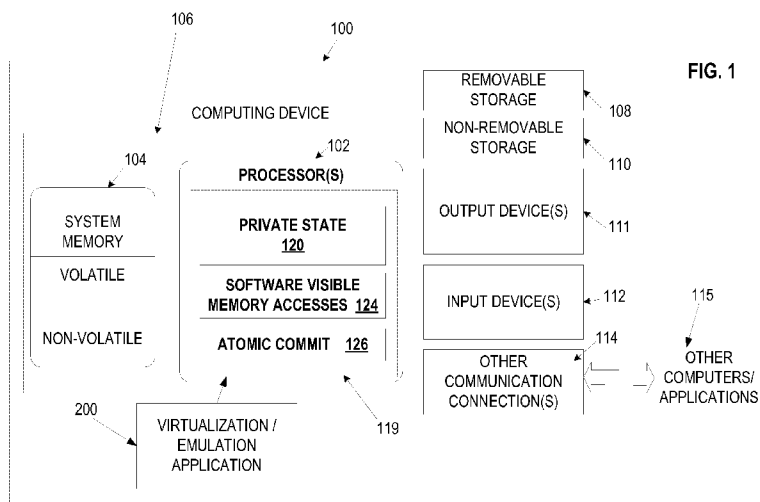
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(54) Title: LEVERAGING TRANSACTIONAL MEMORY HARDWARE TO ACCELERATE VIRTUALIZATION AND EMULATION



(57) Abstract: Various technologies and techniques are disclosed for using transactional memory hardware to accelerate virtualization or emulation. State isolation can be facilitated by providing isolated private state on transactional memory hardware and storing the stack of a host that is performing an emulation in the isolated private state. Memory accesses performed by a central processing unit can be monitored by software to detect that a guest being emulated has made a self modification to its own code sequence. Transactional memory hardware can be used to facilitate dispatch table updates in multithreaded environments by taking advantage of the atomic commit feature. An emulator is provided that uses a dispatch table stored in main memory to convert a guest program counter into a host program counter. The dispatch table is accessed to see if the dispatch table contains a particular host program counter for a particular guest program counter.

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**A. CLASSIFICATION OF SUBJECT MATTER****G06F 13/00(2006.01)i, G06F 9/455(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models applications for Utility Models since 1975, IPC as above

Japanese Utility Models and application for Utility Models since 1975, IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS, IEEEExpl, Google; transactional memory, hardware accelerate, emulate;

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0073528 A1(WILLIAM WATT, et.al) 29 Mar 2007 See all elements.	1-20
A	US 7181608 B2(JAMES J.F, et.al) 20 Feb 2007 See all elements.	1-20
A	US 6983357 B2(THOMA. C. POFF, et.al) 3 Jan 2006 See all elements.	1-20
A	SAHA, B et al. 'Architectural Support for Software Transactional Memory.' In: Microarchitecture, 2006. MICRO-39. 39th Annual IEEE/ACM International Symposium on. IEEE., 9-13 Dec. 2006 . ISBN: 0-7695-2732-9, PP185-196 See abstract and chapter 5 : Hardware Accelerated STM.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

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"&amp;" document member of the same patent family

Date of the actual completion of the international search

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0073528 A1	29.03.2007	EP 1934845 A2	25.06.2008
US 7181608 B2	20.02.2007	EP 1179194 A1 US 2002-0069354 A1	13.02.2002 06.06.2002
US 6983357 B2	03.01.2006	None	