June 30, 1959 R. D. TOLLEFSON ET AL 2,892,943

MULTI-PULSE SYNCHRONIZER

Filed March 14, 1958 2 Sheets-Sheet 1

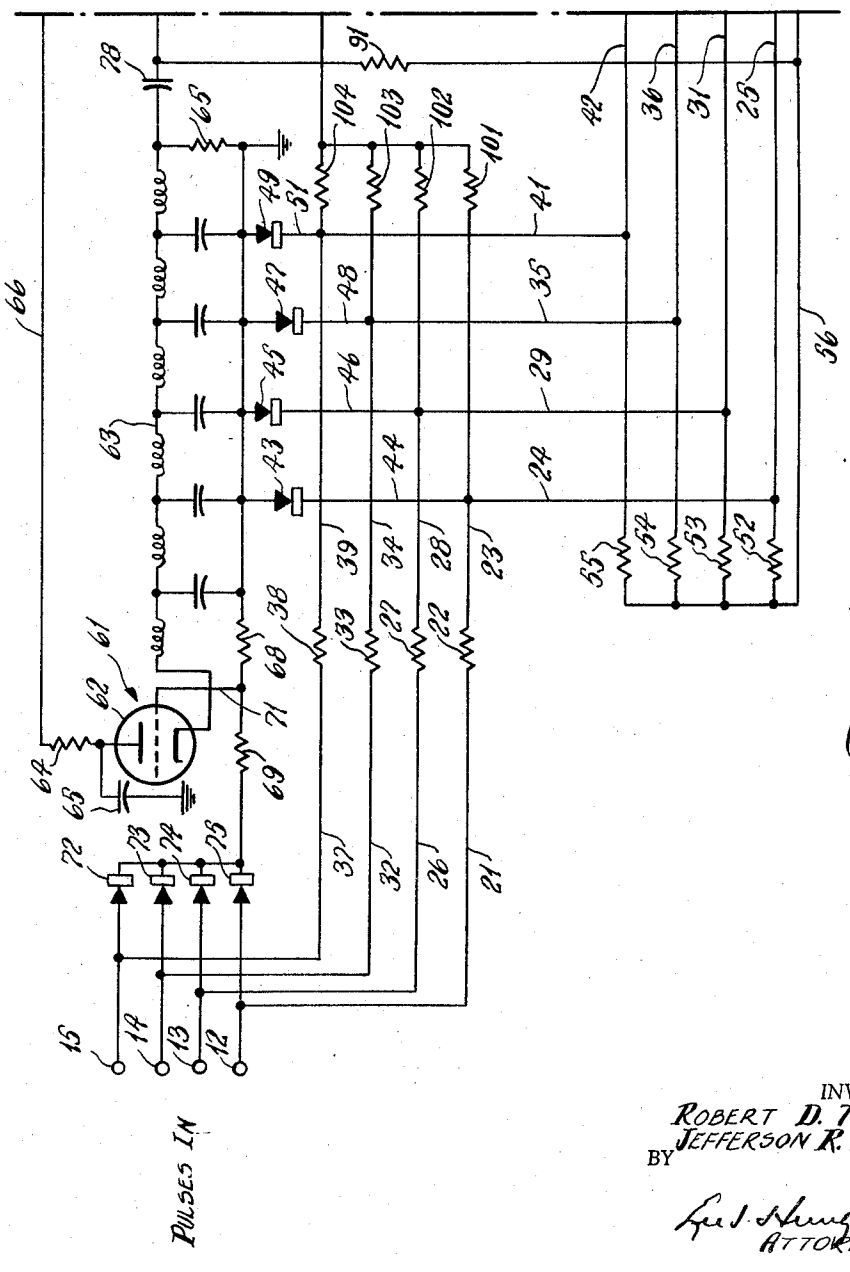

Fig. 1

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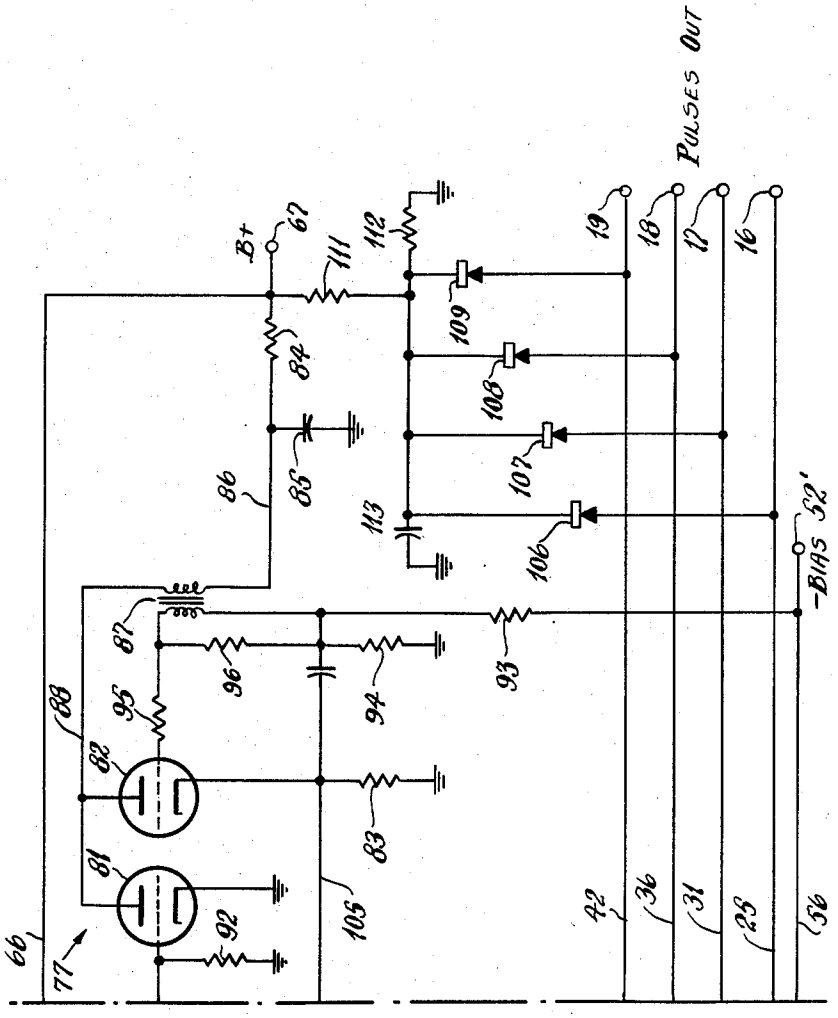

Fig. 2

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MULTI-PULSE SYNCHRONIZER

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6 Claims. (Cl. 250—27)

This invention relates to apparatus for synchronizing several substantially equal width rectangular pulses that are substantially coincident and more particularly to an apparatus for rendering time coincident the leading edges of several such pulses that have leading edge jitter on the order of a fraction of the pulse width.

When digital information is encoded into binary pulse patterns the pulses of each group or pattern are substantially identical and substantially coincident. One type of circuit that utilizes binary pulse patterns is a matcher circuit that stores a particular binary pulse pattern and accepts all incoming pulse patterns and reacts when an incoming binary pulse pattern matches the stored pattern. It has been found that the results obtained from the matcher circuit are not reliable if there is leading edge jitter, that is, a time spread among the leading edges of pulses comprising any one binary pulse pattern. The leading edge jitter may be due to variations in coupling leads and other coupling elements. Regardless of cause, it is important to eliminate the leading edge jitter.

An object of this invention is to provide a multipulse synchronizer apparatus for eliminating leading edge jitter among several substantially coincident rectangular pulses.

A further object is to accomplish the above with a minimum of electron discharge devices and as simple and reliable an apparatus as possible.

Other objects and many of the attendant advantages of this invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawing wherein:

Figs. 1 and 2 are adjacent portions of a composite circuit diagram of one embodiment of this invention.

The particular embodiment of the invention shown on the drawings is an apparatus that can accommodate up to four pulses during any one instant. The apparatus includes four input terminals 12, 13, 14, 15 and four output terminals 16, 17, 18, 19. Each of the input terminals is connected in series with a respective one of the output terminals. Input terminal 12 is connected to output terminal 16 by means of lead 21, resistor 22, and leads 23, 24, and 25. Input terminal 13 is connected to output terminal 17 by means of lead 26, resistor 27, and leads 28, 29, 31. Input terminal 14 is connected to output terminal 18 by means of lead 32, resistor 33, and leads 34, 35, 36. Input terminal 15 is connected to output terminal 19 by means of lead 37, resistor 38, and leads 39, 41, 42.

Each of the output terminals are separately clamped to a source of reference potential, hereinafter referred to as ground, so that they cannot drop below ground potential. Clamping diode 43 is connected at its anode end to ground and at its cathode end to lead 44 which terminates on lead 24. Clamping diode 45 is connected at its anode end to ground and at its cathode end to lead 46 which terminates on lead 29. Clamping diode 47 is connected at its anode end to ground and at its cathode end to lead 48 which terminates on lead 35. Clamping diode 49 is connected at its anode end to ground and at its cathode end to lead 51 which terminates on lead 41.

A negative bias source is provided to normally block any transfer of positive pulses from the input terminals to the output terminal. The negative bias source not shown is connected to terminal 52'. Resistors 52, 53, 54, 55 are connected at one of their ends to lead 56 which terminates on terminal 52 and at their other ends are connected to leads 25, 31, 36, 42 respectively. As mentioned in the preceding paragraph, each clamping diode prevents its corresponding output terminal from dropping below ground potential regardless of the negative bias applied to terminal 52. The choice of bias voltage and the sizes of the resistor groups 22, 27, 33, 38, and 52, 53, 54, 55 for this apparatus are governed by the pulse amplitude limits anticipated at input terminals 12, 13, 14, 15; the size of the resistors in the latter resistance group and the bias voltage are also governed by the maximum operating current for the clamping diodes 43, 45, 47, 49. With the circuitry thus far described only, if a positive pulse arrives at any one(s) of the input terminals, e.g., input terminal 12, the pulse is blocked from corresponding output terminal 16 by the action of the bias source. The resistors 22 and 52 during that instant function as a voltage divider between terminal 12 and the bias source terminal 52 whereby the above-mentioned positive pulse that appears on terminal 12 is entirely attenuated; in other words the output terminal 16 is not driven positive.

Any pulses arriving at the terminals 12, 13, 14, 15 are coupled also into cathode follower 61. The cathode follower includes a triode 62, a delay line 63 connected to the cathode thereof and terminated by a load resistor 65 connected to ground. The delay introduced by delay line 64 is somewhat in excess of the maximum leading edge jitter among pulses of pulse groups coupled into the input terminals. A decoupling circuit including resistor 64 and condenser 65 and lead 66 connects the plate of triode 62 to plate supply terminal 67; the plate supply connected to terminal 67 is not shown on the drawing. The grid circuit includes a resistive voltage divider having resistors 68 and 69; one end of resistor 68 is connected to ground and the grid of triode 62 is connected to the junction of the resistors 68 and 69 by means of a connecting lead 71. The other end of resistor 69 is connected to all the input terminals by means of diodes 72, 73, 74, 75 that serve to prevent cross coupling. When a plurality of substantially coincident positive rectangular pulses of substantially equal length arrive at respective ones of the input terminals and the leading edges of the plurality of pulses are not in time coincidence, the cathode follower will respond to the first leading edge among the pulses and a corresponding leading edge will appear across the load resistor 65 after the delay introduced by the delay line 63 which delay exceeds the jitter or maximum time spread among the leading edges of the plurality of pulses. In this portion of the circuit only the first leading edge is of importance; the succeeding leading edges of the other pulses of the plurality introduced have no effect on operation of the circuit. The first leading edge serves to trigger a pulse generator.

Pulse generator 77 which is in the form of a blocking oscillator, is coupled to cathode follower 63 by means of coupling condenser 78. The pulse generator includes triodes 81 and 82. The cathode of triode 81 is connected directly to ground while triode 82 is connected as a cathode follower having a cathode resistor 83 terminating at ground. The plate supply is connected to triodes 81 and 82 by means of a decoupling circuit having a resistor 84 and condenser 85, lead 86, the primary of pulse transformer 87 and lead 88. Each triode

81 and 82 is normally cut off by a negative bias on the grid. The grid of triode 81 is connected to the junction of a voltage divider having resistors 91 and 92 connected between ground and the negative bias source at terminal 52. The grid bias circuit for the triode 82 includes a voltage divider having resistors 93 and 94 connected between ground and the negative bias source at terminal 52; the grid of triode 82 is connected to the junction between resistors 93 and 94 by means of grid current limiting resistor 95 and resistor 96 that bridges the secondary of pulse transformer 87. This type of pulse generator is desirable for this purpose because it has substantially no inherent delay and the edges of pulses generator thereby are very steep.

Normally the cathode end of resistor 83 is at ground potential. However, when the first leading edge of a group of several pulses that are coupled into the input terminals, is coupled into the pulse generator 78, a positive pulse is generated at the cathode of triode 82. The width of the pulses generated thereby are comparable to the pulse width of the input pulses.

Resistors 101, 102, 103, 104 are connected in common at one of their ends and connected by lead 105 to the output end of cathode resistor 83. The other ends of resistors 101, 102, 103, 104 are connected to respective ones of the output terminals.

Each pulse generated by pulse generator 77 serves to cancel the pulse blocking bias for the duration thereof so that during the interval that each pulse is generated by said pulse generator 77, the portions of the input pulse(s) coupled into the input terminals that are coincident with the generated pulse, appear at the output terminals; conversely, the initial portions of the input pulses which precede the generated pulse are blocked. Of importance is the fact that there appears at the output terminals, pulses corresponding to the pulses coupled into the input terminals and having no leading edge jitter. By eliminating the jutter, non-erratic reliable results are obtained when the pulses are fed into computer device, or comparison devices that compare a pulse pattern with a stored pulse pattern.

An amplitude limiter is connected to the output terminals. It includes diodes 106, 107, 108, 109 connected in common at their cathode ends to the junction of voltage dividing resistors 111 and 112 that are connected between the plate supply terminal 67 and ground. A bypass condenser is connected across resistor 112. The anode ends of the diodes are connected to respective ones of the output terminals.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may be practiced otherwise than as specifically described.

We claim:

1. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses of substantially equal width where the maximum leading edge jitter among the pulses is a fraction of the pulse width, said apparatus comprising: a plurality of input terminals and a corresponding plurality of output terminals, a plurality of resistors separately connecting said input terminals to respective ones of said output terminals, a bias source of polarity that is opposite to that of the pulses, a plurality of resistors separately connecting said bias source to each of said output terminals respectively, a source of a reference potential that is between the bias potential and the pulse potentials, a plurality of clamping diodes connected between said source of reference potential and each of said output terminals respectively whereby said output terminals are normally at the reference potential and can change from the reference potential only in the polarity direction corresponding to the polarity of the pulses, said bias source normally being effective to block the transfer of pulses from said input to said output terminals by causing them to be attenuated in said resistors connecting said input and output terminals, means for providing a bias cancelling pulse in response to the first leading edge of each plurality of substantially coincident rectangular pulses and of length comparable to the length of said substantially coincident pulses and wherein the leading edge of the bias cancelling pulse trails said first leading edge by an amount somewhat in excess of maximum leading edge jitter, the output end of said pulse providing means connected to each of said output terminals, means to prevent cross coupling connecting the input end of said pulse providing means to each of said input terminals, whereby when several substantially coincident rectangular pulses arrive at said input terminals the pulses are blocked from said output terminals by said bias source until a bias cancelling pulse is generated following which the leading edges of the several pulses arrive at said output terminals in time coincidence.

2. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses as defined in claim 1 wherein said means for providing a bias cancelling pulse includes a delay line and a pulse generator coupled to the output end of said delay line.

3. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses as defined in claim 1 wherein said means for providing a bias cancelling pulse includes a cathode follower type of amplifier for impedance matching and having a delay line terminated by a load resistor in the cathode circuit thereof and a pulse generator coupled to said load resistor.

4. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses as defined in claim 3 wherein said pulse generator is a blocking oscillator having a cathode load resistor across which the bias cancelling pulses are developed.

5. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses as defined in claim 1 further including means providing a potential between said reference potential and the potentials of said substantially coincident rectangular pulses, and a limiter diode connected between each output terminal and said last mentioned means whereby pulses arriving at said output terminals are of equal amplitude.

6. An apparatus for synchronizing the leading edges of a plurality of substantially coincident rectangular pulses that are positive relative to a particular reference potential and are of substantially equal width and the maximum leading edge jitter among the pulses is a fraction of the pulse width, said apparatus comprising: a plurality of input terminals and a corresponding plurality of output terminals, a plurality of resistors separately connecting said input terminals to respective ones of said output terminals, a source of said reference potential, a plurality of clamping diodes separately connecting said source of reference potential to each of said output terminals respectively whereby said output terminals are normally at the reference potential and can change only in a positive direction relative to said reference potential, a source of bias that is negative relative to said reference potential, a plurality of resistors separately connecting said bias source to each of said output terminals respectively, said bias source being effective normally to block the transfer of positive pulses from said input to said output terminals by causing them to be attenuated in the resistors connecting said input and output terminals, a cathode follower having in its cathode circuit a delay line terminating in a load resistance, said delay line characterized by a delay in excess of maximum leading edge jitter, a plurality of diodes separately connecting each of said input terminals to the grid circuit of said cathode follower and preventing cross coupling among

said input terminals, a normally cutoff blocking oscillator connected as a cathode follower and coupled at its input end to the load resistor terminating said delay line, said blocking oscillator generating one pulse each time it is triggered, the generated pulse width being comparable to the pulse width of pulses anticipated at said input terminals and of sufficient amplitude to balance out the effect of said bias source, a plurality of resistors separately connecting the output of said blocking oscillator to each of said output terminals respectively, a source of positive potential, and a plurality of amplitude limiting diodes separately connecting each of said output terminals respectively to said source of positive potential whereby pulses arriving at said output terminals are of equal amplitude; whereby when several substantially

coincident rectangular pulses arrive at said input terminals the pulses are blocked from said output terminals by said bias source until a bias cancelling pulse is generated by said pulse generator following which the leading edges of the several pulses arrive at said output terminals in time coincidence.

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