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(19) **United States**(12) **Patent Application Publication****Han et al.**(10) **Pub. No.: US 2005/0003669 A1**(43) **Pub. Date:****Jan. 6, 2005**(54) **HF VAPOR PHASE CLEANING AND OXIDE ETCHING**

(60) Provisional application No. 60/118,937, filed on Feb. 5, 1999.

(75) Inventors: **Yong-Pil Han**, Seoul (KR); **Herbert H. Sawin**, Chestnut Hill, MA (US)**Publication Classification**(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/302**; H01L 21/461(52) **U.S. Cl.** ..... **438/691**

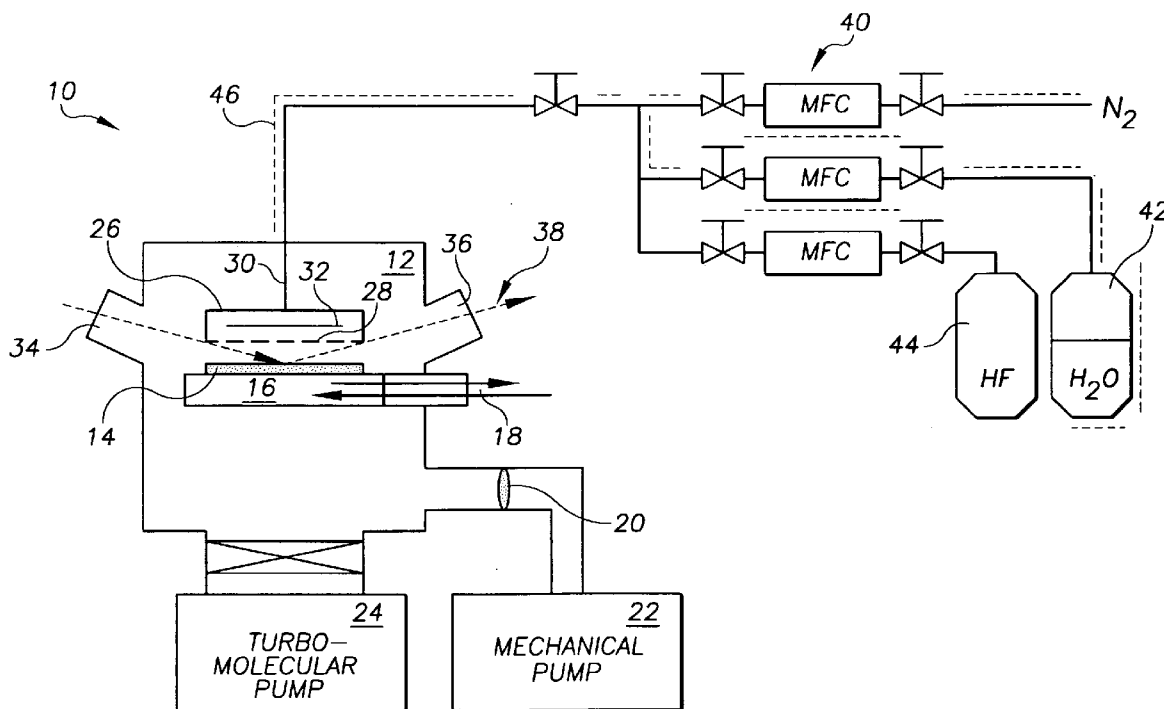
Correspondence Address:

**Theresa A. Lober****T. A. Lober Patent Services****45 Walden Street****Concord, MA 01742 (US)**(73) Assignee: **Massachusetts Institute of Technology**, Cambridge, MA(21) Appl. No.: **10/850,693**(22) Filed: **May 21, 2004****Related U.S. Application Data**

(63) Continuation of application No. 09/498,303, filed on Feb. 4, 2000, now Pat. No. 6,740,247.

(57) **ABSTRACT**

HF vapor processes are provided for etching oxide on a semiconductor substrate, cleaning a substrate, or cleaning a metal structure on a substrate. In the processes, a semiconductor substrate to be cleaned or having oxide to be etched is exposed to anhydrous hydrofluoric acid vapor and water vapor at a substrate temperature greater than about 40° C. Control of substrate temperature, hydrofluoric acid vapor pressure and water vapor pressure inhibits formation of liquid on the substrate and forms on the substrate a sub-monolayer of etch reactant and product molecules by adsorption of etch reactant and product molecules at less than about 95% of oxide adsorption sites.



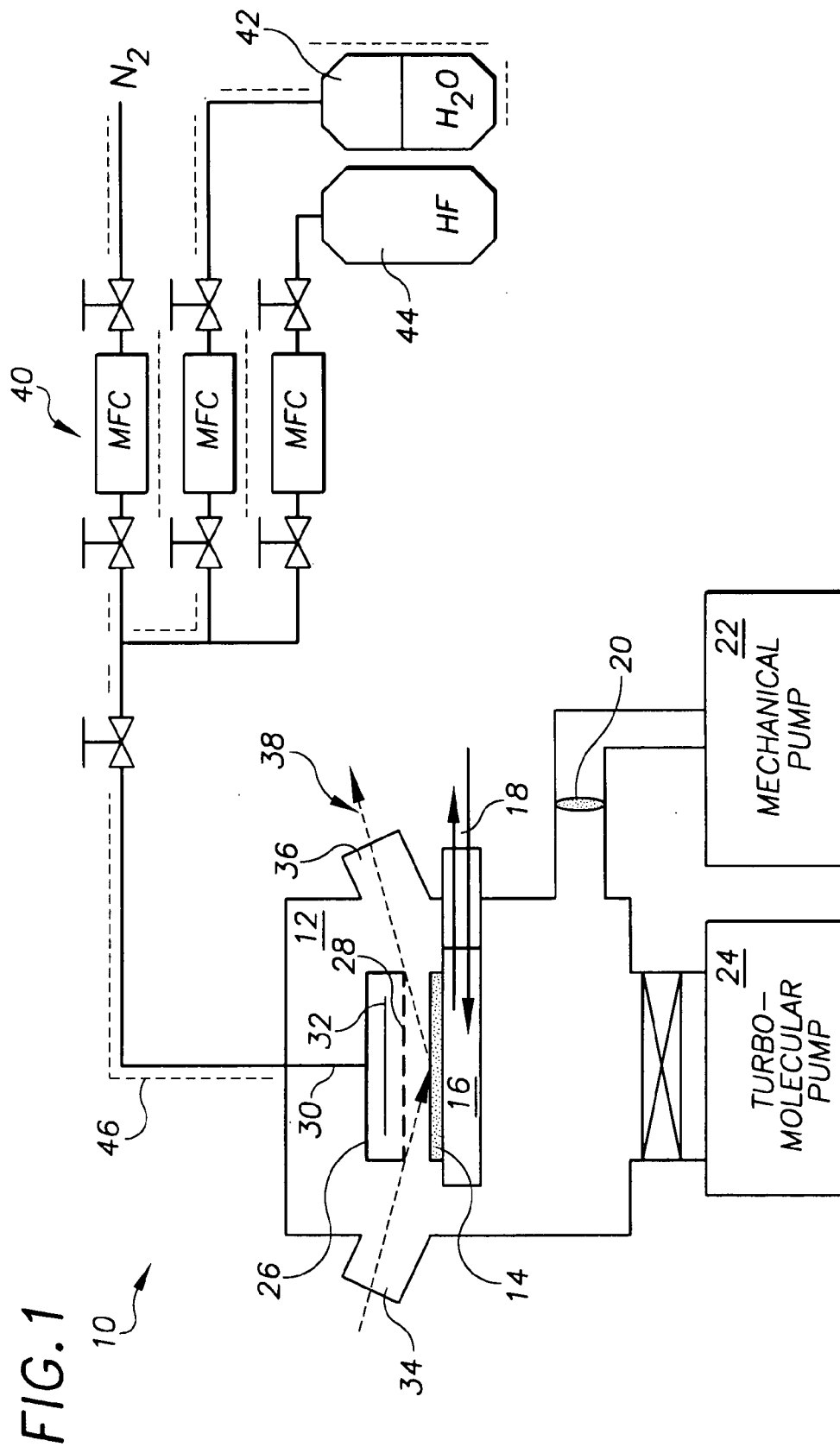
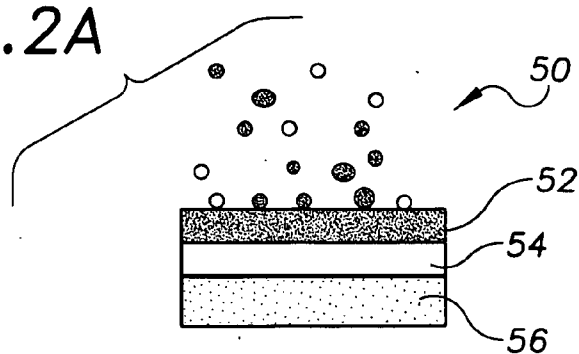
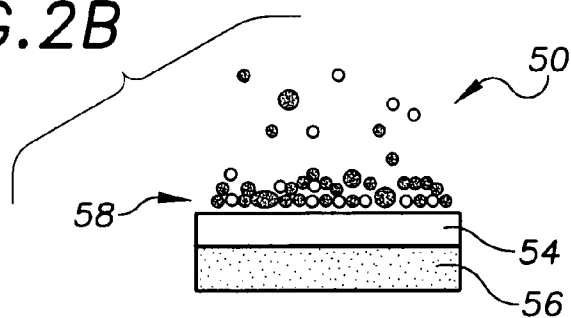


FIG. 2A



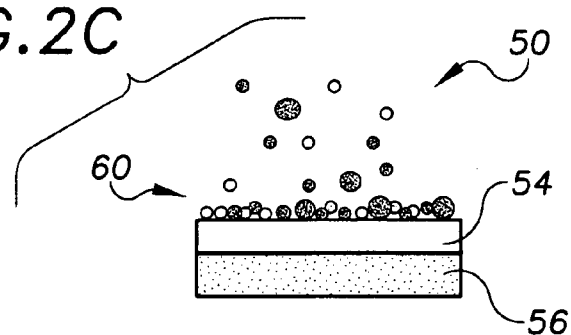
● REACTANTS  
○ PRODUCTS

FIG. 2B



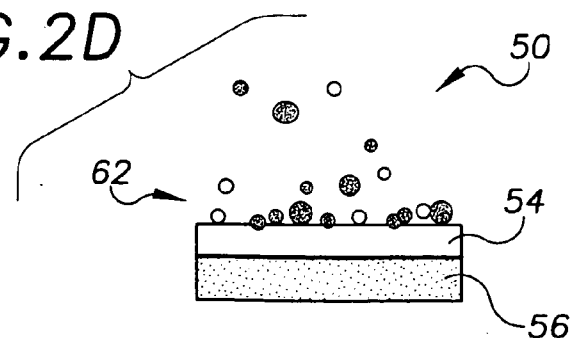
● REACTANTS  
○ PRODUCTS

FIG. 2C



● REACTANTS  
○ PRODUCTS

FIG. 2D



● REACTANTS  
○ PRODUCTS

FIG. 3A

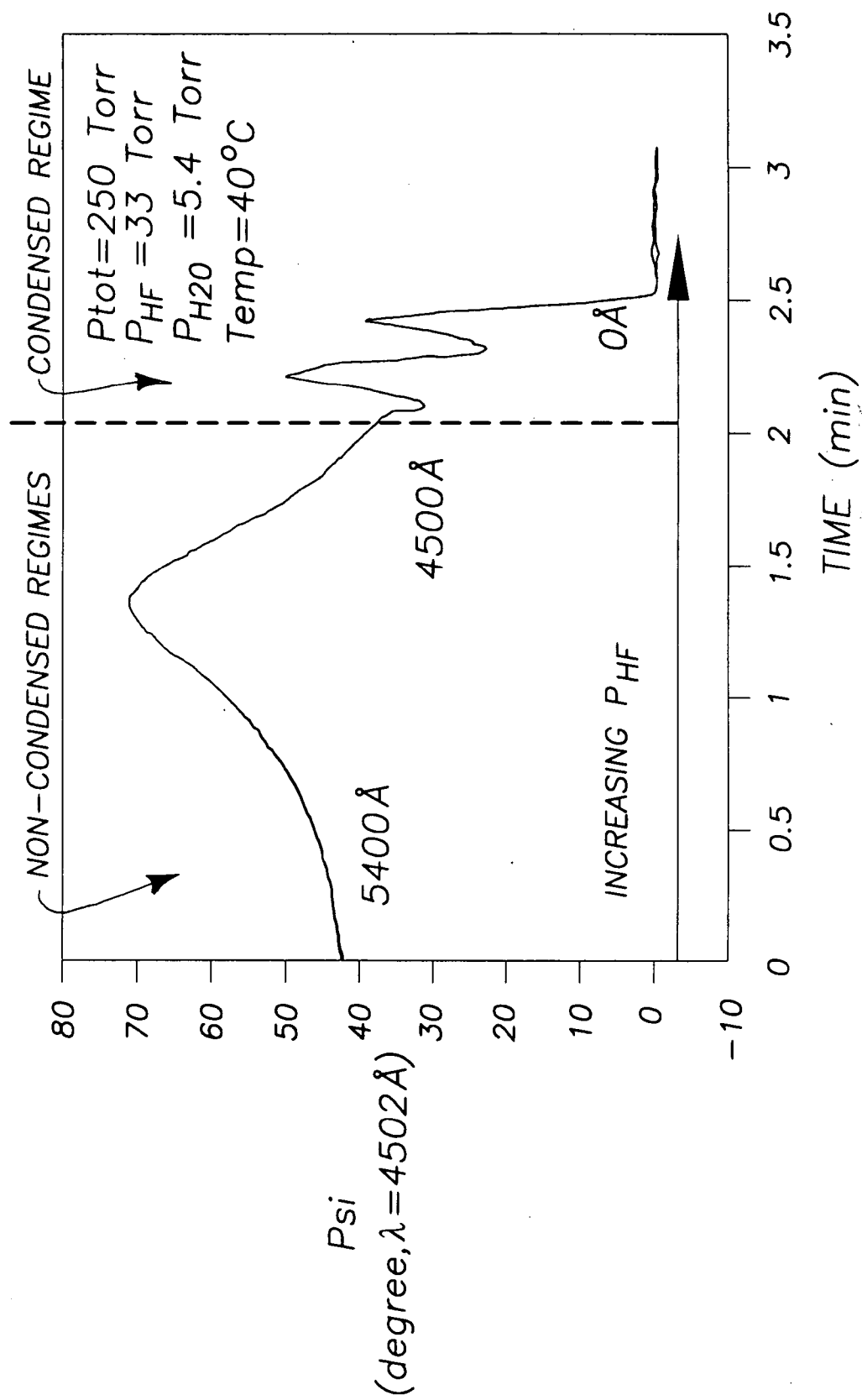


FIG. 3B

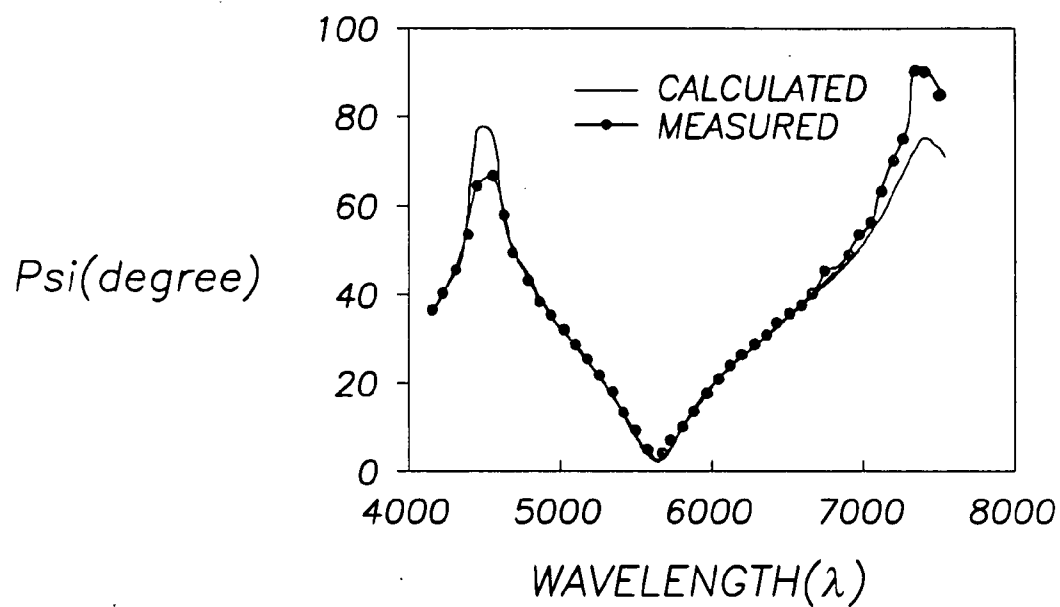


FIG. 3C

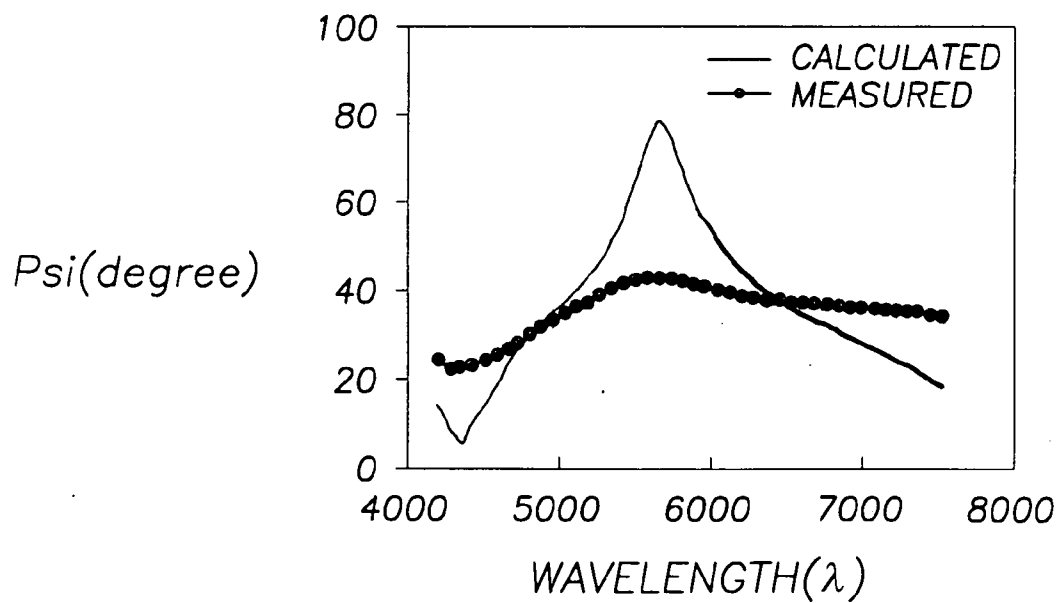


FIG. 4A

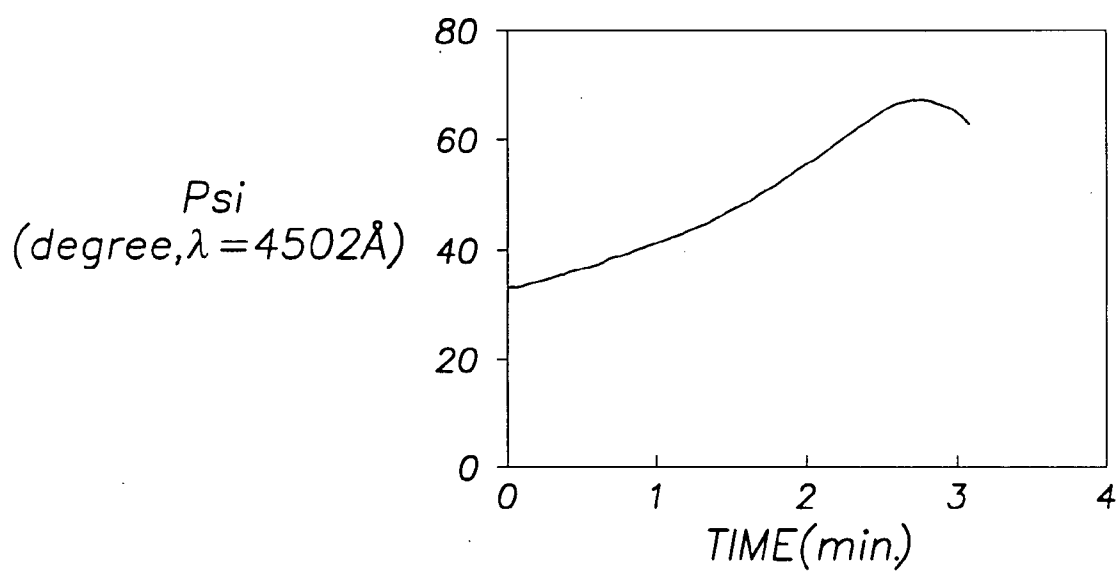


FIG. 4B

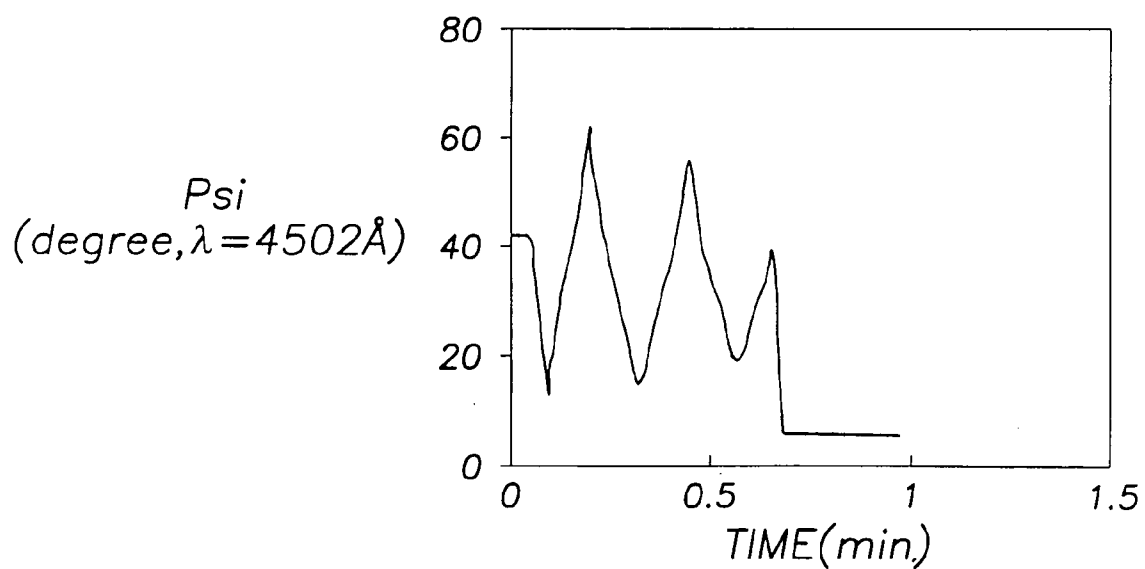


FIG. 5

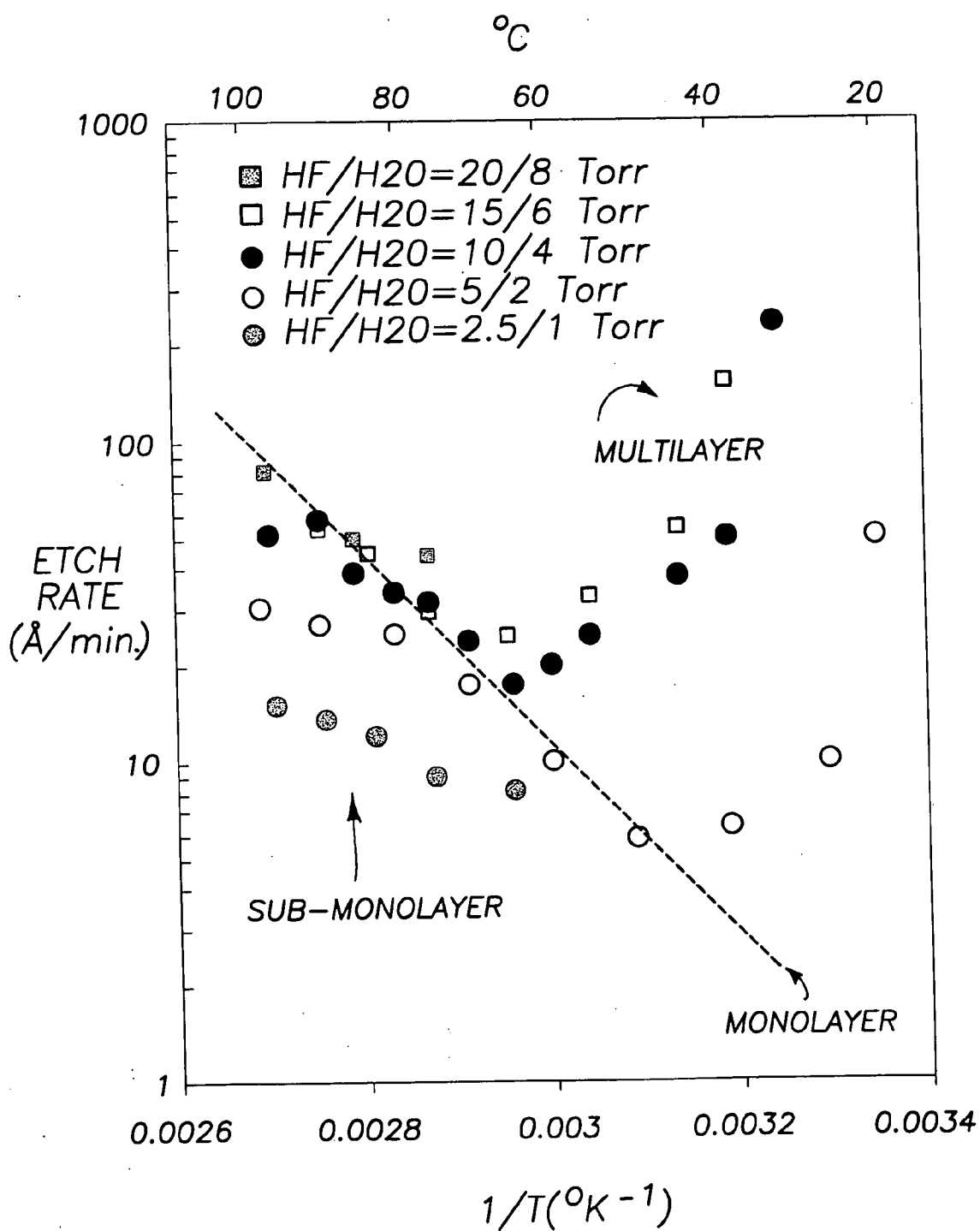


FIG. 6

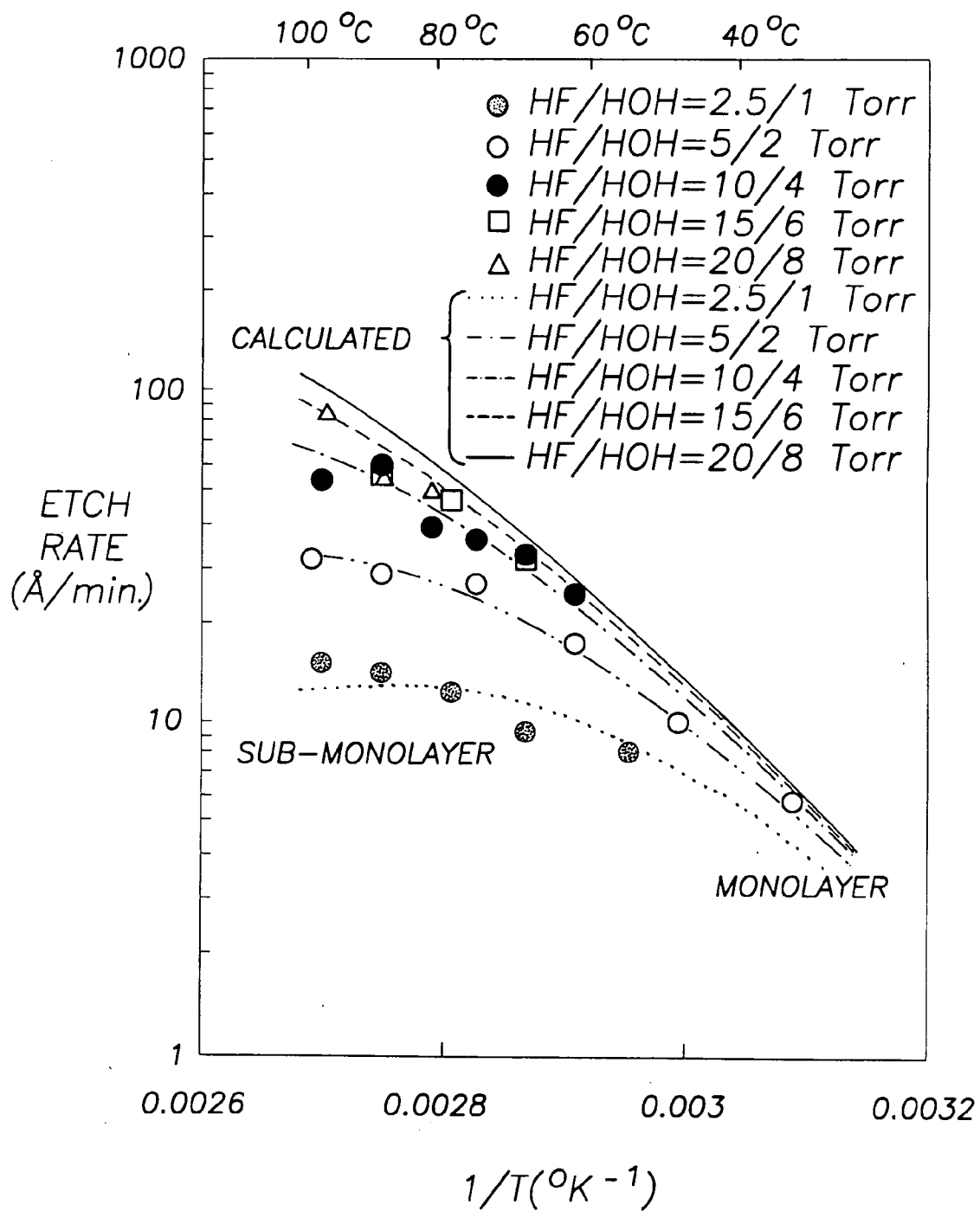


FIG. 7A

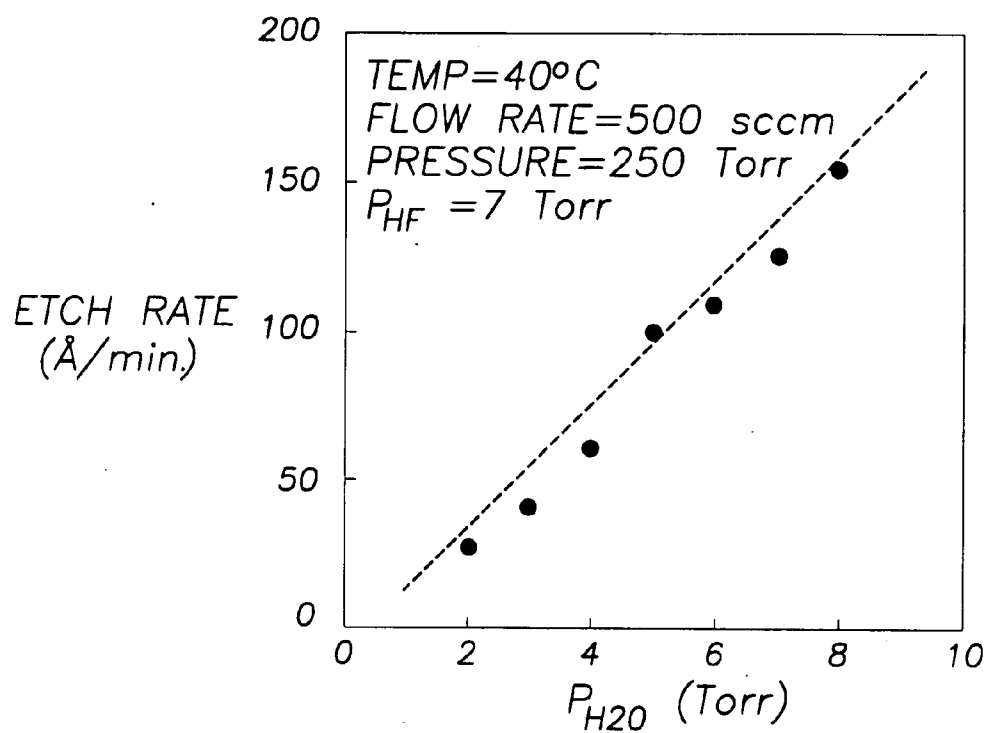
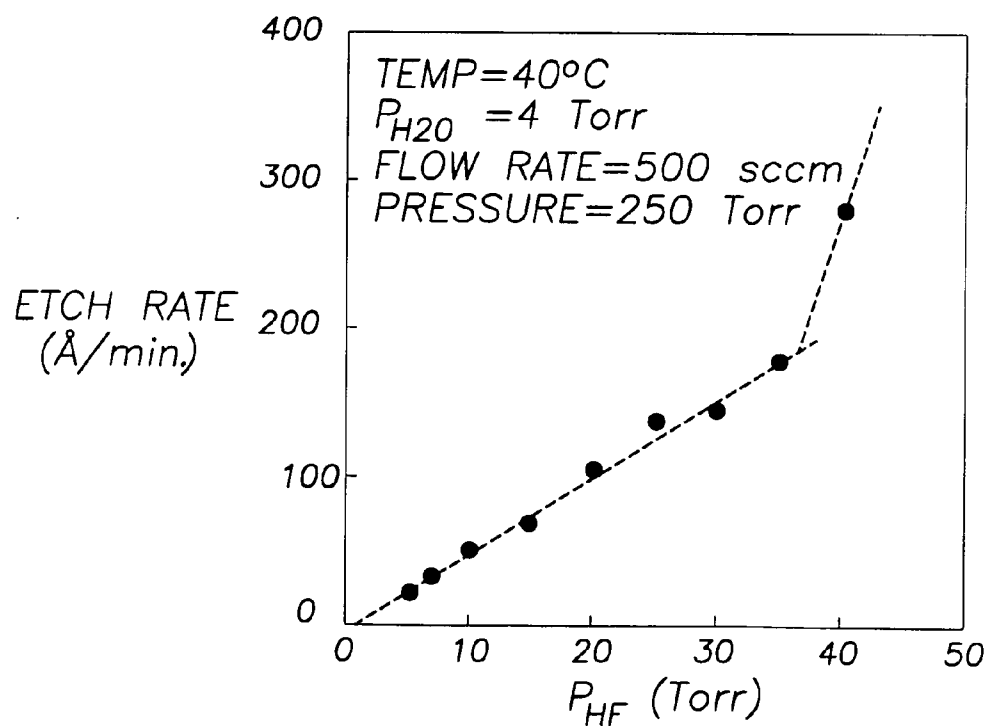
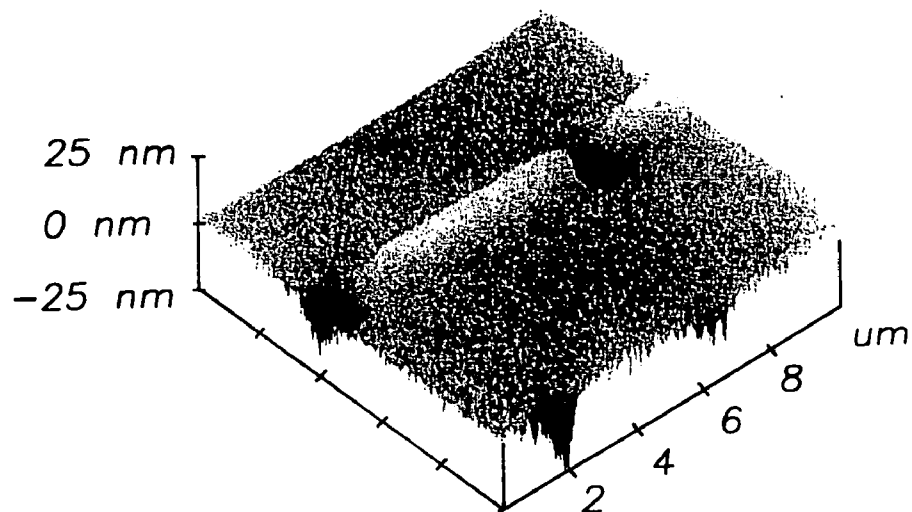


FIG. 7B



*FIG. 8A*



*FIG. 8B*

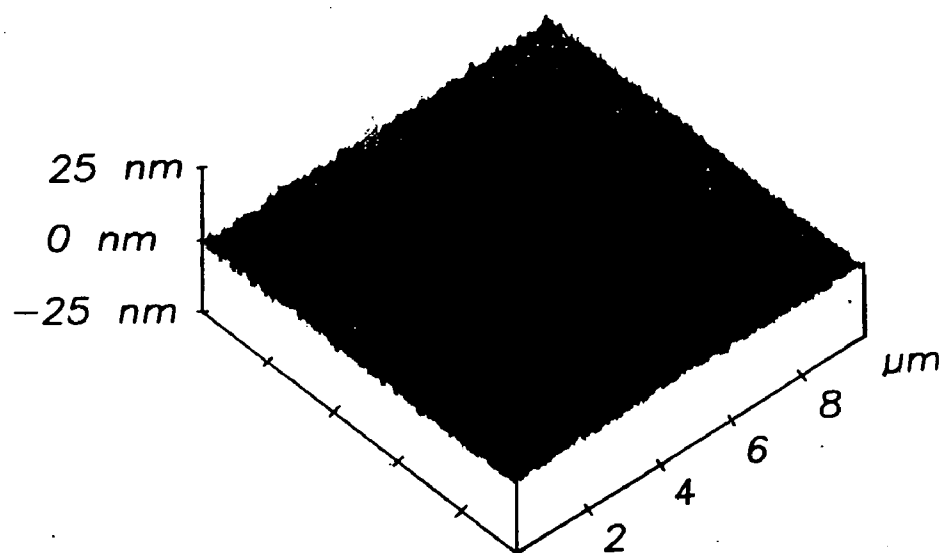


FIG. 9A

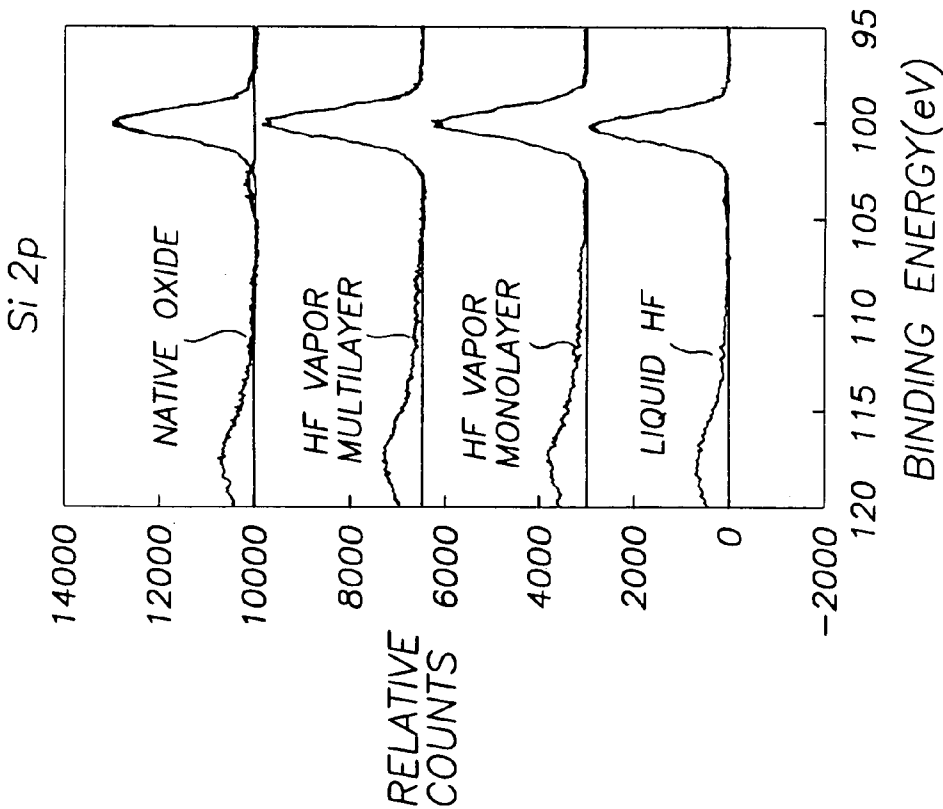


FIG. 9B

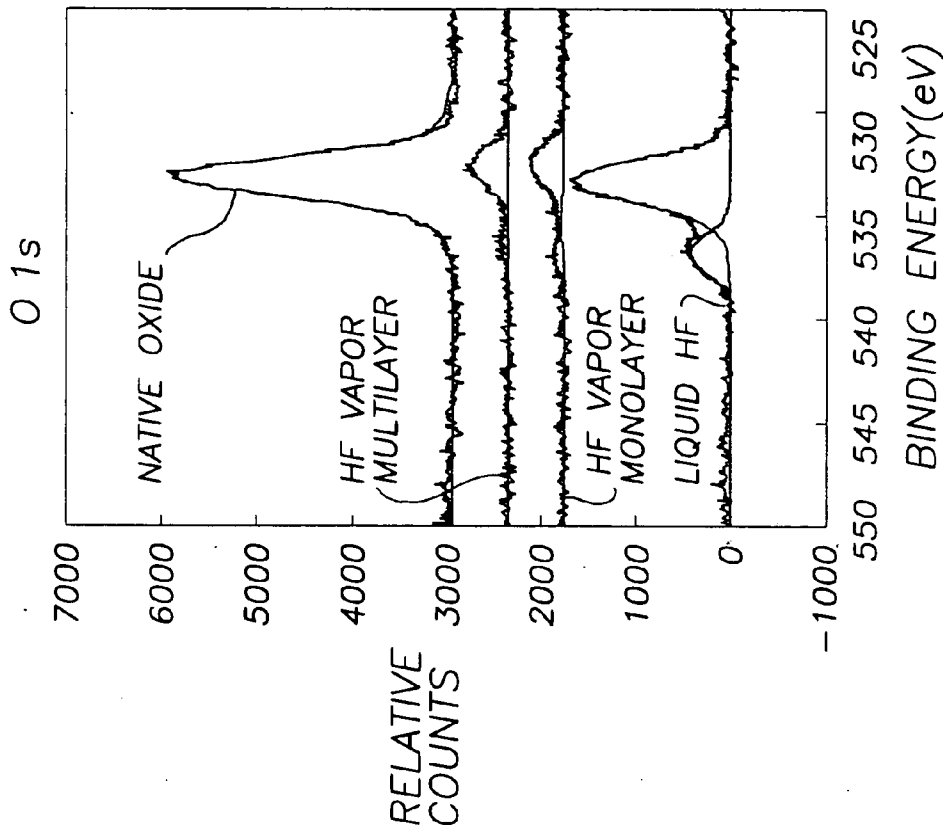


FIG. 9C

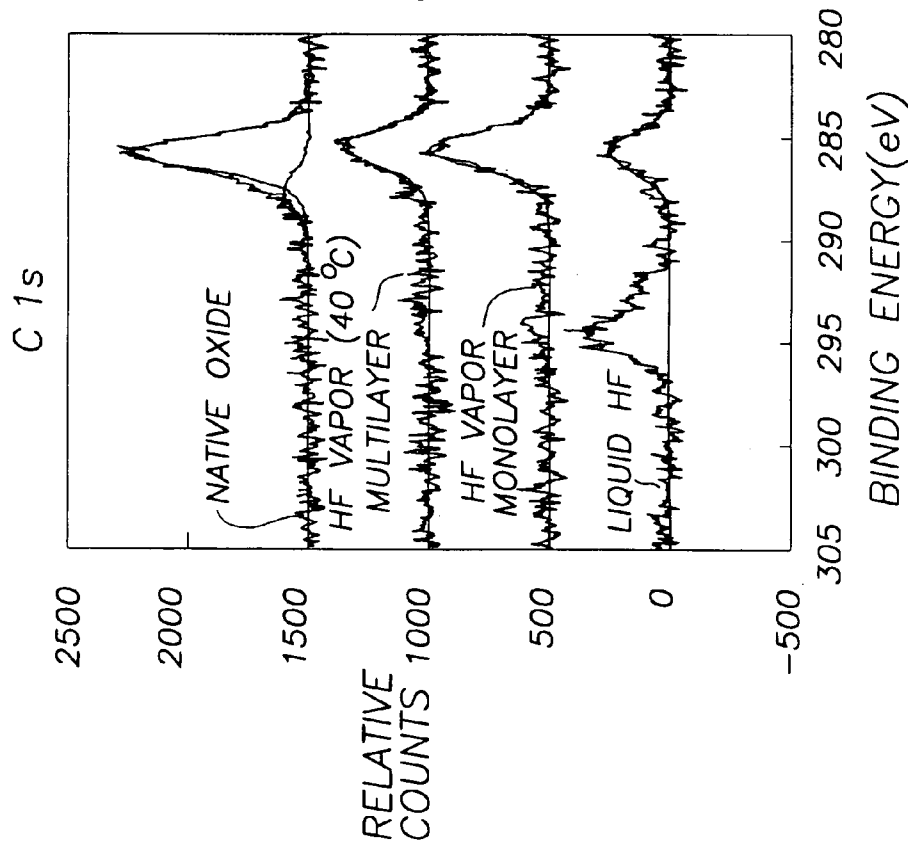


FIG. 9D

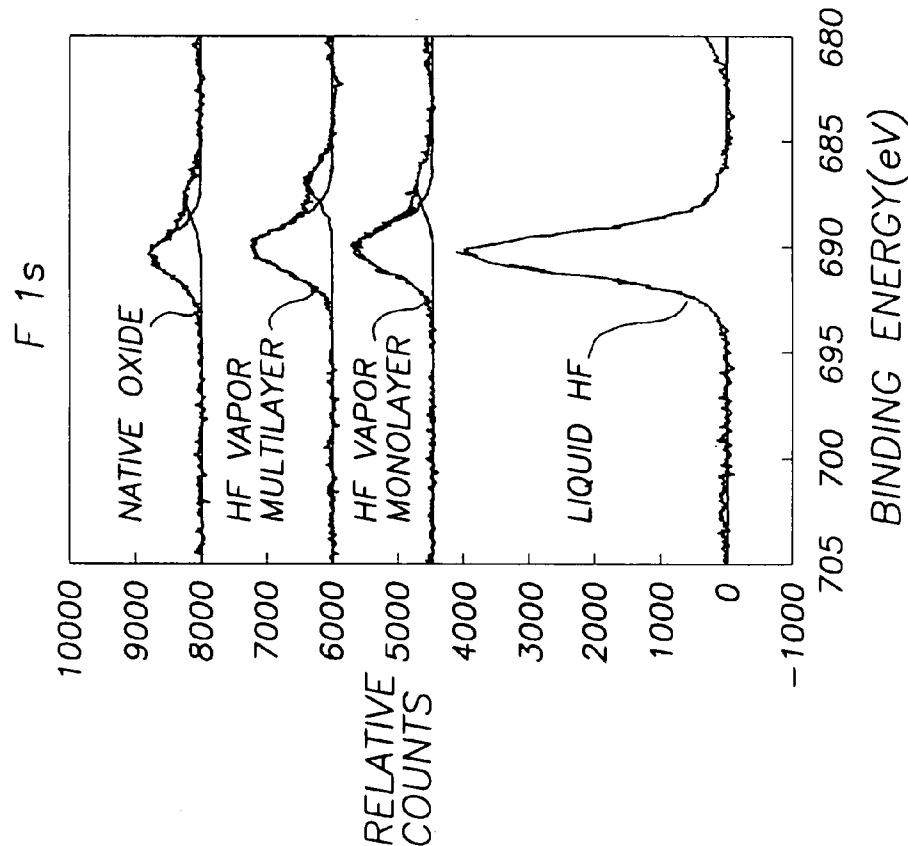
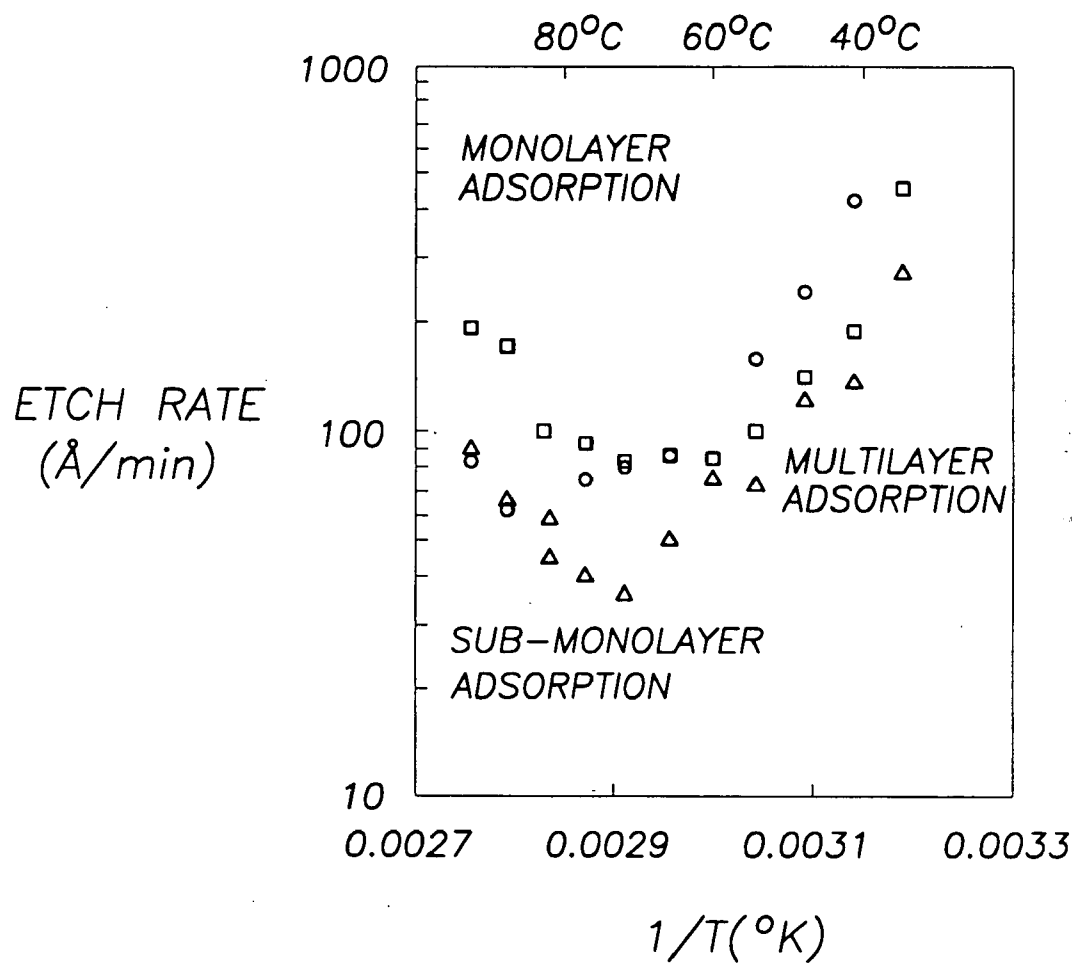


FIG. 10



Δ HF/H<sub>2</sub>O=5/4 TORR  
□ HF/H<sub>2</sub>O=10/4 TORR  
○ HF/H<sub>2</sub>O=10/8 TORR

FIG. 11A

$\psi(^{\circ})$  AT 4052Å

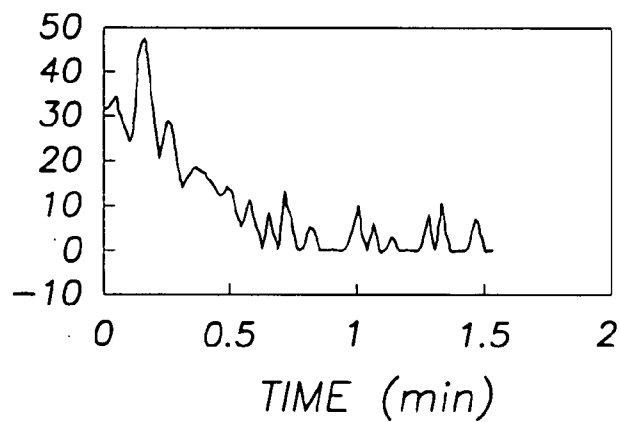


FIG. 11B

$\psi(^{\circ})$  AT 4052Å

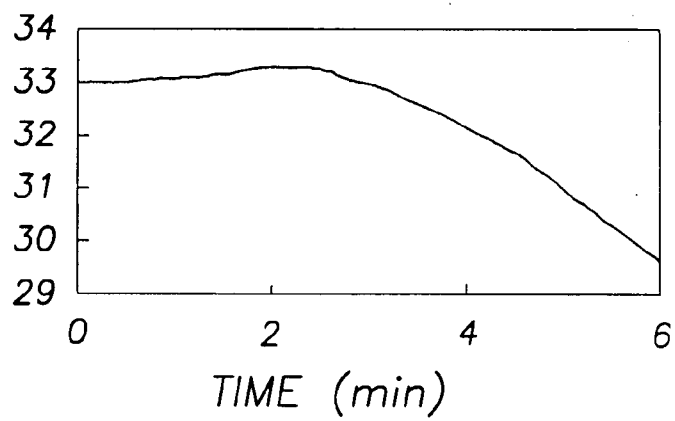
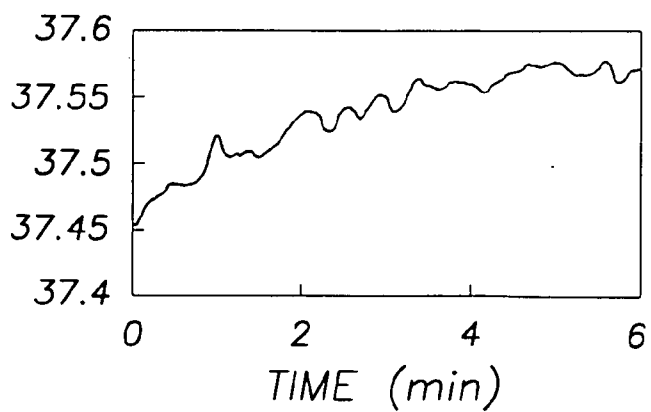


FIG. 11C

$\psi(^{\circ})$  AT 4052Å



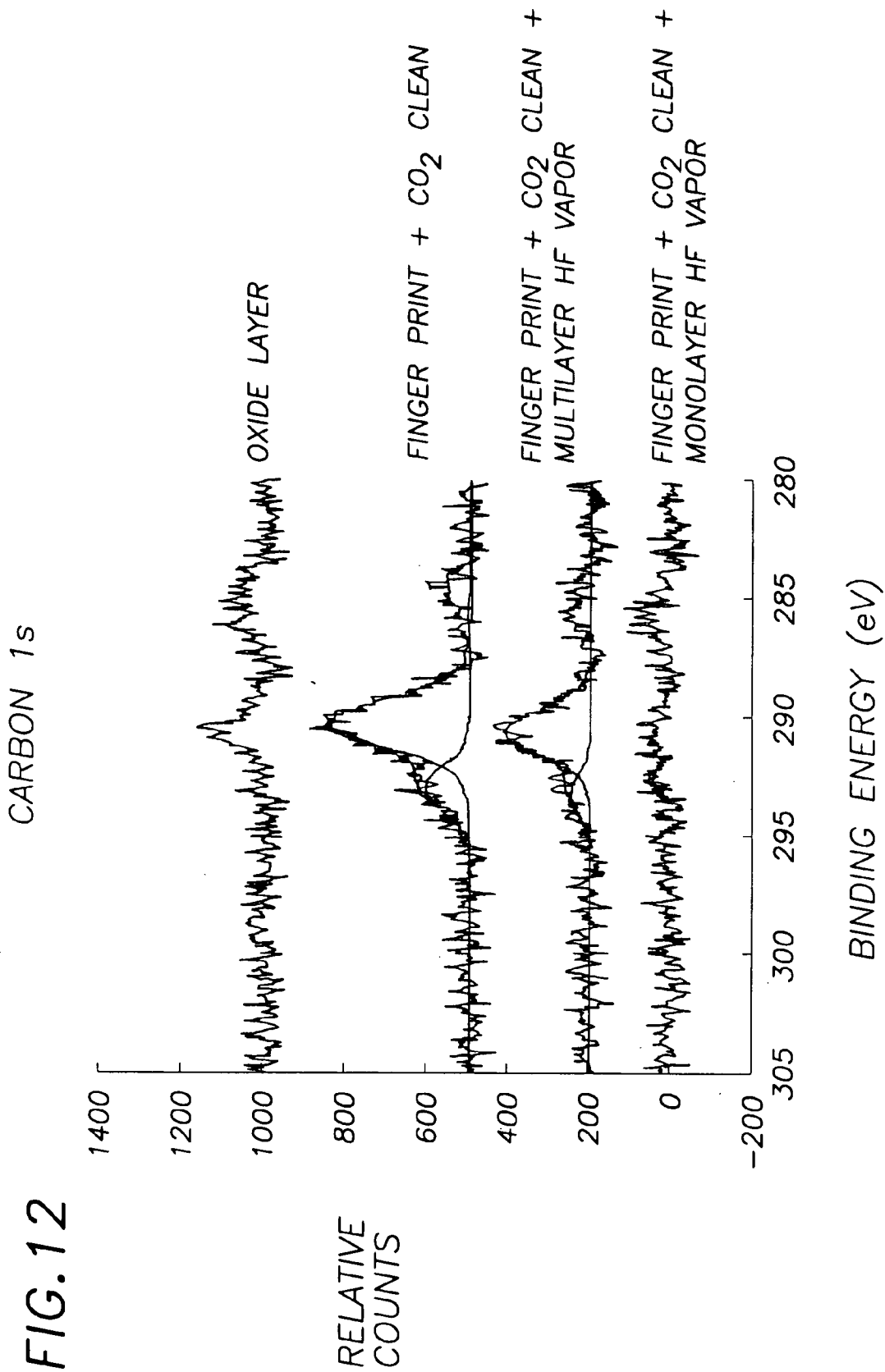


FIG.13

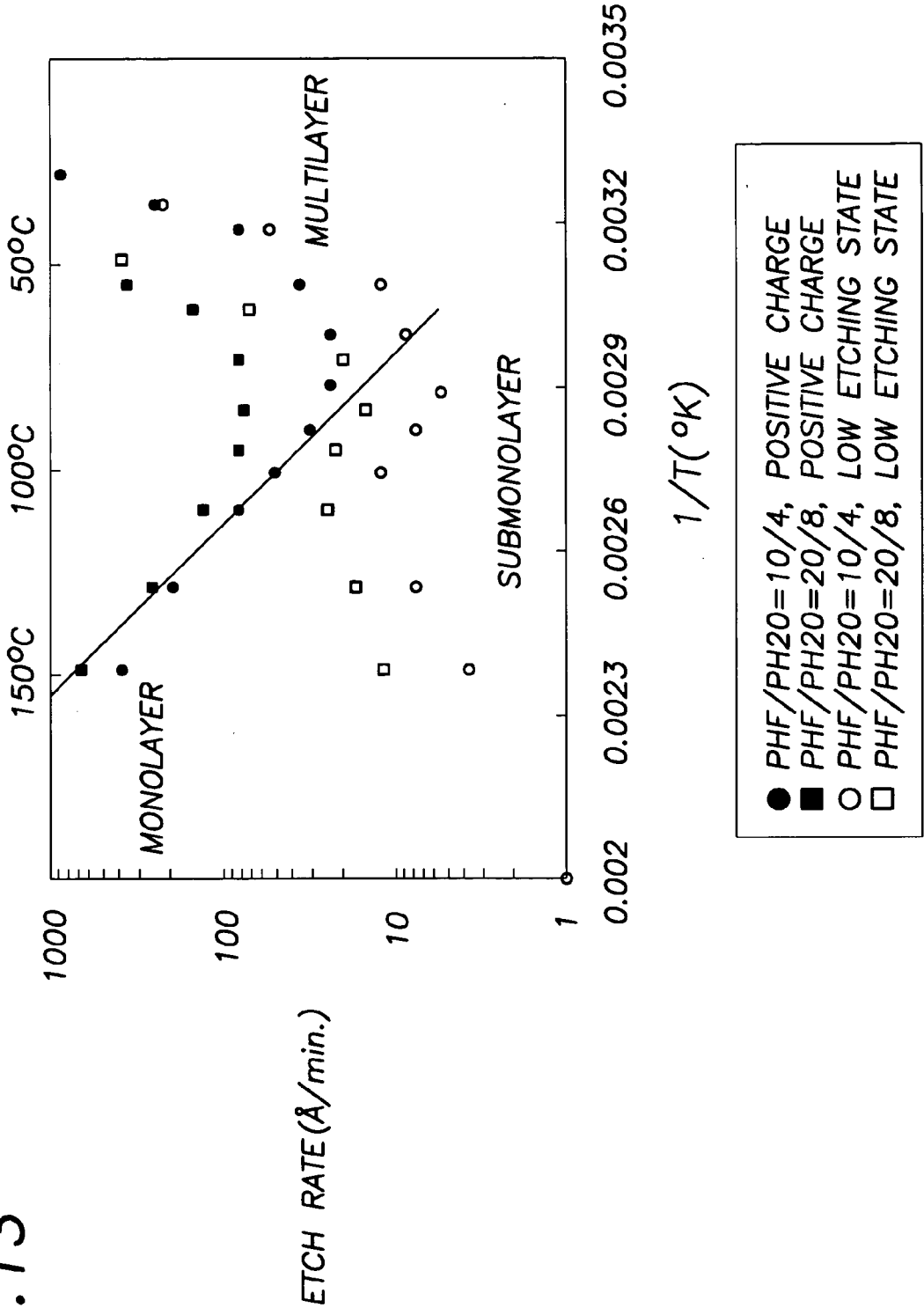


FIG. 14A

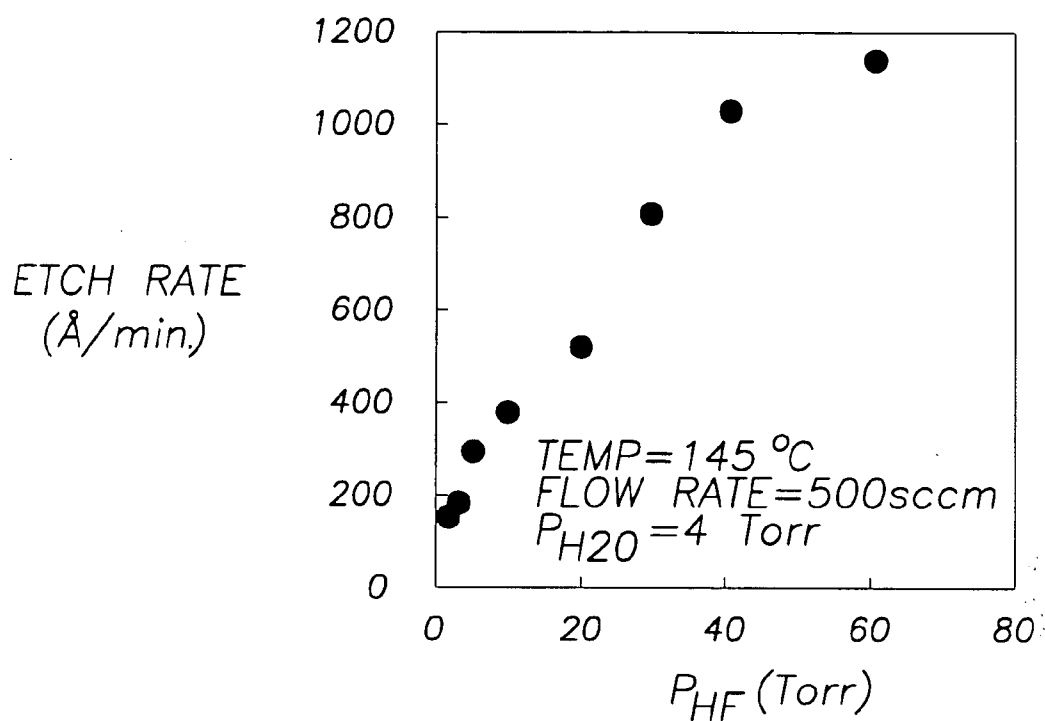


FIG. 14B

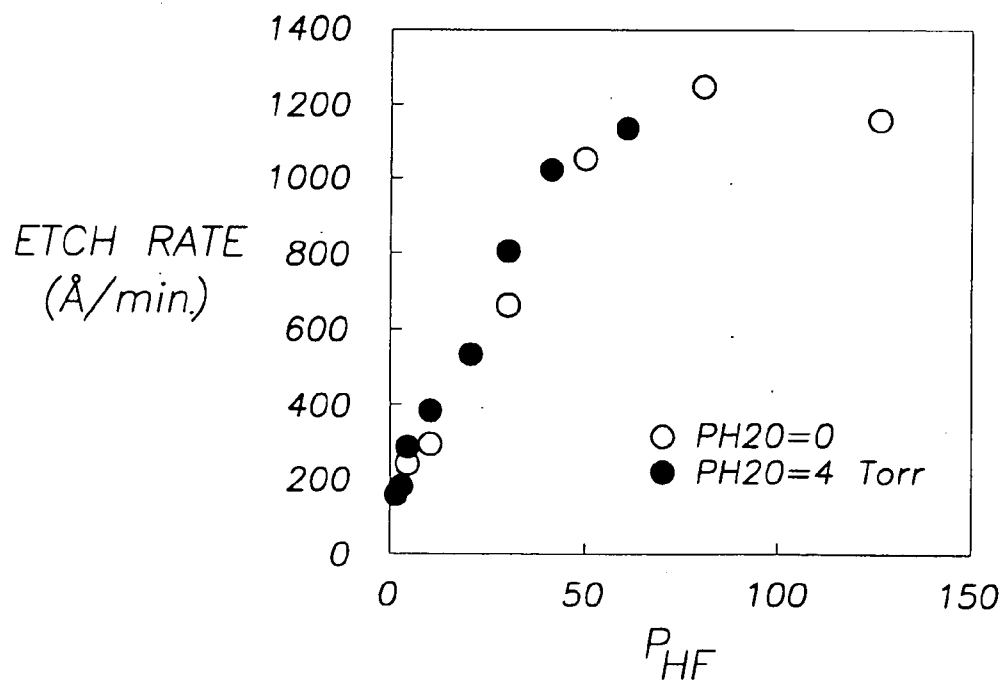


FIG. 15

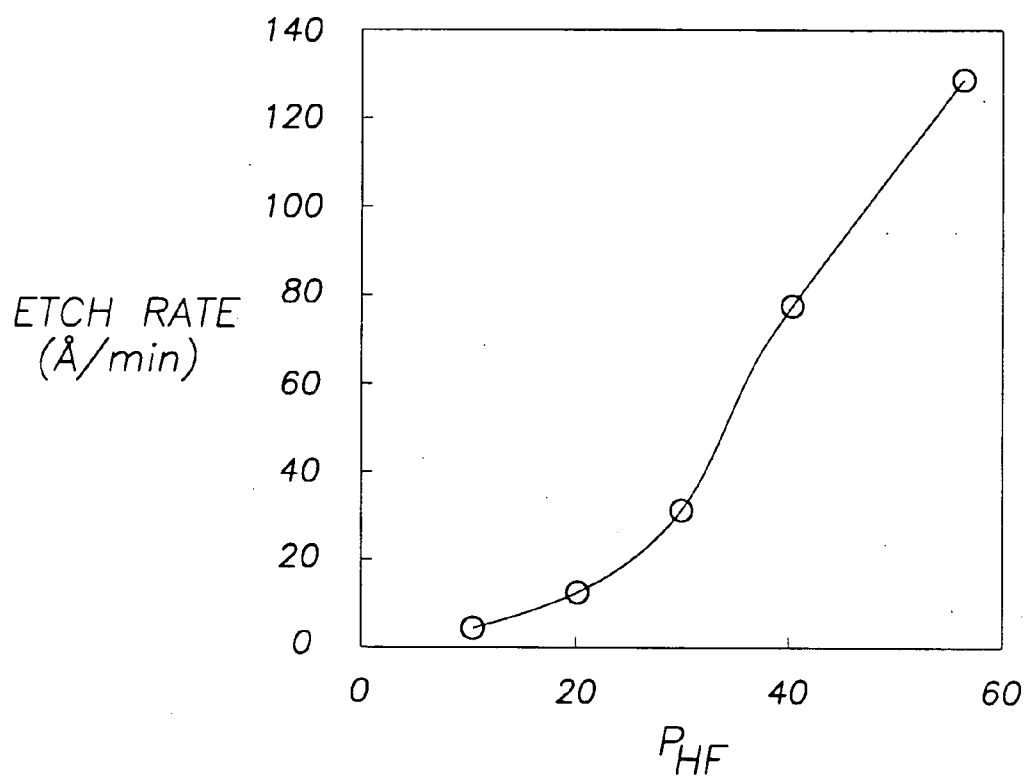


FIG. 16

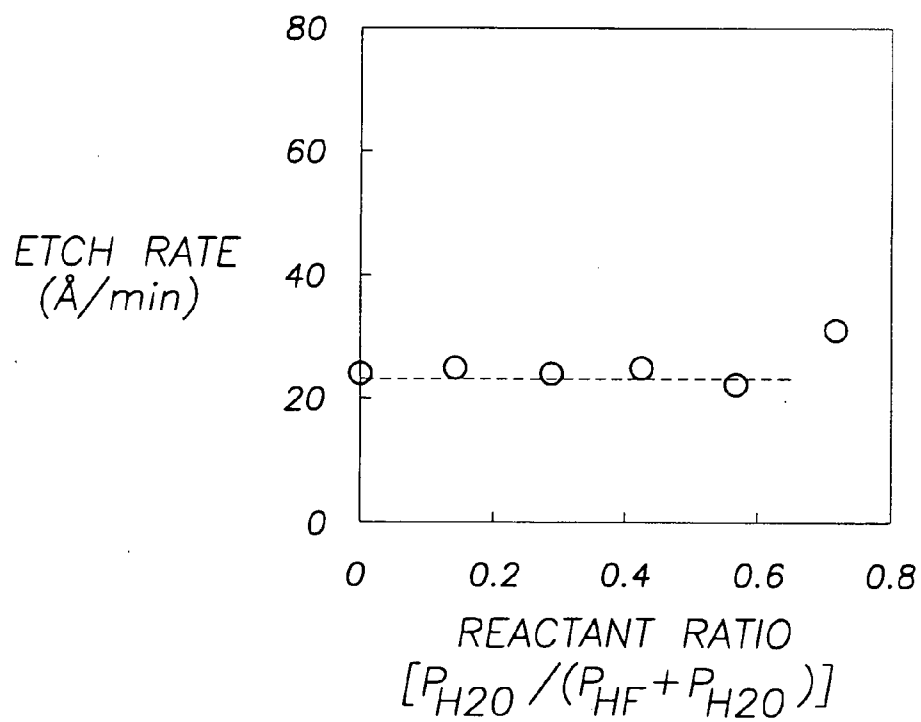
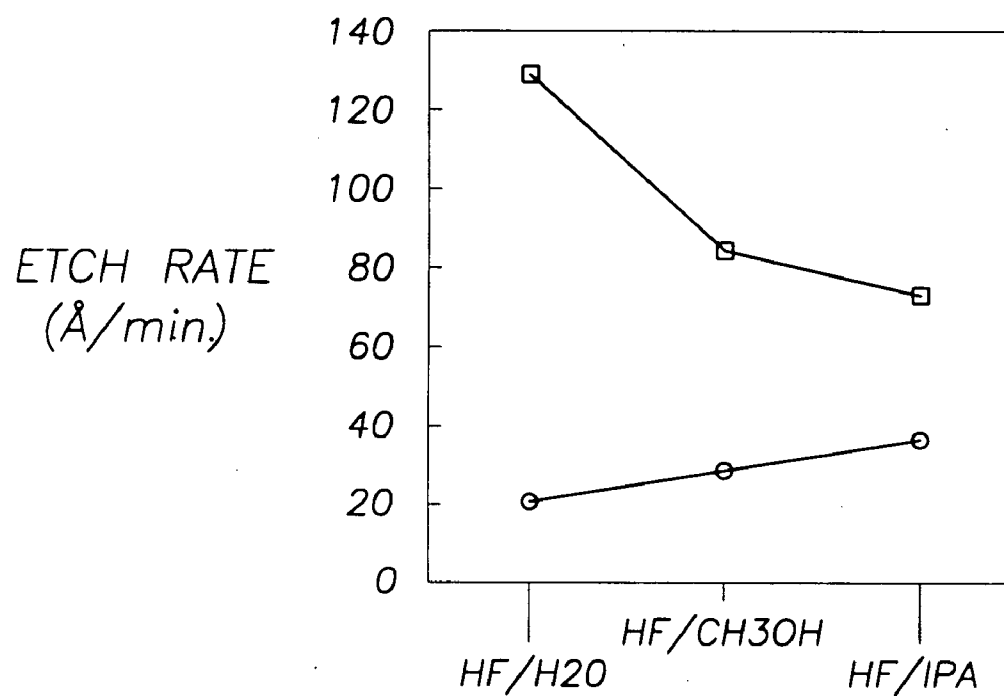
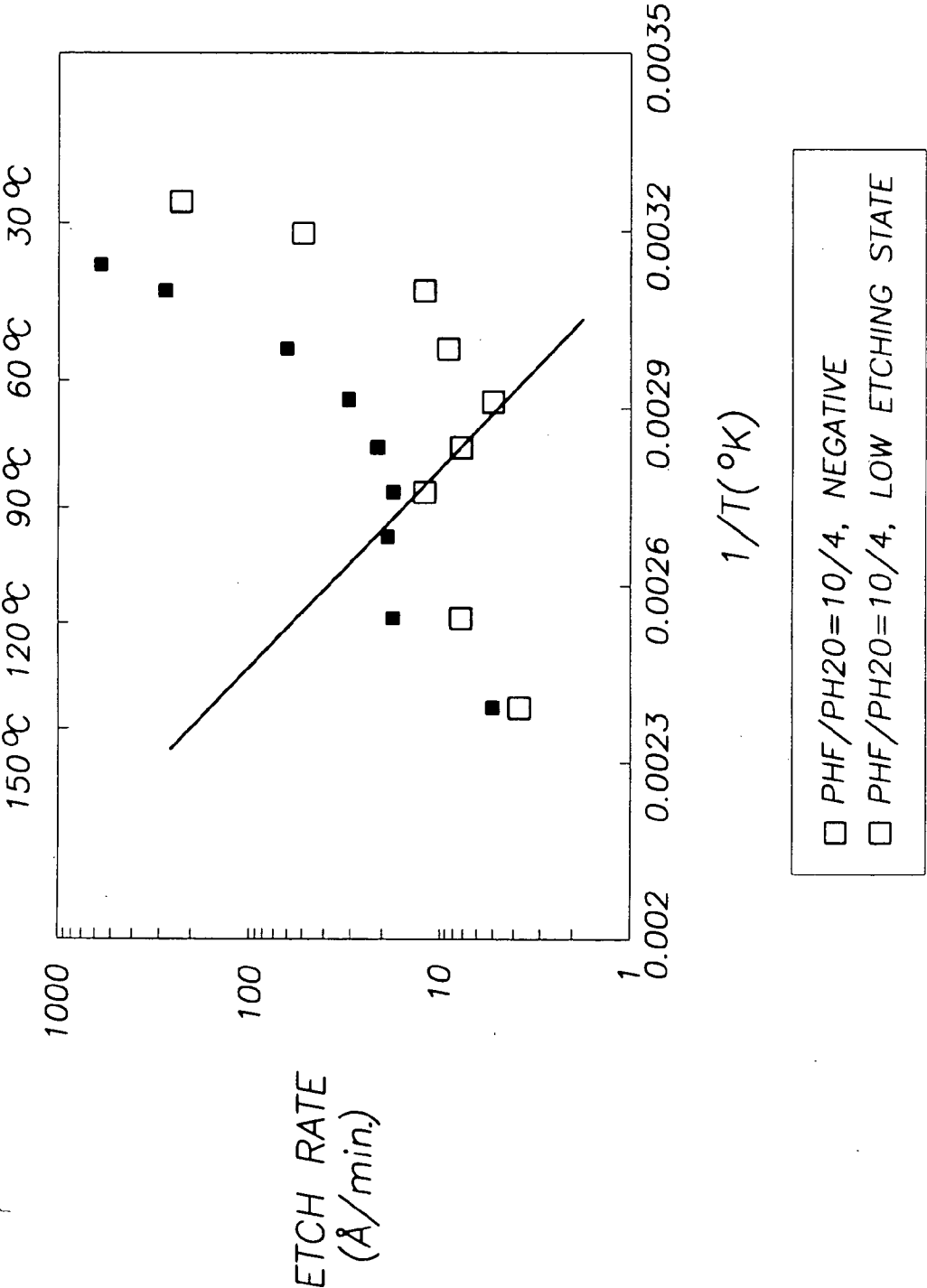


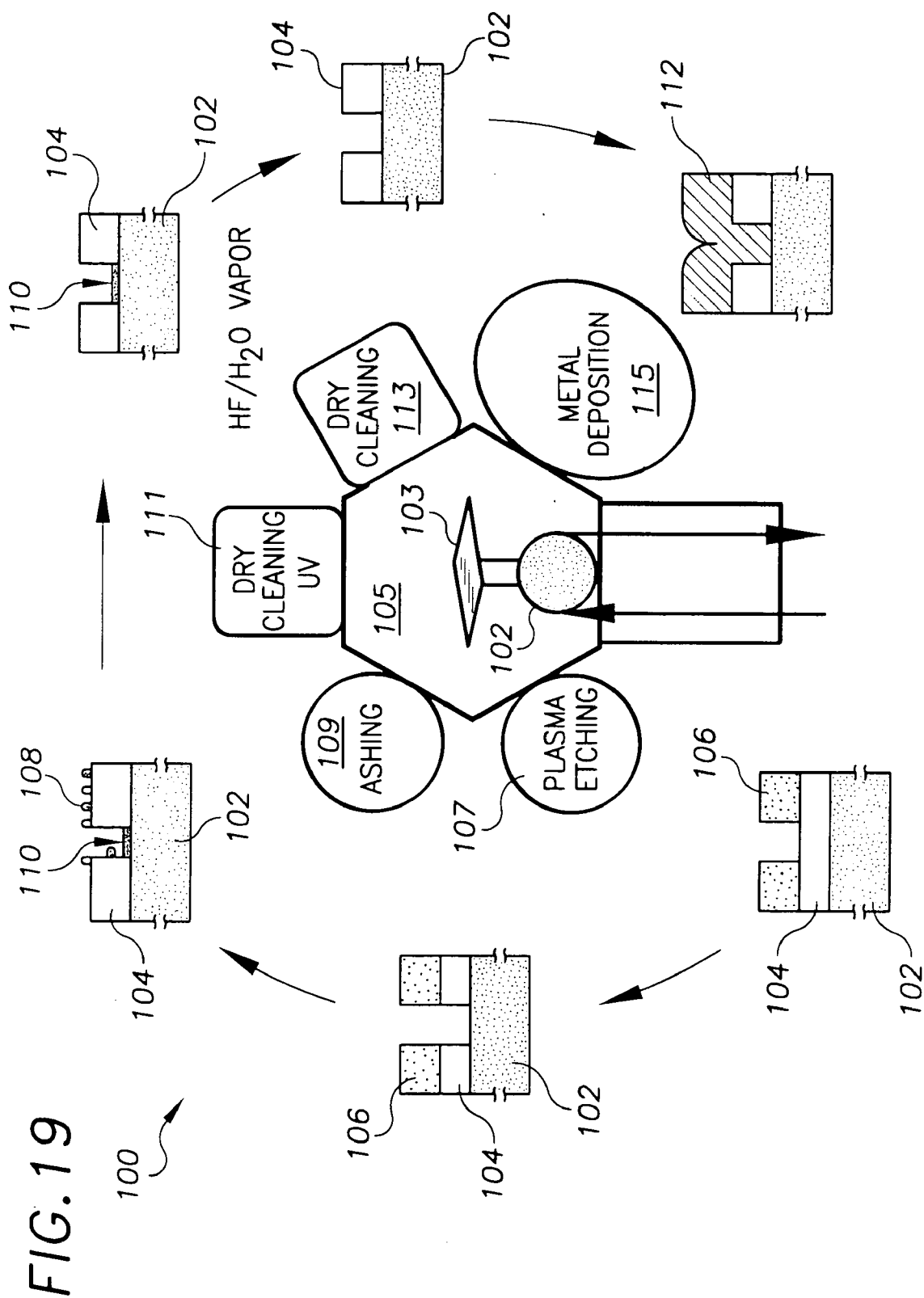
FIG. 17

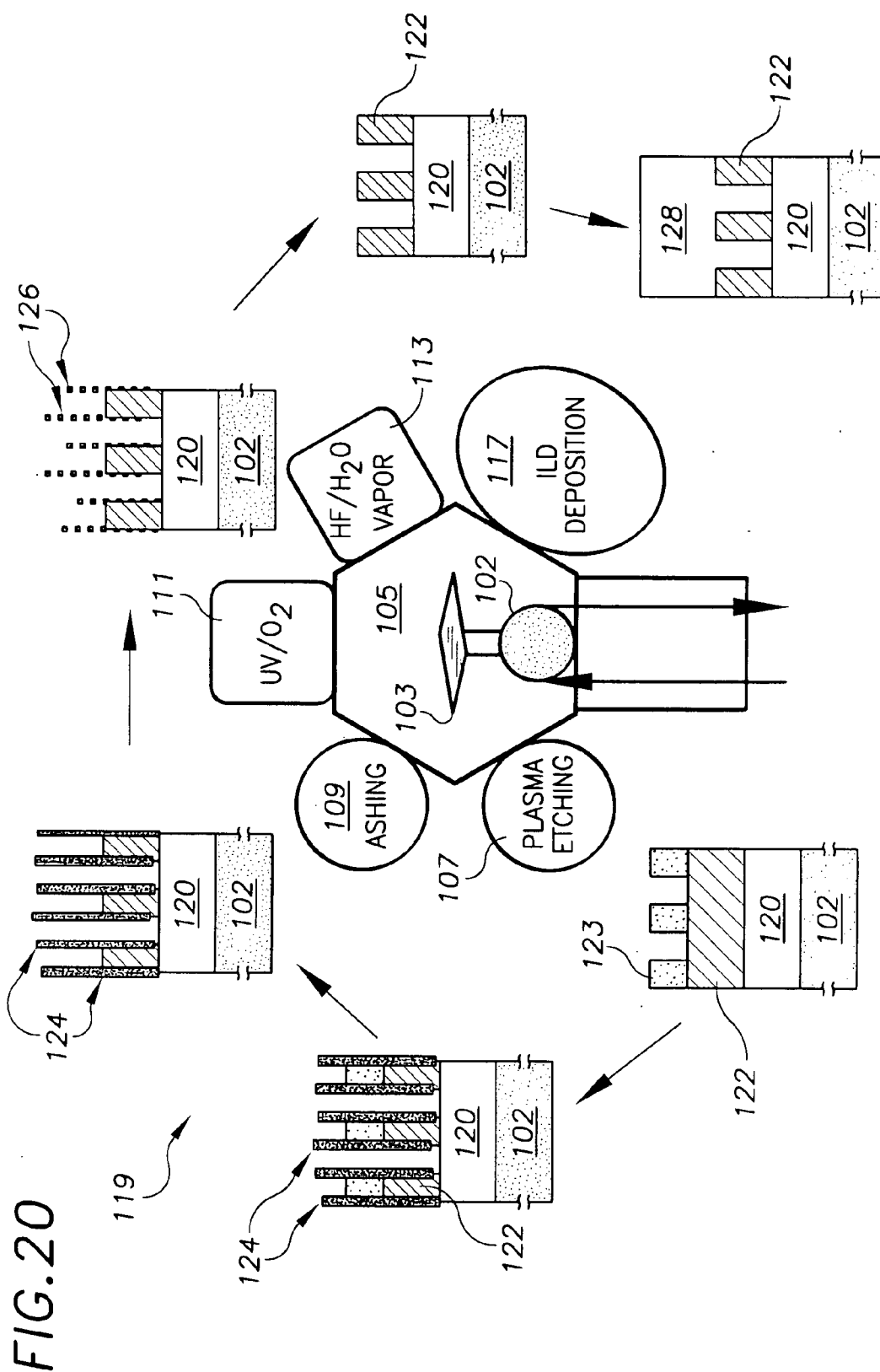


—○— NON-ACTIVATED ETCHING STATE  
—□— ACTIVATED ETCHING STATE

FIG. 18







## HF VAPOR PHASE CLEANING AND OXIDE ETCHING

[0001] This application is a continuation of prior copending U.S. nonprovisional application Ser. No. 09/498,303, filed Feb. 4, 2000, the entirety of which is incorporated by reference, which claims the benefit of U.S. provisional Application No. 60/118,937, filed Feb. 5, 1999, the entirety of which is incorporated by reference.

### BACKGROUND OF THE INVENTION

[0002] This invention relates to processes for cleaning silicon substrates such as silicon wafers and for etching oxide layers on such wafers, and more particularly relates to wafer cleaning and oxide etching techniques employing hydrofluoric acid.

[0003] The effectiveness of cleaning processes for removing contamination from silicon wafers employed for microfabrication is growing ever more important as the critical size of microfabricated electronic devices shrink. Wafer contamination is generally introduced from wafer production and packaging, from exposure to the ambient, and from human exposure during processing, and can consist of particles, organic residue, adsorbed metal ions, and other contaminants. The vital role of wafer cleaning in microfabrication processing is evidenced by the fact that about one-third of the total number of steps in a given microfabrication process are cleaning steps.

[0004] To maximize microfabrication production yield, cleaning processes are relied on to remove wafer contamination without damaging or consuming the wafer and without introducing further contamination to the wafer. For silicon wafers, such cleaning typically includes removal of the native silicon dioxide layer, referred to here as a native oxide layer, for brevity, that is generally present on the wafer. Metal and other contamination can be trapped in this native oxide layer and would critically contaminate high-temperature processing equipment. Removal of the native oxide layer is therefore generally always carried out as an integral wafer cleaning process before any high-temperature processing a wafer.

[0005] Traditionally, silicon wafers are cleaned by way of aqueous phase cleaning processes that typically employ, e.g., acids, bases, and mixtures of various chemicals. Historically, such an aqueous phase process has been effective at removing contaminants and removing the native oxide layer. Now, however, as microelectronic features shrink to the sub-micron regime, as the aspect ratio of wafer topology greatly increases, and as the number of microelectronic metal interconnect layers is increased, traditional aqueous cleaning processes are less effective or completely ineffective. Thorough drying of rinse solutions from around and in small or high aspect ratio features can be difficult and can result in trapping of contamination at those features. Furthermore, new combinations of microelectronic materials and new exotic microelectronic materials can be adversely affected by aqueous cleaning chemicals that historically were considered benign to more conventional materials.

[0006] Aside from structure and materials considerations, it is found that microfabrication process facilities are under increasing pressure to reduce the volume of waste chemicals they generate. Wafer cleaning processes contribute substan-

tially to this waste volume. As environmental regulations are increased, the pressure to reduce or eliminate aqueous wafer cleaning waste will also increase.

[0007] In response to many of these issues, the use of hydrofluoric acid (HF) vapor for cleaning silicon wafers, including etching of native oxide, and etching of thicker silicon dioxide layers, has been extensively studied. Typically, HF vapor wafer cleaning and etching is carried out in an in situ environment and employs vapor phase HF and, e.g., vapor or liquid water, an alcohol, and other optional components such as carrier gases. HF vapor etching is found to selectively etch oxide over silicon and to remove at least partially wafer contaminants.

[0008] HF vapor cleaning and etching has not been fully adopted for cleaning and etching steps in microelectronic fabrication processing, however, due to unwanted contamination that can be introduced by a vapor process itself, and due to a lack of clear understanding of the mechanisms and operational regimes of vapor-based wafer cleaning and etching, with a resulting inability to precisely control the processes. For example, it has been found that under some process conditions, liquid phase condensation of vapor phase reactants on a wafer can occur during a cleaning or etch process, and that high concentrations of reaction products in this condensed phase can result. If such reaction products do not desorb into the vapor phase when the process is stopped, they can produce particulate residue on the wafer. This residue contamination of the wafer is often characterized by diffuse light scattering, referred to as "haze" on the wafer surface. Typically, a post-vapor clean aqueous rinse step is required to remove any such residue contamination. This rinsing both consumes water and produces aqueous waste volume that the vapor process was motivated to do away with, and eliminates the ability to carry out an "all-dry" in situ process that is desirable for multi-process integration. But more fundamentally, the introduction of additional contaminants by a vapor process intended for contaminant removal renders the vapor process inefficient and ineffectual.

[0009] It has also been found that under some process conditions, multilayer adsorption, rather than condensation, of vapor phase reactants can occur on a wafer during a cleaning or etch process, and that localized thick multilayer reaction product regions can result. Such a condition is particularly apt to occur, for multilayer process conditions, during etching of a relatively thicker silicon dioxide layer. The reactant multilayer regions can accelerate the local etch rate and produce a localized piling up of reaction products, leading to pitting of the oxide layer being etched. Like the residue particulate formation discussed above, this oxide pitting is commonly characterized as "haze" on the etched layer surface. The lack of etch control of which this pitting is a symptom that is generally considered to disqualify the vapor etch process for microfabrication steps requiring high-precision.

[0010] Beyond the particular concerns of lack of process uniformity control and unwanted process contamination described above, it has historically been considered extremely difficult to guarantee HF vapor process repeatability or predictability with respect to starting wafer conditions such as contamination conditions. These various concerns, taken together, are generally considered to out-

weigh the potential benefits that HF vapor cleaning and etching might bring to microfabrication process efficacy, precision, economics, and environmental regulatory compliance.

#### SUMMARY OF THE INVENTION

[0011] The invention provides HF vapor processes that can be precisely controlled with a high degree of reproducibility. These HF vapor processes can be employed in accordance with the invention for, e.g., etching oxide on a semiconductor substrate, for cleaning a semiconductor substrate, for cleaning a metal structure on a semiconductor substrate, e.g., by removing etch residue from the metal structure, and for cleaning a metal contact region of a semiconductor substrate, among other applications.

[0012] In the processes provided by the invention, a semiconductor substrate to be cleaned or having oxide to be etched is exposed to anhydrous hydrofluoric acid vapor and water vapor at a substrate temperature greater than about 40° C. Control of substrate temperature, hydrofluoric acid vapor pressure and water vapor pressure is carried out to inhibit formation of liquid on the substrate and to form on the substrate a sub-monolayer of etch reactant and product molecules by adsorption of etch reactant and product molecules at less than about 95% of adsorption sites.

[0013] The sub-monolayer HF vapor process regime is defined in accordance with the invention to proceed under conditions wherein no more than about 95% of a monolayer coverage of the substrate surface by reactant and product molecules occurs. This sub-monolayer surface coverage results in highly uniform, reproducible, and predictable etch and cleaning rates, such that the process is particularly robust for manufacturing scenarios, where, e.g., the oxide to be processed consists of silicon dioxide and the substrate to be processed consists of a silicon wafer. Small-sized and large-aspect ratio features are particularly well-handled by HF vapor processes carried out in the sub-monolayer regime of the invention.

[0014] The HF vapor processes of the invention enable all-dry semiconductor substrate cleaning, oxide etching, and etch residue removal, among other processes, which heretofore have conventionally required large volumes of aqueous chemicals that cannot be precisely controlled. All-dry vacuum cluster systems including chambers for the HF vapor processes of the invention, as provided by the invention, enable high efficiency, precision, and reproducibility for critical and frequent processes required of most micro-electronic fabrication sequences.

[0015] Other applications, features, and advantages of the invention will be apparent from the following description and associated drawings, and from the claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a schematic view of an example vapor processing system provided by the invention for carrying out the HF vapor processes of the invention;

[0017] FIGS. 2A-2D are schematic views of an HF vapor process being carried out in accordance with the invention under conditions of a condensed layer regime, a multilayer adsorption regime, a saturated monolayer adsorption regime, and a sub-monolayer adsorption regime, respectively;

[0018] FIG. 3A is a plot of measured ellipsometric angle,  $\Psi$  (Psi), in degrees, at a wavelength of 4052 Å, as a function of time and increasing partial pressure of HF vapor, for the HF vapor process conditions indicated, highlighting the point at which the process makes a transition from a non-condensed operating regime to a condensed layer operating regime;

[0019] FIGS. 3B-3C are plots of measured and calculated ellipsometric angle,  $\Psi$ , in degrees, as a function of wavelength, for a non-condensed operating regime and for the condensed layer operating regime, respectively;

[0020] FIGS. 4A-4B are plots of measured ellipsometric angle,  $\Psi$ , in degrees, at a wavelength of 4052 Å, as a function of time, taken during the HF vapor etching of a thermal oxide layer in a non-condensed regime and in the condensed regime, respectively;

[0021] FIG. 5 is an Arrhenius plot of measured etch rate, in Å/min, as a function of temperature, for five different HF vapor etch conditions, which include HF vapor processes in the multilayer adsorption regime, the monolayer adsorption regime, and the sub-monolayer adsorption regime of the invention;

[0022] FIG. 6 is an Arrhenius plot including only those points from the plot of FIG. 5 corresponding to the monolayer and sub-monolayer adsorption regimes, and further including calculated values for the points;

[0023]

[0024] FIG. 7A is a plot of measured etch rate, in Å/min, as a function of the partial pressure of water vapor, in Torr, for the HF vapor multilayer process conditions of the invention indicated;

[0025] FIG. 7B is a plot of measured etch rate, in Å/min, as a function of the partial pressure of HF vapor, in Torr, for the HF vapor multilayer process conditions of the invention indicated;

[0026] FIGS. 8A and 8B are plots, produced by atomic force microscopy, of measured layer topology height, in nanometers, as a function of layer extent, in microns, for an oxide layer that has been partially etched by an HF vapor process in the multilayer adsorption regime, and for an oxide layer that has been partially etched by an HF vapor process in the monolayer adsorption regime of the invention, respectively;

[0027] FIGS. 9A-9D are XPS plots of measured relative counts as a function of binding energy, in eV, centered on the energy corresponding to the Si 2p, O 1s, C 1s, and F 1s bonds, respectively, for a native oxide layer on a silicon wafer, for a silicon wafer the native oxide layer of which was etched by HF vapor in the multilayer regime, for a silicon wafer the native oxide layer of which was etched by HF vapor in the monolayer regime of the invention, and for a silicon wafer the native oxide layer of which was etched by liquid HF;

[0028] FIG. 10 is an Arrhenius plot of measured etch rate of a Tetraethylorthosilicate (TEOS) layer, in Å/min, as a function of temperature, for etch conditions in the multilayer, monolayer, and sub-monolayer HF process regimes;

[0029] FIGS. 11A-11C are plots of measured ellipsometric signal angle,  $\Psi$ , in degrees, as a function of time, in

minutes, for three processes in which an oxide layer and overlaying aluminum layer are exposed to an HF vapor process carried out under condensed layer conditions, under multilayer conditions, and under monolayer conditions of the invention, respectively;

[0030] FIG. 12 is an XPS plot of measured relative counts as a function of binding energy, in eV, centered on the energy corresponding to C 1 bonds, for a thermal oxide layer, for a finger print on a thermal oxide layer that has been subjected to a CO<sub>2</sub> cleaning step, for a finger print on a thermal oxide layer that has been subjected to a CO<sub>2</sub> cleaning step and multilayer regime HF vapor process in accordance with the invention, and for a finger print on a thermal oxide layer that has been subjected to a CO<sub>2</sub> cleaning step and a monolayer regime HF vapor process in accordance with the invention;

[0031] FIG. 13 is an Arrhenius plot of measured etch rate, in Å/min, as a function of temperature, for an oxide layer surface which has been positively precharged and for an oxide surface that has been electrically discharged, for two HF vapor etch conditions that include processes in the multilayer adsorption regime, the monolayer adsorption regime, and the sub-monolayer adsorption regime of the invention;

[0032] FIG. 14A is a plot of measured etch rate, in Å/min, as a function of HF vapor partial pressure, for the process conditions indicated, for an oxide layer that has been positively charged in accordance with the invention;

[0033] FIG. 14B is a plot of measured etch rate, in Å/min, as a function of HF vapor partial pressure, including the data of the plot of FIG. 14A and for a process not employing water vapor for etching an oxide layer that has been positively charged in accordance with the invention;

[0034] FIG. 15 is a plot of measured etch rate, in Å/min, as a function of HF vapor partial pressure, for an oxide layer that has been electrically discharged in accordance with the invention;

[0035] FIG. 16 is a plot of measured etch rate, in Å/min, as a function of the ratio of HF vapor partial pressure to total reactant pressure, for an oxide layer that has been electrically discharged in accordance with the invention;

[0036] FIG. 17 is a plot of measured etch rate, in Å/min, for three HF vapor processes, one employing water vapor, one employing methanol, and one employing isopropyl alcohol, all for an oxide layer that has been electrically discharged in accordance with the invention and for an oxide layer that has been electrically positively charged in accordance with the invention;

[0037] FIG. 18 is an Arrhenius plot of measured etch rate, in Å/min, as a function of temperature, for an oxide layer surface which has been negatively precharged and for an oxide surface that has been electrically discharged, for the HF vapor etch conditions indicated, that include processes in the multilayer adsorption regime, the monolayer adsorption regime, and the sub-monolayer adsorption regime of the invention;

[0038] FIG. 19 is a schematic of a vacuum cluster processing system provided by the invention for cleaning metal contacts on a semiconductor substrate as an integral step in an all-dry multi-step process of dielectric patterning and metal deposition; and

[0039] FIG. 20 is a schematic of a vacuum cluster processing system provided by the invention for removing post-etch residue from patterned metal lines as an integral step in an all-dry multi-step process of metal layer patterning and interlayer dielectric deposition.

#### DETAILED DESCRIPTION OF THE INVENTION

[0040] Referring to FIG. 1, there is shown an example system 10 for carrying out the HF vapor processes provided by the invention. The processing system 10 includes a vacuum chamber 12, preferably of stainless steel. A material substrate to be processed, e.g., a wafer 14, is supported on a wafer platen 16, the temperature of which is preferably controlled, e.g., through a conventional water-based heating/cooling loop 18. A throttle valve 20 is provided for maintaining the pressure of the chamber employing, e.g., a mechanical pump 22 and turbo-molecular pump 24. A pressure sensor, e.g., a capacitance manometer, is provided to measure the chamber pressure under process conditions. Preferably, an ion gauge is provided to measure the chamber pressure during evacuation with the turbomolecular pump to assure good vacuum integrity of the chamber.

[0041] Optical ports 34, 36 of the chamber can be employed to conduct ellipsometric measurements 38 during a vapor process, e.g., for monitoring etch rate and film thickness in situ and in real time during a wafer cleaning or etching process. As can be recognized, a conventional ellipsometer, e.g., a model M44 ellipsometer manufactured by J.A. Woollam Co., Inc., of Nebraska can be employed for monitoring multiple wavelengths. The ellipsometer can be connected to, e.g., a computer for directing data to be analyzed by software, e.g., WVASE32, also provided by the J. A. Woollam Co., Inc.

[0042] A shower head 26 is provided for delivering process gases from a gas handling system into the chamber 12. Preferably, the showerhead is stainless steel, of a diameter of, e.g., about 2", 4", or other size corresponding to the diameter of the wafer or substrate to be processed, and includes a stainless steel screen 28 attached at its output to evenly distribute the gas flow delivery from a delivery tube 30 into the chamber. The screen can be provided with, as an example, an open area of about 9%, a 0.007" hole size, and a 0.022" hole pitch with 60° orientation. Additionally, a baffle 32 is preferably included in the shower head to block a direct stream of gas from the delivery tube 30 into the process chamber 12. This configuration enables a condition of relatively uniform mass transport of reactants via stagnation flow, allowing relatively uniform reactant supply across the wafer and reducing product build up. Preferably, the shower head is heated to prevent condensation of reactants on the head and corrosion of the head and to better exhaust reactants.

[0043] Process gases are introduced to the delivery tube 30 through mass flow controllers. The delivery tube is preferably stainless steel and of, e.g., about ¼" diameter. This tubing and shower head could also be lined with inert materials such as Teflon® to reduce contamination of the reactants and the wafer. Water vapor is supplied directly from a water tank 42 through a mass flow controller, preferably without a carrier gas. Preferably the water tank is heated to approximately 100° C. by an electrical resistance

heater such as a heating tape. Anhydrous HF is delivered from a corresponding HF supply tank. Other gases to be optionally employed during a vapor process, e.g.,  $N_2$ , are similarly delivered. Preferably, a heating tape 46 is provided for controlling the temperature of the gas delivery lines and mass flow controllers so as to prevent condensation of gases in the gas delivery system. This heating of the system also enables an increase in accuracy of gas metering and gas flow initiation and quenching, as well as inhibiting corrosion of the system.

[0044] In carrying out an HF vapor process provided by the invention, a wafer to be cleaned or including a film to be etched is loaded into the process chamber and the gas delivery lines are preferably heated by the heating tape to a temperature of between about 35° C. and about 120° C. to suppress condensation of reactants on the delivery lines. The temperatures of the gases to be delivered are preferably maintained at between about 30° C. and about 100° C. by controlling the temperature of the lines and showerhead. The wafer platen supporting the wafer is heated to preferably maintain the wafer at a constant temperature during the vapor process. The chamber walls are heated to prevent condensation of the HF, water, and products on them. Sufficient heating of the chamber walls is distinguished by rapid pump down of the system after the process is complete. For typical processes, a chamber temperature of approximately 60° C. is sufficient.

[0045] The wafer temperature is preferably maintained at between about

[0046] 50° C. and about 200° C., e.g., by thermal conduction to the wafer holder. Preferably, the wafer platen is designed to provide a uniform temperature across the wafer and be in good thermal contact with the wafer; this can be achieved, e.g., by employing an anodized aluminum block having a smooth, flat surface and through which is circulated heating and cooling fluid. If desired, the wafer platen can be rotated during the vapor process to reduce the effects of mass transfer resistance of process reactants and products. The gap between the shower head and the wafer is set at between about 3 mm and about 50 mm, preferably about 12 mm, depending on the conditions of the wafer to be processed. An inert gas, e.g., nitrogen, is optionally flowed, at a flow rate of between about 200 sccm and about 1 liter, preferably about 500 sccm, until a target pressure of between about 10 T and about 500 T, preferably about 50 T, is achieved in the chamber. This enables stabilization of the operating chamber pressure while a pressure controller is on and can be particularly preferable where precise control of the vapor process is desired. Otherwise, the input of the nitrogen gas need not be carried out.

[0047] Water vapor is then introduced to the chamber at a flow rate of between about 5 sccm and about 100 sccm, preferably about 20 sccm. Vapor HF is then introduced at the precise time desired to initiate a wafer etch or cleaning process, at a target flow rate of between about 10 sccm and about 200 sccm, preferably about 50 sccm. Preferably, the HF flow rate is increased slowly from 0 to the target flow rate to prevent an overshoot of the flow rate.

[0048] For the range of HF flow rates suggested, this flow rate increase can be completed typically in about 5 s to about 10 s.

[0049] The flow of water vapor and HF vapor is continued for a time selected to carry out a given cleaning or etch

process, with the partial pressure of HF at between about 5 T and about 100 T and the partial pressure of the water at between about 2 T and about 50 T. Nitrogen flow can be continued or quenched at the start of the vapor process as-desired. During the vapor process, ellipsometric measurements can be taken to determine the etching rate, preferably after about 2 min to minimize any initial effect of the concentration of reactants near the sample at the start of the process, and continued throughout the process as-desired.

[0050] At a selected end time for the vapor process, the gas delivery is quenched and the chamber is pumped out by the mechanical pump. Once the base pressure of the mechanical pump is reached, the valve to that pump is closed and the gate valve to the turbo-molecular pump is opened, for pumping to continue with this second pump. When the pressure of the chamber is below some selected level, e.g., at about  $5 \times 10^{-6}$  T or lower, the sample can be transferred from the chamber for further processing.

[0051] Control of HF vapor process parameters based on the procedures and parameter ranges given above, in accordance with the invention, enable HF vapor process operational regimes that maximize process control and repeatability and that minimize or eliminate particulate contamination and pitting effects commonly associated with HF vapor processes. The inventors herein have discovered that in general a HF vapor process can proceed under any of four different operational regimes. An understanding of the distinct nature of vapor process characteristics in each of the regimes is provided by the invention and enables precise control of a selected regime.

[0052] FIGS. 2A-2D schematically depict four general HF vapor process operational regimes identified by the inventors. The mechanisms by which the four regimes are formed and etch oxide on a silicon wafer depend specifically on the partial pressures of HF and water. The first regime, depicted in FIG. 2A, is one in which vapor-phase reactants 50 and other gases, e.g., HF,  $H_2O$ , and nitrogen, condense to form a condensed, liquid-phase layer 52 on an oxide layer to be etched on a silicon wafer 56. The oxide layer 54 may be a native oxide layer or a thicker oxide layer that was deposited or grown on the wafer. Such a condensed layer forms when, e.g., for a given water vapor pressure, the selected partial pressure of HF, water, and product are sufficiently high that liquid can exist in contact with the vapor. The etch process in this regime proceeds in a manner that is substantially that of conventional liquid-phase HF etching. Etch product residue and particulate contamination can often occur in this etch regime. The thickness of the condensed layer varies as a function of process time and position across the wafer.

[0053] FIG. 2B depicts a second operational regime, here in which the process conditions are selected such that the vapor-phase reactants 50 form a multilayer 58 on an oxide layer 54 to be etched on a silicon wafer 56. The multilayer is produced by the adsorption of the reactant species in a manner that does not form a liquid, and is due primarily to strong bonding between a first layer and overlying layers. Typically only about 2-3 layers can form before a condensed, liquid-phase layer results. The multilayer regime possesses two sub categories: thin and thick. The thick multilayer is formed by increased product buildup by higher etching rates or lower product removal. For given concen-

trations of HF and water, a thin or thick multilayer can exist, with the thick multilayer exhibiting a higher etching rate. A thick multilayer can also form locally, producing areas of higher etching rate (where the thick multilayer exists) and areas of lower etching rate (where the thin multilayer exists). The multilayer regime formation is highly dependent on reaction species and their concentrations, transport of the products away from the surface, temperature, etching rates, and substrate material.

[0054] FIG. 2C depicts a third operational regime, in which the vapor process parameters result in a condition whereby vapor-phase reactants 50 form a monolayer 60 on the surface of an oxide layer 54 to be etched on a silicon wafer 56. The term "monolayer" as used here can be defined as a "saturated monolayer," in which the surface coverage of the oxide layer by the vapor-phase reactants approaches or is substantially at unity, but adsorption on top of this layer, i.e., formation of the multilayer, is not yet significant.

[0055] FIG. 2D depicts the final operational regime, in which the vapor process parameters result in a condition whereby vapor-phase reactants 50 form a sub-monolayer 62 on the surface of an oxide layer 54 to be etched on a silicon wafer 56. The sub-monolayer regime can be generally defined as one in which no more than about 95% of a monolayer exists.

[0056] The inventors herein have discovered that when an HF vapor process is controlled to proceed in the monolayer or sub-monolayer regimes, the oxide layer pitting, associated with processes in the multilayer regime, is reduced or eliminated. Similarly, the generation of etch product residue and particulate contamination associated with vapor processes in the condensed and multilayer regimes is reduced or eliminated in the monolayer and sub-monolayer regimes. Complete removal of native oxide can be accomplished in the monolayer and sub-monolayer regimes, and both are characterized by a substantially uniform etch rate. Wafers having large-aspect ratio features can be fully cleaned and overlying oxide layers etched without particle or residue contamination in the monolayer and submonolayer regimes because the effects of liquid surface tension are eliminated in these regimes. Surface tension and reduced product removal effects in recessed features can lead to locally-altered etching rates in recessed features. Each of these characteristics will be discussed in detail below.

#### EXAMPLE 1

[0057] The process parameters of a vapor-phase HF process for etching an oxide layer of about 540 nm in thickness, grown by thermal oxidation on a silicon wafer was carried out to identify the process conditions corresponding to the condensed regime and the uncondensed multilayer, monolayer, and sub-monolayer regimes described above. A silicon wafer was processed in the system of FIG. 1 and by the procedure described above. The wafer temperature was held at about 40° C., and the partial pressure of water vapor was held at about 5.4 T. The partial pressure of HF vapor was slowly increased over time. As the partial pressure of the HF vapor was increased, real time ellipsometric measurements were taken of the reactants forming on the oxide layer surface.

[0058] Referring to FIG. 3A there is shown a plot of the measured spectroscopic ellipsometric signal at a wavelength

of about 4502 Å as the partial pressure of the HF vapor was increased. FIG. 3B is a plot of measured and calculated ellipsometric signals taken over the range of wavelengths shown, for the conditions to the left in FIG. 3A, where the HF vapor partial pressure was less than about 33 T. FIG. 3C is a plot of measured and calculated ellipsometric signals taken over the range of wavelengths shown, for the conditions to the right in FIG. 3A, where the HF vapor partial pressure was greater than about 33 T.

[0059] It was found that for the temperature and water vapor conditions selected, at an HF vapor partial pressure of about 33 T, a condensed layer of reactants started to form on the oxide layer. Before the occurrence of this condition, the ellipsometric measurements of FIG. 3A gradually increased and then decreased as the oxide film was etched as the HF vapor partial pressure was increased. Once a condensed layer began to form, the ellipsometric measurements were found to increase in frequency, indicating rapid etching as the HF vapor partial pressure was increased beyond the condensation point.

[0060] As shown in FIG. 3B, the calculated ellipsometric signal values and measured values across a range of wavelengths were found to be well fitted by a model for etching of an oxide layer over silicon wherein no condensed layer was formed. Conversely, as shown in FIG. 3C, the calculated ellipsometric signal values and measured values were found to not fit a model for etching of a simple oxide layer over silicon, because of the formation of a condensed layer over the oxide with varying thickness. It is understood that for the non-condensed regimes, vapor-phase molecules adsorbed on the oxide surface did not impact the correctness of the ellipsometric measurement, leading to its good agreement with calculated values. For the condensed regime, the nonuniformity of the condensed layer, as it was formed and grew, set up a condition of interference with the ellipsometric measurement, resulting in unpredictable signal values. Therefore, the ellipsometric measurements were shown to be a sensitive metric of whether a condensed film was present.

#### EXAMPLES 2-3

[0061] A layer of oxide of about 5500 Å in thickness, grown by thermal oxidation on a silicon wafer was etched following the HF vapor etch procedures given above, with the conditions set such that the etch was carried out in a noncondensed regime. FIG. 4A is a plot of ellipsometric spectroscopic signal for a wavelength of 4502 Å taken during the etch process. As the thickness of the oxide layer decreased due to the etch, the signal increased in an expected manner. The etching process was stopped at 3 min after etching about 300 Å of the oxide.

[0062] A layer of thermal oxide of about 5500 Å in thickness was also etched following the HF vapor etch procedures given above, here with the conditions set such that the etch was carried out in the condensed regime. FIG. 4B is a plot of ellipsometric spectroscopic signal for a wavelength of 4502 Å taken during the etch process. As the thickness of the oxide decreased and the condensed layer is formed, the measured signal displayed the characteristic interference due to the etching of the oxide layer; however, the varying thickness of the condensed layer complicates the thickness measurement. The complete etch of the layer was completed in about 0.65 min, as indicated in the plot.

[0063] Examples 1-3 demonstrate that one can identify the state of an HF vapor process as being in the condensed or one of the noncondensed regimes based on the degree of correspondence between calculated and measured ellipsometric signal values and the behavior of the signal as an etch proceeds. Condensed layer etching can be characterized by an ellipsometric signal that displays high rates of etching via the interference cycles and the time for completion and the inability to fit to a thin film model for multiple ellipsometric wavelengths because of nonuniformity in a condensed layer. The multilayer regime cannot be easily distinguished from the ellipsometric measurements, but can be distinguished by its characteristic reduction in etching rate with increasing temperature between the condensed and the monolayer regime.

#### EXAMPLES 4-8

[0064] The impact of temperature and pressure on oxide etch rate was measured for HF vapor processes carried out in the sub-monolayer, monolayer, and multilayer noncondensed regimes to further characterize the distinctions between the three regions. Referring to the Arrhenius plot of FIG. 5, vapor HF oxide etches were carried for a range of temperatures and for five different partial pressure conditions. Each of the wafers was subjected to a pre-etch step in which a positive charge was produced on the oxide layer. Details of this charging step and its impact on the etch characteristics are provided below.

[0065] In all cases, a layer of thermal oxide of a thickness of about 5500 Å was exposed to the etch conditions for about 6 min. The total gas flow rate for all of the etch processes was set at 500 sccm. For the cases where the HF vapor partial pressure was 20 T, 15 T, or 1 T and the water vapor partial pressure was 8 T, 6 T or 4 T, respectively, the total pressure was 125 T. For the case where the HF vapor partial pressure was 5 T and the water vapor partial pressure was 2 T, the total pressure was 62.5 T. For the case where the HF partial pressure was 2.5 T and the water vapor partial pressure was 1 T, the total pressure was 31.8 T. Ellipsometric measurements were taken during each etch process to determine the corresponding etch rate.

[0066] The plotted etch rate trends enable a clear recognition of the three noncondensed layer regimes. In the sub-monolayer regime, for a given temperature, as the reactant partial pressures are increased, the etch rate increases but the effect of increasing pressure diminishes as the monolayer conditions are approached. The etch rate thus asymptotically approaches a saturation point in the etching rate as the pressure is increased. This is consistent with an understanding that the etch rate in the sub-monolayer regime is impacted by the amount of adsorbed reactant molecules. Generally, for given partial pressures, as the temperature is increased, the sub-monolayer etch rate also increases.

[0067] The saturated monolayer regime is distinguished by its positive apparent activation energy, with a positive Arrhenius response, reflected by the downward slope of the dotted line on the Arrhenius plot in FIG. 5 and the corresponding increasing etch rate with increasing temperature. This temperature dependence is stronger than that in the sub-monolayer regime, which does not follow a true Arrhenius response in temperature but demonstrates a positive response with temperature increase. The etch rate of the

saturated monolayer regime is relatively independent of the partial pressures when their ratio is maintained constant; this is consistent with the distinction that the monolayer regime defines a condition wherein the oxide surface is substantially covered and changes in the partial pressure do not greatly affect the coverage.

[0068] The multilayer regime is distinguished from the monolayer regime by a negative Arrhenius response to temperature increase; as the temperature is increased, the etch rate decreases. In the multilayer regime for a given temperature, as the pressure is increased, the etch rate increases. From these observations, it is found that the monolayer regime can be identified by a weak dependence on pressure, with the multilayer regime distinguished by a strong dependence on pressure. The monolayer regime further is distinguished by a first increase in etch rate with increasing temperature at a temperature greater than that at which a negative etch rate-temperature dependence is demonstrated, which characterizes the multilayer regime. The sub-monolayer regime is then characterized by temperatures that are higher than the first temperature increase that indicates a shift from the multilayer to the monolayer regime. Furthermore, a positive Arrhenius temperature response is demonstrated in the sub-monolayer regime approaching the monolayer regime, but a negative Arrhenius response is demonstrated in the multilayer regime approaching the monolayer regime. Finally, the etch rates of the sub-monolayer and monolayer regimes are lower than the etch rates of the multilayer regime at the same temperatures.

[0069] The proportionality between HF and water vapor partial pressure and etch rate in the monolayer and sub-monolayer regimes for a reasonable range of process conditions enables the modeling of the oxide etch rate in the monolayer and sub-monolayer regimes based on Langmuir-Hinshelwood kinetics, where the etch rate is assumed to be roughly proportional to the fraction of HF and water vapor that is adsorbed on an oxide surface. Using this model, and based on the experimental data given above, the oxide etch rate, E.R., in the sub-monolayer and monolayer regimes can be given as:

$$E.R. = \frac{1.059 \times 10^{12} e^{-15500/RT} \times 1.79 \times 10^{-9} e^{13000/RT} P_{HF} \times 9.107 \times 10^{-8} e^{10500/RT} P_{H_2O}}{(1 + 1.79 \times 10^{-9} e^{13000/RT} P_{HF} + 9.107 \times 10^{-8} e^{10500/RT} P_{H_2O})^2} \quad (1)$$

[0070] where E.R. and the pre-exponential factor are expressed in Å/min; where  $P_{H_2O}$  the partial pressure of the water vapor and  $P_{HF}$  is the partial pressure of the HF vapor, both in Torr; R is the ideal gas constant, T is temperature, and where all activation energies are expressed as Kcal/mol.

[0071] The Arrhenius plot of FIG. 6 replots the data from FIG. 5 for the monolayer and sub-monolayer regimes, along with the etch rate values calculated for each condition based on expression (1) given above. The good fit between the calculated and measured values validates the assumption discussed above with regard to the dependence of the sub-monolayer regime on fraction of adsorbed reactants. The oxide etch rate of the sub-monolayer and monolayer regimes is found from the plot of FIG. 6 to be between about 10 Å/min and about 100 Å/min.

[0072] Because the etch rate is approximately proportional to the coverage of the surface in the sub-monolayer and monolayer regimes for a fixed ratio of partial pressures of the HF and water, the etch rate can be used to determine the approximate coverage of the surface at a fixed temperature. For example, given an etch rate of 100 Å for the monolayer coverage, a measured etch rate of 95% of the value would reflect a 95% coverage of the surface by the reactant. The invention defines the sub-monolayer regime as including up to about 95% surface coverage. This etch rate-coverage correspondence is thus found to effectively enable distinctions between the sub-monolayer and monolayer regimes.

#### EXAMPLES 9-10

[0073] The oxide etch characteristics of the multilayer regime were further investigated to provide identifying distinctions of this regime. There is shown in FIG. 7A a plot of oxide etch rate as a function of the partial pressure of water vapor, for a wafer temperature of 40° C., a total flow rate of 500 sccm, a total pressure of 250 T, and an HF vapor pressure of 7 T. These measurements were made on thermal oxide samples of about 5500 Å in thickness that were etched for several minutes while the thickness were measured using ellipsometry. The change in thickness per minute (etch rates) were computed from this data. From the plot it is seen that the multilayer regime is characterized by an oxide etch rate that is substantially linearly proportional to water vapor partial pressure.

[0074] Similarly, referring to the plot of FIG. 7B, it is found that for a partial pressure of water vapor of 4 T, a temperature of 40° C., a total flow rate of 500 sccm, and a pressure of 250 T, the multilayer regime is characterized by a generally proportional response to increases in the partial pressure of HF vapor. It is noted, however, that above an HF vapor partial pressure of about 35 T this linearity fails. Such is understood to be caused by a transition from the thin multilayer regime to a thick multilayer regime. At higher water partial pressures than shown in FIG. 7A, a similar transition is expected. At even higher water and/or HF partial pressure than shown in FIG. 7B, the condensed layer regime would exist. The multilayer regime including both the thin and thick regions at a given temperature lies between monolayer and condensed regimes having higher partial pressures of HF and/or the bordering monolayer regime, but lower partial pressures than the bordering condensed regime.

[0075] Having clearly distinguished the characteristics of the condensed, multilayer, monolayer, and sub-monolayer HF vapor process regimes, the inventors herein have discovered that many of unwanted effects commonly associated with HF vapor processing can be eliminated if the process is carried out in either the monolayer or sub-monolayer regime. For many applications, the sub-monolayer regime is preferred.

[0076] Considering first the common occurrence of oxide layer pitting and haze during HF vapor etching, as discussed earlier, such pitting is typically associated with conditions in the multilayer regime and is the result of localized formation of thicker multilayer regions that accelerates the local etch rate.

#### EXAMPLE 11

[0077] A layer of oxide of 5500 Å in thickness, and thermally grown, was formed on each of two silicon wafers.

Both of the oxide layers were subjected to an electrical charging step, described in more detail below. One of the oxide layers was etched in an HF vapor etch process under multilayer conditions of 40° C., 125 T total pressure, 500 sccm total gas flow rate, 10 T HF vapor partial pressure, and 4 T water vapor partial pressure. The other oxide layer was etched in an HF vapor etch process under monolayer conditions of 90° C., 125 T total pressure, 500 sccm total gas flow rate, 10 T HF vapor partial pressure, and 4 T water vapor partial pressure. As shown in FIG. 6, the etching rate predicted by the Langmuir-Hinshelwood model for this condition lies near the border of the monolayer and sub-monolayer regimes. For both the monolayer and sub-monolayer regimes, the samples were observed to be specular, i.e. not exhibiting hazing which is caused by pitting or particulate contamination of the surfaces.

[0078] Each of the etch processes was suspended after 200 Å of oxide had been etched, as determined by ellipsometric measurements. Atomic force microscopy (AFM) was then carried out to analyze the surface morphology of the partially etched oxide layers.

[0079] FIG. 8A is the AFM profile produced for the sample etched in the multilayer regime and which exhibited hazing, and FIG. 8B is the AFM profile produced for the sample etched under the conditions indicated above and which was specular in appearance. Note that the multilayer-etched sample exhibits substantial pitting, producing surface haze. The elevated feature to the sides of the pitting is an AFM artifact. The size of each pit is about 10,000 Å in diameter and between about 100 Å-200 Å in depth, confirming that each pit is not a deep trench but a recessed area that would be produced by a locally high etch rate.

[0080] The profile of the monolayer-etched sample does not exhibit any pitting; uniform etching across the entire wafer is observed. Similar results can be achieved for conditions in the sub-monolayer regime—both the monolayer and sub-monolayer regimes are found to not produce surface haze. A final aqueous rinse step is conventionally required to remove the buildup of products on the surface which can occur for samples etched in the condensed regime and under some circumstances in the multilayer regime. The invention eliminates the need for such by employing monolayer or submonolayer etch conditions that suppress the pitting mechanisms. Similarly, the invention reduces the need for wafer rotation during an etch process to enhance the mass transfer rate or to enhance the uniformity of mass transfer across an etching layer; even without such enhancements, the monolayer and submonolayer etch regimes of the invention are found to provide more uniform etch results.

#### EXAMPLE 12

[0081] Native oxide removal is a critical requirement for complete cleaning of silicon wafers, as explained above. The effectiveness of multilayer and monolayer HF vapor etching of native oxide silicon layers was compared with that of aqueous HF etching. Three silicon wafers, each with a native oxide layer having a thickness of about 20 Å were subjected to exposure to either a liquid-phase HF etch, a multilayer HF vapor etch, or a monolayer HF vapor etch. The liquid-phase HF was carried out with a 10:1 diluted HF solution. For this aqueous process, the wafer was immersed in the diluted solution for 1 min, followed by a dionized water rinse and

conventional spin drying. Hydrophobicity was observed visually on the silicon surface at the completion of the liquid-phase etch.

[0082] The multilayer native oxide etch was carried out under conditions of 40° C., 125 T total pressure, 500 sccm total gas flow rate, 10 T HF vapor partial pressure, and 4 T water vapor partial pressure. The monolayer native oxide etch was carried out under conditions of 90° C., 125 T total pressure, 500 sccm total gas flow rate, 10 T HF vapor partial pressure, and 4 T water vapor partial pressure. These conditions border the monolayer and sub-monolayer regimes. Because the kinetics of the monolayer and sub-monolayer regimes are similar, similar results are found to be obtained for both regimes, but with lower etching rates and better control in the sub-monolayer regime.

[0083] Referring to FIGS. 9A-9D, there are shown the relevant XPS spectra measured at the completion of the native oxide etches. The multilayer and monolayer HF vapor processes were found for all considerations to be superior over a liquid-phase process. The Si—O peak was still observable after liquid HF etching, but not found for either of the HF vapor processes. Unlike the vapor-etched wafers, the wafer etched in the liquid-phase HF exhibited substantial oxygen after the etch. This result could have been due to imperfect removal of the native oxide by the etch or due to immediate native oxide regrowth by exposure to the ambient.

[0084] The absolute amount of carbon was reduced after all of the etch processes; but carbon contamination was observed for the aqueous process, at a higher binding state, indicating that a fluorocarbon contaminant was likely contained in the HF etch solution. Finally, the fluorine remaining on the wafer after the native oxide etch was found to be dramatically higher for the liquid-phase etch than for the vapor-phase etches. These comparisons illustrate that contamination can be minimized during native oxide removal through the use of multilayer, preferably monolayer, and most preferably sub-monolayer, rather than liquid-phase, HF processes.

#### EXAMPLES 13-15

[0085] Tetraethylorthosilicate (TEOS) is commonly employed as an interlayer dielectric material between metal lines due to the ability to deposit TEOS layers at relatively low temperatures, thereby adding little to the thermal budget of a semiconductor fabrication sequence. Cleaning of exposed metal and semiconductor contact areas is required to remove oxides on the metal and substrate and enable the formation of a via to an adjacent metal line. Such cleaning is required to be done with the interlayer metal dielectric exposed.

[0086] The etch characteristics of TEOS were investigated for multilayer, monolayer, and sub-monolayer HF vapor process regimes. Layers of TEOS were deposited by plasma enhanced chemical vapor deposition on silicon wafers. No annealing of the films was carried out.

[0087] HF vapor etching of the TEOS films was carried out for three different partial pressure combinations of HF and water vapor; 5 T and 10 T for the HF vapor, and 4 T and 8 T for the water vapor, as indicated on the plot. The total pressure of about 125 T was used for these processes with total flow rates of about 500 sccm.

[0088] FIG. 10 is an Arrhenius plot of the etch rate of the TEOS layers as a function of temperature for the three partial pressure combinations. Ellipsometric measurements were employed to determine the plotted etch rates. Comparing this plot with the Arrhenius plot of FIG. 5, it is found that the TEOS and thermal oxide film vapor etch mechanisms follow substantially identical trends. In the monolayer regime, the TEOS is found to etch about 2-3 times faster than thermal oxide for the same process conditions, while in the multilayer regime, the TEOS is found to etch about times faster than thermal oxide for the same process conditions.

[0089] Low etch selectivity between TEOS and thermal oxide is generally favored for cleaning metal contacts, while high selectivity is often desired for selectively removing TEOS from a site. The monolayer and submonolayer regimes are thus found to be well-suited for metal contact cleaning. It is expected that if the TEOS films employed in these experiments had been densified by a heat treatment such as annealing, an even lower selectivity between TEOS and thermal oxide would have been obtained.

#### EXAMPLES 16-18

[0090] Any process that is performed for cleaning metal contacts inherently exposes the metal material, which commonly is aluminum. This is specifically the case for the removal of polymer residue that can remain at the edges of a metal line after a plasma etching process is carried out to pattern metal lines with a photoresist mask. Frequently, polymer residue remains at the edges of an etched metal line even after a plasma ashing procedure is completed. The polymer residue must be removed prior to subsequent processing as it would critically contaminate processing equipment. Liquid-phase diluted HF solution is known to be a good polymer remover, but it corrodes and etches aluminum rapidly.

[0091] The degree of attack of a thin aluminum layer by vapor HF etch processes was investigated for the condensed layer, multilayer, and monolayer regimes. For each regime, a layer of thermal oxide of about 5500 Å in thickness was formed on a silicon wafer and a layer of aluminum having a thickness slightly less than about 20 Å was deposited on the oxide layer. This thickness was selected because of its transparency for enabling determination of the thickness of the underlying oxide layer by ellipsometric measurement. The aluminum deposition was performed in the same vacuum cluster processing system with vacuum transfer between chambers, thereby preventing oxidation of the aluminum by air.

[0092] For the condensed layer regime, the process conditions of the etch were set at a temperature of 40° C., a total pressure of 125 T, a total flow rate of 500 sccm, an HF vapor partial pressure of 40 T, and a water vapor partial pressure of 4 T. For the multilayer regime, the process conditions of the etch were set at a temperature of 40° C., a total pressure of 125 T, a total flow rate of 500 sccm, an HF vapor partial pressure of 10 T and a water vapor partial pressure of 4 T. For the monolayer regime, the process conditions of the etch were set at a temperature of 90° C., a total pressure of 125 T, a total flow rate of 500 sccm, an HF vapor partial pressure of 10 T and a water vapor partial pressure of 4 T.

[0093] FIG. 11A is a plot of the ellipsometric signal at a wavelength of 4052 Å as a function of time for the con-

densified layer etch process. From the plot it was determined that the oxide underlying the aluminum layer was etched immediately upon exposure to the condensed regime conditions, and was etched at a rate of about 10,000 Å/min. This result corresponds to that of aqueous HF and indicates the incompatibility of condensed layer processing with exposed aluminum.

[0094] FIG. 11B is a plot of the ellipsometric signal at a wavelength of 4052 Å as a function of time for the multilayer etch process. An initial etch inhibition period of just about 3 min was followed by oxide etch at a relatively slow rate. This suggests that for the multilayer regime, the thin aluminum layer was not etched as rapidly as in the condensed layer regime, but that that HF molecules adsorbed on the aluminum layer penetrated the layer, resulting in a slow etch of the oxide.

[0095] FIG. 11C is a plot of the ellipsometric signal at a wavelength of 4052 Å as a function of time for the monolayer etch process. As indicated in the plot, the signal changed less than about 0.2 degree for the entire 6 minute-long etch process. This suggests that neither the aluminum layer nor the underlying oxide layer were damaged by the monolayer HF exposure, and therefore that a monolayer HF vapor process can safely be employed to remove residue after metal patterning. The elimination of a rinse step through the use of a vapor process is also benefit in reducing the potential of metal corrosion. It is also understood that the HF vapor process could provide a further benefit by inherently producing a protective fluorinated layer on the surface of the metal.

[0096] Turning to further aspects of the invention, there is provided an optional first step of cleaning a wafer or an oxide layer to be processed by an HF vapor process with an ice jet, e.g., a jet of CO<sub>2</sub>. CO<sub>2</sub> ice jet wafer cleaning is a known surface cleaning method employing a high-velocity stream of carbon dioxide directed at a wafer surface. This procedure can be employed for at least partially removing carbon contamination as well as particulates from a wafer surface.

[0097] The inventors herein have determined that carbon and particulate contamination does not substantially impact the etch rate and etch uniformity of HF vapor processes carried out in the condensed layer and multilayer processing regimes, as the etching kinetics in these regimes are less sensitive to surface contamination. In contrast, etch mechanisms carried out in the sub-monolayer and monolayer regimes can be substantially inhibited or enhanced by carbon and particulate contamination, both in an unpredictable manner. This is due to the high degree of sensitivity of the sub-monolayer and monolayer regimes to the chemical and electrical characteristics of species adsorbed on the surface, given that these regimes are surface reaction limited. As a result, the inventors have recognized that the repeatability of monolayer or sub-monolayer HF vapor processes carried out on contaminated wafers or oxide layers can be very poor.

[0098] The inventors have discovered the surprising result that an initial ice jet cleaning of a carbon-contaminated wafer or oxide layer, even if not complete, reduces the contamination to a level that does not impact the efficacy or uniformity of etch processes in the sub-monolayer and monolayer regimes. In other words, it has been discovered that contrary to conventional wisdom, the surface-reaction

limited sub-monolayer and monolayer regimes can proceed on a contaminated surface in a uniform and predictable manner, if the surface is first exposed to an ice jet cleaning procedure. The invention thus provides for ice jet cleaning processes using CO<sub>2</sub>, Ar, or other suitable gas to prepare a wafer or oxide layer for cleaning or etching in the monolayer and sub-monolayer regimes.

[0099] The ice jet cleaning step of the invention consists of directing a high-velocity stream of small dry ice crystals toward a wafer or oxide surface. Such crystals can be formed by, e.g., the expansion of high-pressure liquid or gaseous carbon dioxide from a small orifice. Adiabatic expansion of the liquid or gas generates a temperature drop within the orifice that is sufficient to produce nucleation of small dry ice particles. Preferably, there is provided for this expansion a source of carbon dioxide liquid or gas, e.g., gas at a pressure at about 830 psi. It can be preferable to provide a dip tube that allows withdrawal of the CO<sub>2</sub> directly from inside a gas storage cylinder, but other arrangements are also suitable.

[0100] A wafer to be cleaned by the ice particles is positioned on, e.g., an aluminum sample holder on which the wafer is held by, e.g., a vacuum suction contact. For some wafer cleaning processes, it can be preferable to prevent condensation of water on the wafer due to excessive cooling by the CO<sub>2</sub>; such can be accomplished by, e.g., providing a wafer holder that is thermally conducting and that is connected to, e.g., a heating block for heating the wafer during the cleaning step.

[0101] In carrying out the ice jet cleaning procedure, it is preferable to first initiate the ice jet formation out of the nozzle with the nozzle directed away from the wafer to be cleaned. Once an ice stream is formed and stabilized, the ice jet stream is then preferably swept from side to side across the entire wafer area. An incident ice jet stream angle of between about 30° and about 45° to the normal to the surface, and a nozzle-to-surface distance of between about 1" and about 1.5", is preferred. For a 4" wafer, ice jet exposure of the entire wafer should take between about 3 min and about 4 min. It is recognized that the use of a gas knife nozzle, in which a broad source of the ice jet can be produced, can be employed to enable a more rapid processing of the wafer.

[0102] The force of adhesion between submicron-sized particles and a wafer or oxide surface is typically much larger than the drag force of conventional fluid-based cleaning. But for the ice jet cleaning process, the cleaning mechanism is primarily by momentum transfer between the ejected ice particles and contaminants on the wafer surface. As a result, the small ice particles from the jet stream can overcome the particle adhesion force and free the particles from the surface by this momentum transfer.

[0103] It is also found that the ice jet stream sweeps away removed particle contamination, removing it from the wafer environment. Thick deposits of hydrocarbon are partially removed by interaction of the ice particles with the ice jet crystals, but some hydrocarbon contamination generally remains after ice jet processing. Similar mechanisms for particulate contamination removal and hydrocarbon removal take place in ice jets created from other gases such as Argon, therefore, their use as a pretreatment for the monolayer and sub-monolayer regimes is contemplated by the invention.

Additional details for carrying out ice jet processing are provided by Tamai et al., in U.S. Pat. No. 5,512,106, Apr. 30, 1996; by Whitlock et al., in U.S. Pat. No. 4,806,171, Feb. 21, 1989; and by Ohmori et al., in U.S. Pat. No. 5,147,466, Sep. 15, 1992; the entirety of all of which are hereby incorporated by reference.

#### EXAMPLE 19

[0104] A layer of thermal oxide of about 5000 Å in thickness was formed on each of two silicon wafers and a finger print was made on the oxide surface of each. Prior to making the finger print, the carbon is XPS spectra of the two oxide surfaces was profiled. With the finger print in place, the two oxide layers were subjected to a CO<sub>2</sub> ice jet cleaning step following the procedures given above. The XPS spectra was then profiled. One of the wafers was then subjected to a multilayer HF vapor process, at conditions of HF vapor partial pressure at 10 T, water vapor partial pressure at 4 T, total pressure at 125 T, flow rate at 500 sccm, and temperature at 40° C. The other wafer was subjected to a monolayer HF vapor process, at conditions of HF vapor partial pressure at 10 T, water vapor partial pressure at 4 T, total pressure at 125 T, flow rate at 500 sccm, and temperature at 90° C. Each of the HF vapor processes were carried out for minutes, etching about 200 Å of oxide during that time.

[0105] Each of the oxide layers was inspected at the completion of the CO<sub>2</sub> cleaning step and at the completion of the HF vapor processing steps. It was found that remnants of the finger print remained using XPS on the oxide layer after the CO<sub>2</sub> cleaning step. It was surprisingly found that the remnant of the fingerprint did not alter the removal of the underlying oxide layer processed in the monolayer HF vapor regime and that the oxide layer was uniformly etched in the monolayer regime after the ice jet exposure. In fact, such contamination was found to be removed by the HF process in both the monolayer and sub-monolayer regimes. This validates the unexpected discovery by the inventors that the ice jet cleaning process synergistically cooperates with the surface-reaction limited monolayer and sub-monolayer HF vapor processes to enable uniform etching of those processes even in the presence of surface contamination.

[0106] In general, monolayer and sub-monolayer surface kinetics are significantly affected by contaminants such as hydrocarbons that block the surface preventing adsorption of the reactants. Thick carbonaceous deposits have been reported to accelerate the etching rate of underlying oxides by absorption of the reactants within the carbonaceous deposit. It is therefore surprising that the contamination left after CO<sub>2</sub> cleaning did not alter the etching of the underlying oxide. This discovery indicates that the general benefits of processing in the sub-monolayer and monolayer regimes can be extended even to wafers and oxide layers having carbon contamination, in contradiction to theoretical prediction.

[0107] FIG. 12 is an XPS plot of measured relative counts for the energy region corresponding to carbon is from the finger print. The carbon peak is shifted to 290 eV from its expected energy of 285 eV due to an electrical charging effect of the XPS measurement. The plot highlights the finding that the monolayer regime was found to be more effective than the multilayer regime at cleaning residual carbon remaining after the ice jet step. In combination with the etch uniformity visually confirmed, it is understood in

accordance with the invention that the surface-reaction limited monolayer and sub-monolayer process regimes are superior for providing etch control and uniformity even in the presence of carbon contamination. This finding indicates that the sub-monolayer and monolayer HF vapor processes of the invention are particularly well-suited for removing polymeric residue from a plasma-etched layer, given that the main constituents of such residue are carbon and silicon dioxide.

[0108] The invention provides further techniques for controlling HF vapor process mechanisms. Specifically, there is provided the parameters for an initial step of electrically charging or discharging an oxide layer surface to control the etch rate of the oxide layer by an HF vapor process in a repeatable, predictable manner. Handling history, cleaning processes, ambient conditions, and many other factors are recognized to all impact the electrical charge state and corresponding HF vapor etch rate of an oxide layer. The prespecified and controlled charge preparation step provided by the invention compensates for such factors to render an HF vapor oxide etch process predictable and repeatable.

[0109] The impact of a particular oxide layer charge polarity on etch rate of the oxide layer is dependent upon the particular operating regime in which the HF vapor process is set to proceed. Two etch states are defined in accordance with the invention: a nonactivated, low-etch rate state, produced by an initial electrical discharge step, and an activated, high-etch rate state, produced by an initial electrical charging step. Given the demonstrated benefits of the non-condensed sub-monolayer, monolayer, and multilayer HF vapor regimes and their preference in accordance with the invention, the invention provides particular charging and discharging parameters for these particular regimes.

[0110] The inventors herein have discovered that for any of the three non-condensed regimes, a nonactivated, low-etch rate state of a given regime can be predictably carried out on an oxide layer by first discharging any static charge build-up that might be present on the oxide layer surface. For the sub-monolayer and monolayer regimes, an activated, high-etch rate state process can be carried out on an oxide layer by first electrically charging the oxide surface with a positive polarity charge. Intermediate charging of the surface can produce etching rates that have intermediate etching rates. For the multilayer regime, an activated, high-etch rate state process can be carried out on an oxide layer by first electrically charging the oxide surface with a negative polarity charge. Each of these techniques are described in turn below.

[0111] Considering first the sub-monolayer and monolayer regimes, a positive electrical charge can be imparted to the surface of an oxide layer to be etched in one of these two regimes by a range of techniques provided by the invention. In a first technique, the oxide layer surface is exposed to a conventional electron beam irradiation scan. For example, a high-energy electron beam, characterized by, e.g., a 10 KeV accelerating voltage and

[0112] 25 μA emission current, with a spot size of about 1 cm in diameter, can be employed to irradiate an oxide surface. The beam is scanned across the surface, for a total irradiation time of, e.g., about 30 minutes. The electron beam scan is understood to charge the oxide surface with a positive polarity due to generation of secondary electrons from the oxide surface.

[0113] Exposure of an oxide layer surface to UV irradiation can also be employed for producing a positive electrical charge on the surface. In accordance with the invention, a UV source is directed toward an oxide surface through a metal screen that is electrically biased by a DC voltage source. The screen is preferably separated from the oxide surface by a gap of about 1 inch. The polarity of the DC bias has no effect on the electrical charging process. It is understood that the UV source introduces sufficient photon energy to excite and free the surface electrons of an oxide layer, resulting in a positively charged surface state.

[0114] A positive surface charge can also be imparted to an oxide layer by processing the layer in a plasma chamber. In a first plasma charging process provided by the invention, a wafer including an oxide layer is supported on the lower metal electrode of the chamber with the wafer insulated from the electrode by an insulating layer such as Kapton tape, a configuration used to electrostatically clamp the wafer to the electrode. The DC power supplied to the lower electrode is set with a negative bias. Plasma processing conditions can be set as, e.g., 1000 V DC voltage, 150 W RF power, 10 mT pressure, and 10 sccm flow of an inert gas such as argon. A plasma process time of less than 1 min is needed to produce an oxide surface charge.

[0115] Less than about 100 Å of oxide are etched during this duration for the process conditions given. With a plasma initiated, the metal electrode and insulated wafer together form a capacitor in which positive electrostatic charge is accumulated on the oxide layer surface.

[0116] The CO<sub>2</sub> ice jet cleaning procedure described previously can also be employed to impart a positive electrical charge to an oxide surface. It is required that the wafer be heated during the ice jet cleaning to produce the positive charge state. This can be accomplished, as described above, by maintaining the wafer on a thermally conductive support block to which a heater is connected during sweep of an ice jet over the oxide layer surface. With this configuration, the ice jet process given above results in positive oxide surface charging.

[0117] A positively charged oxide surface can be produced by a variety of other techniques. In one particularly simple technique, a sheet of clean room grade Kimwipes® or other such anti-static material can be wiped across the surface of the oxide layer to impart a positive electrical charge to the layer. The anti-static coating of the material is found to generate a positive charge on the oxide surface.

[0118] These examples provide a description of several efficient and simple charging techniques. It is to be understood that other techniques can be employed to impart a positive electrical charge to an oxide surface, and the invention is not limited to a particular technique.

[0119] Electrostatic charge release of an oxide layer can be accomplished in accordance with the invention by a variety of techniques. In a first technique, charge is released by a water rinse of the oxide surface. The electrical conductivity of water is understood to enable the release of charge from the layer. In a further charge release technique, the CO<sub>2</sub> ice jet cleaning process described earlier is carried out on an unheated wafer, i.e., condensation is permitted during the ice jet process. As a result, charge is removed by the adsorbed species and swept away with the species by the jet stream.

It is to be recognized that other techniques can be employed to release charge from an oxide surface. The invention is not limited to a particular charge release technique.

#### EXAMPLES 20-21

[0120] A thermal oxide layer was formed on a plurality of silicon wafers. Half of the oxide layers were treated by wiping a Kimwipes® cloth over their surfaces to impart a positive electrical charge to the surface. The remaining oxide layers were subjected to a CO<sub>2</sub> ice jet cleaning while unheated, to release electrostatic charge from their surfaces. One quarter of the charge oxide layers and one quarter of the uncharged oxide layers were subjected to HF vapor process conditions of a partial pressure of HF vapor of 10 T, a partial pressure of water vapor of 4 T, a total flow rate of about 500 sccm and a total pressure of about 125 Torr at a variety of temperature conditions. One quarter of the charge oxide layers and the final quarter of uncharged oxide layers were subjected to HF vapor process conditions of a partial pressure of HF vapor of 20 T, a partial pressure of water vapor of 8 T, a total flow rate about 500 sccm and a total pressure of about 125 Torr.

[0121] The etch rate of each of the vapor processes was determined based on ellipsometric measurements taken during the processes. FIG. 13 is an Arrhenius plot of etch rate, in Å/min, as a function of process temperature, for the two different process conditions and the two different surface charge conditions. It is clearly indicated from the plot that for the sub-monolayer and monolayer process regimes, the positive surface charge resulted in an etch rate increase; this increase was most dramatic for the sub-monolayer regime temperatures, at which a rate increase of a factor of almost 100 is found. The positive surface charge had very little, if any, impact on the etch rate in the multilayer regime, however. These results were reflected in the plots of FIGS. 5, 6, and 10 and described above, where it was indicated that an initial positive polarity electrical surface charge was produced prior to the etch processes.

[0122] It is believed that the positive oxide surface charging enables direct ionization of vapor HF adsorbed on the oxide surface, leading to an increase in the rate of the oxide etch reaction. This is consistent with the fact that the monolayer regime is dependent on surface reaction kinetics and that the sub-monolayer regime is very strongly dependent on surface reaction kinetics.

#### EXAMPLES 22-23

[0123] The plot of FIG. 13 also highlights the impact of positive surface charging on the vapor process dependence on HF vapor partial pressure. For the process temperatures in the sub-monolayer and monolayer regimes between approximately 125° C. and 150° C., it is found that for the electrically charged oxide layers, a doubling of HF and water partial pressures from 10 T to 20 T and 4 T and 8 T, respectively, results in a doubling of the etch rate. Conversely, for the uncharged oxide layers, a doubling of the HF and water partial pressures from results in an etch rate increase by a factor of between three and four.

[0124] This correspondence was further investigated. Thermal oxide layers were produced on silicon wafers and all were positively charged by wiping their surfaces with an anti-static cloth. The wafers were then subjected to HF vapor

processes carried out in the sub-monolayer regime, at a temperature of 145° C., a total flow rate of 500 sccm, and a partial pressure of water vapor of 4 T. The partial pressure of the HF vapor was varied from process to process. The etch rate of each process was determined based on ellipsometric measurements taken during each process.

[0125] FIG. 14A is plot of oxide etch rate, in Å/min, as a function of HF vapor partial pressure, measured for the positively charged oxide layers. This matrix of experiments confirms that in the charge-activated, high-etch rate state, the etch rate of the sub-monolayer and monolayer regimes is directly proportional to the HF partial pressure, following simple first order Langmuir adsorption kinetics.

[0126] The data from FIG. 14A is replotted in FIG. 14B, which also includes etch rate data for a process employing the same process conditions as those relating to the data of FIG. 14A but with no water vapor introduced during the vapor process. Under these conditions and for low HF partial pressures, there is seen to be no substantial difference between the etch rates. This indicates that for positively charged oxide layers being etched under these conditions in the sub-monolayer or monolayer regimes, the effect of water vapor partial pressure is negligible for low pressures and for low water vapor pressures. It is to be recognized, however, that under other conditions, the water vapor partial pressure significantly affects the etch rate in the monolayer and sub-monolayer regimes with positive charge enhancement of the etch rate. The plotted data of FIGS. 5, 6, and 10 confirm this, given that a positive charging of the oxide surface was used to obtain the high etching rate state of those reported experiments.

#### EXAMPLE 24

[0127] The dependence of etch rate on HF vapor partial pressure was also directly investigated for the sub-monolayer and monolayer regimes of etching of uncharged oxide layers. Thermal oxide layers were produced on silicon wafers and subjected to a water rinse to enable release of charge from the oxide surface. The oxide layers were then exposed to HF vapor conditions in the sub-monolayer regime, consisting of a total pressure of 125 T, a temperature of 145° C., a total flow rate of 500 sccm, and no water vapor. Each wafer was processed at a different HF vapor pressure.

[0128] FIG. 15 is a plot of etch rate, in Å/min, as a function of HF pressure, determined based on ellipsometric measurements taken during the etch processes. As indicated by the plot, there is found to be a second order dependency of etch rate on HF vapor pressure for the non-charged oxide layers. This confirms the results plotted in FIG. 13, which also indicate a second order etch rate-HF vapor pressure dependency for the uncharged oxide layer conditions.

#### EXAMPLE 25

[0129] Characteristics of uncharged oxide etch processes in the sub-monolayer and monolayer regimes were further investigated. Thermal oxide layers were produced on silicon wafers and were water-rinsed to release any electrical charge that might be present. The wafers were then exposed to sub-monolayer and monolayer HF vapor conditions of a temperature of 90° C., a total pressure of 125 T, a total flow rate of 500 sccm, and a combined reactant partial pressure of 28 T. Each wafer process employed a different reactant ratio.

[0130] FIG. 16 is a plot of etch rate, in Å/min, as a function of reactant ratio, based on ellipsometric measurements taken during the etch processes. For the non-activated, low-etch rate process data plotted, it is found that the etch rate is not impacted by the ratio of reactant partial pressures. This is in great contrast to the results obtained for the charged, activated process data presented in FIGS. 14A-14B, where it is indicated that the HF vapor partial pressure strongly influences the etch rate. Such is understandable given that the positive surface charging is found to directly ionize adsorbed HF species; a higher degree of HF adsorption would correspond to a higher etch rate.

[0131] These examples highlight the very clear process-dependent effects that can be relied on to distinguish the activated etch state from the non-activated etch state for the sub-monolayer and monolayer etch regimes. Positive charging of an oxide layer to an activated state results in an etch rate increase by a factor of about 5, and a shifting of the etch rate from a second order to a first order dependency on the partial pressure of HF vapor. The activated state is found to be closely impacted by HF vapor partial pressure, with no effect by water vapor pressure, while the non-activated state is found to be not impacted by the reactant partial pressure ratio. The positive charging is found to greatly impact the sub-monolayer and monolayer regimes but to have substantially no impact on the multilayer regime.

#### EXAMPLES 26-28

[0132] The impact of positive-polarity oxide layer charging was further investigated for HF vapor processes employing methanol and isopropyl alcohol instead of water vapor. Thermal oxide layers were grown on silicon wafers, and on half of the layers was produced a positive-polarity charge by wiping with a Kimwipes® cloth. HF vapor processes were carried out, with process conditions of the temperature at 95° C., the total flow rate of 500 sccm, a total pressure of 125 T, and a partial pressure of 20 T. Processes were carried out employing either water vapor, methanol, or isopropyl alcohol, all at a partial pressure of 8 T.

[0133] FIG. 17 is a plot of etch rate, in Å/min, for each the water vapor, methanol, and isopropyl alcohol processes, each for a non-activated, uncharged oxide layer and for an activated, positively charged oxide layer. The results indicate that the largest increase in etch rate by charge activation is achieved for an HF-water vapor process. In the non-activated state, the HF-isopropyl alcohol process results in the highest etch rate, while for the activated state, the HF-water vapor process results in the highest etch rate. This experiment verifies that a step of electrically charging or discharging an oxide layer prior to an HF vapor process can be employed to control the etch rate of the vapor process, including any of water vapor, methanol, or isopropyl alcohol with the HF vapor.

[0134] Turning to processes for producing the charged, activated state for the multilayer regime, the inventors herein have discovered that a negative electrical charging of an oxide surface results in activation of the surface for HF vapor etching in the multilayer regime. This is understood to enhance etch rate in the multilayer regime by enhancing the negative potential of the oxide surface, which in turn enhances adsorption of the polar reactant molecules on the oxide surface. Such enhanced adsorption is found to enable

the formation of a multilayer that is thicker than that produced without oxide layer charging, and is due to the electrostatic enhancement of the adsorption energy of these molecules to the surface. The resulting thicker multilayer exhibits an etch rate higher than a thinner multilayer, as expected.

**[0135]** A negative charge can be imparted to an oxide surface by a variety of techniques provided by the invention. In a first technique, the plasma exposure process described above is employed with the DC voltage bias polarity reversed. Here a positive DC bias placed on the lower electrode of a plasma chamber on which a wafer is supported and insulated results in the generation of negative charge on the oxide layer surface. The plasma conditions given above, e.g., 10 sccm of argon flow, 150 W RF power, 10 mT pressure, and 1000 V DC bias, can be employed here for producing negative surface charge.

**[0136]** An asymmetric diode plasma reactor in which the wafer is mounted on the smaller electrode can also be employed to impart a negative electrical charge to an oxide layer surface. In this configuration, in, e.g., a reactive ion etcher or sputtering chamber, the wafer is mounted on the smaller electrode of the chamber to achieve an RF biasing of the electrode and resulting charging of the wafer surface. Using electrodes of differing areas in contact with the plasma results in a negative charge build up on the surface of an oxide layer on the wafer. Process conditions of, e.g., 30 W RF power to the bottom/smaller electrode, 30 mT of pressure, and 1 min of processing time in a sputtering chamber is sufficient to impart a negative charge to the surface of an oxide layer.

**[0137]** Negative charge can also be produced on an oxide layer by exposing the layer to a low energy electron beam. Conditions of, e.g., an accelerating voltage of about 100 eV and an emission current of about 1000  $\mu$ A can be employed. Exposure of the surface to the beam conditions results in a negative charging of the oxide.

**[0138]** Negative charge build-up on an oxide layer surface can further be produced by exposure of the oxide layer surface to an HF vapor process followed by storage in a vacuum environment for at least about 2 hours. The preliminary HF vapor process can be employed as an initial partial etch of the layer. The HF vapor process is found to fluorinate the oxide surface, with the resultingly exposed fluorine atoms becoming negatively charged by electrons in the vacuum environment, e.g., from an ion gauge or low energy electron beam.

**[0139]** It is to be recognized that there are a wide range of other processes for producing a negative surface charge on an oxide surface. The invention is not limited to a particular technique for producing a negative-charge build-up on an oxide layer surface.

#### EXAMPLES 29-30

**[0140]** Thermal oxide layers were produced on silicon wafers. Half of the oxide layers were rendered in a negative-charge activated state by exposing the oxide layers to a plasma environment of an argon flow rate of 20 sccm, a pressure of 30 mT, an RF power of 30 W, and a positively biased DC voltage applied to an electrostatically-clamped wafer holder with about 600 volts. The other oxide layers were rendered charge-free by a water rinse.

**[0141]** The oxide layers were subjected to HF vapor processes, all with an HF vapor partial pressure of 10 T, a water vapor partial pressure of 4 T, a total pressure of about 125 T and a total flow rate of 500 sccm. Each process was carried out at a different temperature.

**[0142]** FIG. 18 is an Arrhenius plot of etch rate, in Å/min, as a function of temperature, as-determined based on ellipsometric measurements taken during the vapor processes. As indicated by the data of the plot, etch processes in the sub-monolayer and monolayer regimes were not impacted by the negative oxide layer surface charging. The multilayer regime is found, however, to be significantly enhanced by the negative oxide layer surface charge.

**[0143]** It is also found, as further indicated by the plotted data, that the negative oxide layer surface charge results in an increase of the temperature of transition from the monolayer regime to the multilayer regime by about 20° C. This transition temperature shift is understood to result from an enhancement of reactant adsorption by reduced reactant vapor pressures for the etch processes carried out on the charged oxide surface.

**[0144]** It is contemplated in accordance with the invention that the various oxide layer charge conditions described above be directly measured. Such can be accomplished by conventional means for enabling a confirmation of the polarity of charge produced on a given oxide layer.

**[0145]** The examples given above demonstrate the advantages provided by the invention for controlling particular operating regimes of HF vapor processes. Sub-monolayer, monolayer, multilayer, and condensed layer operating regimes have been discovered by the inventors, and distinctive characteristics of each regime have been described to enable identification of the regimes. Specific pre-process steps are provided for enabling further control of the etch rate and for compensating for prior contamination.

**[0146]** For many applications, it is preferred in accordance with the invention to control an HF vapor process to proceed in the sub-monolayer or monolayer regimes. Being surface reaction rate limited, these regimes enable highly uniform etching, resulting in elimination of surface pitting and corresponding "haze" that is conventionally associated with etching in the multilayer regime. Furthermore, the formation of etch residue particulates is eliminated in the sub-monolayer and monolayer regimes by the complete and immediate evaporation of process products during an etch reaction.

**[0147]** Processes in the sub-monolayer and monolayer regimes are found unexpectedly to proceed uniformly, even on silicon wafer surfaces exhibiting prior hydrocarbon contamination, when a first step of dry ice cleaning is performed on the wafer surface in accordance with the invention. Although the ice jet cleaning may not completely remove surface contaminants, it is found that the sub-monolayer and monolayer processing regimes of the invention are rendered repeatable and predictable by a first ice jet cleaning step, contrary to conventional wisdom.

**[0148]** The sub-monolayer and monolayer HF vapor process regimes are characterized by an oxide etch rate on the order of about 5 nm/min, enabling a high degree of control of processing, e.g., to avoid undercutting of thick films when removing thin native oxide layers. In addition, positive charging of an oxide surface can be carried out in accor-

dance with the invention to increase the sub-monolayer and monolayer etch rates while maintaining the benefits of these etch regimes. The selectivity of undensified TEOS oxide and thermal oxide to sub-monolayer and monolayer etching conditions is about 2-3:1, enabling the cleaning of sandwich structures without excessive undercutting of the TEOS film. The sub-monolayer and monolayer etch regimes are also found to not attack metal, e.g., aluminum or copper.

[0149] These advantages enable a process sequence, provided in accordance with the invention, in which a vacuum cluster tool is employed for via etching, contact cleaning of native oxide, and metal deposition. Referring to FIG. 19, there is shown such a configuration 100. Silicon wafers 102 are transferred between various vacuum chambers under vacuum via a robot 103 through a transfer chamber 105. The vacuum process chambers can include, e.g., a plasma etch chamber 107, ashing chamber 109, dry cleaning stations 111, 113, and a metal deposition chamber 115.

[0150] A wafer 102 having an oxide layer 104 formed upon it, can be processed to include a patterned photoresist layer 106 for defining a metal via. The wafer is then introduced to the cluster system and first processed in the plasma etch chamber 107 to etch the via pattern in the oxide layer. The wafer is then transferred to the ashing chamber 109 for removing the photoresist 106. At this point in the process, photoresist residue and metallic impurities 108 likely exist on the oxide layer 104 and a native oxide layer 110 likely exists on the surface of the silicon wafer. Such can be removed in situ by transferring the wafer to the dry cleaning chambers 111, 113 for a pretreatment of, e.g., UV exposure or ice jet cleaning, if desired and then removal of the residue and native oxide by an HF vapor process in the sub-monolayer or monolayer regime. Thereafter, the wafer is immediately transferred to the metal deposition chamber 115 for deposition of a metal layer 112 on a freshly cleaned wafer and oxide surface and via.

[0151] Referring to FIG. 20, in a further example of a vacuum cluster tool sequence provided in accordance with the invention, there is provided the ability to carry out metal line etching, polymeric residue removal, and interlayer dielectric deposition in situ under vacuum in one metal etch system 119. As with the system of FIG. 19, there is here enabled wafer transfer between various vacuum chambers under vacuum via a robot 103 through a transfer chamber 105. The vacuum process chambers can include, e.g., a plasma etch chamber 107, ashing chamber 109, dry cleaning stations 111, 113, and an interlayer dielectric deposition chamber 117.

[0152] A wafer 102 having, e.g., an oxide layer 120 has formed upon it a metal layer 122, e.g., a layer of aluminum. A layer of photoresist 123 is deposited and patterned corresponding to the metal line pattern desired for the metal layer 122. The wafer is introduced to the cluster system 119 and first processed in the plasma etch chamber 107 to pattern the metal layer 122. Typically, at the completion of the metal plasma etch, polymeric residue 124 is built up on the sidewalls of the etched metal lines. The wafer is then introduced through the cluster system to the ashing chamber 109 for removal of the photoresist. Even after this ashing step, polymeric sidewall residue is likely to remain.

[0153] At this point the wafer is transferred through the cluster system to the dry cleaning chamber 111 for a pre-

treatment of, e.g., UV exposure or ice jet cleaning, if desired, or Cl treatment. A hard polymer sidewall residue, typically consisting primarily of oxide, is often found to exist at this point. Removal of this residue is then carried out by transfer of the wafer to the second dry cleaning chamber 113 for completion of an HF vapor process in the sub-monolayer or monolayer regime. Thereafter, the wafer is immediately transferred to the interlayer dielectric deposition chamber 117 for deposition of an interlayer dielectric over the patterned metal layer 122.

[0154] As can be recognized, the functionality of the two vacuum cluster systems just described can be integrated to provide a large scale vacuum system for metal deposition, patterning, and interlayer dielectric deposition. Both of the two vacuum systems, and an integrated system in particular, are cost effective, environmentally friendly, and highly efficient. The relatively high temperature operating conditions of the sub-monolayer and monolayer HF vapor process regimes of the invention enable completely dry cleaning processes for the cluster systems. These regimes are well-suited for a vacuum cluster configuration because they inhibit condensation conditions, thereby enabling rapid vacuum pumping and eliminating the potential for system component corrosion.

[0155] For many applications, including the vacuum cluster configurations just described, it can be preferred to operate an HF vapor process under sub-monolayer, rather than monolayer, conditions. The sub-monolayer process regime was demonstrated in the experimental examples given above to be less temperature-sensitive than the monolayer regime. This decreased temperature sensitivity results in a broadening of the allowable process conditions for the regime, leading to greater ease of process control. Lack of process control in the monolayer regime can result in process nonuniformity and the possible formation of localized multilayer regime regions, these having dramatically higher etch rates and the likely formation of surface pitting and roughness as well as post process residue. Small-sized and large-aspect ratio features are particularly susceptible to such process artifacts. The controllable, slow-etch rate conditions of the sub-monolayer processing regime are found to inhibit these effects and therefore to be a more robust, reliable operation for manufacturing conditions. It is to be recognized, however, that the invention does not entirely dismiss monolayer and multilayer HF vapor processes. Particularly when combined with an initial surface charging or discharging step or an ice jet cleaning step, these processes can be successfully employed for a wide range of applications.

[0156] It is further to be recognized based on the discussion above that the HF vapor processes of the invention can be applied to a wide range of materials beyond the silicon, silicon dioxide and native silicon dioxide materials described. Other oxides and other semiconductor materials can be processed in accordance with the invention. Polymeric residue can be removed from metal and other lines, and carbon and other contamination, including residues, can be removed from substrate surfaces. The process conditions are not limited to semiconductor wafers; substrates of varying size and geometry can be accommodated by the processes of the invention.

[0157] This discussion highlights the wide range of applications of the HF vapor processes of the invention. Truly "all

dry" etch and cleaning processes are provided, whereby semiconductor processing efficiency, repeatability, ease of control, and environmental friendliness are all enhanced.

[0158] It is recognized, of course, that those skilled in the art may make various modifications and additions to the HF vapor processes of the invention without departing from the spirit and scope of the present contribution to the art. Accordingly, it is to be understood that the protection sought to be afforded hereby should be deemed to extend to the subject matter of the claims and all equivalents thereof fairly within the scope of the invention.

We claim:

1. A method for etching oxide on a semiconductor substrate, comprising exposing the oxide to anhydrous hydrofluoric acid vapor and water vapor at a substrate temperature greater than about 40° C., control of substrate temperature, hydrofluoric acid vapor pressure and water vapor pressure inhibiting formation of liquid on the substrate and forming on the substrate a sub-monolayer of etch reactant and product molecules by adsorption of etch reactant and product molecules at less than about 95% of oxide adsorption sites.

2. The method of claim 1 wherein the semiconductor substrate comprises a silicon wafer and the oxide comprises silicon dioxide.

3. The method of claim 1 wherein the substrate temperature, hydrofluoric acid vapor pressure, and water vapor pressure are controlled to etch the oxide at an etch rate of no more than about 100 Å/minute.

4. The method of claim 3 wherein the substrate temperature, hydrofluoric acid vapor pressure, and water vapor pressure are controlled to etch the oxide at an etch rate of no more than about 50 Å/minute.

5. The method of claim 1 wherein the substrate temperature, hydrofluoric acid vapor pressure, and water vapor pressure are controlled to etch the oxide at an etch rate, E.R., that is specified as:

$$E.R. = \frac{(1.059 \times 10^{12} e^{-15500/RT} \times 1.79 \times 10^{-9} e^{13000/RT} P_{HF} \times 9.107 \times 10^{-8} e^{10500/RT} P_{H_2O})}{((1 + 1.79 \times 10^{-9} e^{13000/RT} P_{HF} + 9.107 \times 10^{-8} e^{10500/RT} P_{H_2O})^2)}$$

where E.R. and pre-exponential factors are expressed in Å/min; where  $P_{H_2O}$  is partial pressure of water vapor and  $P_{HF}$  is partial pressure of HF vapor, both in Torr; where R is ideal gas constant, where T is temperature, and where all activation energies are expressed as Kcal/mol.

6. The method of claim 1 further comprising producing a positive electrical charge on the oxide prior to exposure of the oxide to the hydrofluoric acid vapor and water vapor.

7. The method of claim 1 wherein the substrate exposure temperature is controlled to be greater than about 100° C.

8. The method of claim 1 wherein the substrate exposure temperature is controlled by thermal conduction between the substrate and a substrate holder on which the substrate is supported.

9. The method of claim 1 wherein the anhydrous hydrofluoric acid vapor and the water vapor are maintained at a

temperature between about 30° C. and about 100° C. as they are delivered for exposure of the substrate.

10. The method of claim 1 wherein the substrate is exposed to the anhydrous hydrofluoric acid vapor and the water vapor in a process chamber maintained at a temperature of at least about 60° C.

11. The method of claim 1 wherein the substrate is first exposed only to the water vapor and then subsequently exposed to both the water vapor and the anhydrous hydrofluoric acid vapor at a specified start time for the oxide etching.

12. The method of claim 1 wherein the water vapor is provided at a flow rate of between about 5 sccm and about 100 sccm.

13. The method of claim 1 wherein the anhydrous hydrofluoric acid vapor is provided at a flow rate of between about 10 sccm and about 200 sccm.

14. The method of claim 1 wherein the anhydrous hydrofluoric acid vapor is provided at a partial pressure of between about 2.5 Torr and about 100 Torr.

15. The method of claim 1 wherein the water vapor is provided at a partial pressure of between about 1 Torr and about 50 Torr.

16. A method for cleaning a semiconductor substrate, comprising exposing the substrate to anhydrous hydrofluoric acid vapor and water vapor at a substrate temperature greater than about 40° C., control of substrate temperature, hydrofluoric acid vapor pressure and water vapor pressure inhibiting formation of liquid on the substrate and forming on the substrate a sub-monolayer of cleaning reactant and product molecules by adsorption of cleaning reactant and product molecules at less than about 95% of substrate adsorption sites.

17. The method of claim 16 wherein the substrate exposure temperature is controlled to be greater than about 100° C.

18. The method of claim 16 wherein the substrate exposure temperature is controlled by thermal conduction between the substrate and a substrate holder on which the substrate is supported.

19. The method of claim 16 wherein the anhydrous hydrofluoric acid vapor and the water vapor are maintained at a temperature of between about 30° C. and about 100° C. as they are delivered for exposure of the substrate.

20. The method of claim 16 wherein the substrate is exposed to the anhydrous hydrofluoric acid vapor and the water vapor in a process chamber maintained at a temperature of at least about 60° C.

21. The method of claim 16 wherein the water vapor is provided at a flow rate of between about 5 sccm and about 100 sccm.

22. The method of claim 16 wherein the anhydrous hydrofluoric acid vapor is provided at a flow rate of between about 5 sccm and about 200 sccm.

23. The method of claim 16 wherein the anhydrous hydrofluoric acid vapor is provided at a partial pressure of between about 2.5 Torr and about 100 Torr.

24. The method of claim 16 wherein the water vapor is provided at a partial pressure of between about 1 Torr and about 50 Torr.

25. The method of claim 16 wherein cleaning of a semiconductor substrate comprises cleaning of a metal contact region of the semiconductor substrate; and wherein exposure of the substrate to anhydrous hydrofluoric acid

vapor and water vapor comprises exposure of the metal contact region to anhydrous hydrofluoric acid vapor and water vapor.

**26.** A method for cleaning a metal structure on a semiconductor substrate, comprising exposing the metal structure to anhydrous hydrofluoric acid vapor and water vapor at a substrate temperature greater than about 40° C., control of substrate temperature, hydrofluoric acid vapor pressure, and water vapor pressure inhibiting formation of liquid on the substrate and forming on the substrate a sub-monolayer of cleaning reactant and product molecules by adsorption of cleaning reactant and product molecules at less than about 95% of substrate adsorption sites.

**27.** The method of claim 26 wherein the substrate exposure temperature is controlled to be greater than about 100° C.

**28.** The method of claim 26 wherein the substrate exposure temperature is controlled by thermal conduction between the substrate and a substrate holder on which the substrate is supported.

**29.** The method of claim 26 wherein the anhydrous hydrofluoric acid vapor and the water vapor are maintained at a temperature of between about 30° C. and about 100° C. as they are delivered for exposure of the substrate.

**30.** The method of claim 26 wherein the substrate is exposed to the anhydrous hydrofluoric acid vapor and the water vapor in a process chamber maintained at a temperature of at least about 60° C.

**31.** The method of claim 26 wherein the water vapor is provided at a flow rate of between about 5 sccm and about 100 sccm.

**32.** The method of claim 26 wherein the anhydrous hydrofluoric acid vapor is provided at a flow rate of between about 10 sccm and about 200 sccm.

**33.** The method of claim 26 wherein the anhydrous hydrofluoric acid vapor is provided at a partial pressure of between about 2.5 Torr and about 100 Torr.

**34.** The method of claim 26 wherein the water vapor is provided at a partial pressure of between about 1 Torr and about 50 Torr.

**35.** The method of claim 26 wherein the metal structure comprises an aluminum structure.

**36.** The method of claim 26 wherein cleaning of the metal structure comprises removing etch residue from the metal structure.

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