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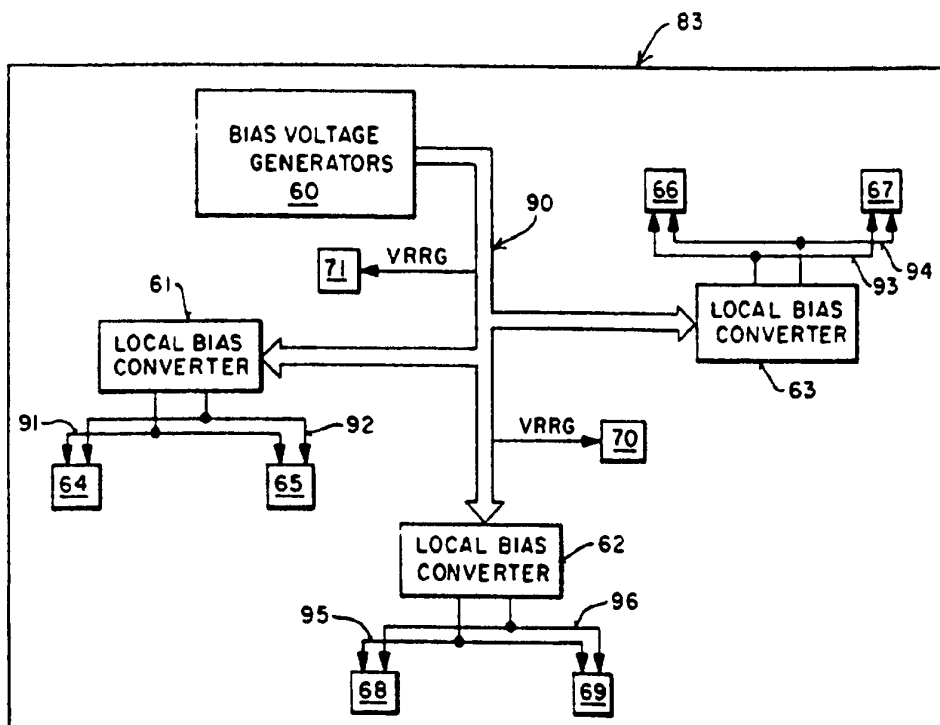
(57) Abstract

The present invention describes a bias potential distribution system which provides bias potentials to MOS devices while ensuring the devices' operating conditions remain constant over temperature, process, and power supply fluctuations. Further, bias potentials are generated at one main location within the logic circuit and then distributed throughout the logic circuit to all of the MOS devices or to bias voltage conversion circuits.

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1

BIAS VOLTAGE DISTRIBUTION SYSTEM

RELATED APPLICATIONS

This application is related to U.S. Patent Application Serial
No. 842,922 which is a continuation-in-part of U.S. Patent No.

5   5,124,580, which are assigned to the assignee of the present
invention.

FIELD OF THE INVENTION

The present invention relates to the field of logic circuits, and
particularly to bias potentials within logic circuits.

10   ## BACKGROUND OF THE INVENTION

The basic element of all emitter coupled logic (ECL) gates or
current mode logic (CML) gates is a differential amplifier. Therefore,
there is a significant incentive to fine tune the operation of the
differential amplifier, thus improving the operation of the overall ECL

15   or CML logic gate.

The differential amplifier typically has two emitter-coupled
bipolar transistors; each having a resistive load coupled between their
collectors and a power supply. The common emitters of the transistor
pair are coupled to a current source. Both the resistive loads and

20   current source are typically semiconductor resistors. However, it is
also common to utilize a bipolar transistor that is biased in its linear
region for the current source. The base of one of the emitter-coupled

2

pair is coupled to a reference potential and the base of the other emitter-coupled transistor is coupled to an input signal.

The differential amplifier functions such that it compares the input signal to the reference potential. Depending on whether the
5   input signal is less than or greater than the reference potential, the differential amplifier steers the current established by the current source through one of the emitter-coupled transistors. This current flow causes a corresponding voltage drop across only one of the load resistors. At the same time, because no current flows through the
10   other transistor, the collector of that transistor remains at approximately ground potential. The output of the differential amplifier is typically taken at the collector of each of the emitter-couple transistors. Thus one collector is always at a voltage potential corresponding to a low logic level and the other collector is
15   at a voltage potential corresponding to a high logic level.

As is commonly known in the industry, ECL/CML gates are desirable because they provide the fastest bipolar logic available. However, the main drawback of the ECL/CML differential amplifier as described above is that they consume the most power of
20   conventional logic technologies and can be adversely effected by temperature and power supply variations.

One method of improving the operation of the differential amplifier described above is suggested in U.S Patent No. 5,124,580 assigned to the assignee of the present invention. U.S. Patent No.

3

5,124,580 describes a bipolar complementary metal-oxide semiconductor (BiCMOS) ECL/CML gate. The basic bipolar ECL/CML gate is improved by replacing the current source comprising a resistive semiconductor with an MOS device biased to

5   function as a current source, i.e., operated in its saturation region.

Further, the two load resistors coupled to the emitter-coupled pair are replaced by two linearly operated MOS devices. The MOS devices are coupled between the collector of each of the emitter-coupled pair and a power supply. Both of the gates of the

10   MOS load devices are coupled to a second common bias potential. The value of the load resistance for the MOS load devices is determined by the second bias potential and the size of the MOS devices. The advantage of utilizing a linearly operated MOS device is that their resistance can be easily adjusted by changing the potential

15   applied to their gate, i.e., the second bias potential. In this manner, the effect of variations such as temperature and power supply on the ECL\CML logic gate output voltage can be offset by proper control of the bias potential on the gate of the MOS load devices. U.S. Patent Application Serial No. 842,922 which is the continuation-

20   in-part of U.S. Patent No. 5,124,580 and is also assigned to the assignee of the present invention, discloses a further improvement to the basic bipolar ECL/CML gate. The BiCMOS ECL/CML gate disclosed in U.S. Patent Application Serial No. 842,922 improves the linearity of the MOS load resistors. In one disclosed embodiment a

25   plurality of parallel MOS devices are coupled between the collector of each of the emitter coupled pair and the power supply. The gates

4

of each of the devices are coupled to a switching network. The switching network determines if the gate of each of the parallel MOS load devices are coupled to a bias potential or a deactivating voltage. The parallel MOS devices are linearly biased such that the effective resistance of the parallel combination is determined by the number and size of load devices coupled to the bias potential.

In both of the BiCMOS ECL/CML gates as disclosed in U.S. Patent No. 5,124,580 and U.S. Patent Application Serial No. 842,922 it is important that the MOS load devices and current sources remain biased at a particular operating point, (i.e., linear for the load devices and saturated for the current source). Consequently, the bias voltages supplied to the gates of these MOS devices needs to remain constant over variations due to effects of temperature, supply voltage and process fluctuations.

U.S. Patent No. 5,124,580 discloses a feedback circuit for supplying stable bias voltages to the gates of the load and current source MOS devices. The feedback circuit provides bias potentials such that the MOS devices remain biased at their respective operating points independent of fluctuations in varying operating conditions. In addition, the feedback circuit allows the added advantage of having the ability of adjusting the voltage swing of the output of the ECL gate.

In a large logic circuit containing many logic gates it is desirable to provide compensated bias voltages to each gate. This

5

would require the inclusion of a feedback circuit, as described above, in the design of each logic gate. However, each feedback circuit includes an operational amplifier and other space consuming circuitry. As a result, including a feedback circuit with each logic gate may not

5   lend itself to a space efficient logic circuit design. In addition, adding the feedback circuitry may become prohibitive in some cases where minimal space is available.

What is needed is a space efficient means for providing bias potentials for a BiCMOS ECL/CML logic gate that ensures that

10   specific operating points are maintained for MOS load and current source devices.

SUMMARY OF THE INVENTION

         The present invention describes a bias potential distribution system. The distribution system provides bias potentials to MOS

15   devices while ensuring the devices' operating conditions remain constant over temperature, process, and power supply fluctuations. Further, bias potentials are generated at one main location within the logic circuit and then distributed throughout the logic circuit to all of the MOS devices or to bias voltage conversion circuits. Since the

20   need to provide compensated bias potentials at local device or conversion locations within the logic circuit is eliminated space is conserved. In addition, bias voltage conversion circuits that are in close proximity to logic gates to be biased are less susceptible to noise.

6

The distribution system comprises a main bias potential generator for providing first and second temperature, process, and power supply compensated bias potentials. The main generator is divided into two circuits. The first circuit generates a first bias

5   potential. This circuit includes a reference MOS device and a feedback circuit which provides compensation in response to operating condition fluctuations. The first bias potential is distributed and coupled to the gates of other remote MOS load devices located within the logic circuit. The remote MOS load devices coupled to this first

10   bias potential have the same resistivity as the reference MOS device if they have the same size since they are biased by the same potential. If the remote MOS load device is a different size, then its resistivity is proportional to the resistivity of the reference MOS device; the ratio of the resistivity and the size being the same. The remote MOS load

15   devices have the added benefit of being biased such that it functions independent of variations in operating conditions without the added space consuming feedback circuitry at the remote locations.

In one embodiment, the reference load comprises a first set of parallel MOS reference load devices. The gates of the parallel

20   devices are coupled to a first switching network. The switching network either couples the gates to the first bias potential or a deactivating potential, (VDD). A first control signal determines which of the gates are coupled to the first bias potential and hence which of the parallel devices are on and biased in their linear regions.

25   The resistance of the "on" devices determines the overall resistance of the parallel combination. Selection of the resistance of the parallel

7

devices also determines the value of the first bias potential.

This first bias potential is then distributed to other remote similar sets of parallel MOS devices which provide resistive loading to other circuitry. The gates of the remote parallel devices are also coupled to switching networks having a second control signal. The second control signal functions in the same manner as the first control signal, i.e., selecting the resistivity of the parallel combination. Since the reference parallel devices and remote parallel devices are both biased by the first bias potential, the resistivity of the remote parallel combination is equal or proportional to the resistivity of parallel reference devices; depending on their relative size. The first and second control signals determine the proportional relationship between the reference and remote sets of parallel load devices and hence, the resistivity of the remote parallel load devices.

The second bias potential is generated in the second circuit within the main bias potential generator. First and second bias potentials are distributed to bias voltage conversion circuits within the logic circuit. The bias voltage conversion circuits provide bias voltages to ECL/CML logic gates within the logic circuit such that the logic gates' load and current conditions are the same as or proportional to that of the load and current conditions within the main bias potential generators. Bias voltage conversion circuits are located relatively closely to the logic gates that they are biasing so that locally converted bias voltages need to travel a shorter distance than the main first and second bias potentials. As a result, locally generated bias

8

voltages are not as susceptible to noise.

The distribution system of the present invention also includes the capability of varying first and second main bias voltages depending on process variations and voltage swing requirements

5   through selected control signals. In addition, local conversion circuits have the capability of adjusting locally converted bias voltages to select specific current conditions of the logic circuit it is biasing. Finally, since compensation for temperature, process, and power supply variations is performed in the main bias potential generators,

10   the need for additional operational amplifiers at local ECL/CML gate locations is obviated.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the bias voltage distribution system of the present invention.

15   Figure 2 is a block diagram illustrating the VRRG and VFFG (N) bias voltage generators of the present invention.

Figure 3 is a circuit schematic illustrating a simplified VRRG generator biasing a remote MOS load device.

Figure 4 is a circuit schematic of a VRRG generator having the

20   capability of adjusting the VRRG bias voltage by selecting PC control codes.

9

Figure 5 is a circuit schematic of a remote resistive load network having the capability of selecting effective device size by selecting RC control codes.

Figure 6 is a simplified circuit schematic of a VFFG generator
5   and V_{II} converter of the present invention coupled to a BiCMOS logic gate utilizing MOS devices for loading and for its current source.

Figure 7 is a schematic of a VFFG generator of the present invention having the capability of adjusting the value of VFFG bias voltages through control code PC.

10   Figure 8 is a schematic of a V_{II} converter of the present invention having the capability of selecting different resistive loads through the RC2 code and different values of VFFG and V(L) through the VC code.

Figure 9 is a schematic of a BiCMOS logic gate as disclosed
15   in U.S. Patent Application Serial No. 842,922 having a parallel PMOS load network and illustrating how V_{II} and VRR bias voltages are coupled to it.

DETAILED DESCRIPTION

In the following description, a bias potential distribution
20   system is described in which numerous specific details are set forth, such as specific conductivity types, circuit configurations, etc., in

10

order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well-known structures and circuits have not been

5   shown in detail in order to avoid unnecessarily obscuring the present invention.

The present invention is a bias potential distribution system that provides bias potentials to many ECL/CML gates within a logic circuit. These potentials are generated in a central location and are

10   temperature, power supply and process variation compensated. In addition, the system includes the flexibility to externally control and scale voltage swing values and power dissipation requirements for individual ECL/CML logic gates within a logic circuit consisting of many ECL/CML gates.

15   Figure 1 shows the block diagram of a logic circuit 83 having the bias potential distribution system of the present invention. As can be seen main bias voltage generator 60 is located in a single location within logic circuit 83. Bias voltage generator 60 provides reference bias voltages, VRRG and VFFG, which are temperature, power

20   supply and process variation compensated. These reference voltages are outputted onto bus 90 and coupled to many local bias converters 61 - 63 distributed throughout circuit 83. The local bias converters transform the VFFG and VRRG bias voltages into the two bias potentials, VRR1 - VRR4 and V_{II}, which then can be utilized to bias

25   local ECL/CML gates 64 - 69 on lines 91 - 96.

11

In addition, VRRG is distributed to and biases remote parallel load devices 70 within logic circuit 83.

Figure 2 shows the block diagram of the reference bias voltage generator 60. Generator 60 is comprised of the VRRG bias voltage
5   generator 100 and N VFFG bias voltage generators 101 - 103, where N is an integer greater than or equal to 1. VRRG is outputted by generator 100 onto lines 104 and 105. Line 104 is coupled directly to bus 90 and is then distributed to local bias generators 61 - 63 and resistive loads 70. VRRG is also coupled to all of the VFFG bias
10   voltage generators on line 105 and contributes in the generation of the VFFG bias voltages. The VFFG bias voltages are outputted onto lines 106 - 108 and coupled to bus 90 to be distributed to local bias converters 61 - 63.

The VRRG Generator

15   To illustrate how the bias distribution system of the present invention functions to provide bias voltages to remote load devices, the main VRRG bias generator and a single load device are shown in a simplified embodiment in Figure 3.

As can be seen, main VRRG generator 100 is shown
20   comprising a single PMOS device 199 of a specific size X. The drain of 199 is coupled to a current source IREF1 and to the positive input of operational amplifier (OP AMP) 153. Current source IREF1 is also coupled to a first power supply, VSS. The negative input of OP AMP 153 is coupled to reference potential VREF1. The source of

12

199 is coupled to a first power supply VDD.

Generator 100 functions such that OP AMP 153 generates bias
voltage, VRRG, in response to differences between its negative and
positive inputs. In other words, OP AMP 153 generates VRRG so as

5   to bias device 199 such that its drain is at the same potential as
VREF1 with a source-to-drain current of IREF1. By forcing device
199 to have specific current and voltage characteristics (in its linear
region), device 199 is being biased to have a constant resistivity. The
resistivity of device 199 is dependent on the values of VREF1 and

10   IREF1. If any changes in operating conditions occur, VRRG adjusts
itself accordingly so as to maintain the operating point of device 199.

Utilizing VRRG to Bias Remote Resistive Loads

After VRRG is generated in one central location, i.e., in main
bias voltage generator 60, it is distributed to the gates of remote MOS

15   load devices 70 via bus 90. Figure 3 illustrates VRRG being coupled
to the gate of remote PMOS load device 198. The source of device
198 is coupled to VDD and its drain is coupled to any circuitry that
may utilize or require some type of resistive loading. If remote
device 198 is the same size as reference device 199 then VRRG biases

20   both devices 198 and 199 to have the same conductivity. In the case
where the sizes of 198 and 199 are different, having some
proportional relationship, then the conductivity of device 198 will also
have the same proportional relationship with the conductivity of device
199. The remote devices are unaffected by fluctuations in operating

13

conditions since VRRG is adjusted so as to compensate itself for changes in operating condition.

As shown in Figure 3, VRRG may be distributed on line 91 to many other MOS load devices located throughout the circuit indicated

5   by L1 - L3. Similar to device 198, the conductivity of load devices L1 - L3 depend on their size.

Adjustable VRRG Generator

As noted above, the value of VRRG is set by the device size of 199 and the values of IREF1 and VREF1. However, it may be

10 desirable to adjust VRRG to account for variations in the voltage and current characteristics of MOS devices due to manufacturing process fluctuations. Figure 4 illustrates a VRRG main bias generator that is not restricted to a single value of VRRG.

As shown, the reference load device 199 shown in Figure 3 is

15 replaced by a set of parallel PMOS devices 117 - 120, (composite device 199'), having their sources coupled to VDD and their drains coupled to the positive input of OP AMP 153'. The positive input of OP AMP 153' is also coupled to IREF1'. The negative input of OP AMP 153' is coupled to VREF1'.

20 The gates of devices 117 - 120 are coupled to a switching network comprising CMOS inverters 113 - 116 through lines VRR(0) - VRR(3). The inputs of inverters 113 - 116 are controlled by process

14

control signals, PC(0) - PC(3). The output of amplifier 153', which supplies VRRG, is coupled to the CMOS switching network, along with VDD.

5   The CMOS switching network provides a digital switching means to control and drive PMOS load network 117 - 120. The gates of devices 117 - 120, lines VRR(0) - VRR(3), are switched to either VDD (device "off" voltage) or VRRG (device "on" voltage), depending on input code PC(0) - PC(3). Devices that are biased "on" by VRRG contribute to the total linear conductance of the PMOS
10   network. In other words, PC(0) - PC(3) determine the effective size and conductance of the PMOS network.

       VRRG generator 85, functions in the same manner as the simplified VRRG generator shown in Figure 3. Specifically, once the effective size of composite device 199' is set by control signals PC(0)
15   - PC(3), then VRRG generates a bias voltage so as to decrease the difference between its positive and negative inputs. In doing this, OP AMP 153' supplies a bias voltage so as to force composite device 199' to have current and voltage characteristics determined by VREF1 and IREF1, depending on the size of composite device 199'.

20   Thus, the PC signal can adjust VRRG by selecting the effective size of composite device 199'. Recognize that composite device 199' may comprise any number of devices. Furthermore, devices 117 -120 may all be of the same size, or may be implemented as a combination of different relative device sizes. Figure 10 shows the currently

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preferred device size combination wherein device 120 has a fixed size (denoted as size = X), device 119 has a size 2X, device 118 has a size 4X, and device 117 has a size 8X larger than device 120. This particular combination of device sizes provides the user with equal
5   increments of 16 different resistance values and 16 different VRRG values.

As described above, VRRG can then be distributed to the gates of other remote load devices within a logic circuit so as to bias them in the same manner or proportional to composite device 199'.
10   However, instead of coupling VRRG to a many remote loads each comprising a single device as illustrated in Figure 3, VRRG may be coupled to many remote loads comprising a parallel PMOS load network similar to composite device 199' shown in Figure 4.

Figure 5 shows a remote resistive load comprising a set of
15   parallel PMOS devices, i.e., composite device 198'. Composite device 198' is coupled to a CMOS switching network 130. Although network 130 is not shown in detail, it is to be understood that it functions in the same manner as the CMOS switching network shown in Figure 4.

20   Control signals RC(0)-RC(3) control the effective size of composite device 198' by causing switching network 130 to couple either VRRG ("on" voltage) or VDD ("off" voltage) to lines VRR(0)-VRR(3). If the selected size of 198' is the same as 199' then device 198' and 199' will be biased to have the same resistivity. If

16

their sizes are different then their conductivity will have the same proportional relationship as the proportional relationship between composite device sizes 199' and 198'.

As with the VRRG generator shown in Figure 4, the device sizes are scaled so as to provide the user with equal increments of 16 different resistance values.

As can be seen, the present invention allows on-line adjustments of bias voltage VRRG by changing the PC code. Also, the ratio between the RC and PC codes along with the reference bias current and voltage, determine the conductance of the remote device.

The VFFG Generator

To illustrate how the bias distribution system of the present invention functions to provide bias voltages to remote logic gates, main VFFG bias generator 103, local V_{tt} and VRR bias converter 61, and logic gate 64 are shown in simplified forms in Figure 6.

Main VFFG generator 103 is shown comprising two PMOS devices, 200 and 201, coupled in series. The source of PMOS devices 200 is coupled to VDD and its drain is coupled to the negative input of OP AMP 154. The drain of PMOS device 201 is coupled to an NMOS device 141. The gate of device 141 is coupled to its drain. The source of device 141 is coupled to VSS.

Device 200 is biased by VRRG and device 201 is biased by the

17

output voltage of OP AMP 154, VFFG(N). The positive input of OP AMP 154 is coupled to VL(N). The relative device sizes of 200 and 201 are such that device 201 is typically much wider that device 200. VRRG biases device 200 in its linear region having some resistivity

5   determined by its size and VRRG.

VFFG Generator 103 functions such that OP AMP 154 generates bias voltage, VFFG, in response to differences between its negative and positive inputs. Bias voltage, VFFG, biases device 201 in its saturation region such that it functions as a current source. The

10   current that VFFG forces device 201 to generate is such that the negative input of OP AMP 154, (node 142A) is at the same voltage potential as OP AMP 154's positive input, i.e., VL(N). The current generated by device 201 is the current required by device 200 to force its drain voltage to equal the logic swing voltage VL(N).

15   Device 141 has a negligible affect on the VFFG generator and only functions to establish the same circuit conditions as in other related circuits to be described.

As with the VRRG generator, if any changes in operating conditions occur, OP AMP 154 responds by adjusting VFFG so as to

20   bias device 201 such that node 142A is maintained at a voltage potential equal to VL(N).

18

Converting VFFG and VRRG to Bias Voltage, V_{II}

Figure 6 shows a local bias converter 61. It is to be understood that although only a single local bias converter is shown in Figure 6, many local converters may be distributed throughout a logic circuit and coupled to main VFFG and VRRG generators.

As can be seen in Figure 6, bias voltages VRRG and VFFG are coupled to the gates of device 202 and device 203, respectively. VRRG biases device 202 in its linear region such that it functions as a resistive load having some resistivity. VFFG biases device 203 as a current source such that it establishes a current though devices 202, 203 and 241 having a specific current density established by the feedback circuit in the VRRG generator circuit 103.

Note that the device size ratio for devices 202 and 203, in local converter 61, is the same as that of devices 200 and 201, in VFFG generator 103. Since the same ratio exists between devices 200/201 and 202/203, and since the current established through both sets of devices is determined by VFFG(N), the current density established through both sets is the same. As a result, the voltage potential at node 142B in local converter 61 is the same as the voltage potential at node 142A in the main VFFG generator, i.e., VL(N).

Device 241 is configured similar to device 141 of VFFG generator 103. Specifically, device 241 is configured as half of a current mirror. When the gate/drain node of device 241 is coupled to the gate of another device having the same size, that other device

19

will be biased to have the same current as device 241. The gate/drain node potential of device 241 is referred to V_{II}.

Utilizing V_{II} and VRRG to Bias a Remote Logic Gate

A simplified remote logic gate 64 is shown in Figure 6. As can be seen, it comprises PMOS load devices 204 and 205 coupled to emitter coupled pair 21 and 22. The emitters of device 21 and 22 are coupled to the drain of NMOS device 24. The source of device 24 is coupled to VSS. Load devices 204 and 205 are the same size and are biased in their linear region and provide the load resistance for the logic gate. Current source device 24 is biased in its saturation region such that it provides a constant current.

Bias voltage VRRG provides the bias voltages to load devices 204 and 205 and bias voltage V_{II} provides the bias voltage to current source device 24. Referring to Figure 6, VRRG is coupled to the gate of each of devices 204 and 205 and V_{II} is coupled to the gate of device 24.

Since device 24 is the same device size as device 241, V_{II} biases device 24 to generate the same current through it as device 241. And, since load devices 204 and 205 are the same size as device 202, the corresponding voltage drop across each of them will be the same for the same current generated by current mirror devices 24 and 241. Therefore, the low logic voltage potential at nodes 30 and 31 in logic gate 64 will be the same as node 142B in remote generator 61. The potential established on 142B is also the same as the potential established at node 142A, i.e., VL(N).

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In other words, node 30 will be at a potential equal to VL(N) if Vin significantly exceeds Vbias and node 31 will be at a potential equal to VL(N) if Vbias exceeds Vin. As can be seen, VL(N) determines the voltage swing of logic gate 64. In addition, if the

5   resistance of device 202 is made to be the same as the resistance of load devices 204 and 205, VL(N) is unaffected if the load resistance of the logic gate is changed or varied.

Since bias voltages VRRG and VFFG are adjusted when fluctuations in operating conditions occurs, V_{π} is correspondingly

10   adjusted so as to ensure that the voltage swing of the logic gate does not vary.

Adjustable VFFG Generator

Figure 7 illustrates a VFFG generator that has the added flexibility to adjust the bias voltage VFFG independent of a specific

15   process code. This is accomplished by varying the effective device sizes of composite devices 200' and 201'.

Referring to Figure 7, switching networks 131 couples either VRRG or VDD on lines VRR (0) - VRR(3) to the gates of devices 133 - 136. This is done by selecting the process control signal PC(0)

20   - PC(3). Thus, control signals PC(0) - PC(3), determine the device size and resistivity of composite device 200'. Similarly, switching network 132 couples either VFFG or VDD to lines VFF(0) - VFF(3) (i.e.. the gates of devices 137 - 140). This is accomplished by

21

selecting process control signals PC(4) - PC(7). Thus, PC(4) - PC(7) determine the device size of composite device 201'.

OP AMP 154' functions to generated bias voltage VFFG in response to differences on its input as described previously for the

5   simplified VFFG generator in Figure 3. Bias voltage VFFG biases composite device 201' such that node 142A' is equal to voltage swing potential VL(N).

As can be seen, by adjusting device sizes of composite devices 200' and 201', VFFG will change accordingly, as will the current

10   though devices 200' and 201'. However, the voltage potential at node 142A' will always be forced to VL(N).

As described above, a single VFFG bias voltage is generated having an associated voltage swing potential, VL(N). However, in certain applications it may be useful to have the capability to be able

15   to select from many voltage swing values. As can be seen in Figure 2, main bias voltage generator 60 of the present invention generates many VFFG bias voltages each having an associated voltage swing reference, VL(N). A different VL(N) is coupled to each VFFG generator on lines 109 - 111 so as to generate a different VFFG on

20   lines 104, and 106 - 108. Each of these VFFG bias voltages along with VRRG may then be coupled to multiple local bias converters 61 so as to generate a V_{II} that forces a voltage swing potential, VL(N), for that particular VFFG.

22

Figure 8 shows an embodiment of a local bias converter which is coupled to the multiple VFFG signals coupled from main bias generator 60. The local converter has the capability of selecting one of the VFFG bias voltages and its associated VL(N). Referring to

5   Figure 8, a multiplexer, MUX 300, is shown having eight inputs, VFFG(0) - VFFG(7). Each VFFG(N) for biasing composite device 203' so as to force different VL(N) value at node 142B'.

Control signals VC(0) - VC(3) determine which VFFG(N) is coupled to input 153 of switching network 144. For instance, in one

10   embodiment, if VC(0) - VC(3) is "000" then bias voltage VFFG(0) is selected.

Switching networks 143 and 144 function the same as previously described switching networks. Network 143 couples either VRRG or VDD to the gates of devices 145 - 148 on lines VRR(3) -

15   VRR(0). Control signals RC2(0) - RC2(3) select the effective device size of composite device 202' and consequently its conductivity. Switching network 144 couples either the selected VFFG or VDD to the gates of devices 149 - 152 on lines VFF(3) VFF(0). Control signals RC2(4) - RC2(7) select the effective device size of composite

20   device 203' and consequently the current flowing through devices 202' and 203'.

If the ratio between composite devices 200'/201' (shown in Figure 7) and 202'/203' (shown in Figure 8) is the same then the voltage potential at node 142B' in the local bias converter (Figure 8),

23

is the same as the voltage potential at node 142A' in the main VFFG

generator (Figure 7), i.e., VL(N). As can be seen, the local bias

converter in Figure 8 allows for selection of a particular VL(N) with

the VC code. Consequently, the V_{II} supplied by the local bias

5   converter forces the current device in the logic gate to generate a

current such that the voltage swing of that logic gate is the selected

VL(N).

Figure 9 illustrates a BiCMOS logic gate as described in U.S.

Patent Application Serial No. 842,922. The logic gate comprises two

10   PMOS load networks each comprising four parallel PMOS devices 71

- 74 and 75 - 78. The drains of all of the devices are coupled to

VDD. The sources of devices 71 - 74 are coupled to the collector of

NPN device 21, (node 30) and the sources of devices 75 - 78 are

coupled to the collector of NPN device 22, (node 31). Their gates are

15   coupled to bias voltages VRR(0) - VRR(3) as illustrated. The emitters

of devices 21 and 22 are coupled to the drain of NMOS device 24.

The source of device 24 is coupled to VSS and its gate is biased by

V_{II}.

The bias voltages, V_{II} and VRR, that are utilized to bias the

20   logic gate shown in Figure 9 are generated by a local bias converter

such as shown in Figure 8. The voltage that biases parallel devices

145 - 148, VRR(0) VRR(3) (Figure 8), is also coupled to the gates of

load devices 71 - 74 and 75 - 78 (Figure 9). As a result, the load

devices of the logic gate have the same resistivity as composite device

25   202'. Further, the current flowing through composite device 202' is

24

the same as the current flowing through the logic gate's load devices since V_{II} is biasing device 24. Therefore, the voltage at node 30 and 31 (Figure 9) is the same as the voltage at node 142B' (Figure 8).

As can be seen, bias voltages VRR and V_{II} are derived from
5   main bias voltages VRRG and VFFG. Consequently, if VRRG and VFFG are compensated when variations in operating conditions occur, then VRR and V_{II} will also be adjusted accordingly.

The resistive load values for the logic gate shown in Figure 9 may be selected by selecting an appropriate control code RC2(0) -
10   RC2(3) while still maintaining the same V(L) value. In addition, logic swing and current may be selected for the same gate by selecting the desired VC code.

It should be noted that a logic circuit may contain many local bias converters, each converter may be set so as to provide different
15   loading and voltage swing conditions. Thus, the present invention offers an extremely flexible bias distribution system. And, since local converters are located in close proximity to logic gates, sensitive V_{II} bias voltages travel shorter distances so that they are less susceptible to noise.

20   It can also be seen that the distribution system of the present invention is able to supply compensated bias voltages to remote logic gates with minimal additional circuitry while still maintaining the advantages of the invention as disclosed and claimed in U.S. Patent

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No. 5,124,580 and U.S. Patent Application Serial No. 842,922. In addition, the distribution system gives the flexibility to adjust bias voltages to compensate for process variations through control signal PC in the VRRG generator.

5   Finally, the present invention provides a flexible distribution system that can be tailored to particular power and logic swing needs.

26

CLAIMS:

We Claim:

1.   In a circuit having a plurality of MOS load devices having their drains coupled to a first working potential, each of said

5   MOS load devices having an associated size and resistivity, a bias potential distribution system for biasing said plurality of load MOS devices comprising:

means for generating a bias potential having a reference MOS device its drain being coupled to said first working potential,

10   said reference MOS device having an associated size, said generating means functioning to provide said bias potential to the gate of said reference MOS device such that said reference MOS device has a specific resistivity despite fluctuations in operating conditions within said circuit, said generating means being coupled to a control signal

15   and said bias potential being variably responsive to said control signal;

a means for coupling said bias potential to the gates of said plurality of MOS load devices, wherein said associated resistivity of said plurality of said MOS load devices remains linear despite fluctuations in said operating conditions of said circuit, and wherein

20   said associated resistivity of said plurality of load MOS devices may be varied by varying said control signal.

2.   The distribution circuit as described in claim 1 wherein said proportional relationship between said associated size of said each of said plurality of MOS load devices and said associated size of said

25   reference MOS device is the same as said proportional relationship between said associated resistivity of said each of said plurality of

27

load MOS devices and said specific resistivity of said reference MOS device.

3.   The distribution circuit as described in claim 2 wherein said each of said plurality of MOS load devices and said MOS

5   reference device each comprise a p-channel metal-oxide-semiconductor (PMOS) transistor.

4.   In a circuit having at least one resistive load network comprising a plurality of MOS devices coupled in parallel and a first switching means, each of said drains of said plurality of MOS devices

10   being coupled to a first operating potential, said at least one resistive load network having an associated size and resistivity, said first switching means in response to a first control signal determining said associated size of said at least one resistive load network, a bias potential distribution system for providing a bias potential to said at

15   least one resistive load network comprising:

means for generating a bias potential, said generating means having a reference resistive load network comprising a plurality of reference MOS devices coupled in parallel and a second switching means, each of the drains of said plurality of reference MOS devices

20   being coupled to said first operating potential, said reference resistive load network having an associated size, said second switching means in response to a second control signal determining said associated size of said reference resistive load network, said generating means functioning to provide said bias potential to said second switching

25   means such that said reference resistive load network has a specific

28

resistivity, said generating means maintaining said specific resistivity despite fluctuations in operating conditions within said circuit by adjusting said bias potential, said bias potential being variably responsive to said second control signal;

5   a means for coupling said bias potential to said at least one resistive load network, wherein said associated resistivity of said at least one resistive load network remains linear despite fluctuations in said operating conditions of said circuit, and wherein said associated resistivity of said at least one resistive load network may be varied by

10   varying said first and said second control signals.

5.   The distribution circuit as described in claim 4 wherein said proportional relationship between said associated size of said resistive load network and said associated size of said reference resistive load network is the same as said proportional relationship

15   between said associated resistivity of said resistive load network and said specific resistivity of said reference resistive load network.

6.   The distribution circuit as described in claim 5 wherein said each of said plurality of MOS devices and each of said plurality of reference MOS devices each comprise a PMOS transistor.

20   7.   In a circuit comprising at least one BiCMOS logic gate, said BiCMOS logic gate comprising an emitter-coupled pair of bipolar transistors for differentially comparing an input signal with a first reference potential, each of the collectors of said pair of bipolar transistors being coupled to one of a pair of resistive load MOS

29

devices each having an associated resistivity, each of said emitters of said bipolar transistors being coupled to a common current source MOS device, a distribution system for providing a first bias potential to said pair of load MOS devices and a second bias potential to said

5   common current source MOS device comprising:

       a means for generating a first intermediate potential, said first generator means functioning to adjust said first intermediate potential so as to compensate for fluctuations in operating conditions of said circuit, said first intermediate potential being variably responsive to

10   a first control signal;

       a means for generating a second intermediate potential, said second generator means being coupled to a first reference potential and said first intermediate potential, said second generation means functioning to adjust said second intermediate potential so as to

15   compensate for fluctuations in operating conditions of said circuit, said second intermediate potential being variably responsive to a second control signal;

       at least one means for converting said first intermediate potential to said first bias potential and said second intermediate

20   potential to said second bias potential, said first bias potential determining said associated resistivity of said each of said pair of load MOS devices, said second bias potential biasing said current MOS device so that said current MOS device generates a current such that the output swing of said logic gate is determined by said first

25   reference potential, said second generator means causing said second bias potential to be adjusted to maintain said output swing despite different values of associated resistivity of said each of said pair of

30

load MOS devices, and said first and second generator means causing said first and second bias potentials to be adjusted so as to compensate for fluctuations in operating conditions of said circuit.

5   8.   The distribution system as described in claim 7 wherein said at least one converting means is physically located in close proximity to said logic gate.

    9.   The distribution system as described in claim 8 wherein said at least one converting means comprises first and second MOS devices coupled in series at a common node, said first MOS device
10   having its drain coupled to said first operating potential and its gate coupled to said first intermediate potential, said second MOS device having its source coupled to a current transference MOS device and its gate coupled to said second intermediate potential, wherein said first intermediate potential biases said first MOS device and said
15   second intermediate potential biases said second MOS device such that said common node is forced to be at a potential approximately equal to said first reference potential, said current transference device having its drain coupled to its gate and its source coupled to a second operating potential wherein said gate of said current transference MOS
20   device provides said second bias potential.

    10.   The distribution system as described in claim 9 wherein said each of said pair of resistive load MOS devices and said first and said second MOS devices each comprise a PMOS transistor.

31

11.   The distribution system as described in claim 10 wherein said common current source MOS device and said current transference MOS device each comprise an n-channel metal-oxide-semiconductor (NMOS) transistor.

5   12.   In a circuit comprising at least one BiCMOS logic gate, said BiCMOS logic gate comprising an emitter-coupled pair of bipolar transistors for differentially comparing an input signal with a first reference potential, each of the collectors of said pair of bipolar transistors being coupled to one of a pair of resistive MOS device
10   networks each having an associated resistivity, each of said emitters of said bipolar transistors being coupled to a common current source MOS device, a distribution system for providing a first set of bias potentials to each of said pair of resistive MOS device networks and a second bias potential to said common current source MOS device
15   comprising:
            a means for generating a first intermediate potential, said first generator means functioning to adjust said first intermediate potential so as to compensate for fluctuations in operating conditions of said circuit, said first intermediate potential being variably responsive to
20   a first control signal;
            a means for generating a second intermediate potential, said second generator means being coupled to a first reference potential and said first intermediate potential, said second generation means functioning to adjust said second intermediate potential so as to
25   compensate for fluctuations in operating conditions of said circuit, said second intermediate potential being variably responsive to a

32

second control signal;

at least one means for converting said first intermediate potential to said first set of bias potentials and said second intermediate potential to said second bias potential, said first set of

5   bias potentials determining said associated resistivity of said each of said pair of resistive MOS device networks, said second bias potential biasing said current MOS device so that said current MOS device generates a current such that the output swing of said logic gate is determined by said first reference potential, said second generator

10   means causing said second bias potential to be adjusted to maintain said output swing despite different values of associated resistivity of said each of said pair of resistive MOS device networks, and said first and second generator means causing said first set of bias potentials and said second bias potential to be adjusted so as to compensate for

15   fluctuations in operating conditions of said circuit.

13.   The distribution system as described in claim 12 wherein said at least one converting means is physically located in close proximity to said logic gate.

14.   The distribution system as described in claim 13

20   wherein said at least one converting means comprises first and second MOS device networks coupled in series at a common node, said first MOS device network being coupled to said first operating potential and to said first intermediate potential, said first MOS device network providing said first set of bias potentials, said second MOS device

25   network being coupled to said second intermediate potential and to a

33

current transference MOS device, wherein said first intermediate potential biases said first MOS device network and said second intermediate potential biases said second MOS device network such that said common node is forced to be at a potential approximately equal to said first reference potential, said current transference device having its drain coupled to its gate and its source coupled to a second operating potential wherein said gate of said current transference MOS device provides said second bias potential.

15.   The distribution system as described in claim 14 wherein said first and second MOS device networks are responsive to a third control signal, said third control signal determining said first set of bias potentials, wherein said associated resistivity of said each of said pair of resistive load networks may be varied by varying said third control signal.

16.   The distribution system as described in claim 15 wherein said each of said pair of resistive MOS device networks and said each of said first and second MOS device networks comprise a plurality of parallel MOS devices and a corresponding switching network, said plurality of parallel MOS devices having an associated cumulative size, said corresponding switching network of said plurality of MOS devices being controlled so as to determine said associated size of said corresponding plurality of parallel MOS devices.

17.   The distribution system as described in claim 16

34

wherein said plurality of parallel MOS devices comprise PMOS transistors.

18.   The distribution system as described in claim 17 wherein said common current source MOS device and said current
5   transference MOS device each comprise an n-channel metal-oxide-semiconductor (NMOS) transistor.

19.   In a circuit comprising at least one logic gate, said logic gate comprising an emitter-coupled pair of bipolar transistors for differentially comparing an input signal with a first reference
10   potential, each of the collectors of said pair of bipolar transistors being coupled to one of a pair of resistive load MOS devices each having an associated resistivity, each of   said emitters of said bipolar transistors being coupled to a common current source MOS device, a distribution system for providing a first bias potential to said
15   pair of load MOS devices and a second bias potential to said common current source MOS device comprising:
        a means for generating a first intermediate potential, said first generator means functioning to adjust said first intermediate potential so as to compensate for fluctuations in operating conditions of said
20   circuit, said first intermediate potential being variably responsive to a first control signal;
        a means for generating a set of second intermediate potentials, said second generator means being coupled to said first intermediate potential and a plurality of first reference potentials each
25   corresponding to one of said set of second intermediate potentials, said

35

second generation means functioning to adjust said set of second intermediate potentials so as to compensate for fluctuations in operating conditions of said circuit, said set of second intermediate potentials being variably responsive to a second control signal;

5   at least one means for converting said first intermediate potential to said first bias potential and said one of said set of second intermediate potentials to said second bias potential, said at least one converting means also comprising a means for selecting which of said one of said set of second intermediate potentials is to be converted to

10   said second bias potential thereby selecting said corresponding first reference potential, said first bias potential determining said associated resistivity of said each of said pair of load MOS devices, said second bias potential biasing said current MOS device so that said current MOS device generates a current such that the output swing of said

15   logic gate is determined by said corresponding first reference potential of a selected one of said set of second intermediate potentials, said second generator means causing said second bias potential to be adjusted to maintain said output swing despite different values of associated resistivity of said each of said pair of load MOS devices,

20   and said first and second generator means causing said first and said second bias potentials to be adjusted so as to compensate for fluctuations in operating conditions of said circuit.

      20.   The distribution system as described in claim 19 wherein said at least one converting means is physically located in

25   close proximity to said BiCMOS logic gate.

36

21.   The distribution system as described in claim 20
wherein said at least one converting means comprises first and second
MOS devices coupled in series at a common node, said first MOS
device having its drain coupled to said first operating potential and its
5   gate coupled to said first intermediate potential, said second MOS
device having its source coupled to a current transference MOS device
and its gate coupled to said selected second intermediate potential,
wherein said first intermediate potential biases said first MOS device
and said selected second intermediate potential biases said second
10   MOS device such that said common node is forced to be at a potential
approximately equal to said corresponding first reference potential of
said selected second intermediate potential, said current transference
device having its drain coupled to its gate and its source coupled to a
second operating potential wherein said gate of said current
15   transference MOS device provides said second bias potential.

22.   The distribution system as described in claim 21
wherein said each of said pair of resistive load MOS devices, said
common current source MOS device, said first and said second MOS
devices, and said current transference MOS device each comprise a
20   PMOS transistor.

23.   In a circuit comprising at least one BiCMOS logic gate,
said BiCMOS logic gate comprising an emitter-coupled pair of bipolar
transistors for differentially comparing an input signal with a first
reference potential, each of the collectors of said pair of bipolar
25   transistors being coupled to one of a pair of resistive MOS device

37

networks each having an associated resistivity, each of said emitters
of said bipolar transistors being coupled to a common current source
MOS device, a distribution system for providing a first set of bias
potentials to each of said pair of resistive MOS device networks and

5   a second bias potential to said common current source MOS device
comprising:

a means for generating a first intermediate potential, said first
generator means functioning to adjust said first intermediate potential
so as to compensate for fluctuations in operating conditions of said

10   circuit, said first intermediate potential being variably responsive to
a first control signal;

a means for generating a set of second intermediate potentials,
said second generator means being coupled to said first intermediate
potential and a plurality of first reference potentials each

15   corresponding to one of said set of second intermediate potentials, said
second generation means functioning to adjust said set of second
intermediate potentials so as to compensate for fluctuations in
operating conditions of said circuit, said set of second intermediate
potentials being variably responsive to a second control signal;

20   at least one means for converting said first intermediate
potential to said first set of bias potentials and said one of said set of
second intermediate potentials to said second bias potential, said at
least one converting means also comprising a means for selecting
which of said one of said set of second intermediate potentials is to be

25   converted to said second bias potential thereby selecting said
corresponding first reference potential, said first set of bias potentials
determining said associated resistivity of said each of said pair of

38

resistive MOS device networks, said second bias potential biasing said current MOS device so that said current MOS device generates a current such that the output swing of said logic gate is determined by said corresponding first reference potential of a selected one of said

5   set of second intermediate potentials, said second generator means causing said second bias potential to be adjusted to maintain said output swing despite different values of associated resistivity of said each of said pair of resistive MOS device networks, and said first and second generator means causing said first set of bias potentials and

10   said second bias potential to be adjusted so as to compensate for fluctuations in operating conditions of said circuit.

24.   The distribution system as described in claim 23 wherein said at least one converting means is physically located in close proximity to said logic gate.

15   25.   The distribution system as described in claim 24 wherein said at least one converting means comprises first and second MOS device networks coupled in series at a common node, said first MOS device network being coupled to said first operating potential and to said first intermediate potential, said first MOS device network

20   providing said first set of bias potentials, said second MOS device network being coupled to said selected second intermediate potential and to a current transference MOS device, wherein said first intermediate potential biases said first MOS device network and said selected second intermediate potential biases said second MOS device

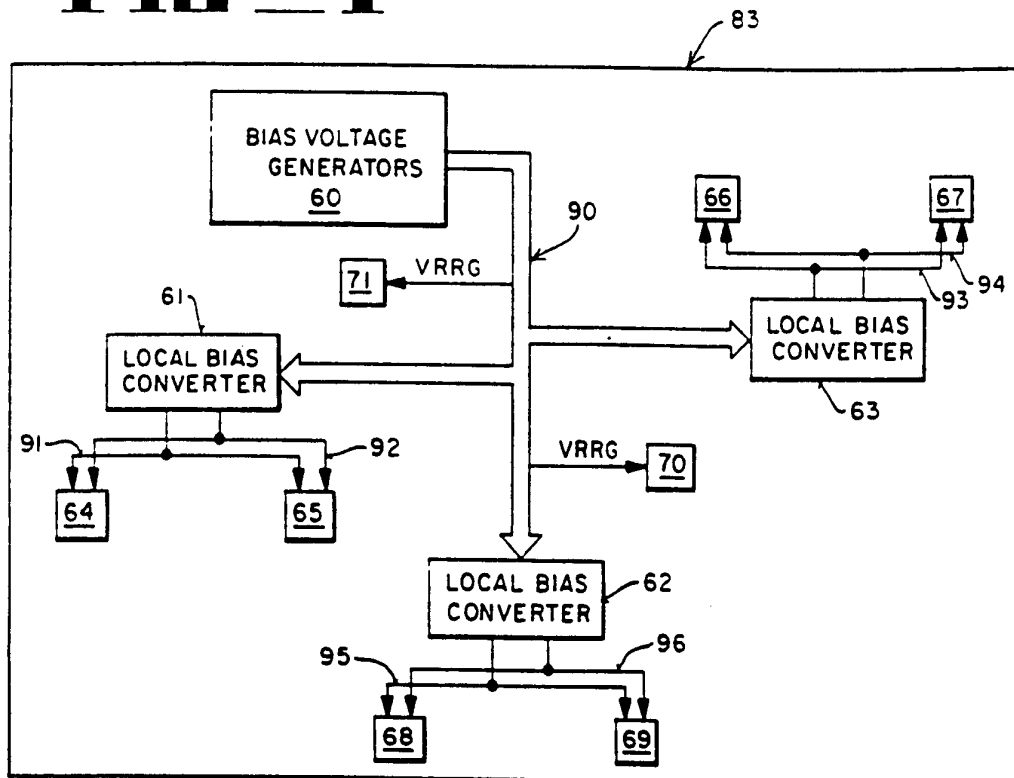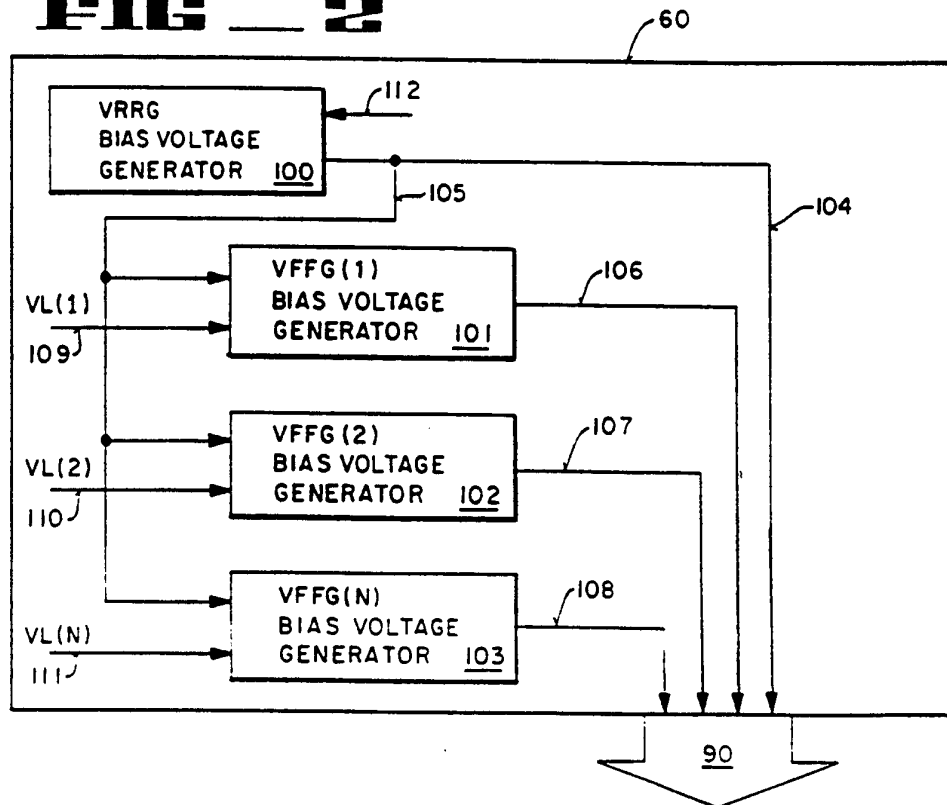25   network such that said common node is forced to be at a potential

39

approximately equal to said corresponding first reference potential of said selected second intermediate potential, said current transference device having its drain coupled to its gate and its source coupled to a second operating potential wherein said gate of said current
5   transference MOS device provides said second bias potential.

26.   The distribution system as described in claim 25 wherein said first and second MOS device networks are responsive to a third control signal, said third control signal determining said first set of bias potentials, wherein said associated resistivity of said each
10   of said pair of resistive load networks may be varied by varying said third control signal.
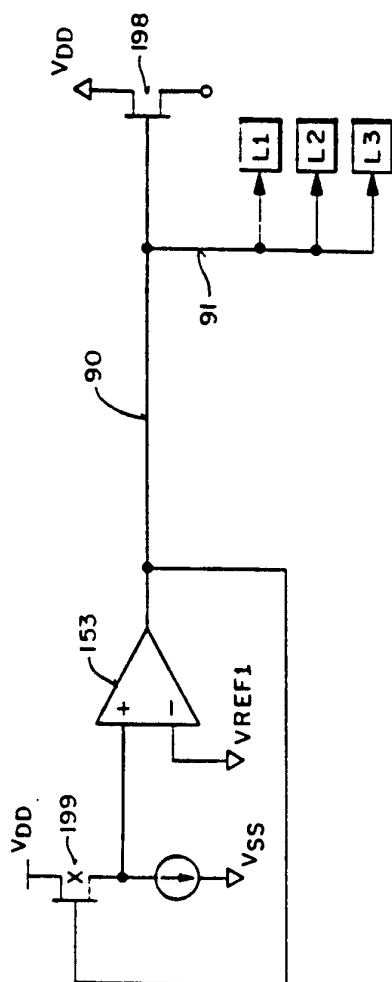
27.   The distribution system as described in claim 25 wherein said each of said pair of resistive MOS device networks and said each of said first and second MOS device networks comprise a
15   plurality of parallel MOS devices and a corresponding switching network, said plurality of parallel MOS devices having an associated cumulative size, said corresponding switching network of said plurality of MOS devices being controlled so as to determine said associated size of said corresponding plurality of parallel MOS
20   devices.

28.   The distribution system as described in claim 27 wherein said plurality of parallel MOS devices comprise PMOS transistors.

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29.   The distribution system as described in claim 28 wherein said common current source MOS device and said current transference MOS device each comprise an n-channel metal-oxide-semiconductor (NMOS) transistor.
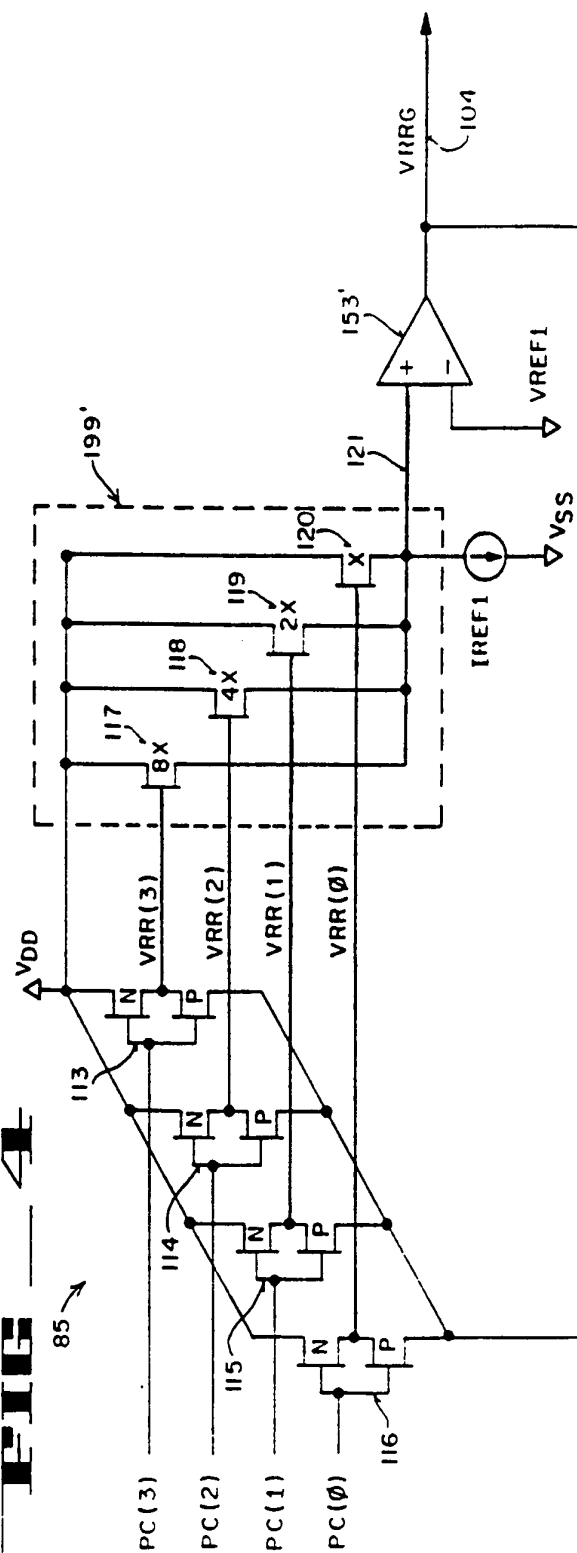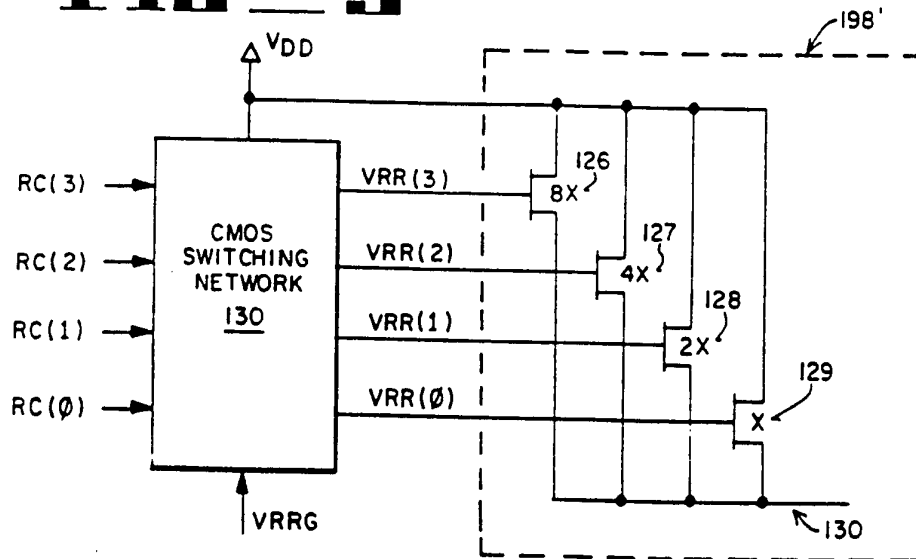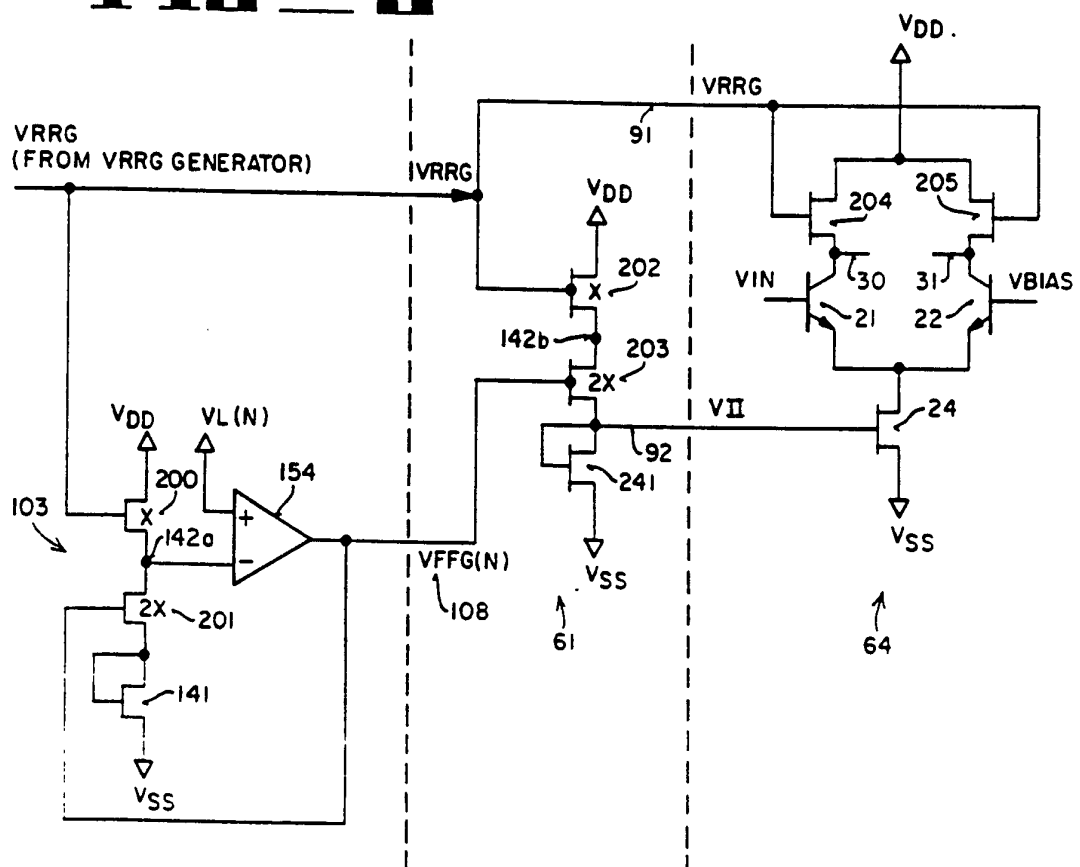
FIG _ 1

83

BIAS VOLTAGE
GENERATORS
60

90

66   67

71   VRRG

61

94
93

LOCAL BIAS
CONVERTER

LOCAL BIAS
CONVERTER
63

91   92

64   65

VRRG   70

LOCAL BIAS   62
CONVERTER

95   96

68   69

FIG _ 2

60

VRRG
BIAS VOLTAGE
GENERATOR 100

112

105

104

VFFG(1)
BIAS VOLTAGE
GENERATOR 101

106

VL(1)
109

VFFG(2)
BIAS VOLTAGE
GENERATOR 102

107

VL(2)
110

VFFG(N)
BIAS VOLTAGE
GENERATOR 103

108

VL(N)
111

90

FIG — 3

FIG — 4

FIG _ 5

FIG _ 6

FIG 7

FIG — 11

FIG _ 9