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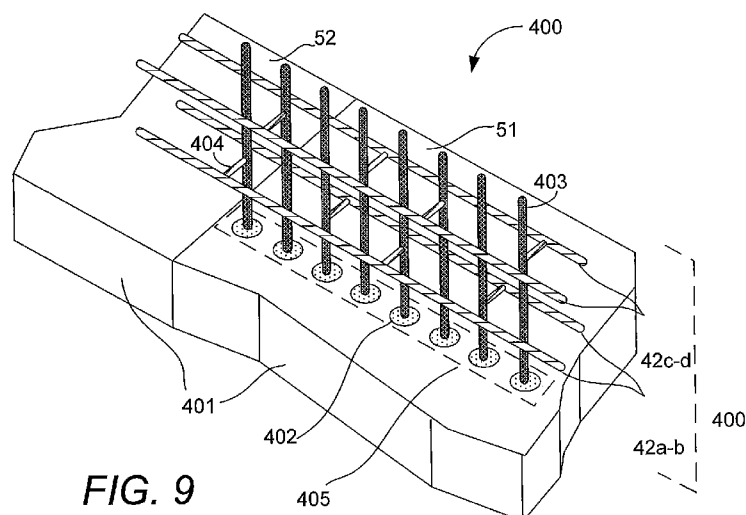
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(54) **Title:** INTERCONNECT STRUCTURE, MODULATION DEVICE AND LITHOGRAPHY SYSTEM COMPRISING SUCH DEVICE



**FIG. 9**

(57) **Abstract:** An interconnect structure (400) arranged on a substrate (401) for electrically transmitting signals. The interconnect structure comprises a plurality of conductive supports (403) extending from a surface of the substrate, and a plurality of conductive lines (42) supported by the conductive supports. At least a portion of each conductive line extending between two of the conductive supports is supported only by the conductive supports at each end of the conductive line portion.



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## INTERCONNECT STRUCTURE, MODULATION DEVICE AND LITHOGRAPHY SYSTEM COMPRISING SUCH DEVICE

### FIELD OF THE INVENTION

[0001] The invention relates generally to interconnect structures for integrated circuits, and  
5 more particularly, to a beamlet modulation device and an interconnect structure for a beamlet  
modulation device in a charged particle lithography system.

### BACKGROUND OF THE INVENTION

[0002] Charged particle lithography systems are known in the art, for example from U.S.  
Patent No. 6,958,804 in the name of the applicant. This lithography system uses a plurality of  
10 electron beamlets to transfer a pattern onto the surface of a target. Pattern data is sent to a  
modulation device, usually taking the form of a beamlet blanker array. Herein, the beamlets  
are modulated, e.g. by electrostatic deflection of the beamlets to switch selected beamlets on  
or off. Such modulation devices comprise an array of electrostatic deflectors, each having  
electrodes arranged close to an aperture through which one of the beamlets passes before  
15 being projected onto the surface of a target to be exposed. To enable high speed transfer of  
the pattern to the target surface, optical transmission of control signals to the modulation  
device may be used.

[0003] To manufacture lithography systems able to perform exposures having smaller  
critical pattern dimensions with sufficiently high throughput, charged particle systems have  
20 been proposed having a very large number of charged particle beamlets, e.g. tens or hundreds  
of thousands or millions of beamlets.

[0004] For such lithography systems, the area in which final projection of the beamlets  
occurs is typically limited to a single field, e.g. 26mm x 33mm, and where the beamlets at  
least for a large part remain separate from one another, i.e. do not have a single common  
25 cross-over in the column. In such systems, the area of the beamlet modulation device is also  
limited and is not much larger than the field size to avoid causing other problems. The  
modulation device may be constructed as a single integrated circuit, or several integrated  
circuits that are stitched together to make a larger modulation device. The construction of a  
modulation device able to individually modulate tens of thousands or more beamlets in such a

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small area presents problems in the construction of an interconnect structure for making electrical interconnections to transmit control signals to a very large number of electrodes in a very small area. Such an interconnect structure must be designed for the very narrow areas between adjacent electrodes.

## 5 BRIEF SUMMARY OF THE INVENTION

[0005] It is therefore an object of the present invention to provide an interconnect structure for transmitting electrical signals to a large number of circuit elements in a very small area, and in particular suitable for use in a modulation device for a multi-beamlet charged particle lithography system able to modulate a very large number of beamlets. It is also an object to  
10 provide a modulation device incorporating the interconnect structure and able to modulate a very large number of beamlets. It is also an object to provide a method for making the interconnect structure and the modulation device of the invention.

[0006] Integrated circuit manufacturing techniques may be used to make such a sufficiently small interconnect structure, and a modulation device with an interconnect structure. Such a  
15 manufacturing process typically involves depositing alternating layers of conductive and insulating materials, and patterning the conductive layers to form the interconnect structure and modulation device electrodes. However, a problem encountered with this construction is that the insulating layers can become charged by charged particles from the beamlets passing through the apertures and impinging on the surface of the beamlet blanking array. This charge  
20 accumulates and may cause undesired deflection of the beamlets, resulting in writing errors in the exposure.

[0007] One solution is to make the insulating layers thinner. However, a relatively thick insulating layer is desired to avoid increasing the parasitic capacitance between the conductive layers, and it is also desired to use a standard fab manufacturing process to avoid  
25 the additional cost and uncertainty of designing a new non-standard process. Another approach is to etch the insulating layers to move them away from the areas near the electron beamlets, e.g. etching the edges of the insulating layers at the walls of the apertures through which the electron beamlets pass. This reduces the charging of the insulating layers and, because the charged edges of the insulating layers are further from the beamlet path, it  
30 reduces the effect that any accumulated charge has on the beamlets. This effect on the

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beamlets is especially reduced if the insulator is etched back horizontally at least twice and preferably more than three times the thickness of the insulator. By doing this the remaining conductive layers act as a shield for the accumulated charge on the insulators. In order to implement this around each electrode an additional area with a width of at least 2-3 times the

thickness of the insulator is required for shielding purposes. As the number of beamlets in the lithography system increases, and the dimensions of the electrodes and the space between them decreases, there is not enough area available for the shielding of the insulators.

Removing the complete insulating layers, and thereby removing the need for shielding is also not possible because the insulating layers are also supporting the conductive layers of the interconnect structure and the electrodes.

[0008] The present invention addresses this problem by providing an interconnect structure arranged on a substrate for electrically transmitting signals. The substrate may be semiconductor, e.g. silicon, doped silicon, silicon on insulator, etc. The interconnect structure comprises a plurality of conductive supports extending from a surface of the substrate, and a plurality of conductive lines supported by the conductive supports. At least a portion of each conductive line extending between two of the conductive supports is supported only by the conductive supports at each end of the conductive line portion.

[0009] Preferably, at least one of the conductive supports at an end of the conductive line portion comprises a via or a contact in direct contact with the substrate. The conductive supports and the conductive lines may comprise conductors, preferably metal, e.g. aluminum, copper, etc. The conductive supports may be formed from portions of conductor formed in via or contact holes of insulating layers which are present during manufacture of the structure.

[0010] The conductive line portion is preferably directly surrounded by air or ambient gas or vacuum along its entire length between the two conductive supports at each end of the conductive line portion. In this way, the conductive line portion can be separated and isolated from other conductive lines in the interconnect structure without an intervening solid insulating material, e.g. without requiring support from the layers of insulating material, such as silicon dioxide, usually used during manufacture of the structure. The conductive supports may be adapted to physically support the conductive line, so that the conductive line may form a free-hanging structure supported by the conductive supports. Adjacent conductive

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lines may be separated by air (or the ambient gas surrounding the structure if this is not air) or vacuum. Because air is a very low-k dielectric, this may also enable higher clock speeds and/or lower power dissipation than conventional interconnect structures in integrated circuits. Suitably, pairs of the conductive supports are electrically isolated from each other.

5 [0011] The structure is preferably formed so that the conductive supports contact the substrate at a plurality of first regions, wherein the first regions comprise electrically insulating material. The insulating material of the first regions preferably comprises a material that is selectively etchable with respect to an inter- or intra-layer dielectric of other structures formed on the substrate. The insulating material of the first regions preferably  
10 comprises a material that is not selectively removed together with the inter- and intra layer dielectric of other structures on the substrate, e.g. the insulating materials used in other parts of the structures on the substrate can be selectively removed while leaving the first regions intact.

[0012] The interconnect structure may be formed so that the conductive supports contact the  
15 substrate at a plurality of first regions, wherein the first regions are isolated from a remaining part of the substrate by insulating barrier regions. The insulating barrier regions may be formed, for example, by using a shallow-trench isolation (STI) technique.

[0013] The interconnect structure may be formed on a substrate comprising a plurality of first regions at the surface of the substrate and at least one second region, the first and second  
20 regions being of a different conductivity type for forming a pn-junction between the regions, and wherein the conductive supports contact the substrate at the plurality of first regions.

[0014] The first and second regions may be formed with different doping, e.g. providing different majority carriers (e.g. holes, electrons). For instance, the first regions may be doped with n-type dopant and the second region may be doped with p-type dopant to create a  
25 plurality of p-n junctions. The different doping of the first regions and the second region electrically insulates the conductive lines of the interconnect structure from the substrate and from each other, e.g. preventing signals from flowing into the substrate. For example, the first regions may form a plurality of n-type wells on the surface of the substrate, with the second region having p-type doping. Alternatively, the first regions may form a plurality of p-type  
30 wells at the surface of the substrate, and the second region may have n-type doping. In these

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arrangements, a plurality of diode junctions may be formed at the junctions of the first regions and the second region. The first regions may comprise a plurality of separate relatively small regions of the substrate and the second region may comprise substantially all of the remaining portion of the substrate, or only a part of the remaining portion of the substrate.

5 [0015] The electrical signals transmitted by the interconnect structure can be arranged so that the voltage on the conductive lines creates a reverse bias across the junctions between the first and second regions of the substrate. This creates a reverse bias of the diode formed at the junction, electrically isolating the conductive lines and the second region of the substrate. This eliminates the need for a layer of insulating material under the conductive supports or  
10 between the conductive lines and the substrate. This simplifies the removal of the insulating/dielectric material after fabrication of the structure, because all insulators in certain areas of the device can be removed by an etching step. Because all insulators can be removed without requiring some insulator material to be left in place, over-etching can be used, i.e. the etching does not have to be stopped by precise timing or by protecting the insulating parts that  
15 should not be etched by means of a mask or by selective etching. For the removal of the insulating material, there are various alternatives such as removal of all insulators from the complete chip or removal of all insulators from certain discrete areas of the chip where the interconnect structure is formed.

[0016] Preferably, each conductive support is adapted to connect to and be fixed on a first  
20 region of the substrate without requiring an extra supporting material, in particular insulating supporting material such as silicon dioxide or low-k dielectric. Alternatively the support structures can be isolated from the substrate by a thin insulating layer. Since this insulator is located far from the electron path, the effect of shielding will be limited. The main advantage of an oxide-free design such as with the pn junctions is that all oxides can be removed by a  
25 “brute force” etching step which is relatively simple to implement.

[0017] The interconnect structure (e.g. the conductive supports and the conductive lines) may comprise part of a chip or integrated circuit formed on the substrate. This enables the use of existing technologies and standard fab processes used for semiconductor manufacturing to make the interconnect structure and blanker electrodes. First regions can be formed of small

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dimensions using a standard fab process to create doped regions, avoiding the costly design and testing of a new process.

[0018] It may be recognized that where the present invention was developed in reaction to a need for ever further decreasing size of structural elements in a blanker chip, the present may very well also be applied to other CMOS devices. Especially the effect of low power device, and/or the effect of increased clock speeds may be highly favorably applied in designs for memory and arithmetic chips such as for contemporary computers and cell phones. It is explicitly noted that the present invention may have a significantly higher effect and economic significance than it has in the application in a blanker chip, i.e. the application of origin of the present invention.

[0019] In the case of use in a charged particle multi-beamlet lithography system, the conductive supports are typically arranged in an area of less than  $65 \text{ mm}^2$ . The number of the conductive supports in the structure may be in the range of 10,000 to 10,000,000,000. In the case of use in a charged particle multi-beamlet lithography system, the conductive supports are typically arranged in an area of less than  $65 \text{ mm}^2$ , and the number of the conductive supports is typically at least 1000 and may even be 100,000 or more. In one specific embodiment of a modulation device the conductive supports are typically arranged in 13260 areas of 100um diameter each. The number of deflectors is at least  $13260 \times 49 \sim 600,000$ . The number of conductive supports per deflector is typically 25 (every 2 micron, 50 micron long). Thus, the number of conductive supports is in the order of 20,000,000. For future nodes this may be up to 10 billion supports.

[0020] The conductive lines may be arranged on a plurality of connection levels at different heights with respect to the substrate, e.g. in a cross-section without electrically connected to each other. The number of the connection levels may correspond with the number of metal layers in the fab process used which are available for connective lines, e.g. 4, 5 or more. The conductive lines may be arranged at a plurality of connection levels. Each of the connection levels may comprise a plurality of conductive lines running substantially parallel to each other over at least a portion of their length.

[0021] The conductive supports may be arranged at a pre-determined pitch for supporting the conductive lines at a plurality of points along their length. Each of the conductive

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supports may be arranged on a separate first region of the substrate. The conductive lines and the conductive supports may be arranged to form an interconnection corridor wherein, over at least a portion of the interconnection corridor, at least a portion or all of the conductive lines extend parallel to each other on a plurality of connection levels at different heights with  
5 respect to the substrate. The interconnect structure may include at least a portion of the conduction lines which cross each other without making electrical contact with each other. It should be noted that the interconnection corridor may be straight or may include curves or bends are necessary to efficiently route the conductive lines through the structure. The conductive lines may extend along the corridor in a generally parallel fashion, although the  
10 distance between adjacent conductive lines may vary. In this way, the interconnection corridor forms a sort of bus-like structure.

[0022] The conductive lines may be electrically connected to the conductive supports via a plurality of connection bridges, the connection bridges extending laterally to the length of the conductive lines and/or substantially perpendicular to the conductive supports and  
15 mechanically supporting the conductive lines.

[0023] The conductive supports may be arranged in a two dimensional array on the surface of the substrate. The conductive supports may form a routing row, and a plurality of parallel routing rows may form an array. The array may be a rectangular  $M \times N$  array,  $M$  and  $N$  being natural numbers. Alternatively, the array of the conductive supports may be a (two  
20 dimensional) hexagonal close-packed array.

[0024] The invention further comprises an interconnect structure including a control circuit, wherein the substrate comprises a plurality of first regions at the surface of the substrate and at least one second region, the first and second regions being of a different conductivity type, and wherein the conductive supports contact the substrate at the plurality of first regions, and  
25 the control circuit may be adapted to supply a voltage signal to the interconnect structure. The voltage signal creates a reverse bias across a junction between the first and second regions of the substrate. The control circuit is preferably adapted to supply a plurality of signals to the conductive lines, each signal for supply to one of a plurality of circuits connected to respective conductive line.

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[0025] The interconnect structure of the present invention may be operated by applying a first voltage ( $V_s$ ) to the interconnect structure and applying a second voltage ( $V_0$ ) on the substrate to create a reverse bias across a junction between the first and second regions of the substrate. In other words, the effectively formed diodes at the junctions may be arranged to be reverse-biased in regard to voltage differences  $V_s - V_0$ . Note that the absolute values of the voltage differences  $|V_s - V_0|$  should be arranged lower than the break down voltage of the diodes.

[0026] A second aspect of the invention relates to a modulation device, e.g. a beamlet blanker array, for use in a charged particle multi-beamlet lithography system adapted to generate a plurality of charged particle beamlets. The modulation device is arranged for modulating the charged particle beamlets in accordance with pattern data and comprises a plate-like substrate; an array of beamlet deflectors arranged for deflecting the beamlets, each deflector comprising a first electrode and second electrode adjacent to an aperture; a plurality of control circuits arranged to receive the pattern data and supply corresponding control signals for control of the beamlet deflectors; and an interconnect structure as described herein connecting the control circuits to the first electrodes of the beamlet deflectors. In this arrangement, the control circuits supply the control signals to the beamlet deflectors via the interconnect structure.

[0027] The first and second deflectors may be conductors and deflect charged particle beamlets by electrostatic forces. The apertures may extend through the plate-like body for letting the beamlets pass through, and the substrate of the interconnect structure may be arranged on the plate-like substrate or form an integral part of the plate-like body. In both cases the apertures may be arranged directly through the substrate.

[0028] The beamlet deflectors may form an integral part of the interconnect structure.

Moreover, at least a portion of the beamlet deflectors and at least a portion of the interconnect structure may be formed as part of a single integrated circuit. At least a portion of the control circuits may also be formed as part of the same single integrated circuit. The modulation device may comprise more than one such integrated circuit. In one embodiment, the modulation device comprises a plurality of integrated circuits wherein the beamlet deflectors, apertures, the interconnect structure and the control circuits are integrated.

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[0029] The body of the modulation device may be divided into a plurality of elongated beam areas and a plurality of elongated non-beam areas. The non-beam areas may be positioned adjacent to the beam areas so that a long edge of each beam area borders a long edge of an adjacent non-beam area. The beam areas are positioned in the normal path of the beamlets and the non-beam areas are positioned outside the normal path of the beamlets. The beamlet deflectors are preferably arranged in the beam areas and the control circuits are preferably arranged in the non-beam areas. The beamlet deflectors may be arranged in groups, each group of beamlet deflectors located in one of the beam areas. The beam area preferably comprises the interconnect structure of the present invention. The non-beam area may comprise the interconnect structure of the present invention or a conventional interconnect structure filled with insulating materials such as silicon oxide.

[0030] The control circuits may include a plurality of light sensitive elements adapted to receive patterned light signals and convert the light signals to electrical signals to generate the control signals. Furthermore, the control circuits may include a plurality of demultiplexers, wherein the light signals received by the light sensitive elements are multiplexed signals which include pattern information for more than one beamlet deflector, and wherein the multiplexed signals are demultiplexed by the demultiplexers.

[0031] The modulation device may be formed so that a plurality of the conductive lines extend parallel to each other in a corridor between two rows of the beamlet deflectors. Each beamlet deflector is preferably addressed by a single conductive line. Alternatively, the interconnects of the plurality of beamlet deflectors may be arranged in an addressable array, e.g. a first subset of the conductive lines form wordlines and a second subset of the conductive lines form bitlines for addressing the beamlet deflectors. The wordlines and the bitlines may be arranged at different connection levels in the interconnect structure. In this embodiment, a plurality of memory cells may be arranged in a close proximity (e.g. less than 1 micron) with a plurality of respective beamlet deflectors for temporarily storing a control signal. The temporarily stored signal may be dedicated for the respective beamlet deflector for a predetermined period of time. The memory cells may be formed on or within the substrate.

[0032] The first and second electrodes of the modulation device may be formed of a plurality of layers of conductive material connected with each other by one or more vias. The

first electrodes may be supported by one or more conductive supports or vias to a surface of the substrate, the conductive supports or vias supported by one or more of the first regions of the substrate. The first electrodes may form a free-hanging structure supported by one or more conductive supports or vias.

5 [0033] The first electrodes may be arranged for individually receiving electrical signals from the control circuits via the conductive lines, and the second electrodes may be connected to a common potential. The common potential may be a ground potential. The electrodes of the beamlet deflectors are shaped as two half circles, and the conductive line which supplies a signal to the first electrode may be arranged in a close proximity (e.g. less than 1 micron) with  
10 a tangent of the first electrodes. For the purpose of arranging beamlet deflectors with as many as possible in a small area, the distance between two adjacent beamlet deflectors is preferably less than 55  $\mu\text{m}$ , and may be less than 8  $\mu\text{m}$  or even less than 1  $\mu\text{m}$ .

[0034] A third aspect of the invention relates to an integrated circuit comprising the interconnect structure as described herein. The integrated circuit may be e.g. an embedded  
15 memory circuit, an on-chip bus, a logic circuit, or a processor, with the interconnect structure forming part of the memory, on-chip bus, logic circuit, or processor. The interconnect structure according to the invention may be applied to many different types of integrated circuits, and to various functional blocks in a digital circuit formed on a substrate.

[0035] A fourth aspect of the present invention relates to a charged particle lithography  
20 system comprising a beam generator arranged for generating a plurality of charged particle beamlets; a modulation device according to the second aspect of the present invention adapted to modulate the beamlets; and a projection system arranged for projecting the modulated beamlets onto a target (e.g. a wafer or substrate) to be exposed. Each beam area of the modulation device may be positioned in the path of one of the groups of beamlets and  
25 each non-beam area positioned outside the path of the groups of beamlets.

[0036] A fifth aspect of the present invention relates to a method for manufacturing an integrated circuit comprising the steps of:

providing a substrate;

selectively doping the substrate to create a plurality of first regions at a surface of the  
30 substrate and at least one second region, the first and second regions having different doping;

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creating a multi-level structure in a pre-determined area of the substrate by depositing and etching alternating layers of conductive and insulating materials, the conductive material forming a plurality of conductive lines formed in a pre-determined pattern on a surface of one or more layers of the insulating material, and a plurality of  
5 conductive supports connected to the conductive lines and the surface of the substrate and extending through one or more of the insulating layers; and

removing substantially all of the insulating material in the pre-determined areas.

[0037] The substrate may be provided as already doped. For instance, the substrate may be doped as the boule (e.g. comprising silicon) is grown, giving each wafer an almost uniform  
10 initial doping, or may be doped afterwards. Subsequently, doping of the first regions may be carried out by processes such as diffusion or ion implantation, the latter method being more preferable in large production runs because of increased controllability.

[0038] The pattern of the conductive material comprises a plurality of conductive supports passing through more than one level. Each of the conductive supports is supported by one of  
15 the first regions and extends substantially perpendicular to a surface of the substrate. The pattern of the conductive material further comprises a plurality of conductive lines. Each of the conductive lines may extend at one connection level. The pattern of the conductive material may further comprise a plurality of connection bridges for electrically connecting the conductive lines to the conductive supports. The connection bridges may be adapted to  
20 physically support the conductive lines.

[0039] The first regions may form a plurality of n-type wells on the substrate, and the second region may be doped with p-type dopant. The removal of the supporting insulating material may include wet etching. The etchant preferably comprises hydrofluoric acid (HF).

[0040] In case the insulators only need to be removed in a large amount of small areas  
25 (typically > 10,000 areas of 50um to 120um in diameter) the rest of the circuitry needs to be protected from the etchant. This can for instance be done by first etching trenches around the areas from which the insulators need to be removed. The etching of the trenches can for instance be done with a dry etch step. In this etching step only the insulators are removed, not the conductors. After this the trenches can be filled with a protective material and the surface  
30 can be covered by a protective material, such as a resist or polymer. After this the protective

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material can be removed from the surface of the areas from which the insulators need to be removed. After this the insulators can be etched away. As a last step the protective material may be removed.

[0041] For the purpose for use in a charged particle multi-beamlet lithography system, the method may further comprise forming a plurality of apertures through the substrate, e.g. after the provision of the multi-level structure and before the removal of all supporting insulating material. Moreover, the pattern of the conductive material may further comprise a plurality of electrodes surrounding the apertures, e.g. to form a plurality of beamlet deflectors. Each electrode preferably comprises a plurality of portions formed at a plurality of levels, and different portions of the electrode are preferably electrically connected to each other.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0042] These and other objects of the invention will be further described with reference to the drawings showing exemplary embodiments of the invention, in which:

[0043] Fig. 1 shows a conceptual schematic diagram of a charged particle multi-beamlet lithography system;

[0044] Fig. 2 shows a modular arrangement of components of the lithography system of Fig. 1;

[0045] Fig. 3 shows a simplified schematic view of an example of a beamlet blanker array of the lithography system of Figs. 1-2;

[0046] Fig. 4 schematically shows a plan view of a portion of the beamlet blanker array of Fig. 3;

[0047] Fig. 5 schematically shows a plan view of an arrangement of components for the beamlet blanker array of Figs. 3-4;

[0048] Fig. 6 shows a cross-sectional view of an embodiment of a beamlet deflector;

[0049] Fig. 7 shows a cross-sectional view of an embodiment of a beamlet deflector with insulating layers removed;

[0050] Fig. 8 shows a plan view of an embodiment of an interconnect structure and beamlet deflectors;

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[0051] Fig. 9 shows a perspective view of a portion of the interconnect structure of Fig. 8;

[0052] Fig. 10 shows a cross-sectional view of another embodiment of an interconnect structure and beamlet deflectors;

[0053] Fig. 11 schematically shows a plan view of another arrangement of components for the beamlet blanker array with bitlines and wordlines;

[0054] Figs 12 A-F shows cross-sectional views of the beamlet deflector of Fig. 7 showing the steps of manufacturing.

[0055] Fig. 13 shows a cross-sectional view of an embodiment of modulation device in accordance with the invention as illustrated in Fig. 10, wherein a current limiting aperture array has been integrated in the metal stack;

[0056] Fig. 14 shows a schematic simplified cross-sectional view of an embodiment of the modulation device in accordance with the invention;

[0057] Fig. 15 shows a schematic simplified top-view of the modulation device of Fig. 14;

[0058] Fig. 16 shows a schematic simplified cross-sectional view of an alternative embodiment of the modulation device in accordance with the invention;

[0059] Fig. 17 shows a schematic simplified top-view of the modulation device of Fig. 16;

[0060] Fig. 18 shows a schematic simplified cross-sectional view of a further alternative embodiment of the modulation device in accordance with the invention, and

[0061] Fig. 19 shows a schematic simplified top-view of the modulation device of Fig. 18.

#### DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0062] The following is a description of certain embodiments of the invention, given by way of example only and with reference to the drawings. The drawings are not drawn to scale. Equivalent elements in different drawings are referred to with same reference numerals.

[0063] The expression “interconnect structure” as used in the context of this application refers to a structure for making electrical connections such as typically applied in integrated circuits. The interconnect structure may comprise multiple connection levels arranged at

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different layers of an integrated circuit, typically from four up to ten connection levels. The individual levels are mutually interconnected, e.g. using vertical connections, also referred to as vias. An interconnect as discussed below may comprise a portion residing within one or more connection levels as well as comprise portions corresponding to one or more vias.

5 [0064] Fig.1 shows the conceptual schematic drawing of a charged particle multi-beamlet lithography system 100 based upon an electron beam optical system without a common cross-over of all the electron beamlets. Such lithography systems are described for example in U.S. Patent Nos. 6,897,458 and 6,958,804 and 7,019,908 and 7,084,414 and 7,129,502 and 8,089,056, U.S. patent application publication no. 2007/0064213 and 2009/0261267 and US 10 2011/0079739 and US 2012/0091358, which are all assigned to the owner of the present invention and are all hereby incorporated by reference in their entirety.

[0065] In the embodiment shown in Fig. 1, the lithography apparatus 100 comprises an electron-optical column having an electron source 101 for producing an expanding electron beam 120. The expanding electron beam 120 is collimated by collimator lens system 102.

15 The collimated electron beam 121 impinges on an aperture array 103, which blocks part of the beam to create a plurality of beams 122. A condenser lens array 104 is included behind aperture array 103, for focusing the beams 122, e.g. towards a corresponding opening in the beam stop array 108. The beams 122 impinge a multi-aperture array 105 which blocks part of each sub-beam to create a plurality of beamlets 123 from each beam 122. In this example, the 20 aperture array 105 produces three beamlets from each beam, but in practice a much larger number of beamlets may be produced, e.g. 49 beamlets per sub-beam or more, so that the system generates a very large number of beamlets 122, preferably about 10,000 to 1,000,000 beamlets

[0066] The electron beamlets 123 pass through apertures in a modulation device, e.g. a 25 beamlet blanker array 106 comprising a plurality of modulators, e.g. beamlet deflectors 30. The aperture array 105 may be integrated with the beamlet blanker array 106, e.g. arranged close together or as a single unit. In this embodiment the beam limiting apertures are now formed by holes in one of the metal layer of the blanker. The advantages are the higher accuracy because of the CMOS fabrication process, and better alignment of aperture to 30 deflector. The beamlet blanker array 106 and beam stop array 108 operate together to

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modulate or switch beamlets on or off. The beam blanker array 106 includes a plurality of beamlet deflectors, which may be in the form of blanker electrodes positioned near each aperture of the array. By introducing a voltage across the blanker electrodes of an aperture, the beamlet or beamlets passing through the aperture may be slightly deflected. After passing  
5 through the beamlet blanker array, the beamlets 123 arrive at beam stop array 108, which has a plurality of apertures positioned so that the undeflected beamlets pass through the beam stop array and deflected beamlets are blocked by the beam stop array (or vice versa). If beamlet blanker array 106 deflects a beamlet, it will not pass through the corresponding aperture in beam stop array 108, but instead will be blocked. But if beamlet blanker array 106  
10 does not deflect a beamlet, then it will pass through the corresponding aperture in beam stop array 108, and through beam deflection array 109 and projection lens arrays 110. Thus, the beamlet blanker array 106 and beam stop array 108 operate together to block or let pass the beamlets 123.

[0067] Beam deflector array 109 provides for deflection of the beamlets 124 in the X and/or  
15 Y direction substantially perpendicular to a mechanical movement of the target or substrate 130. Next, the beamlets 124 pass through projection lens arrays 110 and are projected onto the surface of substrate 130. The projection lens arrangement preferably provides a demagnification of about 10 to 200 times. The beamlets 124 impinge on the surface of substrate 130 positioned on moveable stage 132 for carrying the substrate. For lithography  
20 applications, the substrate usually comprises a wafer provided with a charged-particle sensitive layer or resist layer.

[0068] A control unit 140 may be provided for providing signals for control of the beamlet blanker array 106. The control unit 140 may comprise a data storage unit 142, a processor unit 143 and data converter 144. The control unit 140 may be located remote from the rest of  
25 the system, for example outside the inner part of a clean room. The control system may further be connected to an actuator system 146 for control of movement of the moveable stage 132 and scanning of the beamlets by the deflector array 109. The control unit 140 may be arranged for processing pattern data to generate signals for control of the blanker electrodes. The pattern data is preferably converted to modulated light beams for transmission  
30 to the beamlet blanker array 106 using optical fibers. A plurality of control circuits, including

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light sensitive elements and/or demultiplexors, may be arranged to receive the pattern data and supply corresponding control signals to the beamlet deflectors 30. In one embodiment, the modulated light beams projected from optical fiber ends onto corresponding light sensitive elements located on the beamlet blanker array 106. The light sensitive elements may  
5 be arranged to convert the light signals into electrical signals for control of the blanker electrodes.

[0069] The charged particle lithography apparatus 100 operates in a vacuum environment. A vacuum is desired to remove particles which may be ionized by the charged particle beams and become attracted to the source, may dissociate and be deposited onto the machine  
10 components, and may disperse the charged particle beams. A vacuum of at least  $10^{-6}$  bar is typically required. In order to maintain the vacuum environment, the charged particle lithography system is located in a vacuum chamber 135. All of the major elements of the lithography apparatus 100 are preferably housed in a common vacuum chamber, including the charged particle source, projector system for projecting the beamlets onto the substrate, and  
15 the moveable stage.

[0070] Fig. 2 shows a simplified block diagram illustrating the principal elements of a modular lithography apparatus 500. The lithography apparatus 500 is preferably designed in a modular fashion to permit ease of maintenance. Major subsystems are preferably constructed in self-contained and removable modules, so that they can be removed from the lithography  
20 apparatus with as little disturbance to other subsystems as possible. This is particularly advantageous for a lithography machine enclosed in a vacuum chamber, where access to the machine is limited. Thus, a faulty subsystem can be removed and replaced quickly, without unnecessarily disconnecting or disturbing other systems.

[0071] In the embodiment shown in Fig. 2, these modular subsystems include an  
25 illumination optics module 501 including the charged particle beam source 101 and beam collimating system 102, an aperture array and condenser lens module 502 including aperture array 103 and condenser lens array 104, a beam switching module 503 including the multi-aperture array 105 and beamlet blanker array 106, and projection optics module 504 including beam stop array 108, beam deflector array 109, and projection lens arrays 110. The modules  
30 are designed to slide in and out from an alignment frame. In the embodiment shown in Fig. 2,

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the alignment frame comprises an alignment inner subframe 505 and an alignment outer subframe 506. A frame 508 conductive supports the alignment subframes 505 and 506 via vibration damping mounts 507. In alternative embodiments the frame 506 is hanging as a pendulum. The substrate 130 rests on substrate support structure 509, which is in turn placed  
5 on a chuck 510. The chuck 510 sits on the stage short stroke 511 and long stroke 512. The lithography apparatus is enclosed in vacuum chamber 135, which may include a mu metal shielding layer or layers 515, and rests on base plate 520 supported by frame members 521.

[0072] Fig. 3 shows a simplified schematic view of an example of a beamlet blanker array 106. The beamlet blanker array 106 may comprise a plate-like body or substrate on which the  
10 beamlet deflectors are arranged.

[0073] In the embodiment shown in Fig. 3, the beamlet blanker array 106 is subdivided into beam areas 51 and non-beam areas 52, the embodiment shown having 5 beam areas 51 and 10 non-beam areas 52, although other arrangements are also possible. The electron beamlets 123 are directed onto the beam areas 51 of the beamlet blanker array 106 by the upstream  
15 elements of the lithography system. A beam area 51 comprises a plurality of apertures (e.g. holes in the beamlet blanker array substrate) through which the electron beamlets 123 pass, a plurality of blanker electrodes positioned adjacent to the apertures for deflecting the electron beamlets 123, and conductive lines connecting the blanker electrodes to control circuits for energizing the blanker electrodes. A non-beam area 52, on the other hand, is positioned  
20 outside the normal path of the beamlets 123, and does not include blanker electrodes and corresponding holes, but includes circuits for control of the blanker electrodes located in the adjacent beam areas 51. A non-beam area 52 may include light sensitive elements such as photo-diodes for receiving modulated optical signals carrying the pattern data and converting the optical signals into electrical signals for control the beamlet deflectors. Optical fibers for  
25 guiding the modulated optical signals towards the light sensitive elements may be routed in the non-beam areas to avoid interfering with the beamlets 123. The control circuits in the non-beam areas may also include timing circuits, circuits for demultiplexing a multiplexed optical control signal to derive separate control signals for control of multiple beamlet deflectors, power supply circuits, and other circuits.

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[0074] A power supply for the beamlet blanker array may comprise a power unit 300 with connections 301 to a number of power connectors 201. In the shown embodiment, the power connectors 201 are in the form of thin conductive plates or slabs, which are positioned in the non-beam areas 52 to avoid interfering with the beamlets 123. The power slabs 201 may be oriented substantially perpendicular to the surface of the blanker array 106, having a long edge parallel to the surface of the blanker array 106 for making connections thereto, and a short edge perpendicular to (or at an angle to) the surface of the blanker array 106 for making connections to the power unit 300 via connections 301. The power connectors 201 could also take the form of a ribbon comprising a plurality of parallel conductors, of other suitable form.

[0075] Each beam area 51 may be served by two adjacent non-beam areas 52, as shown in Fig. 3. In a preferred embodiment, the blanker electrodes in a beam area 51 are controlled by signals received by light sensitive elements in the non-beam areas 52 located on both sides of the beam area. Moreover, for each beam area 51, electrical power is supplied by the two adjacent power connectors 201 connected to the non-beam areas on either side of the beam area. This arrangement permits the shortest path for control and power signals from a non-beam area to blanker electrodes in an adjacent beam area.

[0076] For use in lithography machines, the active area of the blanker array 106 (e.g. encompassing all the beam areas 51) is typically less than 10x10 cm. The beamlet blanker array 106 typically has a length L in a direction parallel to the power connectors 201 of about 40 mm, and a width W in a perpendicular direction of about 30 mm, and the active area of the beamlet blanker array 106 is preferably substantially in the form of square having sides of 25-30 mm, e.g. 27 mm. The width of an individual beam area 51 can be varied to an appropriate value, for example in a range between 0.1 and 10 mm, to allow sufficient area for the non-beam areas.

[0077] The beamlet blanker array 106 may be constructed from one or more integrated circuits assembled to form the beam and non-beam areas. For example, each beam area 51 and portions of two adjacent non-beam areas 52 serving the beam area, may be formed as a single unit, with the beamlet deflectors and interconnecting signal lines, and optionally some or all of the control circuits, formed as an integrated circuit. In the embodiment shown in Fig. 3, the active area of the beamlet blanker array 106 is divided into five integrated circuits 50.

The integrated circuit 50 typically has a width of less than 6.5 mm and a length of less than 30mm, the substrate having an area of less than 200 mm<sup>2</sup>. The width of the beam areas 51 and non-beam areas 52 may be substantially the same. In this case, the beam area 51 in a integrated circuit 50 typically has an area of less than 65 mm<sup>2</sup>.

5 [0078] Fig. 4 schematically shows a top view of a more detailed lay-out of a portion of the integrated circuit 50. In the shown embodiment, two non-beam areas 52 are arranged on each side of the beam area 51. The non-beam area 52 contains the electrical circuits and components responsible for controlling the deflection of the beamlets 123 which pass through the beam area, such as light sensitive elements and/or demultiplexers. In this embodiment, the  
10 non-beam areas 52 effectively cover all the surface area of the integrated circuit 50 that is not reserved for the beam area. Power is supplied by two power connectors 201 arranged on and electrically connected to the non-beam area 52.

[0079] The non-beam areas 52 include an optical interface area 53 and a power interface area 55, and may further include an additional interface area 57. The optical interface area 53  
15 is reserved for establishing an optical interface between a plurality of optical fibers and light sensitive elements on the beamlet blanker array. The optical fibers are arranged for guiding the modulated light beams towards the light sensitive elements placed within the optical interface area 53. The optical fibers are suitably arranged so that they do not physically block electron beamlets within the beam area 51 during use of the lithography system.

20 [0080] In one embodiment, the optical interface area 53 is a long rectangular area (e.g. 27 mm × 2.0 mm). One long edge of the optical interface area 53 is the boundary with the beam area 51. The beamlet deflectors 30 in the beam area 51 are distributed along the length of the beam area. The light sensitive elements are preferably distributed along the length of the optical interface area 53 so that each light sensitive element is located close to the beamlet  
25 deflector(s) 30 in the beam area 51 which are controlled by signals from the light sensitive element. The other long edge of the optical interface area 53 is the boundary with the power interface area 55 where the power connector 201 is connected. The non-beam area 52 may further include an additional interface area 57 to accommodate further circuitry, for example clock and/or control circuits.

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[0081] The beam area 51 comprises a plurality of beamlet deflectors 30 distributed over the beam area. The beamlet deflectors 30 are preferably electrostatic deflectors with a first electrode 32 and a second electrode 34. Fig. 4 shows an example of an arrangement of individual beamlet deflectors 30, each comprising round / circle shaped electrodes 32, 34 surrounding an aperture 35 extending through the beamlet blanker array substrate. The round / circle shaped shape results in the electrodes 32, 34 having a shape conformed to the cylindrical apertures 35, which is beneficial for reducing certain optical aberrations such as astigmatism. By carefully choosing the layout and deflection direction of the electrodes, the deflection of the beamlets can be spread out in various directions, preventing undesirable buildup of charge in specific locations of the lithography system.

[0082] It is desired to provide a multi-beamlet charged particle lithography system able to achieve smaller critical dimensions, e.g. 22 nm, while maintaining sufficient wafer throughput, e.g. 10 or more wafers per hour. A higher resolution can be obtained by reducing the spot size and increasing the charged particle beam current generated in the system. A reduced point spread function of beamlets is also required to maintain sufficient exposure latitude, e.g. a relatively high ratio of peak exposure level on the target from one feature compared to base or background level of exposure normally caused by neighboring features, which reduces the current applied to the target by each beamlet. The requirements of reduced spot size, increased beam current, and reduced point spread function implies a considerable increase in the number of beamlets in the system. This creates a problem due to the limited physical dimensions of the projection optics in a multi-beamlet system, which is typically limited to a size corresponding to the size of the die to be exposed.

[0083] In such a high throughput lithography system, the number of electron beamlets and corresponding beamlet deflectors 30 may be very large, e.g. millions or billions of beamlets and beamlet deflectors. As the number of beamlet deflectors in the blanker array increases, the spacing between the beamlet deflectors decreases. This creates problems in designing and fabricating an interconnect structure able to route control signals to control each of the beamlet deflectors from the control circuits.

[0084] Fig. 5 schematically shows a top view of a topographic arrangement of components that may be used in an integrated circuit 50 of the beamlet blanker array 106 as discussed with

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reference to Figs. 1-4. The beamlet blanker array is divided into beam areas 51 including beamlet deflectors 30, and non-beam areas 52 including control circuits 39 including light sensitive elements 40 and demultiplexers 41 but no beamlet deflectors. The light signals received by the light sensitive elements 40 may be multiplexed to include control signals for more than one beamlet deflector 30. The light signals are transferred to a demultiplexer 41 to be demultiplexed and forwarded to individual deflectors 30 via dedicated conductive lines 43.

[0085] This arrangement results in the number of light sensitive elements 40 being lower than the number of deflectors 30, and enables reduction of the dimensions of the non-beam areas 52. The deflectors 30 in the beam areas 51 may then be placed more closely together to increase the number of beamlet deflectors 30 per unit area in the integrated circuit 50, resulting in a more compact layout for a given number of beamlet deflectors with increased number of beamlet deflectors for the same beamlet blanker area.

[0086] Fig. 6 shows a cross-sectional view of a beamlet deflector 30 in a beam area 51. The beam area 51 is constructed in layers on a substrate 401, e.g. a silicon substrate, and the beamlet deflector 30 has electrodes 32, 34 located on opposing sides of the aperture 35 for generating an electric field across the aperture 35. The aperture 35 forms a hole through the substrate 401 forming a path for passage of an electron beamlet. An interconnection line 404 is shown for transmitting an electrical signal to the electrode 32 for control of the beamlet deflector 30. The structure can be manufactured using standard processing techniques typically used for manufacturing integrated circuits, by depositing and etching alternating layers of conductive and insulating materials. The beamlet deflector electrodes 32, 34 can be formed on a single layer of the beam area 51, but are preferably formed as a multi-layer structure to provide a greater area to generate a greater electrostatic field. The electrodes 32, 34 must be capable of generating an electrostatic field of sufficient strength to deflect a charged particle beamlet passing through the aperture 35. Forming the electrodes on multiple layers of the beam area structure provides electrodes with a greater surface area through the depth of the aperture, so that the electrostatic field generated by the electrodes acts upon the electron beamlet over a greater distance (or at multiple points) along the beamlet's path through the aperture.

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[0087] In the embodiment shown, the electrodes 32, 34 are formed from four layers 32a-d, 34a-d of conductive material separated by layers of insulating material 145, and the planar conductive layers are electrically connected by one or more conductive vias 36 through the insulating layers 145. This structure is preferably built up using standard processing techniques of depositing and etching alternating layers of conductive and insulating materials. This structure results in multiple levels 136a-d on which planar conductive layers are formed for the deflector electrodes and interconnections, and multiple levels 137 of insulator through which the vias 36 are formed. The embodiment shown has four levels of planar conductive layers, but it will be understood that more (or fewer) levels may be used.

[0088] A problem encountered with this construction is that the insulating layers become charged by electrons from the electron beamlets passing through the apertures 35 and impinging on the surface of the beamlet blanking array. This charge accumulates and may cause undesired deflection of the beamlets, resulting in writing errors in the exposure. One solution is to make the insulating layers thinner. However, a relatively thick insulating layer is desired to avoid increasing the parasitic capacitance between the planar conductive layers, and it is also desired to use a standard fab manufacturing process to avoid the additional cost and uncertainty of designing a new non-standard process.

[0089] Another approach is to etch the insulating layers 145 to move them back from the walls 35a of the apertures 35. This creates a shielding width, i.e. the distance between the edge of the insulating layers and the aperture wall 35a. This reduces the charging of the insulating layers and, because the charged edges of the insulating layers are further from the beamlet path, it reduces the effect that any accumulated charge has on the beamlets. The ratio between the shielding width and the thickness of the insulating layers should be at least 2, and preferably as high as 3. However, the shielding width required to solve the charged insulator problem becomes a limiting factor as the number of beamlets in the lithography system is increased. As the number of beamlets and beamlet deflectors is increased, and the dimensions of the electrodes and the space between adjacent beamlet deflectors are decreased, the etching of the insulating layers 145 away from the apertures 35 will result in insufficient physical support for the planar conductive layers. Without something to support the planar conductive layers 32a-d, 34a-d, they will collapse onto the substrate 401. Contact between the planar

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conductive layers and the substrate is not desired due to the relatively high conductivity of a typical silicon substrate.

[0090] One solution is to make the substrate from a material with sufficiently low conductivity, or use a thin insulating layer on the surface of the substrate that will not be removed when the other insulating layers are removed. However, these approaches are not favored when they result in moving away from a standard fab process or introduce additional complexities into the manufacturing process. Another solution, adopted in certain embodiments of the invention, is to create doped regions to physically support the planar conductive layers.

[0091] Fig. 7 shows the same cross-section of a beamlet deflector 30 having the same features as in Fig. 6. However, doped regions 402 are formed at the surface of substrate 401 and vias 36 are formed on the doped regions to support the planar conductive layers. In the embodiment shown, doped regions 402 are formed under the first electrode 32 and vias 36 are formed on the doped regions 402 to support the first electrode 32. The second electrode is supported directly on the substrate surface, e.g. in designs where the second electrodes are connected to a common voltage, but doped regions may also be formed to support the second electrode. A doped region 402 is also shown at the surface of substrate 401 and support 403 is formed on the doped region to support the interconnecting line 42a.

[0092] Using this construction, the doped regions 402 may be doped with n-type dopant and the substrate doped with p-type dopant, or the doped regions 402 may be p-type and the substrate n-type. Thus, the regions 402 form a first doped region and the substrate 401 forms a second doped region. With this construction, a voltage may be applied to the overlying planar conductive layers (e.g. electrode 32) to create a reverse-biased diode at the junction of the first doped region 402 and the second doped region (the substrate 401). This reverse biased diode effectively insulates the planar conductive layers from the substrate and insulates the first electrode 32 from the second electrode 34. The first doped regions 402 can be formed in the surface of the substrate 401 using standard well-developed techniques, and can be created with sufficiently small size.

[0093] In the embodiment shown in Fig. 7, the insulating layers 145 shown in Fig. 6 have been completely removed in the area around the beamlet deflectors 30. This may be achieved

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using a wet etch process as described in more detail below. This removes the problem of charge accumulation on the insulating layers. However, it is not essential that the insulating layers 145 have been completely removed. The object of the invention is also reached if the insulating layers 145 have been partially removed within a region 450 abutting and enclosing the aperture 145 as illustrated in Fig. 7. Completely removal, however, is less complex, as no masking is required. The first doped regions 402 supporting the first electrode 32 are shown directly underneath the conductive elements 32a-d forming the electrode, but they may also be formed at one or more points under or adjacent to the electrode, e.g. as shown in the embodiment of Fig. 8.

[0094] The first electrodes 32 of the beamlet deflectors 30 need to each receive a control signal to operate. In a lithography system in which each beamlet can be individually switched or modulated, each first electrode 32 needs a separate signal applied to it to operate (the second electrodes 34 are usually connected to a common voltage to avoid the need to make individual connections to these electrodes). In a system with a very large number of beamlets and a corresponding number of beamlet deflectors, there is not enough space between the beamlet deflectors for control circuits. This necessitates arranging the beamlet deflectors in groups and locating the control circuits at the edge of the group. In one embodiment this group is the same as the group of beamlets that is imaged by the same projection lens / that originates from the same beam. This arrangement requires a large number of interconnections between the control circuits 39 and the first electrodes 32 of the beamlet deflectors 30 to transmit the required control signals to the electrodes.

[0095] For example, a lithograph system may generate an electron beam 120 which is divided into 13,260 beams 122, each beam being further divided into 49 beamlets 123 (e.g. in a 7x7 array) to generate a spot size on the target of 25nm. In a practical system, the resulting pitch between the beamlets 123 (and beamlet deflectors 30) at the beamlet blanker array 106 is about 8 um (micrometers). To reduce the spot size to 17.7 um with corresponding increase in total beam current, each sub-beam 122 may be divided into 400 beamlets 123 (e.g. in a 20x20 array), reducing the pitch between the beamlet deflectors 30 to about 2.6 um. Further reductions in spot size result in a still larger number of beamlets and further reductions in the pitch between beamlet deflectors.

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[0096] To route the interconnections from the control circuits 39 to the deflector electrodes 32, a large number of connecting lines 42 must fit in the gap between adjacent beamlet deflectors. For example, 400 beamlets 123 may be generated from each sub-beam 122 and are arranged in a group, so that the beamlet blanker array 106 has beamlet deflectors 30 for the group arranged at a pitch of 2.6  $\mu\text{m}$  between adjacent beamlet deflectors. Nine connecting lines will be required to fit between the gap between beamlet deflectors, assuming the beamlet deflectors are arranged in a 20x20 array, the control circuits for driving the beamlet deflectors are arranged on each side of the array, and the beamlet deflectors at the edge of the array do not require connecting lines routed through the gap. These connecting lines could be arranged, e.g. on five levels with two connecting lines on each level, assuming a process with five layers of conductive material available for making these connecting lines.

[0097] In a variation to the embodiment of Fig. 7 the substrate 401 is conductive and acting as a deflector 32, 34. It is the conductive support which efficiently connects the respective deflector to the respective substrate. In order to be able to provide different voltages to the respective half regions of the substrate around the aperture 35, the substrate needs to be divided into isolated electrical regions. Such electrical isolation may be achieved by using a deep plug of insulating material around said aperture but spaced apart therefrom. Moreover, said substrate within the insulating trench must be divided into two parts, for example by making a further trench of insulating material, which cuts the substrate region around the aperture 35 into two halves. It must be stressed at this stage that the presence of insulating dielectric near the aperture is something, which the invention aims to prevent or reduce. Thus, optionally, such insulating material may be selectively removed, such that no charge carriers may be trapped near the aperture 35.

[0098] Fig. 8 shows a plan view of a portion of an integrated circuit with an embodiment of an interconnect structure 400, which may be used for routing connecting lines in very small areas in the integrated circuit structure, e.g. for routing connecting lines 42 from control circuits 39 to beamlet deflectors 30. Fig. 9 shows a perspective view of the interconnect structure 400 (but omitting the deflector electrodes). The interconnect structure uses the same features described for the beamlet electrodes shown in Fig. 7 for support of the connecting lines.

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[0099] The interconnect structure 400 includes a plurality of conductive connecting lines 42 for electrically transmitting signals, and a plurality of conductive supports 403 for supporting the conductive lines 42. The substrate comprises a plurality of first regions 402 at the surface of the substrate 401 and at least one second region, the doping of the first and second regions being different. For example, the first regions 401 may be doped with n-type dopant and the second region doped with p-type dopant, or vice versa. The conductive supports 403 are formed at the location of the first regions 402, and extend out from the substrate 401, preferably extending substantially perpendicular to the surface of the substrate 401. The conductive supports 403 connect with and support the conductive lines 42.

[00100] The conductive lines 42, supported by the conductive supports 403, form a free-hanging structure. The interconnect structure 400 may be oriented in different positions, e.g. it may be oriented so that the first regions are formed at an upper surface of the substrate 401 and the conductive supports 403 extend upwards from the substrate 401 to support the conductive lines 42. Or the structure may be oriented with the first regions formed at a downwards facing surface of the substrate 401 and the conductive supports 403 extending downwards from the substrate 401. Other orientations are also possible.

[00101] In the embodiment shown in FIGS. 8 and 9, four conductive lines 42 are shown, arranged to form two routing rows 405, each having two lines 42 extending parallel to each other with a series of conductive supports 403 positioned between the two lines. A plurality of separate first regions 402 are formed as circular doped wells in the surface of substrate 401, spaced along the length of each routing row 405. A plurality of conductive supports 403 are spaced along the length of each routing row, with one support formed above each first region 402. The conductive supports 403 are connected to the conductive lines 42 via connection bridges 404. In the embodiment shown, the connection bridges 404 extend laterally out from and substantially perpendicular to the conductive supports 403.

[00102] The first regions 402 may be formed by selectively doping the substrate 401, and these regions may be made relatively small using a standard fab process. For example, the first regions 402 may be formed with a diameter of 180nm using a 65nm process. The conductive lines 42 may be formed with a width and spacing substantially less with the width of the first regions 402. In the embodiment illustrated, the first regions 402 and conductive

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supports 403 are aligned in rows with a conductive line 42 arranged on each side of the row for support. This arrangement permits the conductive supports 403 to connect to and support conductive lines 42 at more than one level 136 within the structure 400.

[00103] Fig. 9 shows an embodiment with two conductive lines 42a-b extending along opposite sides of the routing row 405 at a first level a certain height above the surface of the substrate 401, and two other conductive lines 42c-d arranged in a similar way at a second level at a greater height above the substrate surface. Additional connection levels may be included, and each of the connection levels may have a plurality of conductive lines running substantially parallel to each other.

[00104] The conductive lines 42 and conductive supports 403 are thus arranged to form an interconnection corridor in which the conductive lines extend substantially parallel to each other on a plurality of connection levels 136 at different heights with respect to the substrate 401. Note that for each conductive line 42, the distance between conductive supports 403 which support that conductive line increases with the number of connection levels if the pitch between the conductive supports 403 is constant. Thus, a balance is made between the number of levels of the connection lines and the frequency of conductive supports for each conductive line. Typical distance between the support structures is 0.5 to 5 micron. The interconnection corridor may be straight or may include curves or bends where necessary to efficiently route the conductive lines through the structure. The conductive lines may extend along the corridor in a generally parallel fashion as shown in Fig. 9, although the distance between adjacent conductive lines may vary and the conductive lines may cross-over (without contacting each other). In this way, the interconnection corridor forms a sort of bus-like structure for efficiently routing a large number of conductive lines through the structures formed on the substrate.

[00105] Fig. 10 shows a cross section of another embodiment of an interconnect structure 400, in combination with blanker deflector electrodes 32, 34. The structure includes the same features described above for the embodiments of FIGS. 7-9. The electrodes 32, 34 and interconnect structure 400 are arranged to hang from the bottom surface of the substrate 401. In this embodiment, the interconnect structure 400 comprises a single routing row with five connection levels 136 and two conductive lines 42 per level arranged with one line on each

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side of the conductive supports 403, and the conductive supports 403 connected to a first region 402 on the surface of the substrate 401. The interconnect structure is positioned between a first electrode 32 of a first deflector 30 at one aperture 35, and a second electrode 34 of a second deflector 30 at an adjacent aperture 35. In this embodiment the structure the aperture array 105 is integrated in the beamlet blanker array 106. An individual beam limiting aperture of the aperture array 105 may be formed by the protrusion 105A formed from the metal layer closest to the substrate. This will be further explained in the description of Fig. 13.

[00106] In the interconnect structure 400 shown in FIGS. 8-10, and the beamlet deflector 30 shown in FIGS. 7, 8 and 10, the adjacent conductive lines 42 and electrodes 32, 34 are separated by air (or by the ambient gas if it is not air) or vacuum. The conductive lines 42 and electrodes 32, 34 are separated and isolated from each other without an intervening solid insulating material. The conductive lines 42 and electrodes 32, 34 are suspended in position by the conductive supports 403 and/or vias 36. The small size of the structures results in gravitational force on the structure being negligible. When in operation, electromagnetic and electrostatic forces will generally exert much greater forces on the structure, but these can be calculated and the structure designed to adequately withstand such forces.

[00107] In the interconnect structure 400 and beamlet deflector 30, the first regions 401 may be doped with n-type dopant and the second region doped with p-type dopant, or vice versa.

Furthermore the dopant material and/or dopant concentration may be different for the different regions. The first regions 402 may be formed as a plurality of separate relatively small regions or doped wells at the surface of the substrate 401, and the second region 406 may comprise a part or substantially all of the remaining portion of the substrate 401. A p-n or n-p junction 407 may be formed at the intersection of the first and second regions, creating a diode. This diode junction 407 electrically isolates the second region 406 and/or the body of the substrate 401 from the conductive supports 403 and conductive lines 42, which are preferably connected to a common or ground potential. The diode junction should be designed so that the control signals transmitted via the conductive lines 42 and/or applied to the electrodes 32 create a reverse bias across the diode 107, and the control signals should be lower than the breakdown voltage of the diode.

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[00108] The interconnect structure 400 and/or the beamlet electrodes 32, 34 may be manufactured as and form part of a single integrated circuit 50 formed on the substrate 401. Control circuits 39 may optionally also be manufactured as part of the single integrated circuit. The interconnect structure 400 and/or the beamlet electrodes 32, 34 are preferably made using standard processing techniques of depositing and etching alternating layers of conductive and insulating materials. The planar conductive layers, from which the electrodes 32, 34, conductive lines 42, vias 36, conductive supports 403, and connection bridges 404 are formed, are typically formed of suitable metals, such as copper or aluminum. The insulating layers typically comprise silicon dioxide, low-k dielectric (with a small dielectric constant relative to silicon dioxide) or other suitable insulating materials. This structure results in multiple levels 136a-d on which planar conductive layers are formed for the deflector electrodes 32, 34 and conductive lines 42, and multiple levels 137 of insulator through which the vias 36 and support 403 are formed.

[00109] In a charged-particle multi-beamlet lithography system generating a large number of beamlets, e.g. thousands or millions of beamlets, wherein the integrated circuit 50 typically has a beam area 51 less than  $65 \text{ mm}^2$ , the number of the conductive supports 403 in the interconnect structure may easily be 1000 or more. The first regions 402 may be arranged with a pitch of approximately 180 nm, and the beamlet deflectors 30 a pitch of about 1 micron. In the embodiment shown in FIGS. 8 and 9 the first regions 402 and conductive supports 403 are arranged in a rectangular array, but other arrangement are also possible, e.g. hexagonal close packed. The beam area 51 and the non-beam areas 52 may share the same substrate 401. The interconnect structure in non-beam areas 52 may be the interconnect structure as discussed with reference to FIGS. 8-10 or a conventional multi-layer structure.

[00110] Fig. 11 schematically shows a top view of an alternative arrangement of components that may be used in an integrated circuit 50 with reference to Fig. 5. In this embodiment, the beamlet deflectors 30 are arranged in columns and rows to allow addressing via wordlines 80 and bitlines 90. Such arraywise addressing reduces the number of connections extending from the demultiplexer 41 to the beamlet deflectors 30. For example, in Fig. 11 only 10 connection lines are present, while individual addressing would result in 25 connection lines to address the 25 beamlet deflectors 30. In other words, the connections may occupy less space if placed

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in such arraywise addressing arrangement. Suitably, the demultiplexers 41 may be moved towards the beam-area 51 to shorten the connections with the respective beamlet deflectors 30. This is particularly useful when the distance between light sensitive elements 40 and the deflectors 30 is relatively large, for example in the order of 100 micrometer or more.

5 [00111] In order to ensure that the beamlet deflectors 30 deflect a passing beamlet during a full deflection period, the beam area 51 may further include memory cells 95 coupled to respective beamlet deflectors 30 for temporarily storing a control signal dedicated for the respective beamlet deflector 30 for a predetermined period of time, as shown in Fig. 11. The predetermined period of time may correspond to or be larger than the full deflection period to  
10 ensure that the control signal is available for such entire deflection period. This arrangement allows the deflection step to be independent from the transmission of control signals time wise. Furthermore, the transmission of control signals may thus be done sequentially, whereas the deflection of beamlets is performed simultaneously.

[00112] The interconnect structure 400 of the present invention, e.g. the embodiments shown  
15 in Figs. 8-10, may be applied in the arrangement in Fig. 11. For example, the routing conductive supports 403 may be arranged to form a two dimensional routing rows 405, e.g. arranged in a direction with a pre-determined pitch, in a perpendicular direction with another pre-determined pitch. Wordlines may connect to the electrodes at a different level within the interconnect structure 400 than bitlines. Consequently, the density of connection lines per unit  
20 area of the beamlet blanker array may improve, which provides the opportunity to place the beamlet deflectors at a closer pitch than would be possible if all connections were to be located within the same level. The memory cells 95 may be arranged within the substrate 401 in a close proximity with the beamlet deflectors 30. Suitably, the memory cells 95 should be manufactured relative small compared to the pitch of the deflectors 30 so that the memory  
25 cells may be arranged at a place not to be easily charged by the beamlets 123.

[00113] Figs. 12A-12F schematically show a cross-sectional view of steps of a method for manufacturing of the interconnect structure 400 with reference to Figs. 7-10 in the beamlet blanker array 106 with reference to Figs. 1-5. There may be various other ways to manufacture the same structure in terms of order or process steps, material choices, etching  
30 method and chemistry, and so on.

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[00114] Fig. 12 A shows a first stage in the manufacturing process, which includes selectively doping the substrate 401, e.g. a p-type substrate, with a plurality of the first regions 402, e.g. n-type wells in the surface of the substrate.

[00115] Fig. 12B shows a second stage in the process, after alternating layers of conductive and insulating material have been deposited and etched to form routing conductive supports 403, conductive lines 42, vias 36, multi-level first electrodes 32a-c, and multi-level second electrodes 34a-c, as described with reference to Figs. 8-11. The resulting multi-level structure comprises conductive elements (conductive lines 42, conductive supports 403, vias 36, connecting bridges 404), formed on the surface of an underlying insulating layer 145 and surrounded by insulating material 145. In the embodiment shown in Fig. 12B, the conductive lines 42 and the major body of the electrodes 32, 34 are arranged at levels 136a-d, and the vias 36 for electrically connecting different portions of the electrodes are arranged at levels 137, and the conductive supports 403 are arranged through one or more layers 136 and 137. Aperture areas may be kept free of metal structures and filled with insulating material 145.

[00116] Other possible active elements for the beamlet blanker array 106 such as memory cells 95 and amplifiers may be arranged within the substrate 401. The substrate 401 typically comprises doped silicon, or doped silicon-on-insulator, or another modified doped silicon substrate, such as SiGe. Although not shown, the interconnect structure 400 may be covered with a passivation layer for protecting the structure. For use in an application for charged particle lithography, such passivation layer is preferably covered with a conductive coating to avoid any undesired buildup of charge within the system.

[00117] The multi-level structure may be manufactured using known semiconductor processing techniques, for example techniques to produce a CMOS-chip. The use of known semiconductor processing techniques to provide a basic building block of the beamlet blanker array significantly reduces the costs of manufacturing. Furthermore, the use of such body improves the reliability of the beamlet blanker array manufactured in accordance with the process of manufacturing described below.

[00118] In Fig. 12C, the interconnect structure 400 may be covered by a resist layer 151. The resist layer 151 may be exposed in accordance with a pattern to obtain the shown structure using well know processes. Next, the first resist layer 151 may be used as an etch mask for

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removal of insulating material 145. The etching may again include ICP etching in a suitable plasma, e.g. a fluorine-based plasma. A result of this etching step is shown in Fig. 12D forming the aperture 35.

[00119] In Fig. 12E, apertures 35 are etched in the substrate 401, preferably using an  
5 anisotropic etching technique. A suitable etching technique is so-called Bosch-etching, in particular if the substrate is a silicon substrate.

[00120] Finally, as shown in Fig. 12F, a chemically selective etching technique may be used to remove the insulating material 145. A suitable chemically selective etching technique includes wet etching, and suitable etchant may comprise hydrofluoric acid.

10 [00121] It is not essential that the insulating layers 145 have been completely removed. The object of the invention is also reached if the insulating layers 145 have been partially removed within a safety region 450 abutting and enclosing the aperture 145 as illustrated in Fig. 7. Complete removal, however, is less complex, as no masking is required.

[00122] Fig. 13 shows a cross-sectional view of an embodiment of modulation device in  
15 accordance with the invention as illustrated in Fig. 10, wherein a current limiting aperture array 105 has been integrated in the metal stack. The figure shows only two apertures 35, each having a grounded electrode GE (for example, having a half circle shape) and an active (deflector) electrode AE (for example, having a half circle shape) located on opposite sides of the aperture 35. Note that the grounded electrodes GE may be connected to an electrical  
20 ground potential or same other common reference potential. Although only two apertures 35 have been illustrated, in a modulation device for a charged particle lithography machine there may be ten thousands or up to several million of such apertures integrated in a single substrate 401. Putting so many apertures 35 in a certain area implies that there is not much routing space available for connecting all the electrodes to their respective drivers. The invention  
25 advantageously provides a routing concept which uses the available routing space to the maximum extent possible. The earlier described routing conductive supports 403 and conductive lines 42a-d are arranged between electrodes GE and AE. In order to isolate the routing conductive supports from the substrate and the grounded electrodes GE (the substrate 401 is grounded or connected to the same common potential as the grounded electrodes, and

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form part of the grounded electrodes), pn-junctions that are reverse biased are formed in the substrate 401 at the regions 402, underneath the conductive supports 403 as earlier explained.

[00123] On the left hand side of the left aperture 35 in Fig. 13, the boundaries of the internal grounded electrode GE and the active electrode AE have been illustrated by means of the

5 thick lines enclosing respective patterned areas. The process technology in the example shown in Fig. 13 features 10 metallization layers M1-M10 used for making interconnections (polysilicon layer(s) not counted and not shown in the drawing). However, the invention is not limited to any specific number of interconnect layers. Typically in a process technology the upper layers M8, M9 have a larger minimum pitch and a larger minimum width in

10 addition to a larger layer thickness. In this embodiment the upper layer M10 is an Aluminum layer, which is conventionally used for shielding purposes. In this embodiment, this layer is conveniently used as an upper interconnect layer of the grounded electrodes GE only, which is connecting all grounded electrodes GE together. Between the substrate and neighboring pairs of the interconnect layers M1, M2, M3, M4, M5, M6, M7, M8, M9, M10 there are

15 respective insulating layers, denoted as layers CO, V1, V2, V3, V4, V5, V6, V7, V8, V9 through which conductive vias may be formed. The conductive material forming the vias on these layers are typically square shaped, while the conductive material on the interconnect layers may take many shapes, such as rectangles for routing, circles for the electrodes, etc.

The ground electrode GE comprises the substrate 401 and metallization layers M1-M10 and via layers V1-V9. The active electrode AE only comprises the metallization layers M2 to M9 and via layers V1 to as illustrated in Fig. 13.

[00124] A very interesting aspect in the embodiment of Fig. 13 is that a current-limiting aperture array 105 has been formed in conductive layer M1 of the modulation device (rather than as a separate substrate that is mounted upstream of the modulation device). Such array is made current-limiting by making the width of the opening in the M1 layer smaller than that of the aperture 35 at the protrusion 105A. The embodiment of Fig. 13 is an advantageous embodiment, because the substrate 401 is only connected to one potential, e.g. the ground potential. In order to make the design less complex also the first metallization layer M1 forming the aperture area is connected to the same potential (e.g. ground or a common

25  
30 potential).

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[00125] It must be noted that the modulation device in Fig. 13 has been drawn-upside down, in that the electron beams 123 come from the bottom, i.e. the upstream side of the modulation device is the bottom side in the figure.

[00126] It has already been mentioned with reference to Fig. 7 that it is not essential that the substrate 401 is electrically isolated from the deflector electrodes, even though from a process point-of-view this measure provides for less complexity in the manufacturing process. In case it is desired to avoid the use of diodes to electrically isolate the substrate from the deflectors, different options exist, which are explained in the next figures. A first option is to define separate regions in the substrate 401, which are electrically isolated from each other.

[00127] Fig. 14 shows a schematic simplified cross-sectional view of an embodiment of the modulation device in accordance with the invention. Fig. 15 shows a schematic simplified top-view of the modulation device of Fig. 14. In this embodiment a silicon-on-insulator (SOI) substrate is used (for example a substrate 401 with a buried oxide layer 403), a silicon-on-sapphire (SOS) (a substrate with a buried aluminum oxide layer 403), or a silicon-on-anything (SOA) is used (a substrate with a silicon layer, provided on any other suitable material, such as glass, ceramic, etc). The buried insulator layer 403 electrically isolates the upper layer 401A (active layer) from the lower layer 401B (bulk).

[00128] It is further necessary to electrically isolate the upper layer 401A underneath the electrodes from the environment (because those regions need to carry a different potential) and from each other (because the active electrode AE carries a varying potential and the grounded electrode GE is connected to ground or common potential). For this lateral electrical isolation, different techniques exist, such as the shallow-trench isolation (STI) technique (successor of LOCOS), which is mainstream in today's CMOS processes. An STI region 408 is shown in Figs. 14 and 15, comprising a shallow trench filled with insulator. In the manufacturing of the STI regions (which in a conventional CMOS process effectively define regions where no transistor is to be formed) the STI regions extend towards the buried insulating layer 403, which electrically isolates the active layer 401A of the substrate around the aperture 35 from the environment. In order to create two sub-regions within this isolated region, a further trench 410 of shallow-trench isolation may be formed which extends from the circle-shaped STI region towards the aperture 35. Referring to the earlier-described

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problem that the invention aims to solve (the charge trapping in the dielectric layer near the aperture 35), it can be understood that both the buried oxide layer 403 as well as the shallow trench isolation regions 410 may deteriorate the performance of the modulation device, because those regions may capture charged particles similar to the insulating layers in the metallization stack. In order to improve the performance, both regions may be (selectively) etched back as illustrated by the arrows in Figs. 14 and 15, such that the region of layer 403 abutting the aperture is made substantially free of dielectric material. It must be stressed, however, that the etch-back may not be necessary in case the buried insulating layer 403 is relatively thin. Etching techniques, as such, are considered to be well-known by the person skilled in the art. These may include both wet etching (using an etchant dissolved in a fluid) as well as dry etching techniques (using a plasma).

[00129] It must be noted that alternative techniques are possible for the shallow trench isolation regions 408, 410. Basically, any electrical insulator could be used (for example silicon nitride). However, in a fabrication environment there will be clear limitations as to what materials and processes may be chosen at this stage of the processing. One aspect, which must be kept in mind in the embodiment of Figs. 14 and 15 is that it has to be taken into account that isolating regions 408 and 410 and buried layer 403 can be selectively removed with respect to the insulating layers in the metal stack, if so desired.

[00130] Fig. 16 shows a schematic simplified cross-sectional view of an alternative embodiment of the modulation device in accordance with the invention. Fig. 17 shows a schematic simplified top-view of the modulation device of Fig. 16. This embodiment will be discussed in as far as it differs from Figs. 14 and 15. In this embodiment the shallow-trench isolation regions 408' and 410' have been removed, which effectively exposes the underlying buried insulating layer 403. Similar to Figs. 14 and 15 a (selective) etch-back has been performed indicated by the arrows. In an embodiment of the invention the emptied shallow-trench isolation regions 408' are formed during the step of selective removal of the insulating layers in the metallization stack (for example in case both insulating materials comprise silicon oxide).

[00131] Fig. 18 shows a schematic simplified cross-sectional view of a further alternative embodiment of the modulation device in accordance with the invention. Fig. 19 shows a

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schematic simplified top-view of the modulation device of Fig. 18. This embodiment will be discussed in as far as it differs from the embodiments in Figs. 14 to 17. The main difference is that this embodiment does not use the substrate 401 as deflector. Instead, the substrate 401 is electrically insulated by means of an insulating layer 409 on the substrate 401, or

5 alternatively, manufactured in the substrate 401. Suitable materials comprise silicon oxide and silicon nitride, but other insulators also possible. Similar, to what has been mentioned with regards to the embodiments of Figs. 14 to 17, also in this embodiment, preferably, an etch-back is carried out as indicated by the arrows, in order to remove the dielectric material near the aperture 35.

10 [00132] It must be noted that the modulation device of the invention may be manufactured using techniques and processes, which are as such well-known to the person skilled in the art. It must also be noted that the person skilled in the art may come up with various modifications of the manufacturing process here described. All such variations and modifications are considered to fall within the scope of the invention as claimed.

15 [00133] The modulation device may also be described using the following clauses:

1. A modulation device (106) for use in a charged particle multi-beamlet lithography system (100) adapted to generate a plurality of charged particle beamlets (123), the modulation device comprising:

a substrate (401) comprising a plurality of apertures (35) formed therein, each aperture  
20 forming a path for passage of one of the plurality of charged particle beamlets (123) through the substrate; at least two electrodes (32, 34) located on opposing sides of each aperture (35) for generating a field across the aperture (35), wherein the electrodes (32, 34) each comprise one or more planar conductive layers (32a-d, 34a-d) and a first conductive support (36) mechanically coupled between a first one of the planar conductive layers (32a, 34a) and the  
25 substrate (401) for supporting said first planar conductive layer, wherein at least the first planar conductive layer (32a, 34a) and the first conductive support (36) of the electrodes (32, 34) are directly surrounded by air or ambient gas or vacuum, and wherein the conductive supports (36) comprise a via or a contact in direct contact with the substrate (401).

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2. The modulation device (106) of clause 1, wherein the electrodes (32, 34) each comprise a first plurality of conductive supports (36) mechanically coupled to the substrate (401) for supporting the first planar conductive layers (32a, 34a).
3. The modulation device (106) of clause 1 or 2, wherein the at least two electrodes  
5 (32, 34) each comprise a second planar conductive layer (32b, 34b) arranged above the first planar conductive layer (32a, 34a), and a second plurality of conductive supports (36) mechanically coupled between the second planar conductive layer (32b, 34b) and the first planar conductive layer (32a, 34a) for supporting the second planar conductive layers (32b, 34b).
- 10 4. The modulation device (106) of clause 3, wherein the second plurality of conductive supports (36) are directly surrounded by air or ambient gas or vacuum.
5. The modulation device (106) of any one of the preceding clauses, wherein the substrate (401) comprises a semiconductor substrate.
6. The modulation device (106) of clause 5, wherein the semiconductor substrate (401)  
15 comprises one or more first regions (402) of a first conductivity type underneath and in electrical contact with respective supports (36), and further comprises a second region (406) of a second conductivity type, the one or more first regions (402) being formed in the second region (406) for forming a pn-junction between the different regions.
7. The modulation device (106) of clause 6, wherein the first regions (402) form a  
20 plurality of n-type wells (402) at the surface of the substrate (401), and the second region (406) has p-type doping.
8. The modulation device (106) of clause 6, wherein the first regions (402) form a plurality of p-type wells (402) at the surface of the substrate (401), and the second region (406) has n-type doping.
- 25 9. The modulation device (106) of clause 7 or 8, wherein the first regions (402) comprise a plurality of separate relatively small regions of the substrate (401) and the second region (406) comprises substantially all of the remaining portion of the substrate (401).
10. The modulation device (106) of any one of the preceding clauses, further comprising a plurality of conductive lines (42), each conductive line (42) being coupled to a respective

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one of the electrodes (32, 34), and wherein each conductive line (42) is supported by a respective further conductive support (403) that is mechanically coupled between the respective conductive line (403) and the substrate (401) for supporting the first conductive line (403).

5 11. The modulation device (106) of clause 10, wherein the further conductive supports (403) and the conductive lines (42) comprise part of an integrated circuit (50) formed on the substrate (401).

12. The modulation device (106) of clause 10 or 11, wherein the conductive lines (42) form a free-hanging structure supported by the supports (403).

10 13. The modulation device (106) of clause 12, wherein adjacent conductive lines (42) are separated by air or ambient gas or vacuum.

14. The modulation device (106) of clauses 10-13, wherein the conductive lines (42a, 42b, 42c, 42d) are arranged on a plurality of connection levels (136) at different heights with respect to the substrate (401).

15 15. The modulation device (106) of clause 14, wherein each of the connection levels comprises a plurality of conductive lines (42a, 42b, 42c, 42d) running substantially parallel to each other.

16. The modulation device (106) of any one of clauses 10-15, wherein the conductive supports (403) are arranged at a pre-determined pitch for supporting the conductive lines (42)  
20 at a plurality of points along their length.

17. The modulation device (106) of any one of clauses 10-16, wherein each of the supports (403) is arranged on a separate first region of the substrate (401).

18. The modulation device (106) of any one of clauses 10-17, wherein the conductive lines (42) and supports (403) are arranged to form an interconnection corridor wherein the  
25 conductive lines extend substantially parallel to each other on a plurality of connection levels (136) at different heights with respect to the substrate (401).

19. The modulation device (106) of any one of clauses 10-18, wherein the conductive lines (42) are electrically connected to the supports (403) via a plurality of connection bridges

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(404), the connection bridges extending substantially perpendicular to the supports and mechanically supporting the connecting lines.

20. The modulation device (106) of any one of clauses 6-19 in as far as directly or indirectly dependent on clause 6, further comprising a control circuit (39) adapted to supply a voltage signal to the respective conductive lines (42), wherein the voltage signal creates a reverse bias across a junction between the first and second regions of the substrate (401).

21. The modulation device (106) of clause 20, wherein the control circuit is adapted to supply a plurality of signals to the conductive lines (42), each signal for control of one of the electrodes (32).

22. The modulation device (106) of any one of the preceding clauses, wherein the number of supports (403) is in the range of 10,000 to 1,000,000,000.

23. The modulation device of any one of the preceding clauses, wherein each aperture (35) and associated at least two electrodes (32, 34) form a beamlet deflector (30) arranged for deflecting a beamlet (123) passing through the aperture, and wherein the modulation device further comprises:

a plurality of control circuits (39) arranged to receive pattern data and supply corresponding control signals for control of the beamlet deflectors; and

an interconnect structure (400) connecting the control circuits to respective first electrodes of the beamlet deflectors.

24. The modulation device of clause 23, wherein at least a portion of the beamlet deflectors and at least a portion of the interconnect structure are formed as part of a single integrated circuit (50).

25. The modulation device of clause 24, wherein at least a portion of the control circuits (39) is also formed as part of the single integrated circuit (50).

26. The modulation device of any one of clauses 23-25, wherein the modulation device (106) is divided into a plurality of beam areas (51) positioned in the normal path of the beamlets (123) and a plurality of non-beam areas (52) positioned outside the normal path of

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the beamlets, wherein the beamlet deflectors (30) are arranged in the beam areas and control circuits (39) are arranged in the non-beam areas.

27. The modulation device of any one of clauses 23-26, wherein the control circuits (39) include a plurality of light sensitive elements (40) adapted to receive patterned light signals  
5 and convert the light signals to electrical signals to generate the control signals.

28. The modulation device of clause 27, wherein the control circuits include a plurality of demultiplexers (41), wherein the light signals received by the light sensitive elements are multiplexed signals which include pattern information for more than one beamlet deflector (30), and wherein the multiplexed signals are demultiplexed by the demultiplexers.

10 29. The modulation device of any one of clauses 23-28, wherein the plurality of the conductive lines (42) extend parallel to each other in a corridor between two rows of the beamlet deflectors (30).

30. The modulation device of any one of clauses 23-29, wherein the beamlet deflectors (30) are arranged in an addressable array, a first subset of the conductive lines (42) forming  
15 wordlines and a second subset of the conductive lines forming bitlines for addressing the beamlet deflectors.

31. The modulation device of clause 30, wherein the wordlines and the bitlines are arranged at different connection levels (136) in the interconnect structure (400).

32. The modulation device of any one of clauses 23-31, wherein a plurality of memory  
20 cells (95) are arranged in a close proximity with a plurality of respective beamlet deflectors (30) for temporarily storing a control signal, the temporarily stored signal being dedicated for the respective beamlet deflector for a predetermined period of time.

33. The modulation device of any one of clauses 30-32, wherein the distance of two of the adjacent beamlet deflectors (30) is less than 55  $\mu\text{m}$ .

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[00134] The interconnect structure of the invention may be used in various types of integrated circuits such as embedded memory circuits, logic circuits, and processors, and may be used to form an on-chip bus for these or other types of circuits.

5 [00135] The invention has been described by reference to certain embodiments discussed above. It will be recognized that these embodiments are susceptible to various modifications and alternative forms well known to those of skill in the art without departing from the spirit and scope of the invention. Accordingly, although specific embodiments have been described, these are examples only and are not limiting upon the scope of the invention, which is defined in the accompanying claims.

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## WHAT IS CLAIMED IS:

1. An interconnect structure (400) arranged on a substrate (401) for electrically transmitting signals, the interconnect structure comprising:
  - a plurality of conductive supports (403) extending from a surface of the substrate;
  - 5 a plurality of conductive lines (42) supported by the conductive supports;
  - wherein at least a portion of each conductive line extending between two of the conductive supports is supported only by the conductive supports at each end of the conductive line portion.
- 10 2. The interconnect structure of claim 1, wherein at least one of the conductive supports (403) at an end of the conductive line portion comprises a via or a contact in direct contact with the substrate (401).
3. The interconnect structure of claim 1 or claim 2, wherein the conductive line portion  
15 is directly surrounded by air or ambient gas or vacuum along its entire length between the two conductive supports at each end of the conductive line portion.
4. The interconnect structure of any one of the preceding claims, wherein pairs of the conductive supports (403) are electrically isolated from each other.  
20
5. The interconnect structure of any one of the preceding claims, wherein the conductive supports (403) contact the substrate (401) at a plurality of first regions, wherein the first regions comprise electrically insulating material.
- 25 6. The interconnect structure of claim 5, wherein the insulating material of the first regions preferably comprises a material that is selectively etchable with respect to an inter- or intra-layer dielectric of other structures on the substrate.
7. The interconnect structure of any one of the preceding claims, wherein the conductive  
30 supports (403) contact the substrate (401) at a plurality of first regions, wherein the first regions are isolated from a remaining part of the substrate by insulating barrier regions.

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8. The interconnect structure of any one of claims 1-4, wherein the substrate comprises a plurality of first regions at the surface of the substrate and at least one second region, the first and second regions being of a different conductivity type for forming a pn-junction between said regions, and wherein the conductive supports (403) contact the substrate (401) at the plurality of first regions.

9. The interconnect structure of claim 8, wherein the first regions form a plurality of n-type wells (402) at the surface of the substrate (401), and the second region has p-type doping.

10. The interconnect structure of claim 8, wherein the first regions form a plurality of p-type wells (402) at the surface of the substrate (401), and the second region has n-type doping.

11. The interconnect structure of any one claims 8-10, wherein the first regions comprise a plurality of separate relatively small regions of the substrate and the second region comprises substantially all of the remaining portion of the substrate.

12. The interconnect structure of any one of the preceding claims, wherein the conductive supports (403) and the conductive lines (42) comprise part of an integrated circuit (50) formed on the substrate (401).

13. The interconnect structure of any one of the preceding claims, wherein the conductive lines (42) form a free-hanging structure supported by the conductive supports (403).

14. The interconnect structure of any one of the preceding claims, wherein adjacent conductive lines (42) are separated and isolated from each other without an intervening solid insulating material.

15. The interconnect structure of any one of the preceding claims, wherein the conductive lines (42) are arranged on a plurality of connection levels (136) at different heights with respect to the substrate (401).

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16. The interconnect structure of claim 15, wherein each of the connection levels comprises a plurality of conductive lines running substantially parallel to each other over at least a portion of their length.

5

17. The interconnect structure of any one of the preceding claims, wherein the conductive supports (403) are arranged at a pre-determined pitch for supporting the conductive lines (42) at a plurality of points along their length.

10 18. The interconnect structure of any one of the preceding claims, wherein each of the conductive supports (403) is arranged on a separate first region of the substrate.

15 19. The interconnect structure of any one of the preceding claims, wherein the conductive lines (42) and conductive supports (403) are arranged to form an interconnection corridor, wherein, over at least a portion of the interconnection corridor, at least a portion or all of the conductive lines extend parallel to each other on a plurality of connection levels (136) at different heights with respect to the substrate (401).

20 20. The interconnect structure of any one of the preceding claims, wherein at least a portion of the plurality of conduction lines cross each other without making electrical contact with each other.

25 21. The interconnect structure of any one of the preceding claims, wherein the conductive lines (42) are electrically connected to the conductive supports (403) via a plurality of connection bridges (404), the connection bridges extending substantially perpendicular to the conductive supports and mechanically supporting the connecting lines.

30 22. The interconnect structure of any one of the preceding claims, wherein a plurality of the conductive supports (403) are arranged in a two dimensional array on the surface of the substrate.

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23. The interconnect structure of any one of the preceding claims, wherein the substrate comprises a plurality of first regions at the surface of the substrate and at least one second region, the first and second regions being of a different conductivity type, and wherein the conductive supports (403) contact the substrate (401) at the plurality of first regions, and  
5 further comprising a control circuit (39) adapted to supply a voltage signal to the interconnect structure, wherein the voltage signal creates a reverse bias across a junction between the first and second regions of the substrate (401).

24. The interconnect structure of claim 23, wherein the control circuit is adapted to supply  
10 a plurality of signals to the conductive lines (42), each signal for control of one of the first electrodes (32).

25. A method for operating the interconnect structure (400) of claim 23 or 24, comprising applying a first voltage ( $V_s$ ) to the interconnect structure and applying a second voltage ( $V_0$ )  
15 on the substrate (401) to create a reverse bias across a junction between the first and second regions of the substrate.

26. A modulation device for use in a charged particle multi-beamlet lithography system (100) adapted to generate a plurality of charged particle beamlets (123), the modulation  
20 device (106) arranged for modulating the charged particle beamlets in accordance with pattern data and comprising:

a plate-like substrate (401);

an array of beamlet deflectors (30) arranged for deflecting the beamlets, each deflector comprising a first electrode (32) and a second electrode (34) adjacent to an aperture (35);

25 a plurality of control circuits (39) arranged to receive the pattern data and supply corresponding control signals for control of the beamlet deflectors; and

an interconnect structure (400) according to any one of claims 1-24 connecting the control circuits to the first electrodes of the beamlet deflectors.

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27. The modulation device of claim 26, wherein at least a portion of the beamlet deflectors and at least a portion of the interconnect structure are formed as part of a single integrated circuit (50).

5 28. The modulation device of claim 27, wherein at least a portion of the control circuits (39) are also formed as part of the single integrated circuit (50).

29. The modulation device of any one of claims 26-28, wherein the modulation device (106) is divided into a plurality of beam areas (51) positioned in the normal path of the  
10 beamlets (123) and a plurality of non-beam areas (52) positioned outside the normal path of the beamlets, wherein the beamlet deflectors (30) are arranged in the beam areas and control circuits (39) are arranged in the non-beam areas.

30. The modulation device of any one of claims 26-29, wherein the control circuits (39)  
15 include a plurality of light sensitive elements (40) adapted to receive patterned light signals and convert the light signals to electrical signals to generate the control signals.

31. The modulation device of claim 30, wherein the control circuits include a plurality of demultiplexers (41), wherein the light signals received by the light sensitive elements are  
20 multiplexed signals which include pattern information for more than one beamlet deflector (30), and wherein the multiplexed signals are demultiplexed by the demultiplexers.

32. The modulation device of any one of claims 26-31, wherein a plurality of the conductive lines (42) extend parallel to each other in a corridor between two rows of the  
25 beamlet deflectors (30).

33. The modulation device of any one of claims 26-32, wherein the beamlet deflectors (30) are arranged in an addressable array, a first subset of the conductive lines (42) forming wordlines and a second subset of the conductive lines forming bitlines for addressing the  
30 beamlet deflectors.

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34. The modulation device of claim 33, wherein the wordlines and the bitlines are arranged at different connection levels (136) in the interconnect structure (400).

35. The modulation device of any one of claims 26-34, wherein a plurality of memory  
5 cells (95) are arranged in a close proximity with a plurality of respective beamlet deflectors (30) for temporarily storing a control signal, the temporarily stored signal being dedicated for the respective beamlet deflector for a predetermined period of time.

36. The modulation device of any one of claims 26-35, wherein the first and second  
10 electrodes (32, 34) are formed of a plurality of layers of conductive material (32a-d, 34a-d) connected with each other by one or more vias (36).

37. The modulation device of any one of claims 26-36, wherein the first electrodes (32)  
15 are supported by one or more conductive supports (403) or vias (36) to a surface of the substrate, the conductive supports or vias supported by one or more of the first regions of the substrate.

38. The modulation device of any one of claims 26-37, wherein the first electrodes form a  
20 free-hanging structure supported by one or more conductive supports (403) or vias (36).

39. The modulation device of any one of claims 26-38, wherein the distance of two of the adjacent beamlet deflectors (30) is less than 55  $\mu\text{m}$ .

40. An integrated circuit comprising the interconnect structure according to any one of  
25 claims 1-24.

41. The integrated circuit of claim 40, wherein the interconnect structure forms part of one of a group comprising: an embedded memory circuit, an on-chip bus, a logic circuit, and a processor.

30

42. A charged particle lithography system (100) comprising:

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a beam generator (101, 102, 103, 105) arranged for generating a plurality of charged particle beamlets (123);

a modulation device according to any one of claims 27-40 adapted to modulate the beamlets; and

5 a projection system (110) arranged for projecting the modulated beamlets onto a target (130) to be exposed.

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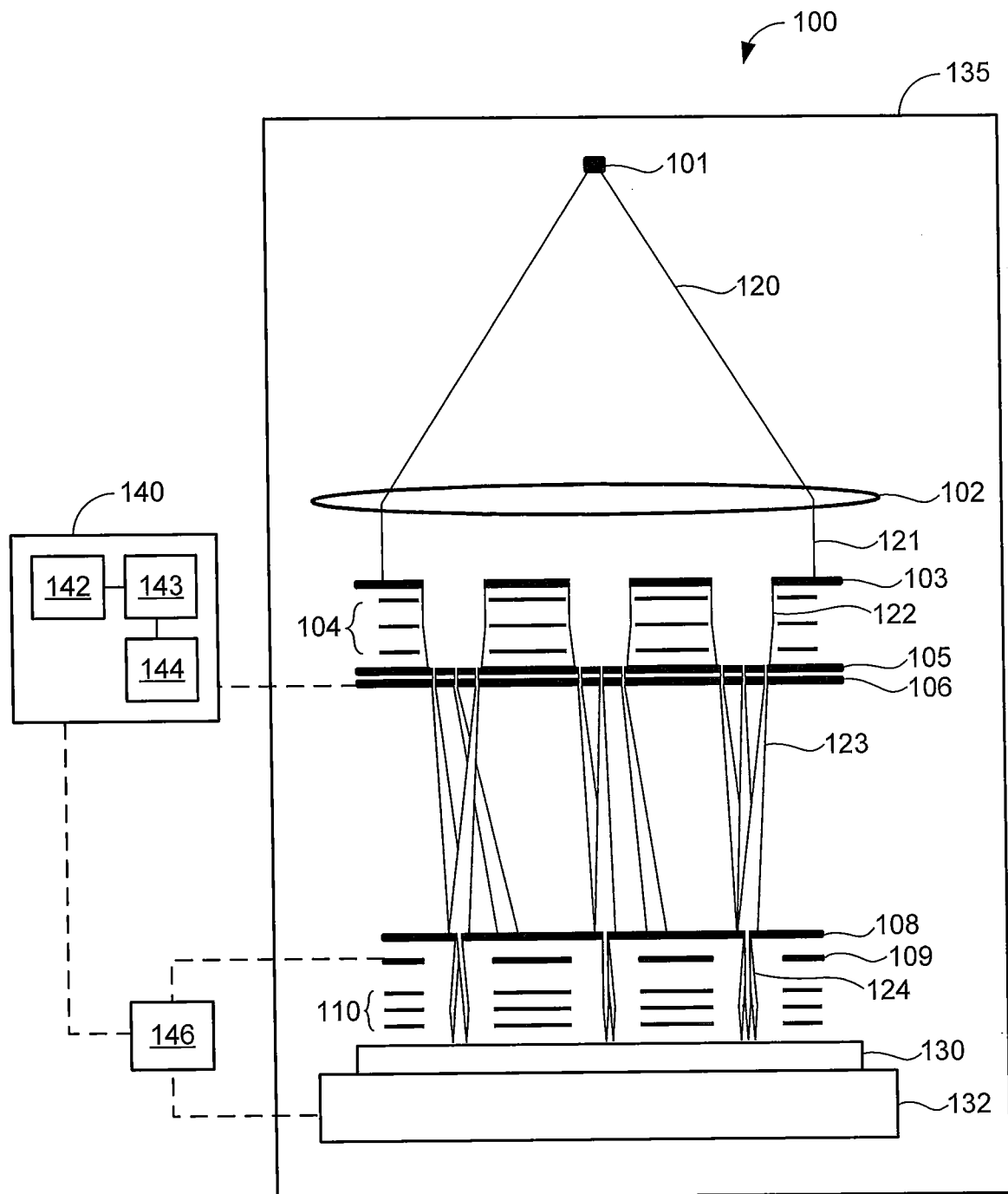


FIG. 1

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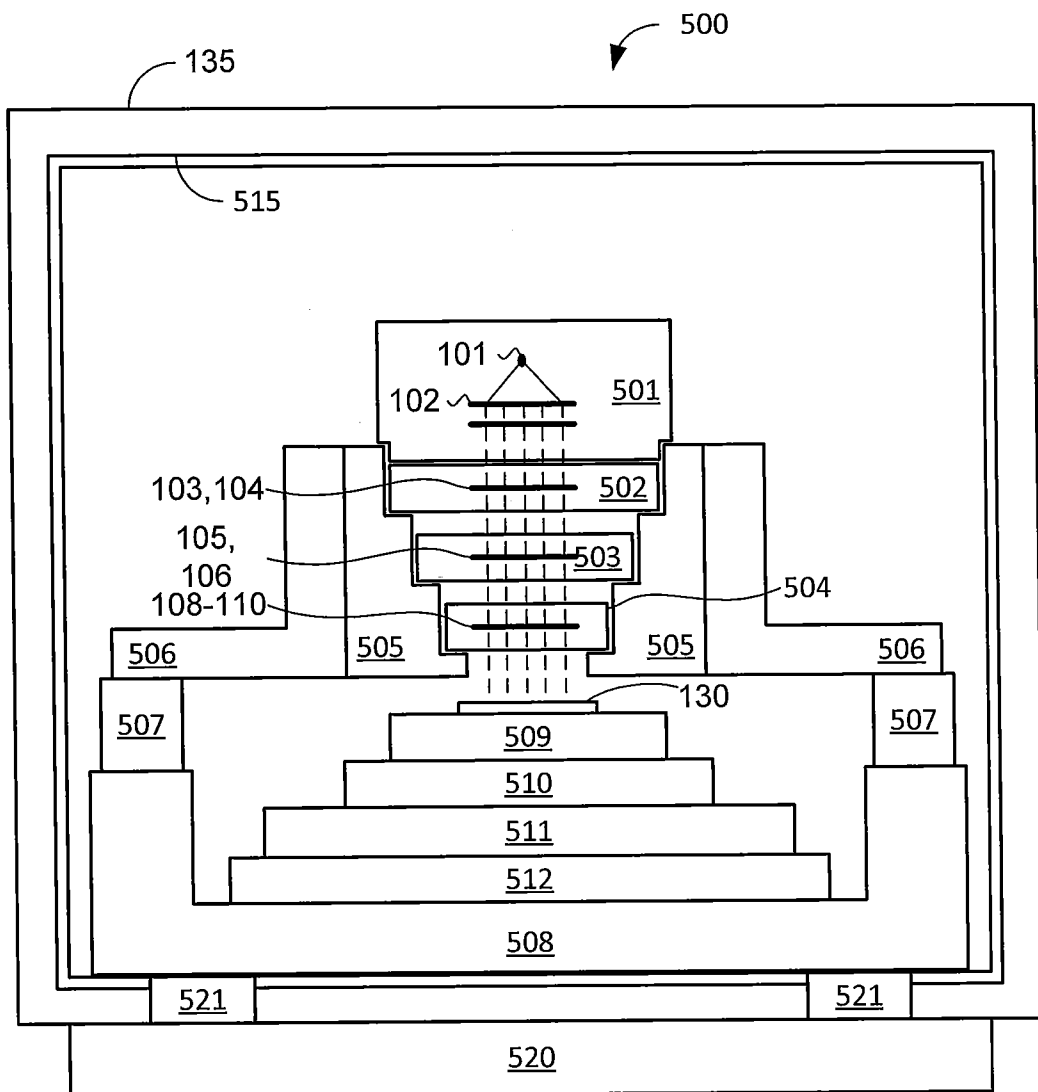


FIG. 2

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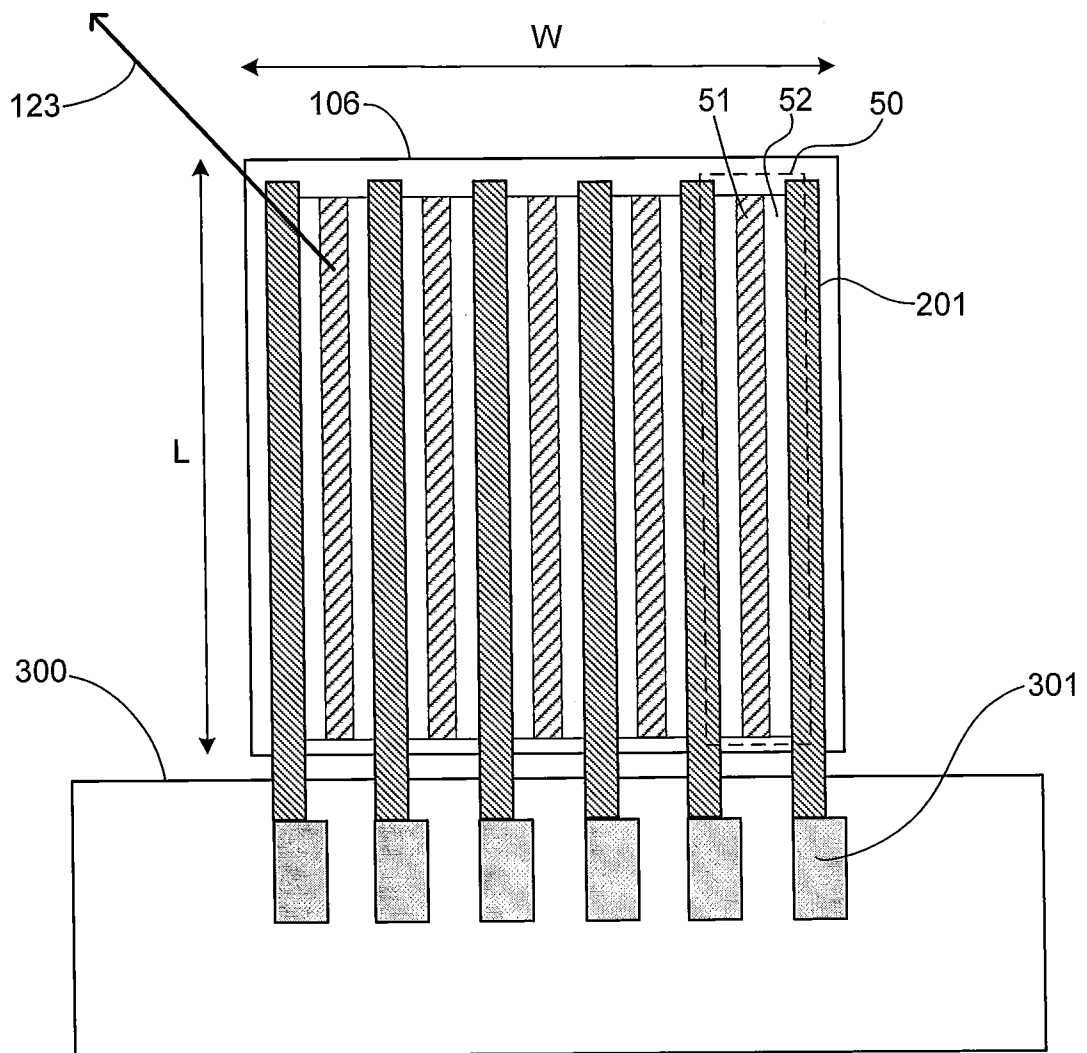


FIG. 3

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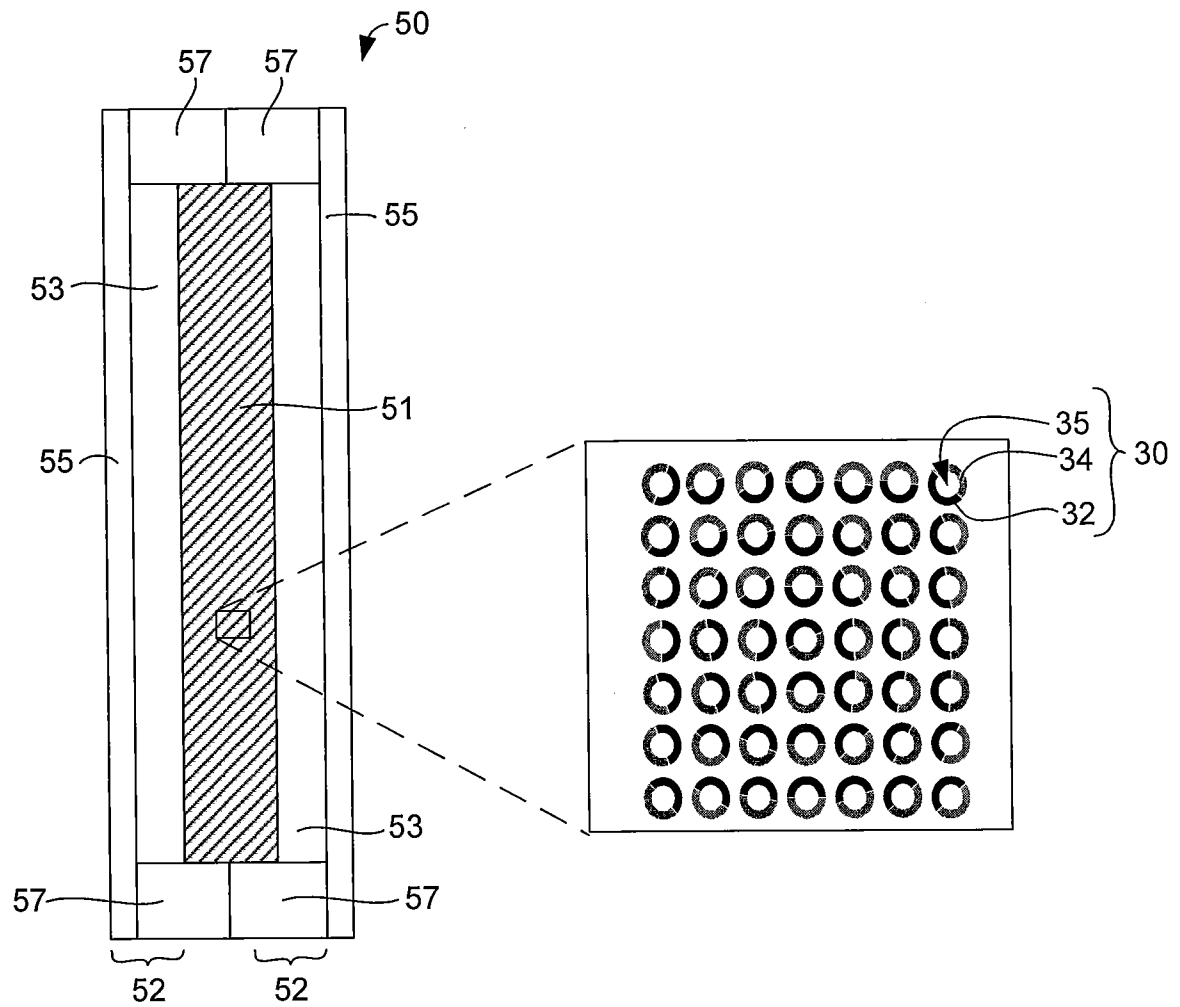


FIG. 4

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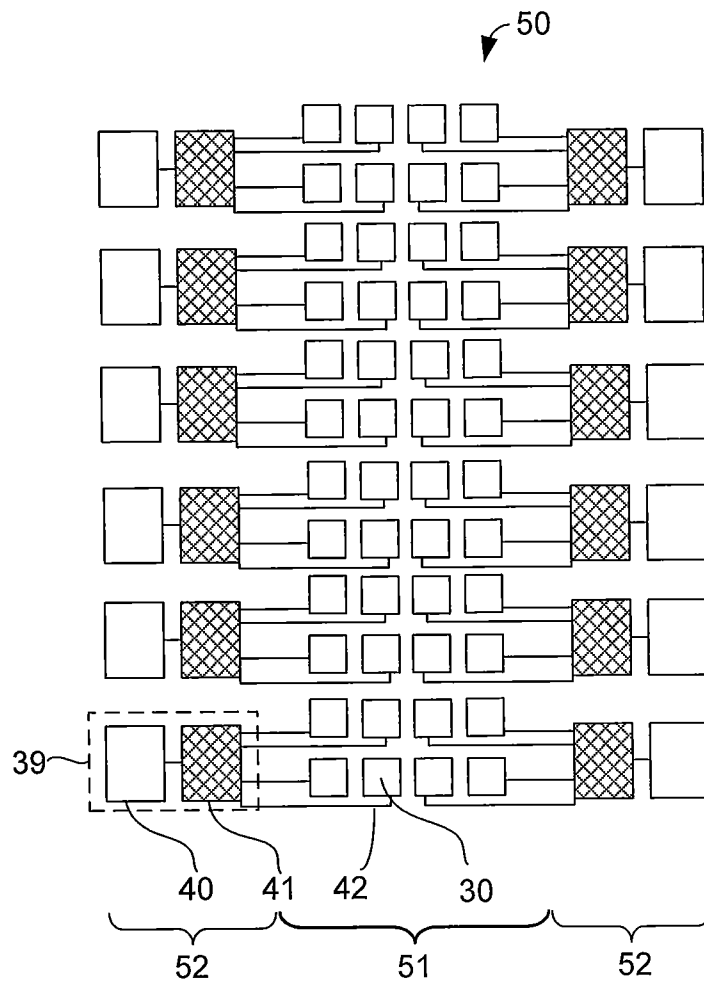
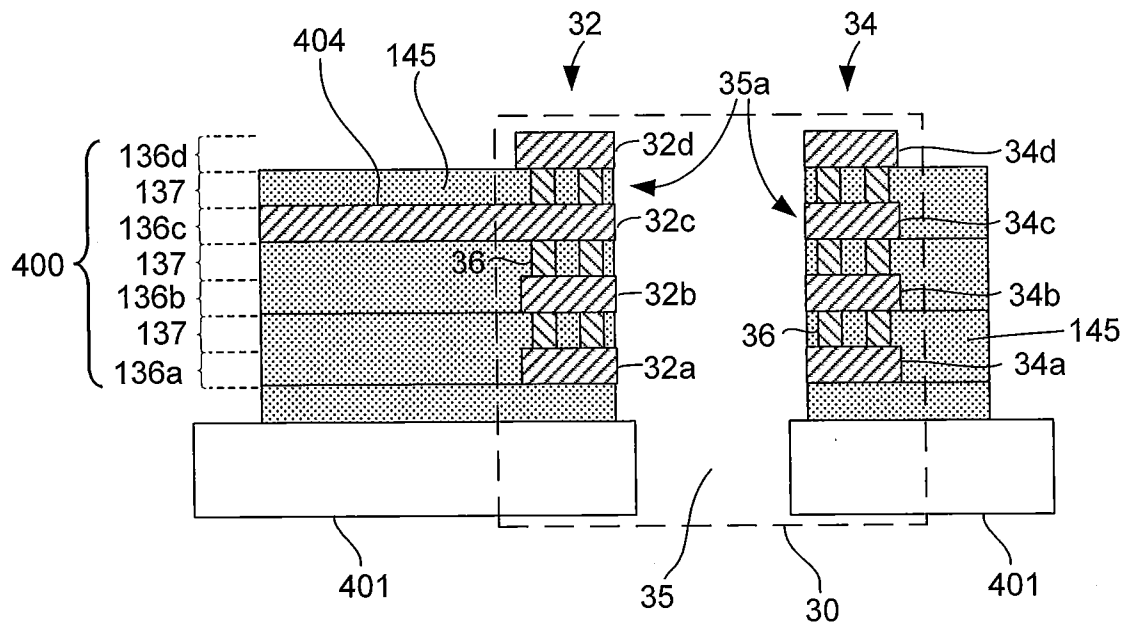
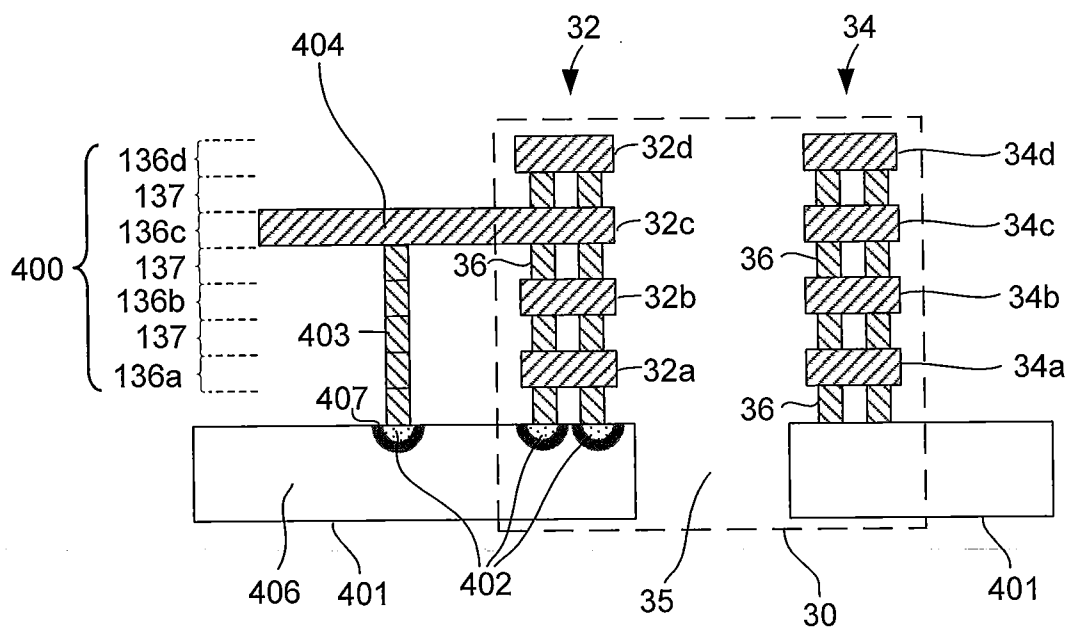


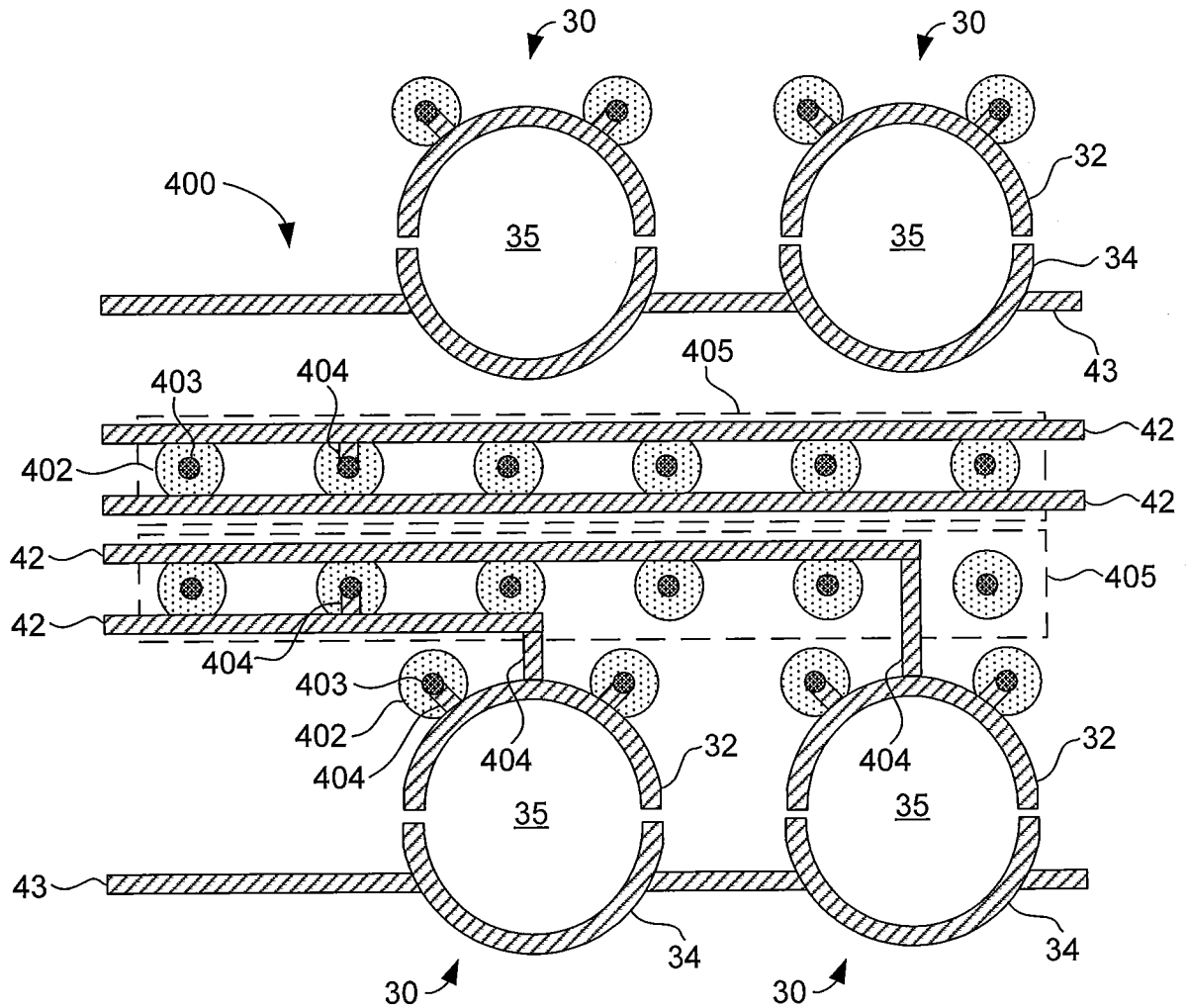
FIG. 5



**FIG. 6**

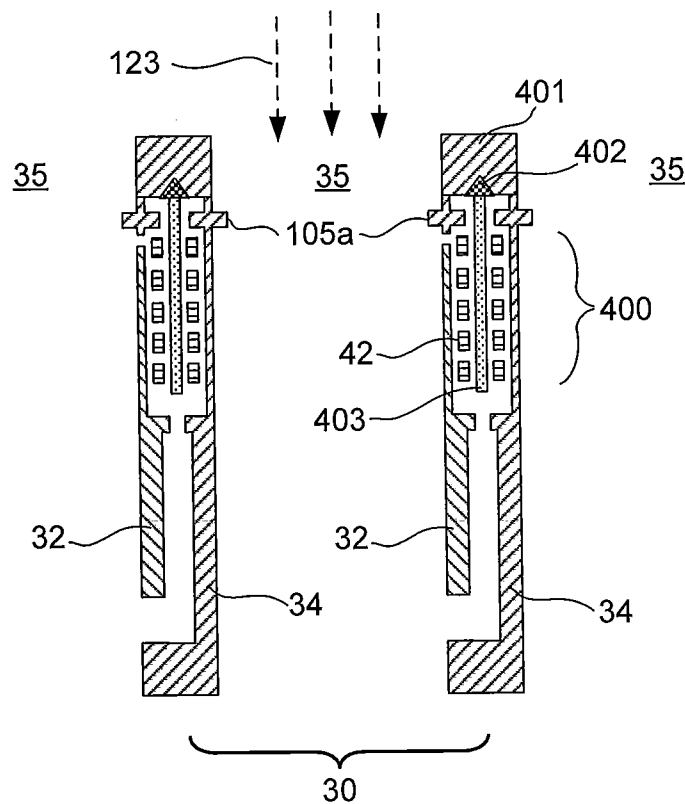
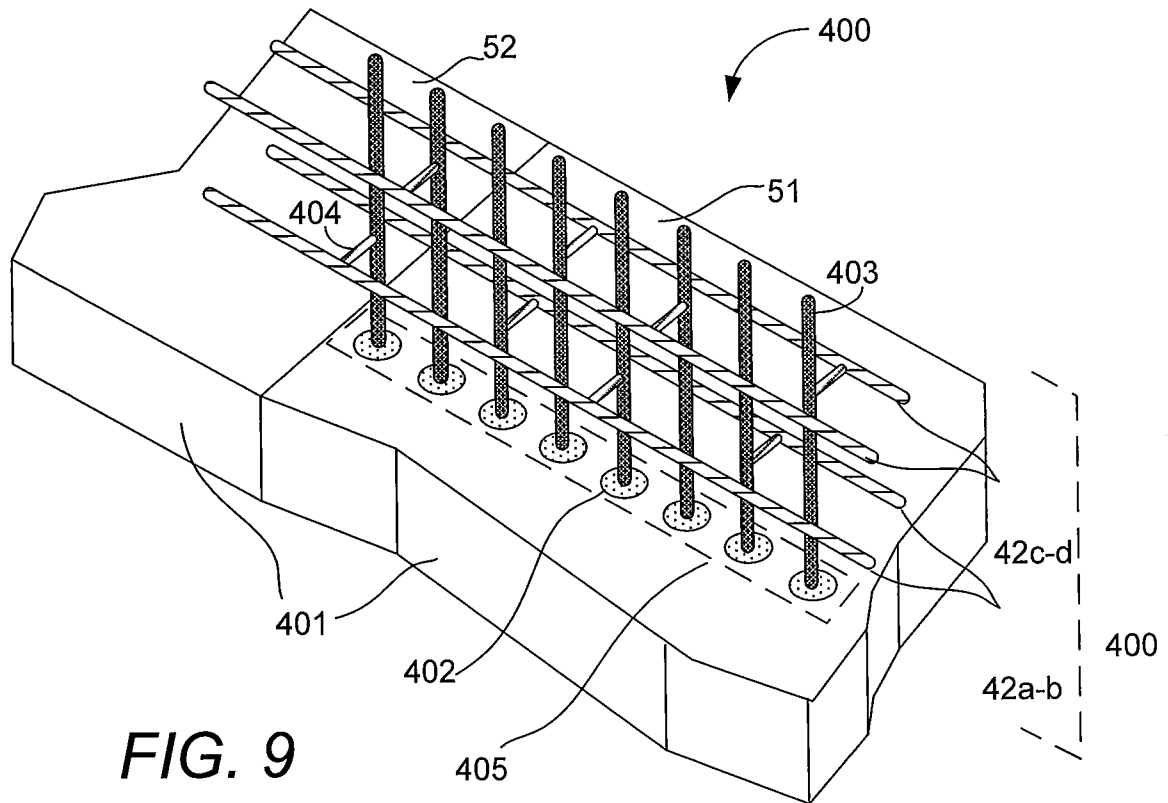


**FIG. 7**

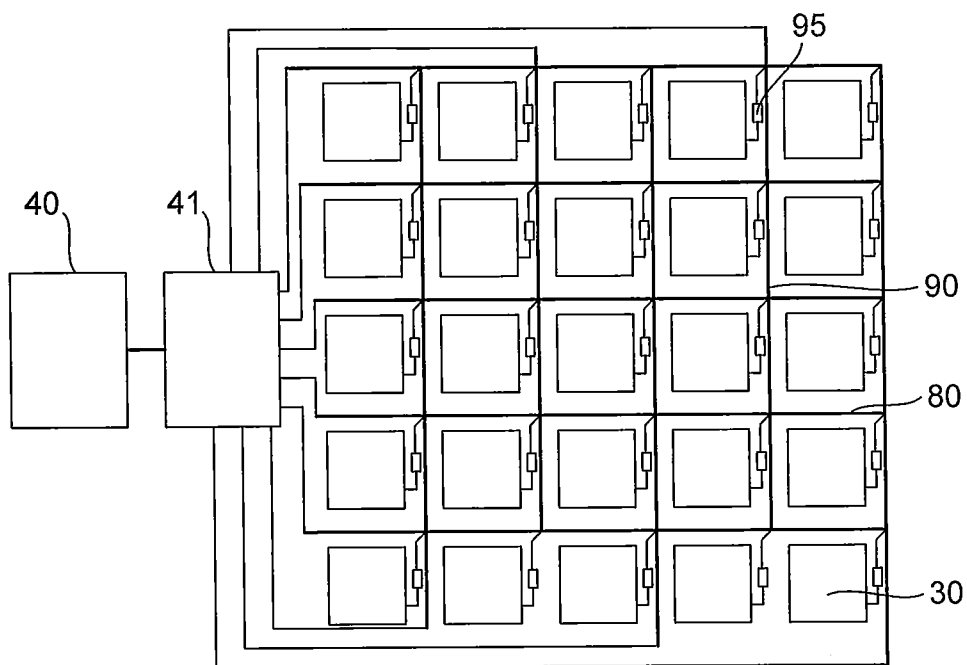


**FIG. 8**

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*FIG. 11*

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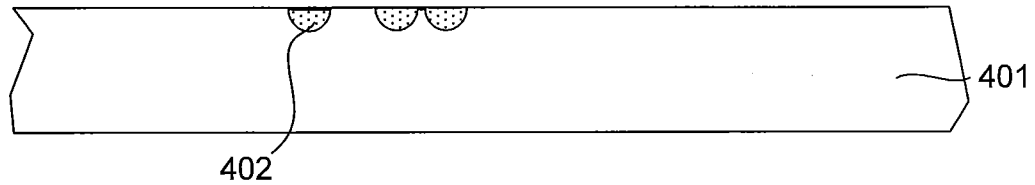


FIG. 12A

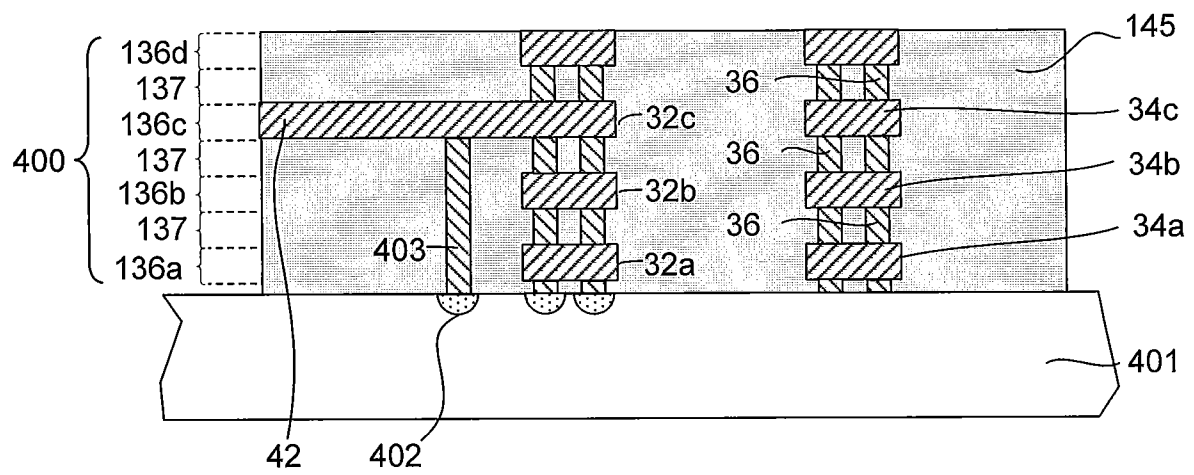


FIG. 12B

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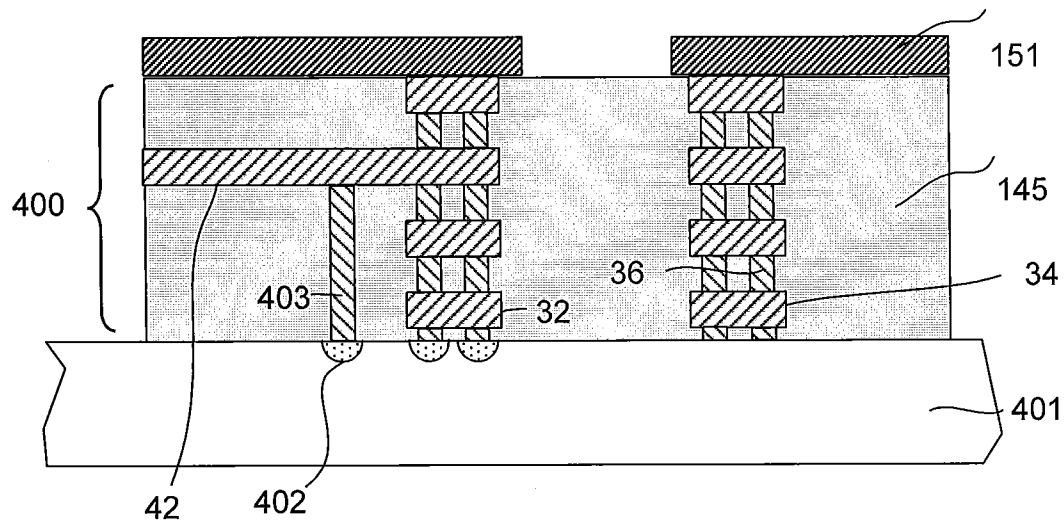


FIG. 12C

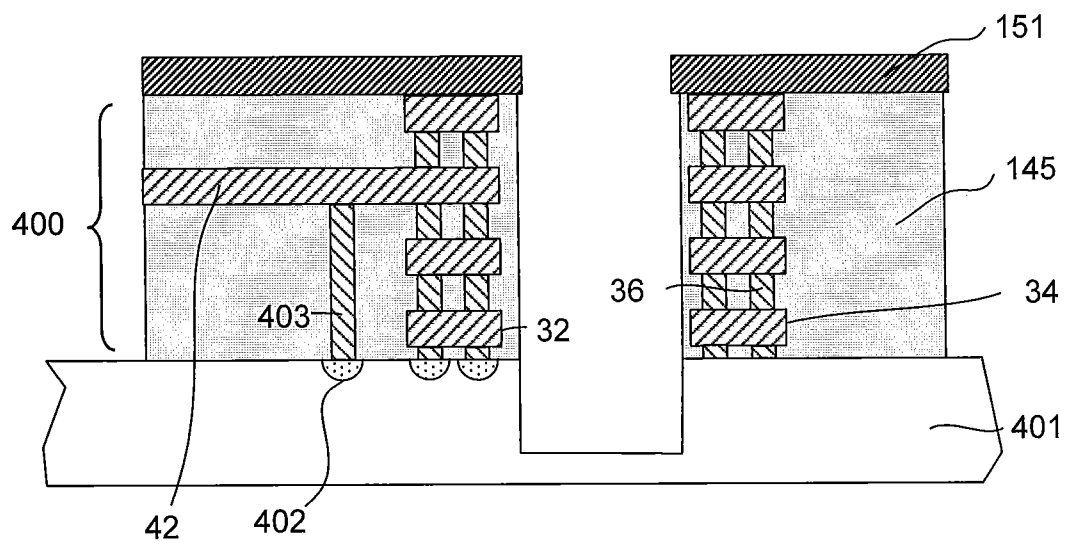


FIG. 12D

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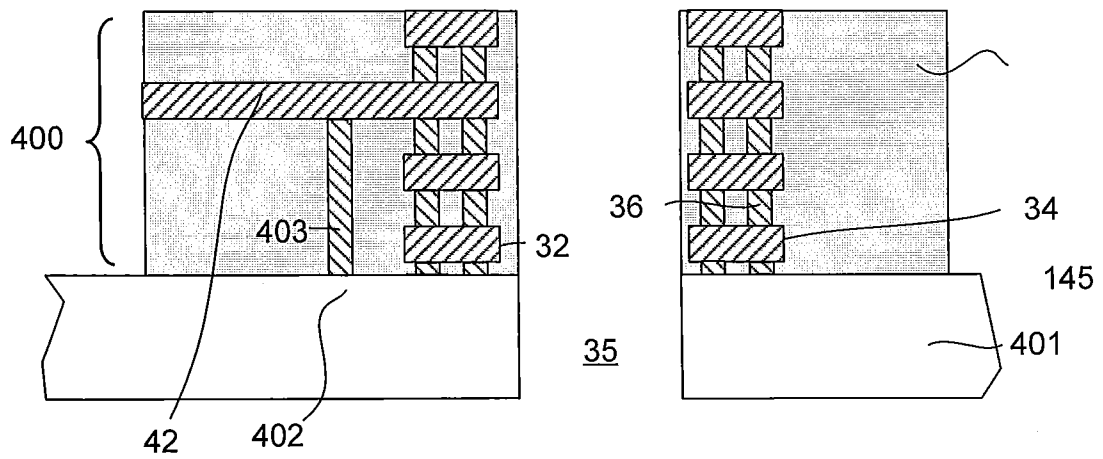


FIG. 12E

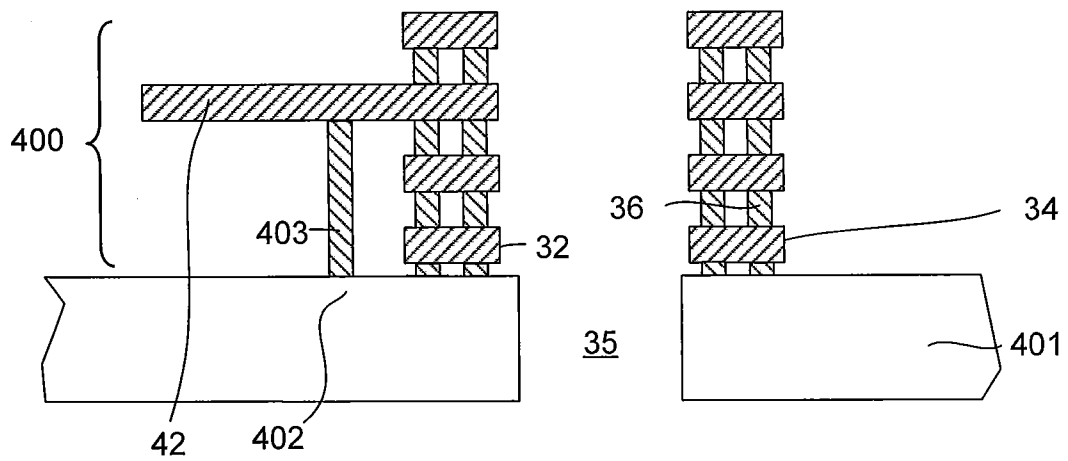


FIG. 12F

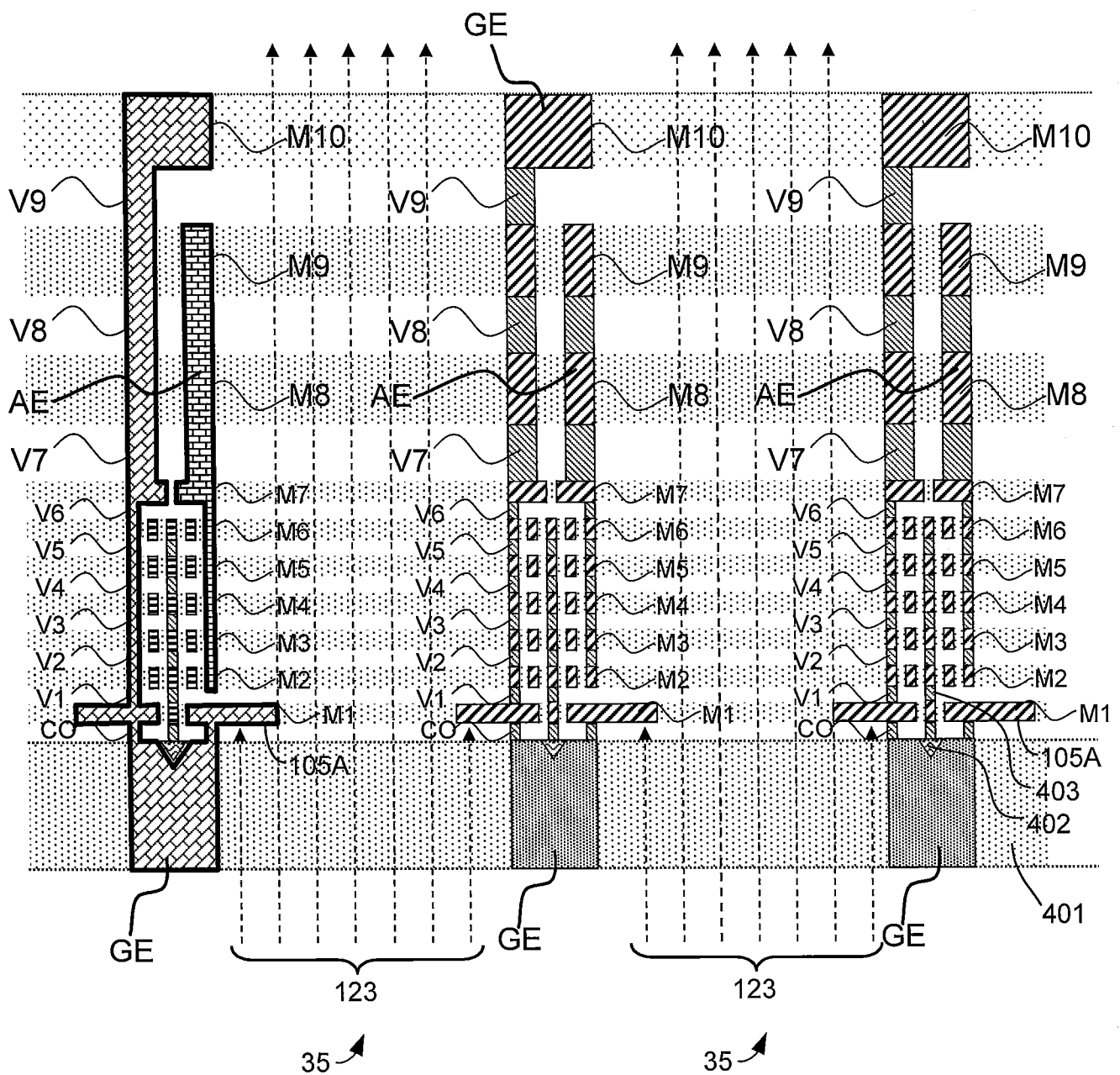


FIG. 13

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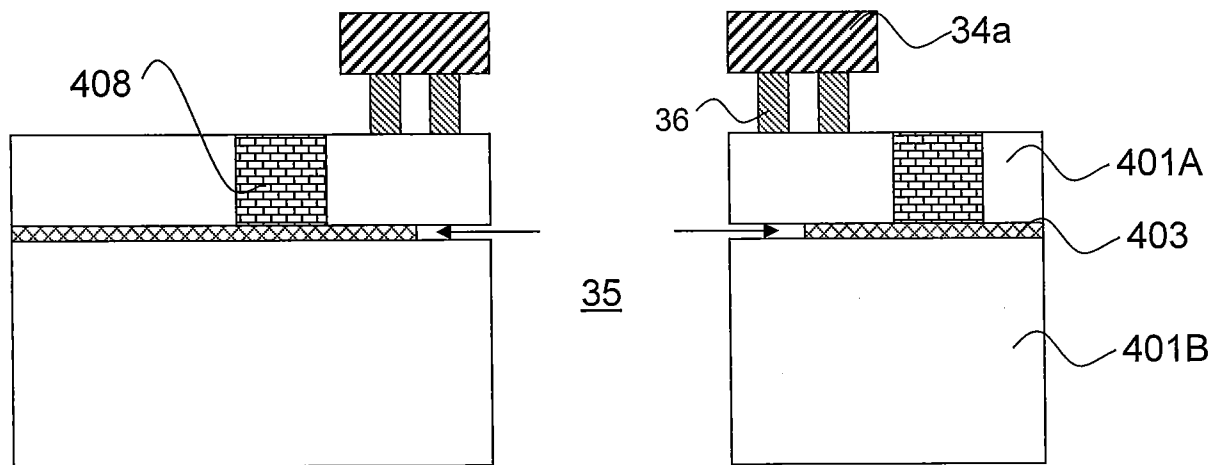


FIG. 14

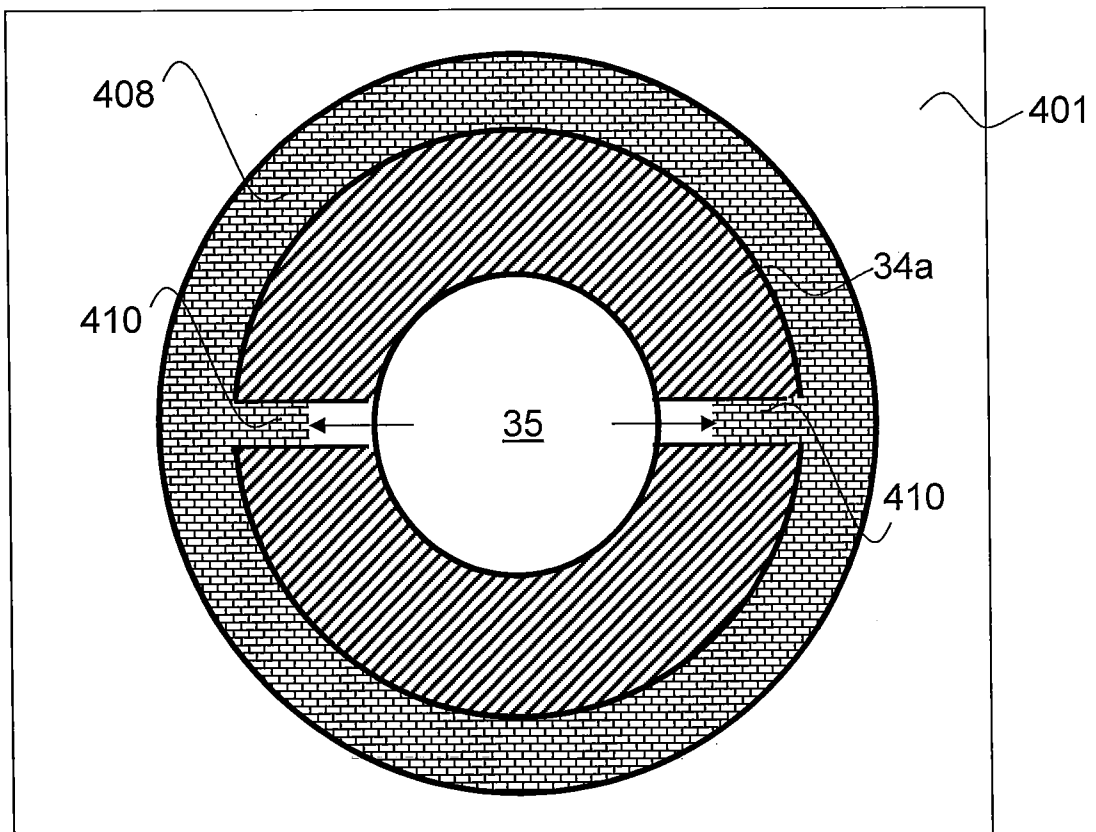


FIG. 15

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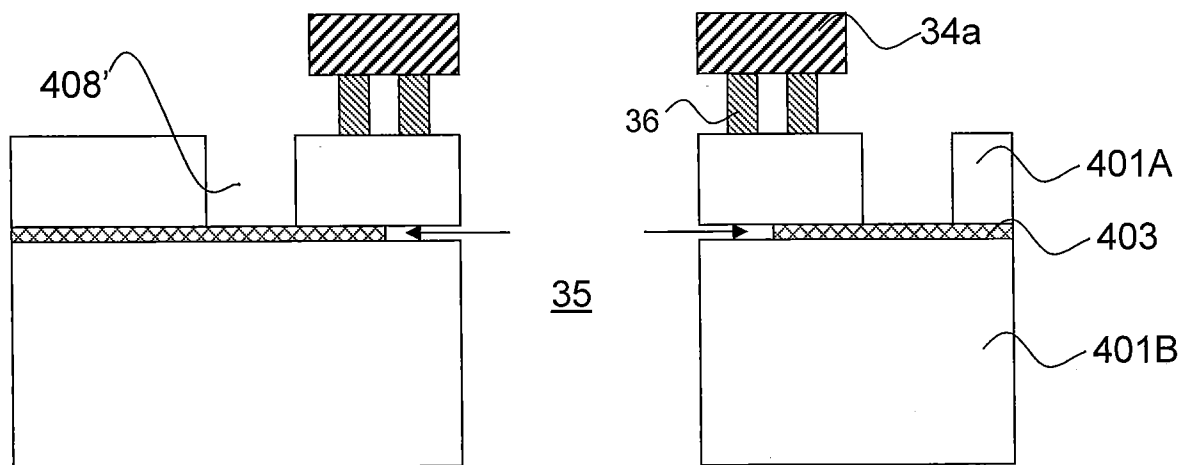


FIG. 16

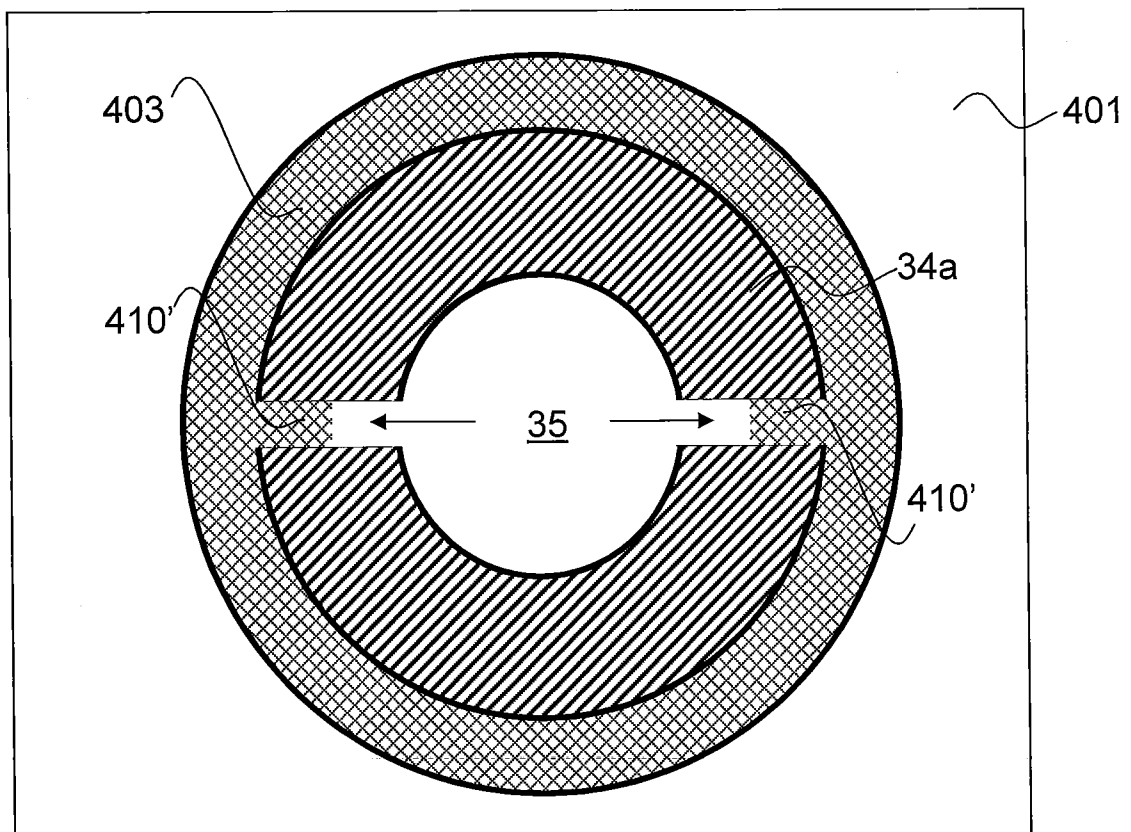


FIG. 17

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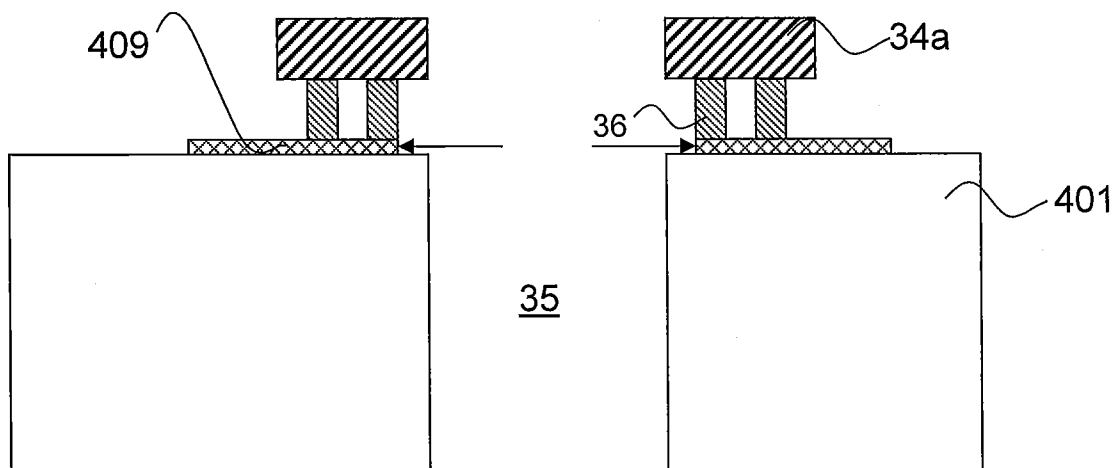


FIG. 18

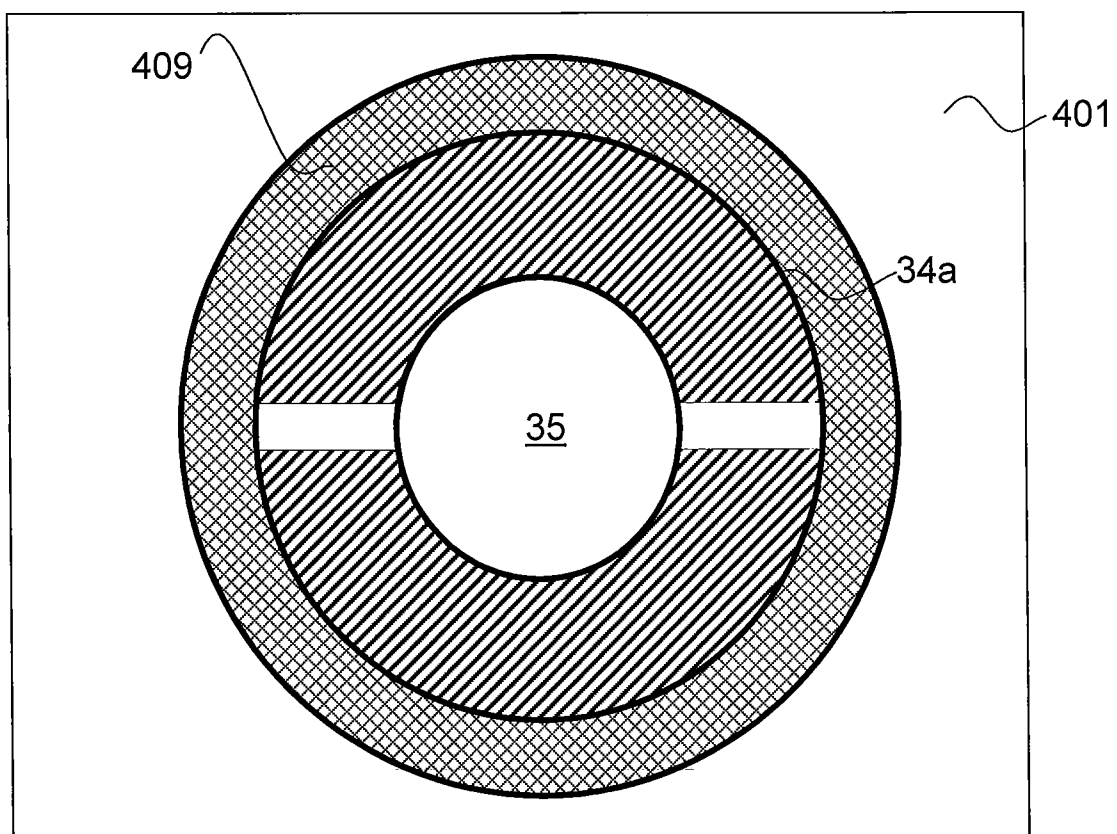


FIG. 19

# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/EP2013/077068

## Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-7, 12-20, 22, 40, 41

### Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

## INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/077068

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/768 H01J37/04 H01J37/317  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H05K H01J H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, COMPENDEX, INSPEC, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 899 439 A (POTTER CURTIS N [US] ET AL) 13 February 1990 (1990-02-13)	1-6, 12-20, 22,40,41
Y	column 1, lines 6-28 column 2, line 39 - column 6, line 7; figures 1-13	7
Y	----- US 2009/152673 A1 (KWON O-KYUN [KR] ET AL) 18 June 2009 (2009-06-18) abstract; figures paragraphs [0036] - [0042]	7
X	----- US 4 920 639 A (YEE IAN Y K [US]) 1 May 1990 (1990-05-01) abstract; figures column 1, lines 6-40 column 2, line 54 - column 5, line 7 ----- -/-	1-6, 12-20,22



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

11 March 2014

Date of mailing of the international search report

28/05/2014

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
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Fax: (+31-70) 340-3016

Authorized officer

Schmidt-Kärst, S

## INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/077068

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 277 703 B1 (BARLOCCHI GABRIELE [IT] ET AL) 21 August 2001 (2001-08-21) the whole document -----	7

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2013/077068

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4899439	A	13-02-1990	NONE
-----			
US 2009152673	A1	18-06-2009	KR 20090064929 A 22-06-2009
			US 2009152673 A1 18-06-2009
			US 2010301448 A1 02-12-2010
-----			
US 4920639	A	01-05-1990	NONE
-----			
US 6277703	B1	21-08-2001	EP 0957515 A1 17-11-1999
			JP 2000031440 A 28-01-2000
			US 6277703 B1 21-08-2001
-----			

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7, 12-20, 22, 40, 41

Interconnect structure comprising a plurality of conductive supports extending from a surface of a substrate at a plurality of first portions and a plurality of conductive lines supported by the conductive supports, at least a portion of each conductive line extending between two of the conductive supports being supported only by the conductive supports at each end of the conductive line portion, wherein the first regions are isolated from a remaining part of the substrate by insulating barrier regions.

---

2. claims: 8-11, 23-25

Interconnect structure comprising a plurality of conductive supports extending from a surface of a substrate at a plurality of first portions and a plurality of conductive lines supported by the conductive supports, at least a portion of each conductive line extending between two of the conductive supports being supported only by the conductive supports at each end of the conductive line portion, wherein the substrate comprises at least one second region of a different conductivity type than the first regions for forming a pn-junction between said regions.

---

3. claim: 21

Interconnect structure comprising a plurality of conductive supports extending from a surface of a substrate and a plurality of conductive lines supported by the conductive supports, at least a portion of each conductive line extending between two of the conductive supports being supported only by the conductive supports at each end of the conductive line portion, wherein the conductive lines are electrically connected to the conductive supports via a plurality of connection bridges extending substantially perpendicular to the conductive supports and mechanically supporting the connecting lines.

---

4. claims: 26-39, 42

Modulation device arranged for modulating the charged particle beamlets in accordance with pattern data and charged particle lithography system with such a modulation device, wherein the device comprises a plate-like substrate, an array of beamlet deflectors with a first electrode and a second electrode adjacent to an aperture, a plurality of control circuits for control of the beamlet deflectors, wherein the control circuits are connected to the first

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

electrodes of the beamlet deflectors by an interconnect structure with a plurality of conductive supports extending from a surface of a substrate and a plurality of conductive lines supported by the conductive supports.

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