April 7, 1970 Z. TARCZY-HORNOCH ET AL 3,505,594

INTERPOLATING TIME INTERVAL COUNTER WITH COURSE COUNT AMBIGUITY ELIMINATING MEANS

Original Filed June 25, 1964 3 Sheets-Sheet 1

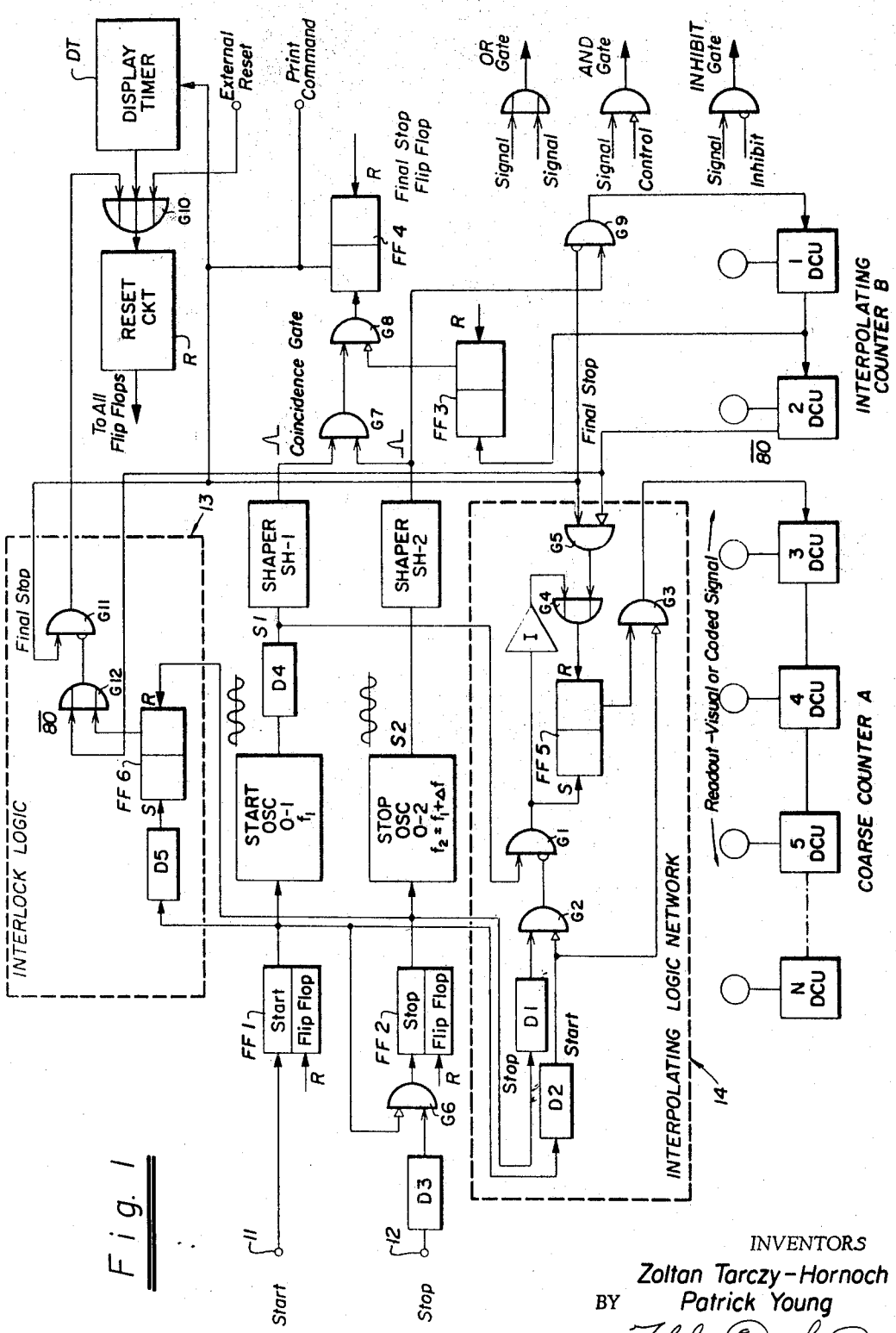


Fig. 1

INVENTORS
Zoltan Tarczy-Hornoch
Patrick Young
BY Flehr and Swain
Attorneys

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Original Filed June 25, 1964 3 Sheets-Sheet 2

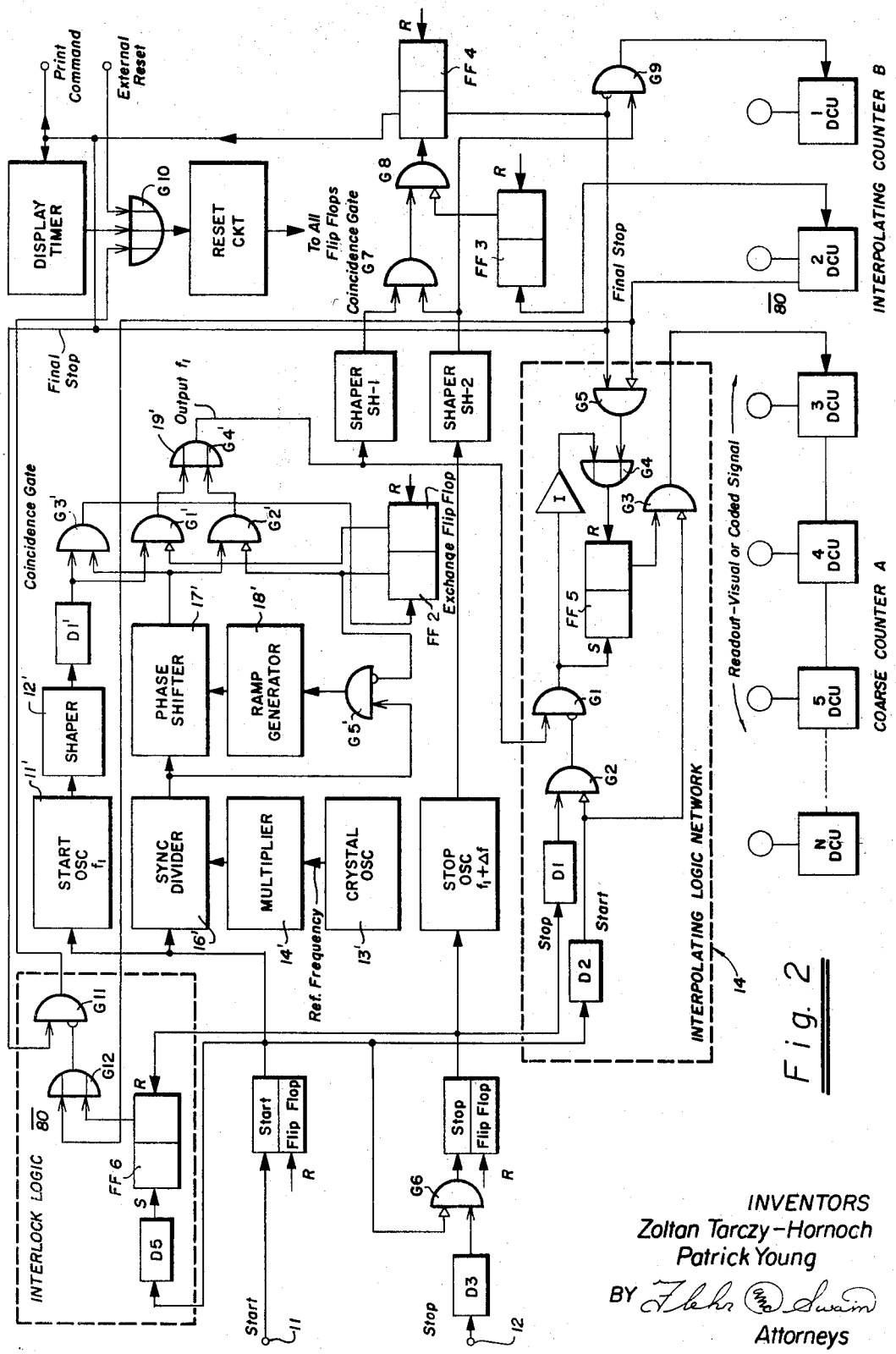


Fig. 2

INVENTORS
Zoltan Tarczy-Hornoch
Patrick Young
BY Flehr & Swain
Attorneys

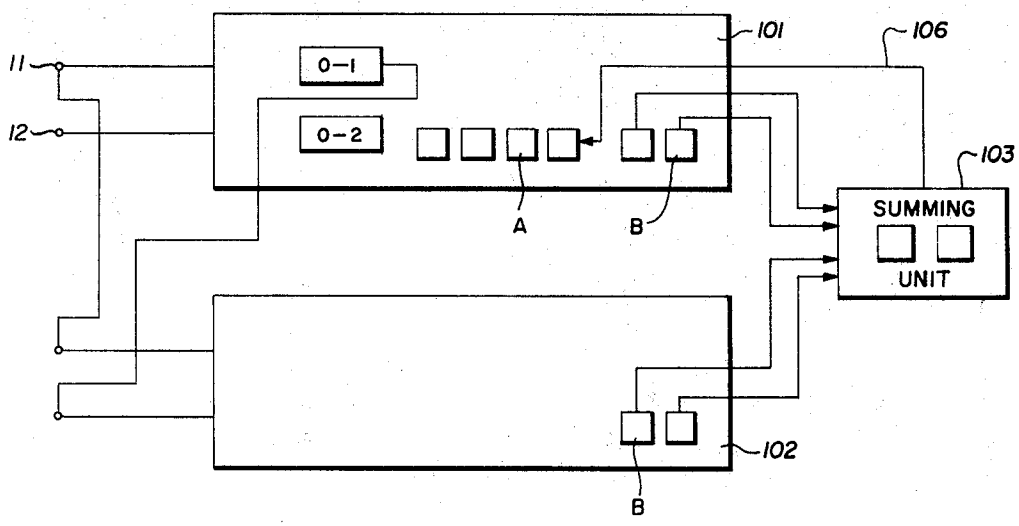


Fig. 3

INVENTORS
Zoltan Tarczy-Hornoch
BY Patrick Young
Flehr & Swain
Attorneys

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INTERPOLATING TIME INTERVAL COUNTER WITH COURSE COUNT AMBIGUITY ELIMINATING MEANS

Zoltan Tarczy-Hornoch and Patrick Young, Berkeley, Calif., assignors to W. K. Rosenberry, doing business as Zeta Research, Lafayette, Calif.

Continuation of application Ser. No. 377,972, June 25, 1964. This application Feb. 9, 1968, Ser. No. 704,947
Int. Cl. G04f 11/08
U.S. Cl. 324—68 11 Claims

ABSTRACT OF THE DISCLOSURE

High resolution interpolating time interval counter utilizing vernier interpolating techniques based upon frequency difference between clock generators, having coarse count ambiguity eliminating means, stop before start command preventing means and means for preventing the recognition of an early phase coincidence between the clock generators.

This application is a continuation of application Ser. No. 377,972, filed June 25, 1964.

This invention relates to an interpolating time interval counter and method and more particularly to a high speed interpolating time interval counter utilizing low speed circuitry.

In making time interval measurements, the elapsed time between initiation and termination of an event is the measurement of interest. In most conventional time interval counters, the output of a high frequency oscillator is gated on at the beginning of the event and off at the end of the event. During the gate on period, each output cycle of the oscillator is totalized in a counting chain. With such time interval counters, the higher the oscillator frequency used, the better the resolution obtained in the measurement. By way of example, the design of a one nanosecond time interval counter by conventional techniques would require a one gigacycle (10^3 mc.) clock generator, a high speed gate, and a one gigacycle counting unit. In the light of the present day technology, it is possible to make such an instrument but its cost would be excessive. Furthermore, readings from such an instrument would be accurate to only ± 1 count or ± 1 nanosecond due to the arbitrary relation between the end points the time interval and the phase of the reference frequency. To overcome these difficulties, attempts have been made to devise interpolating time interval counters such as disclosed on pages 508–514 in paragraph 16–10 of "Pulse and Digital Circuits" by Millman and Taub, published by McGraw-Hill Book Company, Inc. in 1956. Such counters make it possible to use low speed circuitry to provide high resolution. However, such counters have the limitation of only being able to count a time interval when the start of the time interval is synchronized to the interval reference oscillator. In addition such counters have the disadvantage that the coarse and vernier counts must be arithmetically manipulated to obtain the correct reading. Also the vernier count can be in error by one count. With such counters the vernier method can be used in an externally synchronized (unsynchronized to the reference oscillator) system but the difficulties of arithmetic manipulation and one count error still exist. There is therefore a need for a new and improved interpolating time interval counter and method.

In general, it is an object of the present invention to provide an improved interpolating time interval counter and method which can be utilized for making very short or long time interval measurements with high accuracy and resolution.

Another object of the invention is to provide an interpolating time interval counter and method of the above character which can measure time intervals with arbitrary starting times.

Another object of the invention is to provide an interpolating time interval counter of the above character which eliminates the possible one count error from both the coarse and vernier counts.

Another object of the invention is to provide an interpolating time interval counter and method of the above character which does not require arithmetic manipulation of the coarse and vernier counts.

Another object of the invention is to provide an interpolating time interval counter and method of the above character which is relatively simple, highly reliable, low in cost and in which low speed techniques and circuitry can be utilized.

Another object of the invention is to provide an interpolating time interval counter and method of the above character in which phase locked and non-phase locked reference oscillators can be used.

Additional objects and features of the invention will appear from the following description in which the preferred embodiments are set forth in conjunction with the accompanying drawings.

Referring to the drawings:

FIGURE 1 is a block diagram of an interpolating time interval counter incorporating the present invention and utilizing a phase locked reference oscillator.

FIGURE 2 is a block diagram similar to FIGURE 1 but in addition incorporating a high stability phase locked oscillator.

FIGURE 3 is a block diagram of another embodiment of an interpolating time interval counter incorporating the present invention and utilizing a non-phase locked reference oscillator.

The problems encountered in making interpolating or vernier type time interval counters is discussed in the reference pointed out above and in copending application Ser. No. 377,971, filed June 25, 1964 now Patent No. 3,444,462.

Let it be assumed that it is desired to measure a total time interval of

$$T=N_1\tau_1+N_2\tau_2 \tag{1}$$

where

T is the total time interval or quantity to be measured
τ_1 is a coarse quantum or time unit
τ_2 is a vernier quantum or time unit and equals $\tau_1\alpha^{-k}$
N_1 is a positive integer
N_2 is a positive integer
α is a positive integer and preferably equal to 10
k is a positive integer

The first step in measuring the total time interval is to measure $N_1\tau_1$ by determining

$$N_1\tau_1<T<(N_1+1)\tau_1 \tag{2}$$

This can be accomplished by counting the clock frequency f_1 for a duration of T where

$$f_1=1/\tau_1 \tag{3}$$

Let it be assumed that this clock frequeny f_1 is counted by a suitable main or coarse counter A which will accumulate N_1 counts. The counter A can be arranged in a suitable manner such as in a decimal scale, but, if desired, can be counted in any scale identified as the scale of α. Let it be assumed that the interpolation time interval counter is constructed in such a manner that the zero phase of the clock signal $S_1=E_1e^{j2\pi f_1 t}$ from a first clock generator which produces the clock frequency f_1 will always be in synchronism with the start time τ_t starting the

time interval T to be measured. One such generator is described in copending application Ser. No. 377,825, filed June 25, 1965, now Patent No. 3,319,181. As stated therein, the first clock generator can be identified as being "phase locked." Let it also be assumed that the counter A advances at or around the time of the zero phase of the clock signal S_1 and that the initial zero phase at the start of the time interval T is not counted.

The next step in determining the time interval T is to determine N_2. One possible way is to generate a second clock signal $S_2=E_2e^{j2\pi f_2 t}$ from a second clock generator which produces the clock frequency f_2 which is phase locked to a stop signal that indicates the end of the time interval T to be measured.

If it is assumed that

$$f_2=f_1+\Delta f=\frac{1}{\tau_1-\tau_2} \quad (4)$$

Then the initial phase difference of $N_2\tau_2$ between S_1 and S_2 will be reduced to $N_2-1)\tau_2$ after one $\tau_1-\tau_2$ period, etc. until after $N_2(\tau_1-\tau)$ periods, the phase difference will become zero, and the zero phase points of S_1 and S_2 will be in coincidence. An interpolating or vernier counter B, which preferably uses the decimal scale but can use scale such as the scale of α, is enabled to count the second clock frequency f_2 from the time of termination τ_p of the time interval T until the time of coincidence τ_c. The counter B will accumulate N_2 counts assuming again that the first zero phase (at τ_p) is not counted and the last one (at τ_c) is counted.

From the foregoing it can be seen that the digital measurement for the time interval $T=N_1\tau_1+N_2\tau_2$ is accomplished with a resolution of τ_2 by using counting circuitry with essentially α^k times slower resolution. The numerical readout provided by the counters A and B gives an appropriate display of the integers N_1 and N_2 and requires no additional information and no other arithmetic operation.

An interpolation time interval counter constructed as set forth above will give a correct reading for all situations except for the situation where the time interval T closely equals $N_1\tau_1$ or, in other words, when the end of the time interval T is very close to the zero phase of the clock signal S_1. Since the main counter A does not necessarily advance at zero phase, and certainly not with τ_2 or better resolution, it is possible for the counter to count N_1-1 or N_1+1 depending upon whether the time interval T is just over or just under $N_1\tau_1$ respectively, or in other words, the zero phase of the signal S_1 is just after or just before the end of the time interval T. Thus, it is not possible to tell instantaneously whether the counter A did or did not count the last count which might be needed or surplus at the time that the counter A was gated off, and therefore, a ± 1 main count ambiguity is presented.

The range of critical stop time in which ambiguity can occur, as pointed out above, can be minimized by designing circuits having better resolution and faster rise times but, no matter how much the circuit is improved, the ambiguity cannot be eliminated.

The interpolating time interval counter incorporating the present invention and shown on a typical block diagram in FIGURE 1 includes an interpolating logic **14** which resolves the above mentioned ambiguity and which is described in copending application Ser. No. 377,971, filed June 25, 1964. The interpolating time interval counter also may include an interlock logic **13** which is described in copending application Ser. No. 377,975, filed June 25, 1964, now Patent No. 3,392,330 and a high stability phase locked oscillator described in copending application Ser. No. 377,825, filed June 25, 1964. The interpolating time interval counter incorporating the present invention also incorporates a number of additional novel features which form an integral part thereof, and which are hereinafter described.

The interpolating time interval counter as shown in FIGURE 1 for generating signals S_1 and S_2 utilizes a reference or a start oscillator O–**1** and stop oscillator O–**2** which are of the phase locked type. Oscillators of this type are well known and for example can be constructed as shown in figures 4.45 and 4.46 on pages 140–148 of vol. XIX, MIT Series, entitled "Waveforms" published by McGraw-Hill Book Company in 1949. A great number of additional components are included as a part of the interpolating time interval counter and are shown in block form because they are conventional. The function of these components will appear from the following description of the mode of operation of the interpolating time interval counter shown in FIGURE 1.

In order to facilitate the explanation of the operation of the time interval counter shown in FIGURE 1 in practicing the present method let it be assumed that the clock signal S_1 from the start oscillator O–**1** has a frequency f_1 of 10 mc. and that the clock signal S_2 from the stop oscillater O–**2** is offset from the frequency f_1 by Δf and has an output frequency f_2 near to 10.1 mc. or to be exact $^{1000}/_{99}$ mc.

A measurement cycle is begun when a start command at τ_t is supplied to the start terminal **11** which triggers start flip-flop **FF1**. The start flip-flop **FF1** produces a step output which supplies the start signal to the start oscillator O–**1**. The start oscillator O–**1** is phase locked to the start signal and starts its output signal with a period of $\tau_1=100$ ns. in a fixed phase relationship with the start signal.

The start flip-flop **FF1** also performs the function of supplying a step signal to the interlock logic **13** to the delay line **D5**. The interlock logic is described in copending application Ser. No. 377,975, filed June 25, 1964 and is utilized for determining whether or not the interpolating time interval counter has counted a positive time (stop after start) when the start and stop signals come very close to each other.

In addition, the start flip-flop **FF1** supplies a gating signal through the delay **D2** to the interpolating logic **14** which is utilized to eliminate the above mentioned counting ambiguity and which is described in detail copending application Ser. No. 377,971, filed June 25, 1964.

Output S_1 of oscillator O–**1** through D_4 is also supplied to gate G_1 of the interpolating logic **14**. The operation of this logic is such that after a temporary storage it supplies output pulses from gate **G3** at rate f_1 to the main counter A, until stopped. Counter A therefore accumulates N_1 counts with at most one count error, thereby measuring coarse time interval $N_1\tau_1$.

The stop signal at τ_p is received from terminal **12** through the delay **D3** to one input of the gate **G6** and to stop flip-flop **FF2** since the start signal has already enabled gate **G6**. The stop flip-flop **FF2** generates a step function which is supplied to the flip-flop **FF6** of the interlock logic **13**, and to the **D1** delay of interpolating logic **14**.

The stop signal from the stop binary is also supplied to the stop oscillator O–**2** which is also of the phase locked type and produces signal S_2 which is in a fixed relationship with the stop signal. In this example, S_2 has a frequency of 10.10101 mc. therefore its period is 99 ns. (nanosecond, one ns. shorter than period of signal S_1). The outputs of the start oscillator O–**1** together with delay **D4** and the stop oscillator O–**2** are supplied through shapers **SH–1**, **SH–2**, respectively to a coincidence gate **G7**. The clock signal **S2** is also supplied to an inhibit gate **G9** which when enabled supplies **S2** directly to the interpolating counter B and thus the cycles of S_2 are counted. After N_2 cycles of S_2 at τ_c time gate **G7** will sense coincidence as hereinbefore explained, and if gate **G8** is enabled, a pulse from gate **G7** will trigger final stop flip-flop **FF4** into its set condition.

Triggering flip-flop **FF4** causes the gate **G9** to be inhibited so that the signal S_2 is removed from counter B. Interpolating counter B therefore stops at count N_2 and

displays the number of interpolating or vernier cycles which is a measure of innterpolating $N_2\tau_2$.

It was assumed in the foregoing, that periods of signals S_1 and S_2, that is τ_1 and $\tau_1-\tau_2$ are perfectly constant. This is not the case with conventional phase-locked oscillators the type used for O–1 and O–2 which are starting their oscillations at the time of an external command. The first few cycles of such oscillators will contain some transients and therefore the period of these cycles will change somewhat. It should be noted, that since the vernier quantum τ_2 is only a small fraction of τ_1 period, small changes in periods τ_1 and $\tau_1-\tau_2$ may cause relatively large errors in determining the time of coincidence.

For reasons explained above it has been found desirable to ignore any coincidence pulse generated by gate G7 during the first few, for example ten, cycles of either oscillator O–1 or O–2. One possible embodiment for exclusion of early coincidence pulses is shown on FIGURE 1. At the start of a time interval measurement flip-flop FF3 is in reset condition thereby inhibiting gate G8. Coincidence gate G7 can not have any output until after stop time τ_p when oscillator O–2 begins to operate. Let it be assumed that the phase relationships between O–1 and O–2 are such, that during the first few cycles of signal S_2 a coincidence pulse is generated which may have an incorrect timing. Gate G8 prevents this pulse from triggering final stop flip-flop FF4, therefore the coincidence pulse has no effect and the measurement continues.

It should be pointed out that, insofar as the coarse and the interpolating counts are concerned, the output cycles from the start oscillator O–1 and stop oscillator O–2 are not inhibited and are fully counted. Assuming that, as shown in FIGURE 1, interpolating counter B consists of two binary coded decimal counting units (DCU's), after the first ten cycles of S_2 the first DCU output will trigger flip-flop FF3 into its set condition and gate G8 becomes enabled. Any coincidence pulse therefore arriving after the first ten interpolating counts will be able to trigger final stop flip-flop FF4, and flip-flop FF3 and gate G8 will have no effect.

The fact that the first ten cycles of stop oscillator O–2, and since O–1 started sooner, at least the same number of cycles of O–1 are not used for determining coincidence, has no effect on accuracy of the count made by the coarse counter A and the interpolating counter B. As explained above, if coincidence arrives after the first ten cycles of signal S_2 the circuitry for removing the first predetermined number of cycles from consideration has no effect upon the operation of the final stop flip-flop FF4 because the gate G8 is enabled. It is only when coincidence arrives during the time that the gate G8 is inhibited because the predetermined number of counts have not been counted by the interpolating counter B that the circuits FF3 and G8 will have any effect upon the operation of the instrument.

If the final stop flip-flop FF4 is not set, counter B will continue to count even though the zero phases of signal S_1 and signal S_2 have once been in coincidence. Start oscillator O–1 and stop oscillator O–2 will continue operating and they will merely go through another complete cycle until the zero phases are again in exact coincidence. At this time, the gate G8 will be enabled and the final stop flip-flop FF4 will be operated to prevent any further cycles being registered by the interpolating counter B.

The interpolating counter B will not know whether it was the first coincidence, the second coincidence or a later coincidence because the number it will display is the same it would have registered on the first correct coincidence. This is because the interpolating counter is only comprised of two DCU's and the same number is therefore repeated every additional 100 counts, or with the frequencies assumed above at every 10 μ's. The main counter also will not know whether the coincidence which operated the final stop flip-flop FF4 is the first coincidence or a later coincidence, since counter B supplies no carry pulses to counter A. Thus it can be seen, that the coincidence exclusion circuit effectively eliminates the adverse effects of transients on the correct coincidence time. Although it increases the processing time of the interpolation, it has no other effect on the measurement.

Additional circuitry is provided for operation of the time interval counter and consists of a display timer DT of a conventional type which receives a signal from the final stop flip-flop FF4 and displays the reading for a predetermined time. The display timer thereafter through the OR gate G10 supplies a pulse to the reset circuit R to reset all flip-flops of the instrument including the flip-flops in the DCU's and permits a new time interval measurement to be made. The final stop flip-flop FF4 also supplies a signal entitled "print command" which can be utilized to initiate the data recording process such as printing or tape punching.

If the stop command arrives at or near the same time as the zero phase of S_1 an additional count can be added in error to the reading or omitted from the reading of the main counter A as hereinbefore described. A special logic circuitry identified as interpolating logic **14** is utilized to remove this possible ambiguity as explained in detail in copending application Serial No. 377,971, filed June 25, 1964.

The operation of the interpolating logic can be summarized as follows. At the start time τ_t gate G1 is enabled, and signal S_1 coming from oscillator O–1 through delay D4 is able to trigger periodically flip-flop FF5 into its set state and through additional inverter I and OR gate G_4 into its reset state. Every time at τ_1 intervals FF5 is reset, it will feed a carry pulse through gate G3 to coarse counter A. Gate G3 is enabled at start time after appropriate delay D2, selected to inhibit a carry pulse during the first τ_1 period. Triggering of FF5 stops essentially at stop time τ_p except for minor delaying effect of D1. Delays D1 and D2 supply signal to AND gate G2, which inhibits gate G1.

Ideally counter A should advance at zero phase time of signal S_1, but in a practical circuit this could result in count ambiguities. Flip-flop FF5 therefore is arranged to get set somewhat before zero phase time and reset about $\tau_1/2$ period later, thereby serving as a temporary storage element. Delay D1, D2, D3, D4 together with the inherent delays of the gates and other circuitry are selected to provide the appropriate relative triggering times for FF5 as specified above.

After stop command, if FF5 is found in a reset state, it proves that counter A received the correct number of counts since ambiguity can occur only around the ideal carry time when FF5 is in its set state.

If the stop command comes too late in the τ_1 period to find FF5 already set, there is no error in the coarse count and no correction is needed. On the other hand, if the stop command comes early in the τ_1 period when FF5 is still in its set state, the coarse count number is short by one and correction is necessary. Interpolating counter B will indicate but only a relatively long time later at coincidence time τ_c whether stop time was late or early within the τ_1 period by displaying a high or a low count number respectively. Therefore if the count is low, say under 80 designated as $\overline{80}$ at time τ_c, a reset pulse will be presented to FF5 which, if set, will be caused to reset and the resulting carry pulse will correct the count number in counter A. AND gate G5 has the function of supplying the reset pulse.

Another logic network is shown in the drawing and is entitled interlock logic **13**. It is provided for the purpose of resolving ambiguities caused by the start and stop signals coming too close together or even having the stop signal arrive before start signal to give a negative time relationship. As explained in copending application Ser. No. 377,975, filed June 25, 1964, the interlock logic will

only be effective if the start and stop pulses are closer than a predetermined time interval.

Delays D3 and D5 are selected such that flip-flop FF6 will be in the set condition at time τ_c if and only if start and stop pulses occurred within for example ±20 ns. A decision will be made whether this condition represents a negative time or not by observing the output of counter B after final stop time. A high count, for example above 80, indicates that the stop command came before the start command, and therefore the measurement should be rejected. This is accomplished by G11 gate supplying a command pulse at τ_c time to reset circuit R which nullifies the reading by resetting the instrument. In cases when the reading is under 80, or FF6 is in its reset state, OR gate G12 inhibits gate G11 thereby indicating that the start-stop time is positive and the measurement is correct.

To further illustrate the operation of an instrument described in connection with block diagram FIGURE 1, let it be assumed that the start oscillator O–1 is operating at a frequency of 10 mc. and that the offset frequency produced by the stop oscillator O–2 is close to 10.1 mc. With such frequencies, the main counter A advances one count for every τ_1=100 ns. and every count of interpolating counter B will represent τ_2=1 nanosecond interpolating time.

For purposes of illustration let it also be assumed that the time interval to be measured is 635 ns. The main counter A is advanced one count at the reset time of flip-flop FF5 which occurs only toward the middle of the cycle. Therefore, most likely, it will accumulate 5 counts until stop time τ_p and FF5 will stop in its set state. Since the phase locked stop oscillator O–2 is initially 35 ns. behind the zero phase of signal S_1, it will require 35 cycles of 100 ns. each to elapse before coincidence is arrived at in gate G7, since the period of the stop oscillator is only 1 ns. shorter than the period of the start oscillator O–1. When G7 senses coincidence by triggering FF4, it stops the interpolating counter B on number 35. Since this number is less than 80, at time τ_c flip-flop FF5 gets a reset pulse, and changes count storage of counter A from 5 to 6. Thus the last three DCU's of the instrument will display 6, 3, and 5 respectively, correctly showing the measured time as 635 ns.

Assuming now the same inputs but a relatively early reset time, it can happen that at τ_p FF5 is already reset at the 6th time. That means counter A accumulated 6 counts so far. Counter B will operate exactly as before, and because 35<80, at τ_c time FF5 will receive a reset pulse. Nothing can happen though, since FF5 is already reset. The main count number therefore will not change and the display, as before, will indicate 635 ns.

In the illustration above interlock logic flip-flop FF6 will first be set by the start flip-flop FF1 but subsequently reset by the later command of the stop flip-flop FF2. Gate G11 therefore is inhibited and the reading is preserved.

Another embodiment of the interpolating time interval counter is shown in FIGURE 2 which is substantially identical to the interpolating time interval counter as shown in FIGURE 1 with the exception that it incorporates a high stability phase locked oscillator **15** which is substituted in place of the start oscillator O–1 and the delay D4. This high stability phase locked oscillator is explained in detail in copending application Serial No. 377,825, filed June 25, 1964. As pointed out in that application, the high stability phase locked oscillator utilizes the best features of a started oscillator and a crystal oscillator. The started oscillator starts in phase with the start signal. Within a short time later the phase shifted output of a crystal controlled oscillator is exchanged for that of a started oscillator at the time that the phase of the crystal oscillator and the started oscillator come into coincidence. Thereafter, the frequency stability of the oscillator is limited only by the accuracy of the frequency standard utilized.

An interpolating time interval counter of the type shown in FIGURE 2 is utilized whenever long term stability is desired.

Still another embodiment of the interpolating time interval counter is shown in FIGURE 3 which makes it possible to utilize a non-phase locked reference oscillator such as a continuously running crystal oscillator. If non-phase locked reference oscillators are utilized, it is necessary to make an interpolation for the beginning as well as the end of the time interval being measured.

The interpolating time interval counter as shown in FIGURE 3 consists of two of the interpolating time interval counters shown in FIGURE 1 with certain minor modifications which have been identified as **101** and **102** in FIGURE 3. The interpolating time interval counter **101** is provided with one non-phase locked reference oscillator in place of the oscillator O–1 used in the embodiment shown in FIGURE 1. A summing unit **103** of a conventional type is connected to the counters B of each of the units **101** and **102** for providing a sum of the two outputs as hereinafter explained.

In operation, the start command is supplied to both of the inputs **11** simultaneously. The oscillator O–1 in the instrument **101** is running and operating FF5 continuously. Main counter A will start and continue counting after the start pulse enables G3 and until the stop pulse through G2 and G1 stops FF5. After the stop pulse is received on the terminal **12**, the interpolating counter B of the instrument **101** will count the number of counts between the stop command and the time that coincidence is achieved in the instrument **101**. The instrument **102** will be started by the common start pulse and will be stopped by the first zero phase of reference oscillator O–1 of **101**. The interpolating counter B of **102** will count the number of cycles of the signal S_2 from the stop oscillator until a coincidence is achieved. The main counter A can be omitted in the second instrument because the second instrument can only count a time interval between zero and one full cycle of the crystal oscillator O–1 of the instrument **101**. The summing unit **103** sums the results of the count in the two interpolation counters B in the instruments **101** and **102** so that the sum of the two interpolating counters will be indicated by the summing unit **103** and the carry pulse if any will be supplied to counter A of **101**. Thereafter, by reading the main counter A in the instrument **101** and the readout of the summing unit **103**, a true indication of the time interval measured will be given.

It can be seen with this arrangement it is possible to measure a time interval by using a non phase locked reference oscillator. The interpolating counter in one instrument measures between the start command and the zero phase of the reference oscillator and the other interpolating counter measures the time between the zero phase of the oscillator and the stop command.

There is only one notable difference between the use of phase locked and non phase locked reference oscillators. If phase locked oscillators are used, the reading will show no ambiguity even in the vernier count. Successive measurements of a time interval will repeat the same reading which will be always within ± one half count of the true value. If a non phase locked reference oscillator is utilized two interpolations are made each accurate to ± one half count. These two half counts can add up to one count and an ambiguity is presented. Successive readings will not necessarily show the same vernier count. This is a characteristic of all conventional and vernier type time interval counters using non phase locked reference oscillators.

We claim:

1. In an interpolating interval counter of the type which is operable by start and stop commands, a first generator for producing a first cyclic signal having a predetermined constant frequency, a second generator for producing a second cyclic signal having a predetermined

constant frequency differing from the frequency of said first signal, a coarse counter for counting the cycles of the first signal to accumulate a course cycle count, means supplying the first signal to the coarse counter upon receipt of a start command, an interpolating counter for counting the cycles of the second signal to accumulate an interpolating cycle count, means for supplying the second signal to the interpolating counter upon receipt of a stop command, means for preventing the coarse counter from counting any additional cycles of the first signal as soon as the stop command is received, coincidence means for determining when the first and second signals are in coincidence after receipt of the stop command, means connected to said coincidence means for preventing the interpolating counter from counting any additional cycles of the second signal after coincidence is achieved and logic means including a bistable element connected to said interpolating counter and receiving information in the form of an electrical signal about said interpolating cycle count therefrom, said logic means causing the accumulation of an additional cycle count by said coarse counter if the accumulated coarse cycle count accumulated prior to the accumulation of the interpolating cycle count is in error.

2. A counter as in claim 1 wherein said start command occurs at a constant predetermined phase angle of the first cyclic signal.

3. A counter as in claim 1 wherein said start command occurs at an arbitrary phase angle of the first cyclic signal.

4. A counter as in claim 1 together with means to prevent a measurement from being read out when the stop command occurs within a predetermined time preceding the start command.

5. In an interpolating interval counter of a type operable by start and stop commands, a first generator for producing a first cyclic signal having a predetermined constant frequency, a second generator for producing a second cyclic signal having a predetermined constant frequency differing from the frequency of said first signal, a coarse counter for counting the cycles of the first signal, means supplying the first signal to the coarse counter upon receipt of the start command, an interpolating counter for counting the cycles of the second signal, means for supplying the second signal to the interpolating counter upon receipt of a stop command, means for preventing the coarse counter from counting any additional cycles of the first signal as soon as the stop command is received, coincidence means for determining when the first and second signals are in coincidence after receipt of the stop command, means connected to said coincidence means for preventing the interpolating counter from counting any additional cycles of the second signal after coincidence is achieved, means for retroactively determining after coincidence whether the number of cycles counted by the coarse counter is correct, and means for preventing the interpolating counter from being prevented from counting additional cycles of the second signal within a predetermined number of cycles.

6. A counter as in claim 5 wherein said means for preventing said interpolating counter from counting additional cycles of the second signal includes a first bistable element, and a gate connected to the coincidence means, a second bistable element connected to said gate and also connected to the interpolating counter, so that a signal is supplied to the second bistable element after a predetermined number of counts are supplied to the interpolating counter, said second bistable element serving to enable the gate to permit the signal to be supplied by the coincidence means to the first bistable element.

7. In an interpolating time interval counter of the type operable by start and stop commands a first generator for producing a first cyclic signal having a predetermined frequency, a second generator for producing a second cyclic signal having a predetermined constant frequency differing from the frequency of said first signal, a coarse counter for counting the cycles of the first signal, means including logic means connected to said first generator and to said coarse counter for supplying pulses upon receipt of a start command to the coarse counter at the rate determined by said first signal, an interpolating counter for counting the cycles of the second signal, means for supplying the second signal to the interpolating counter upon receipt of a stop command, means for preventing the coarse counter from counting any additional cycles of the first signal as soon as the stop command is received, coincidence means for determining when the first and second signals are in coincidence after receipt of the stop command, means connected to said coincidence means for preventing the interpolating counter from counting any additional cycles of the second signal after coincidence is achieved and additional logic means connected to said interpolating counter and said first named logic means for causing an additional pulse to be supplied to said coarse counter to eliminate any possible error in the number of pulses supplied to said coarse counter when the stop command arrives at a time which is close to the end of a cycle of the first signal.

8. In a method for determining a time interval T between a start command and a stop command, generating a first cyclic signal having a predetermined constant frequency, generating a second cyclic signal having a constant frequency differing from the frequency of said first signal, temporarily storing and then counting cycle by cycle the cycles of the first signal beginning at the receipt of a start command and stopping at the receipt of a stop command to provide a coarse cycle count and counting the number of cycles of the second signal after receipt of the stop command to provide an interpolating cycle count, determining when the first and second signals are in phase coincidence after receipt of the stop command, preventing further counting of the cycles of the second signal after achieving coincidence, retroactively determining after coincidence whether the coarse cycle count is correct by correlating the interpolating cycle count with the temporarily stored cycle of the first signal and correcting the coarse cycle count if it is incorrect.

9. A method as in claim 8 wherein said start command occurs at a constant predetermined phase angle of the first cyclic signal.

10. A method as in claim 8 wherein said start command occurs at an arbitrary phase angle of the first cyclic signal.

11. A method as in claim 10 together with the step of preventing the prevention of cycles of the second signal from being counted until a predetermined number of cycles of the second signal have elapsed.

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ALFRED E. SMITH, Primary Examiner

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