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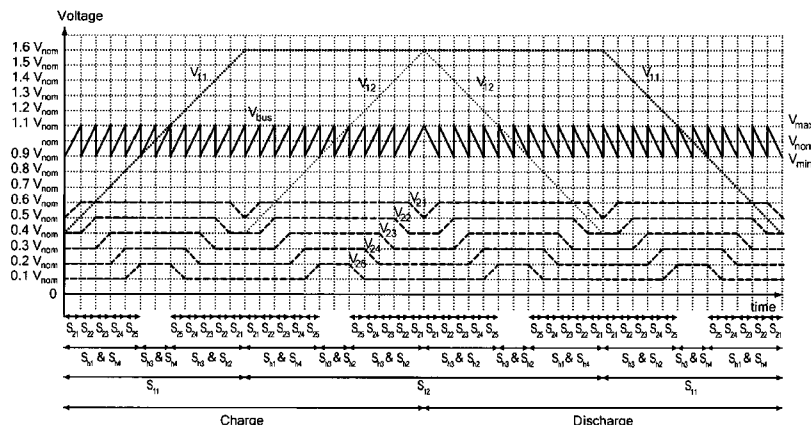
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[Continued on next page]

- (54) Title: ENHANCED STACKED SWITCHED CAPACITOR ENERGY BUFFER CIRCUIT

**FIG. 18A**



- (57) Abstract: A stacked switched capacitor (SSC) energy buffer circuit includes a switching network and a plurality of energy storage capacitors. The switching network need operate at only a relatively low switching frequency and can take advantage of soft charging of the energy storage capacitors to reduce loss. Thus, efficiency of the SSC energy buffer circuit can be extremely high compared with the efficiency of other energy buffer circuits. Since circuits utilizing the SSC energy buffer architecture need not utilize electrolytic capacitors, circuits utilizing the SSC energy buffer architecture overcome limitations of energy buffers utilizing electrolytic capacitors. Circuits utilizing the SSC energy buffer architecture (without electrolytic capacitors) can achieve an effective energy density characteristic comparable to energy buffers utilizing electrolytic capacitors. The SSC energy buffer architecture exhibits losses that scale with the amount of energy buffered, such that a relatively high efficiency can be achieved across a desired operating range.

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**ENHANCED STACKED SWITCHED CAPACITOR ENERGY BUFFER CIRCUIT****BACKGROUND**

[0001] As is known in the art, power conversion systems that interface between direct current (DC) and single-phase alternating current (AC) require an energy storage capability (or an energy buffer) which provides buffering between a constant power desired by a DC source or a load and a continuously varying power desired for a single-phase AC system.

[0002] As is also known, the flow to and from such an energy buffer is at twice the line frequency (e.g., 120 Hz in the United States). The buffering energy requirement can be calculated as  $E_{\text{buf}} = P/\omega_{\text{line}}$ . Because the energy storage requirement of the buffer is proportional to the system average power (P) and the (relatively long) line period ( $T = 2\pi/\omega$ ), the size of the required energy buffer cannot be reduced simply through increases in switching frequency of an interface power converter. Thus, energy buffering requirements represent a significant limitation on miniaturization of grid interface systems.

[0003] One important consideration associated with twice-line-frequency energy buffering relates to lifetime and reliability. Conventional power conversion systems typically utilize electrolytic capacitors to provide high-density energy storage for buffering. It is, however, widely appreciated that despite providing the best available energy density and providing small DC bus voltage variation, electrolytic capacitors also represent a significant source of system lifetime and reliability problems. Also, electrolytic capacitors can only be operated over a narrow charge/discharge range at 120 Hz for thermal and efficiency reasons (i.e., associated with RMS current limits and efficiency requirements). These considerations directly limit the energy buffering capability of electrolytic capacitors at 120 Hz. Thus, while typical peak energy storage densities of up to  $0.9 \text{ J/cm}^3$  can be achieved with electrolytic capacitors, the allowable energy swing at 120 Hz yields practical energy densities that are about an order of magnitude lower. Hence, the development of energy buffering circuits that eliminate electrolytic capacitors while maintaining high energy

storage density and high efficiency is one important requirement to achieving future grid interface systems that have both a small size and a high reliability.

[0004] It is known that film capacitors have a reliability and lifetime which is higher than electrolytic capacitors, but it is also known that film capacitors have considerably lower peak energy density than electrolytic capacitors (by an order of magnitude).

[0005] However, because film capacitors can be efficiently charged and discharged over a much wider voltage range compared with charge/dis-charge voltage ranges of electrolytic capacitors, for 120 Hz buffering, energy densities similar to those achieved with practical systems which utilize electrolytic capacitors can be achieved with high-reliability film capacitors, so long as a wide variation of the capacitor voltage can be used.

[0006] One approach to develop energy buffering circuits that eliminate electrolytic capacitors utilizes active filter blocks (essentially bidirectional DC-DC converters). The active filter block approach effectively utilizes film capacitors while maintaining a desired narrow-range bus voltage. While this approach is flexible in terms of its use, it unfortunately leads to low buffering efficiency if high power density is to be maintained, due to losses in the active filter.

[0007] Other systems have incorporated the required energy buffering as part of the operation of the grid interface power stage. This approach can offset a portion of the buffering loss associated with introduction of a complete additional power conversion stage, but still introduces high-frequency loss and is quite restrictive in terms of operation and application.

[0008] As is also known in the prior art, energy buffering can be employed in many non-line-frequency applications where there is an energy transferred between a first source or load having a slow rate of varying power and/or a limited instantaneous power rating (perhaps a dc source or load) and a second source or load that has a component of power that varies faster and/or to an

instantaneous value larger than that desired to be sourced or absorbed by the first source or load. For example, such applications include interfacing a battery system (which is desired to be efficiently charged or discharged at a limited rate and with a limited peak power) to a mechanical system that requires rapidly varying power flow and perhaps large peak power (e.g., by using a power converter driving an electromechanical system such as a motor). In such a system, an energy buffer is desired to provide the local-time difference between the power sourced or absorbed by the first source or load and the second source or load (e.g., the difference between that desired for the battery and that required by the power converter and motor for the mechanical system). In such applications, an energy buffer may be provided by an ultracapacitor or energy buffer system including one or more ultracapacitors. Applications requiring energy buffering of the nature described here may include, without limitation, motor drives, electric and hybrid vehicle drive trains, cranes, renewable energy systems including wind and wave energy systems, active filter and reactive power compensation systems, traction systems, laser driver systems, electromagnetic launch systems, electromagnetic guns, electromagnetic brakes and propulsion systems, and power systems for implanted medical devices.

#### **SUMMARY**

[0009] In accordance with the concepts, systems, circuits and techniques described herein, a stacked switched capacitor (SSC) energy buffer circuit comprises a plurality of series-connected blocks of switches and capacitors. The capacitors are preferably of a type that can be efficiently charged and discharged over a wide voltage range over a buffering time period of interest (e.g., film capacitors for line-frequency applications, and electrolytic capacitors or ultracapacitors for mechanical system time scale applications). Thus, selection of the particular capacitor type and characteristics depends, at least in part, upon the particular application and the buffering time period. In some embodiments, ultra-capacitors or electrolytic capacitors could be used. The switches are disposed to selectively couple the capacitors to enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to a buffer port. The switches are cooperatively operated as a switching network such that

the voltage seen at the buffer port varies only over a small range as the capacitors charge and discharge over a wide range to buffer energy.

[0010] With this particular arrangement, an energy buffer circuit having an effective energy density which is relatively high compared with the effective energy density of conventional energy buffer circuits is provided. In some embodiments, efficiency can be extremely high because the switching network need operate at relatively low (e.g. line-scale) switching frequencies, and the system can take advantage of soft charging or adiabatic charging of the energy storage capacitors to reduce loss. Moreover, the stacked switched capacitor buffer architecture described herein exhibits losses that reduce as energy buffering requirements reduce such that high efficiency can be achieved across an entire desired operating range.

[0011] In accordance with a further aspect of the concepts, systems, circuits and techniques described herein a grid interface power converter comprises an first filter having a first port adapted to receive an input voltage from a DC source, a resonant high frequency isolated DC-DC converter having a first port coupled to a second port of the first filter, a resonant high frequency inverter having a first port coupled to a second port of the resonant high frequency isolated DC-DC converter and having a second port coupled to a first port of a second filter with the second filter having a second port adapted to receive an input voltage from a AC source. The grid interface power converter further comprises a stacked switched capacitor (SSC) energy buffer circuit coupled between the second port of the resonant high frequency isolated DC-DC converter and the first port of the resonant high frequency inverter. By appropriately modifying switch states of the SSC energy buffer circuit, the SSC energy buffer circuit absorbs and delivers energy over a wide individual capacitor voltage range, while maintaining a narrow-range voltage at the input port. This enables maximal utilization of the energy storage capability.

[0012] In accordance with a further aspect of the concepts, systems, circuits and techniques described herein a grid interface power converter

comprises a DC-DC converter having a first port adapted to connect to a DC source or load, a DC-AC converter having a first port coupled to a second port of the DC-DC converter and having a second port adapted to connect to a AC source or load. The grid interface power converter further comprises a stacked switched capacitor (SSC) energy buffer circuit coupled between the second port of the DC-DC converter and the first port of the DC-AC converter. By appropriately modifying switch states of the SSC energy buffer circuit, the SSC energy buffer circuit absorbs and delivers energy over a wide individual capacitor voltage range, while maintaining a narrow-range voltage at the input port. This enables relatively high utilization, and in some cases maximal utilization, of the energy storage capability.

[0013] With this particular arrangement, an energy buffering approach applicable to a wide range of grid-interface power electronic applications is provided. Grid-interface power electronic applications include but are not limited to photovoltaic inverters, motor drives, power supplies, off-line LED drivers and plug-in hybrid electric vehicle chargers. Use of the energy buffering approach described herein results in improved reliability and lifetime in these and other applications.

[0014] In one embodiment, a stacked switched capacitor (SSC) energy buffer circuit includes a switching network comprised of a plurality of switches and a plurality of energy storage capacitors which may be provided as film capacitors. Switches in the switching network are configured to selectively couple at least one of the energy storage capacitors in series across a bus voltage. The switching network need operate at only a relatively low switching frequency, and the system can take advantage of soft charging of the energy storage capacitors to reduce loss. Thus, efficiency of the SSC energy buffer circuit can be extremely high compared with the efficiency of other energy buffer circuits. Furthermore, since circuits utilizing the SSC energy buffer architecture need not utilize electrolytic capacitors, circuits utilizing the SSC energy buffer architecture overcome limitations of energy buffers which do utilize electrolytic capacitors. Furthermore, circuits utilizing the SSC energy buffer architecture

(but not using utilizing electrolytic capacitors) can achieve an effective energy density characteristic comparable to energy buffers which utilize electrolytic capacitors. In some cases, circuits using the SSC energy buffer architecture, either with or without electrolytic capacitors, can achieve higher effective energy than a circuit using electrolytic capacitors alone for the same voltage ripple. Moreover, the SSC energy buffer architecture exhibits losses that scale with the amount of energy that must be buffered, such that a relatively high efficiency can be achieved across a desired operating range.

[0015] In accordance with a further aspect of the concepts, systems, circuits and techniques described herein, a stacked switched capacitor (SSC) energy buffer circuit having first and second terminals includes a first sub-circuit comprising one or more capacitors, a second sub-circuit comprising one or more capacitors and one or more switches disposed in at least one of said first and second sub-circuits. The one or more switches are cooperatively operated to selectively couple the one or more capacitors within and/or between the first and second sub-circuits. In a first operating mode, the first and second sub-circuits are serially coupled and the one or more switches are operable to enable dynamic reconfiguration of how the capacitors are coupled to the terminals of the sub-circuit.

[0016] In one embodiment, the one or more switches are operable to dynamically reconfigure the interconnection among the capacitors within at least one of said first and second sub-circuits.

[0017] In one embodiment, in at least some operating modes of the SSC energy buffer circuit, the one or more switches are operable to prevent the capacitors from ever being connected together at both terminals.

[0018] In accordance with a further aspect of the concepts, systems, circuits and techniques described herein, a switched capacitor based energy buffer architecture that restricts the apparent voltage ripple while utilizing a large fraction of energy in stored in capacitors is described. The switched capacitor

based energy buffer architecture allows successfully replacement of electrolytic capacitors with film capacitors to achieve longer lifetimes while at the same time maintaining small volume. Also, when used with film capacitors, it can increase the life of grid-interfaced power converters by eliminating limited-life electrolytic capacitors while maintaining comparable energy density.

[0019] In one embodiment, an enhanced version of a bipolar SSC energy buffer that achieves a higher effective energy density and round-trip efficiency, while maintaining favorable bus voltage ripple is described. The enhanced buffer uses fewer capacitors and switches than the previous designs. The enhancement in performance is achieved by modifying the control and switching patterns of the buffer switches. A prototype enhanced SSC energy buffer, designed for a 320V bus and a 135W load, has been built and tested. The design methodology and experimental results for the enhanced SSC energy buffer are presented and compared with the original design. The Stacked Switched Capacitor (SSC) energy buffer is an architecture for buffering energy between single-phase ac and dc.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0020] FIG. 1A is circuit diagram of a parallel-series switched capacitor circuit.

[0021] FIGS. 1B and 1C are circuit diagrams of two configurations associated with FIG. 1A for different switch states.

[0022] FIG. 2 is a circuit diagram of a stacked switched capacitor (SSC) energy buffer circuit.

[0023] FIG. 3 is a block diagram of a grid interface power converter system using the SSC energy buffer circuit of FIG. 2.

[0024] FIG. 3A is a block diagram of a general grid interface power converter system using the SSC energy buffer circuit of FIG. 2.

[0025] FIG. 4 is a circuit diagram of an example of the SSC energy buffer circuit called a 2-4 bipolar SSC energy buffer circuit.

[0026] FIG. 5 is a plot of switch states vs. voltages of the circuit in FIG 4.

[0027] FIG. 6 is a circuit diagram of another example of the SSC energy buffer circuit called a 1-3 unipolar SSC energy buffer circuit.

[0028] FIG. 7 is a plot of switch states vs. voltages of the circuit in FIG 6.

[0029] FIG. 8 is a plot of switch states vs. voltages of the circuit in FIG 6 using a modified control.

[0030] FIG. 9 is a circuit diagram of a generalized example of the SSC energy buffer circuit of FIG. 6 called a 1-m unipolar SSC energy buffer circuit.

[0031] FIG. 10 is a circuit diagram of an example of the SSC energy buffer circuit of FIG. 2 called a 1-3 bipolar SSC energy buffer circuit.

[0032] FIG. 11 is a plot of switch states vs. voltages of the circuit in FIG 10.

[0033] FIG. 12 is a circuit diagram of an example of the SSC energy buffer circuit of FIG. 2 called an n-m bipolar SSC energy buffer circuit.

[0034] FIG. 13 is a plot of energy buffering ratio versus a number of m capacitors with a voltage ripple ratio of 12.5% for different numbers of n capacitors.

[0035] FIGS. 14A is a plot of energy buffering ratio versus a number of m capacitors with a voltage ripple ratio of 25% for different numbers of n capacitors.

[0036] FIG. 14B is a plot of energy buffering ratio versus a number of m capacitors with a voltage ripple ratio of 6.25% for different numbers of n capacitors.

[0037] FIG. 15 is a circuit diagram of another example of the SSC energy buffer circuit called a 2-6 bipolar SSC energy buffer circuit.

[0038] FIG. 16 is a plot of switch states vs. voltages of the circuit in FIG 15.

[0039] FIG. 17 is a plot of energy buffering ratio versus and the number of m capacitors for different numbers of n capacitors and whether under modified control.

#### **DETAILED DESCRIPTION**

[0040] Described herein is a switched capacitor structure referred to herein as stacked switched capacitor (SSC) energy buffer circuit. Although

reference is sometimes made herein to use of an energy buffer circuit in a particular application, it should be appreciated that the energy buffer circuits, concepts and techniques described herein find use in a wide variety of applications. For example, many applications exist in which an energy buffer is used because either a peak power rating or a desired energy transfer rating of a first source or load is different from that of the source or load to which it interfaces. It should be recognized that the concepts, systems, circuits and techniques described herein can be used in these applications to achieve one or more of: higher energy density / smaller size at a given voltage variation level, higher reliability by using more desirable energy storage elements.

[0041] The SSC energy buffer circuit provides a small variation of a bus voltage,  $V_{bus}$  while also providing high utilization of available peak energy storage capacity. In one embodiment, a variation of 12.5% or less is provided while providing utilization of available peak energy storage capacity of 72.7 % or better. The SSC energy buffer circuit and related techniques described herein achieves extremely high efficiency (e.g., by using film capacitors) and uses simpler circuitry. The SSC energy buffer circuit and related techniques described herein achieves extremely high energy density e.g., by incorporating film capacitors, electrolytic capacitors or ultracapacitors and employing them over a wider voltage range than appears at the input port. The SSC energy buffer circuit and related techniques described herein provide performance characteristics comparable to or better than conventional energy buffer circuits while at the same time utilizing fewer switches and capacitors than conventional energy buffer circuits. The SSC energy buffer circuit includes a number of variations as will be described herein.

[0042] Referring to FIGS. 1A to 1C, switched capacitor circuits that reconfigure capacitors between parallel and series combinations have been used to improve the energy utilization of ultracapacitors. A circuit 10 is a simple version of a parallel-series switched capacitor circuit. The circuit 10 includes switches  $S_1$ ,  $S_2$ ,  $S_3$  and two capacitors  $C_1$  and  $C_2$ . The circuit 10 also includes a terminal 12 and a terminal 14 (collectively referred to herein as a buffer port) to

provide a bus voltage,  $V_{bus}$ , across the terminals 12, 14. When switches  $S_1$  and  $S_3$  are open and  $S_2$  is closed, the resulting configuration is represented by a circuit 10' as shown in FIG. 1B depicting capacitors  $C_1$  and  $C_2$  in series. When switches  $S_1$  and  $S_3$  are closed and  $S_2$  is open, the resulting configuration is represented by a circuit 10'' shown in FIG. 1C depicting capacitors  $C_1$  and  $C_2$  in parallel.

[0043] While the circuit 10 has a high capacitor energy utilization of 93.75% which is relatively high compared with prior art approaches, the circuit 10 also has a voltage ripple ratio of 33.3% which is also relatively high compared with prior art approaches. That is, the value of the bus voltage,  $V_{bus}$ , varies by as much as 33.3%. For example, in one embodiment, the voltage of the dc bus varies from  $0.67V_{nom}$  to  $1.33V_{nom}$  where  $V_{nom}$  is the average (nominal) value of the bus voltage. More complex parallel-series switched capacitor circuits have also been developed which achieve a better voltage ripple ratio; however, these complex parallel-series switched capacitors have high circuit complexity when high energy utilization and small voltage ripple are required. For example, a circuit currently having among the best performance (e.g., a 8-6-5-4-3 parallel-series switched capacitor circuit) has an energy utilization of 92.09% and a voltage ripple ratio of 14.3%, but requires 41 switches and 120 capacitors making the circuit relatively complicated and thus relatively difficult to implement for use in practical circuits and systems.

[0044] Referring to FIG. 2, a stacked switched capacitor (SSC) energy buffer circuit 100 overcomes the deficiencies of the switched capacitor circuits like that of the circuit 10 (FIG. 1). The SSC energy buffer circuit 100 includes a first set of circuitry 102 and a second set of circuitry 104 connected in series. SSC energy buffer circuit 100 further includes a pre-charge circuit 105. For reasons which will become apparent from the description provided herein below, pre-charge circuit 105 is coupled to each of the two sub-circuits 102, 104 and pre-charge circuit 105 is operable to charge each of one or more capacitors in two sub-circuits 102, 104 to specified initial conditions before entering a first operating mode. In some cases, the pre-charge circuit 105 may be coupled in

series with each of the two sub-circuits 102, 104 before entering a first operating mode, and further connections of the pre-charge circuit 105 to capacitors within the two sub-circuits 102, 104 may be made with switches in the two sub-circuits 102, 104

[0045] The circuit 100 also includes a terminal 112, a terminal 113 and a terminal 114. Terminals 112, 114 collectively form a buffer port to provide the bus voltage,  $V_{BUS}$ . Each set of circuitry 102, 104 includes capacitors.

[0046] As illustrated in Fig. 2, the first set of circuitry 102 includes capacitors  $C_{11}, C_{12}, \dots, C_{1n}$  and the second set of circuitry 104 includes capacitors  $C_{21}, C_{22}, \dots, C_{2m}$  where  $n$  and  $m$  are integers greater than or equal to one. The capacitors  $C_{11}, C_{12}, \dots, C_{1n}, C_{21}, C_{22}, \dots, C_{2m}$ , are of a type that can be efficiently charged and discharged over a wide voltage range (e.g., film capacitors electrolytic capacitors and ultra capacitors).

[0047] Each set of circuitry also includes switches. As illustrated in Fig. 2, the first set of circuitry 102 includes switches  $S_{11}, S_{12}, \dots, S_{1n}$  and the second set of circuitry 104 includes switches  $S_{21}, S_{22}, \dots, S_{2m}$  connected in series with a respective one capacitor. For example, the switch  $S_{11}$  is in series with the capacitor  $C_{11}$ , the switch  $S_{12}$  is in series with the capacitor  $C_{12}$ , the switch  $S_{21}$  is in series with the capacitor  $C_{21}$ , the switch  $S_{22}$  is in series with the capacitor  $C_{22}$  and so forth. The switches  $S_{11}, S_{12}, \dots, S_{1n}$  and  $S_{21}, S_{22}, \dots, S_{2m}$  enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer port to provide the bus voltage,  $V_{bus}$ .

[0048] It should, of course, be appreciated that in some implementations there is no one-to-one correspondence between capacitors and switches, that is, a "leg" can be just a capacitor as  $C_{11}$  is in FIG. 6, just a switch as  $S_{11}$  is in FIG. 6, or a switch in series with a capacitor as in many cases. Also one of the blocks can have switches not associated with a "leg" to allow the "legs" of that block to be connected in reverse, as  $S_{h1}, S_{h2}, S_{h3}$  and  $S_{h4}$  do in Fig. 4.

[0049] The switching in the circuit 100 (i.e., opening and closing of the switches) is preferably performed such that the voltage seen at the buffer port,  $V_{bus}$ , varies only over a small range as the capacitors charge and discharge over a wide voltage range to buffer energy, thereby providing a high effective energy density. By appropriately modifying the switch states, the buffer capacitors absorb and deliver energy over a relatively wide individual voltage range, while maintaining a relatively narrow-range voltage at the input port. This enables a high degree of utilization (and in some cases, even maximal utilization) of the capacitor energy storage capability. Efficiency of the circuit 100 can be extremely high because the switches in the circuit 100 need operate at only very low (line-scale) switching frequencies. Also, the circuit 100 can take advantage of soft charging of the energy storage capacitors to reduce loss. Moreover, the circuit 100 exhibits losses that reduce as energy buffering requirements reduce such that high efficiency can be achieved across the full operating range.

[0050] Referring to FIG. 3, the SSC energy buffer circuit 100 may be included into a grid interface power converter system 200. The system 200 includes a DC power source 202 coupled to an input filter with parasitic compensation 204, a resonant high frequency isolated DC-DC converter 206 coupled to the SSC energy buffer circuit 100 through the terminals 112, 114 that provide the bus voltage,  $V_{bus}$ . The system 200 also includes an AC power source 212 coupled to an input filter with parasitic compensation 214, a resonant high frequency inverter 216 coupled to the SSC energy buffer circuit 100 through the terminals 112, 114. This energy buffering approach is applicable to a wide range of grid-interface power electronic applications (including photovoltaic inverters, motor drives, power supplies, off-line LED drivers and plug-in hybrid electric vehicle chargers and so forth), enabling improved reliability and lifetime in these applications.

[0051] Referring to FIG. 3A, a grid interface power converter includes a DC-DC converter having a first port adapted to connect to a DC source or load. The grid interface power converter further includes a DC-AC converter having a first port coupled to a second port of the DC-DC converter and having a second

port adapted to connect to an AC source or load. The grid interface power converter further comprises a stacked switched capacitor (SSC) energy buffer circuit coupled between the second port of the DC-DC converter and the first port of the DC-AC converter. By appropriately modifying switch states of the SSC energy buffer circuit, the SSC energy buffer circuit absorbs and delivers energy over a wide individual capacitor voltage range, while maintaining a narrow-range voltage at the input port. This enables relatively high utilization, and in some cases maximal utilization, of the energy storage capability

[0052] Referring to FIG. 4, one particular example of the SSC energy buffer circuit 100 is a circuit 300 called a 2-4 bipolar SSC energy buffer circuit. The circuit 300 includes a first set of circuitry 302 and a second set of circuitry 304 in series with the first set of circuitry 302. The first set of circuitry 302 includes four "legs" each of which comprise four switches  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{24}$  series coupled with respective ones of four capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  (e.g., the switch  $S_{21}$  is in series with the capacitor  $C_{21}$ , the switch  $S_{22}$  is in series with the capacitor  $C_{22}$ , the switch  $S_{23}$  is in series with the capacitor  $C_{23}$ , and the switch  $S_{24}$  is in series with the capacitor  $C_{24}$  and so forth). The capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  can be in the circuit 300 in a positive or a negative manner (hence the term "bipolar").

[0053] The first circuitry 302 also includes switches  $S_{H2}$ ,  $S_{H1}$ ,  $S_{H3}$ ,  $S_{H4}$  (sometimes referred herein collectively as an H-bridge) and selectively opening and closing the switches allows for bi-polar charging. The second set of circuitry 304 includes two capacitors  $C_{11}$ ,  $C_{12}$  and two switches  $S_{11}$ ,  $S_{12}$  serially coupled to a respective one of the two capacitors  $C_{11}$ ,  $C_{12}$  (e.g., the switch  $S_{11}$  is in series with the capacitor  $C_{11}$  and the switch  $S_{12}$  is in series with the capacitor  $C_{12}$ ). The circuit 300 also includes a terminal 312 and a terminal 314 that collectively form a buffer port to provide the bus voltage,  $V_{BUS}$ .

[0054] The capacitors  $C_{11}$ ,  $C_{12}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  have corresponding voltages  $V_{11}$ ,  $V_{12}$ ,  $V_{21}$ ,  $V_{22}$ ,  $V_{23}$ ,  $V_{24}$  respectively. The capacitors  $C_{11}$ ,  $C_{12}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  have identical capacitance, but different voltage ratings. For

example, the capacitors,  $C_{11}$ ,  $C_{12}$  each have a voltage rating of  $13/8 V_{nom}$ , where  $V_{nom}$  is the nominal value of the bus voltage,  $V_{bus}$ . The voltage rating of the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  are  $5/8 V_{nom}$ ,  $4/8 V_{nom}$ ,  $3/8 V_{nom}$ , and  $2/8 V_{nom}$ , respectively. Pre-charging circuitry (not shown in FIG. 4) ensures that the following initial voltages  $V_{11}$ ,  $V_{12}$ ,  $V_{21}$ ,  $V_{22}$ ,  $V_{23}$ ,  $V_{24}$  for the capacitors  $C_{11}$ ,  $C_{12}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  are  $3/8 V_{nom}$ ,  $3/8 V_{nom}$ ,  $4/8 V_{nom}$ ,  $3/8 V_{nom}$ ,  $2/8 V_{nom}$ , and  $1/8 V_{nom}$ , respectively.

[0055] Referring to FIG. 5, when the circuit 300 begins charging from its minimum state of charge, switches  $S_{h1}$ ,  $S_{h4}$ ,  $S_{21}$ ,  $S_{11}$  are turned on while switches  $S_{h2}$ ,  $S_{h3}$ ,  $S_{12}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{24}$  are turned off. In the minimum state of charge, the capacitors  $C_{11}$ ,  $C_{21}$  are connected in series and charged until the bus voltage,  $V_{bus}$ , rises from  $7/8 V_{nom}$  to  $9/8 V_{nom}$ . At this instant, the voltage,  $V_{21}$ , of the capacitor  $C_{21}$  reaches  $5/8 V_{nom}$  and the voltage,  $V_{11}$ , of the capacitor  $C_{11}$  reaches  $4/8 V_{nom}$ .

[0056] Then, the switch  $S_{21}$  is turned off, the switch  $S_{22}$  is turned on; and the bus voltage,  $V_{bus}$ , drops back down to  $7/8 V_{nom}$ . After a similar period of time (assuming a constant charging current) the voltage,  $V_{22}$ , of the capacitor  $C_{22}$  reaches  $4/8 V_{nom}$  and the voltage,  $V_{11}$ , of the capacitor  $C_{11}$  reaches  $5/8 V_{nom}$  and the bus voltage,  $V_{bus}$ , again reaches  $9/8 V_{nom}$ .

[0057] Next, the switch  $S_{22}$  is turned off, the switch  $S_{23}$  is turned on and the capacitor  $C_{23}$  is charged. This process is repeated until the capacitor  $C_{24}$  is charged. At this point, the capacitor voltages  $V_{11}$ ,  $V_{12}$ ,  $V_{21}$ ,  $V_{22}$ ,  $V_{23}$ , and  $V_{24}$ , are  $7/8 V_{nom}$ ;  $3/8 V_{nom}$ ;  $5/8 V_{nom}$ ;  $4/8 V_{nom}$ ;  $3/8 V_{nom}$ ; and  $2/8 V_{nom}$ , respectively. The bus voltage,  $V_{bus}$ , is  $9/8 V_{nom}$ .

[0058] Next, the capacitor  $C_{11}$  is charged directly through the switches  $S_{h3}$ ,  $S_{h4}$ ,  $S_{11}$  (with all other switches  $S_{h1}$ ,  $S_{h1}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{24}$  off) until the voltage,  $V_{11}$ , and the bus voltage,  $V_{bus}$ , reach  $9/8 V_{nom}$ . Now, the switch  $S_{h4}$  is turned off, and the switch  $S_{h2}$  is turned on along with the switch  $S_{h3}$ . Hence, the bus voltage,  $V_{bus}$ , again drops to  $7/8 V_{nom}$ .

[0059] Now, the capacitor  $C_{11}$  can continue to charge up through the now negatively connected capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  through a process similar to the one described above, except that the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ ,  $C_{24}$  are discharged in reverse order, i.e., first through  $C_{24}$ , then through  $C_{23}$ , and so on until finally through  $C_{21}$ .

[0060] At this instant, the capacitor  $C_{11}$  is fully charged to  $13/8 V_{nom}$  and charging of the capacitor  $C_{12}$  must begin. For this, the H-bridge switches are toggled (i.e., the switches  $S_{h2}$  and  $S_{h3}$  are turned off, and the switches  $S_{h1}$  and  $S_{h4}$  are turned on), the switch  $S_{11}$  is turned off and the switch  $S_{12}$  is turned on. The charging process for the capacitor  $C_{12}$  is identical to the charging process for the capacitor  $C_{11}$ . The switch states, the capacitor voltages (as seen from a port outside the H-bridge, e.g. terminals 312 and 313 between sub-circuit 302 and sub-circuit 304) and the resulting bus voltages,  $V_{bus}$ , over a complete charge and discharge cycle are shown in FIG. 5.

[0061] During the discharge period, the capacitors  $C_{11}$ ,  $C_{12}$  are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period. Throughout the charging and discharging period of the circuit 300, the bus voltage,  $V_{bus}$ , stays within the  $7/8 V_{nom}$  to  $9/8 V_{nom}$  range. Hence, the circuit 300 has a (nominal to peak) voltage ripple of 12.5%.

[0062] It is meaningful to compare various energy buffering circuits in terms of their energy buffering ratio,  $\gamma_b$ . An energy buffering ratio,  $\gamma_b$ , is a measure of how effectively a circuit makes use of the total energy storage capacity of its capacitors,  $E_{rated}$ . It is defined as the ratio of the energy that can be extracted in one cycle to  $E_{rated}$ . If an energy buffering architecture can be charged up to a maximum energy of  $E_{max}$  and drained down to a minimum energy of  $E_{min}$ , then the energy buffering ratio,  $\gamma_b$ , is given by:

$$\gamma_b = (E_{max} - E_{min}) / (E_{rated})$$

[0063] The exemplary circuit 300 achieves an energy buffering ratio,  $\gamma_b$  of 81.6%.

[0064] Referring to FIG. 6, another example of the SSC energy buffer 100 is a circuit 400 called a 1-3 unipolar SSC energy buffer circuit. The circuit 400 includes a first set of circuitry 402 and a second set of circuitry 404. The first set of circuitry 402 includes switches  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$  connected in series to capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ , respectively, and these "legs" (switches in series with capacitors) are connected in parallel. The first set of circuitry 402 also includes a switch  $S_{11}$  coupled in parallel to the capacitor switch pairs  $C_{21}$ - $S_{21}$ ,  $C_{22}$ - $S_{22}$  and  $C_{23}$ - $S_{23}$ . The second set of circuitry 404 includes a capacitor  $C_{11}$ .

[0065] The capacitors  $C_{11}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  have corresponding voltages  $V_{11}$ ,  $V_{21}$ ,  $V_{22}$ , and  $V_{23}$ , respectively. The capacitors  $C_{11}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  have identical capacitance, but different voltage ratings:  $9/8 V_{nom}$  for  $C_{11}$ ,  $4/8 V_{nom}$  for  $C_{21}$ ,  $3/8 V_{nom}$  for  $C_{22}$  and  $2/8 V_{nom}$  for  $C_{23}$ , where  $V_{nom}$  is the nominal value of the bus voltage,  $V_{bus}$ . Most of the energy is buffered by the capacitor  $C_{11}$ , which also supports most of the voltage, while the capacitors  $C_{21}$ ,  $C_{22}$  and  $C_{23}$  play a supportive function, by buffering a small amount of energy and providing some voltage support.

[0066] FIG. 7 depicts the voltage waveforms for the capacitors  $C_{11}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  during a charging period for the circuit 400. Pre-charging circuitry (not shown in FIG. 6) ensures that each of capacitors  $C_{11}$ ,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  are charged to respective ones of the following initial voltages  $V_{11}$ ,  $V_{21}$ ,  $V_{22}$  and  $V_{23}$ . In one embodiment, the initial voltages  $V_{11}$ ,  $V_{21}$ ,  $V_{22}$ ,  $V_{23}$  correspond to voltages of  $4/8 V_{nom}$ ;  $3/8 V_{nom}$ ;  $2/8 V_{nom}$ ; and  $1/8 V_{nom}$ . Once the circuit 400 starts to charge, the switch  $S_{21}$  is turned on and the other switches  $S_{22}$ ,  $S_{23}$  and  $S_{11}$  are turned off. In this case, the capacitors  $C_{11}$ ,  $C_{21}$  are placed in series with each other and charged until the bus voltage,  $V_{bus}$ , reaches  $9/8 V_{nom}$ , when the voltage,  $V_{21}$ , reaches  $4/8 V_{nom}$ , and the voltage,  $V_{11}$ , reaches  $5/8 V_{nom}$ . Then, the switch  $S_{21}$  is turned off, the switch  $S_{22}$  is turned on. After a next period of time (which may be the same as or similar to the period of time taken to charge caps  $C_{11}$ ,  $C_{21}$

assuming a constant charging current), the voltage,  $V_{22}$ , reaches  $3/8 V_{nom}$  and the voltage,  $V_{11}$  reaches  $6/8 V_{nom}$ . Then, the switch  $S_{23}$  is turned on and the capacitor  $C_{23}$  is charged. In this way, switches  $S_{21}$ ,  $S_{22}$ ,  $S_{23}$ ,  $S_{11}$  are turned on and off one after another and the voltages  $V_{21}$ ,  $V_{22}$ ,  $V_{23}$ ,  $V_{11}$  finally reach the voltage values  $4/8 V_{nom}$ ,  $3/8 V_{nom}$ ,  $2/8 V_{nom}$  and  $9/8 V_{nom}$ , respectively. Then, the circuit 400 enters the discharging period. The switches are turned on and off in reverse order in the discharge cycle. Hence, the voltage waveforms during the discharging period are the reverse of those in the charging period (not shown in FIG. 7).

[0067] Thus, by changing the switch configurations appropriately as energy is delivered to and from the buffer port, individual capacitors can be charged/discharged over a wide range (from their initial voltages to rated voltages), while the voltage at the buffer port,  $V_{bus}$ , is maintained within a narrow range (within  $\pm 12.5\%$  of  $V_{nom}$ ) as shown in FIG. 7. It can be shown that this simple structure can provide energy buffering of up to  $8/11$  ( $\sim 72.7\%$ ) of the peak energy storage rating of the capacitors, while providing a buffer port voltage,  $V_{bus}$ , that remains within  $\pm 12.5\%$  of a nominal bus voltage,  $V_{nom}$ .

[0068] Referring to FIG. 8, the circuit 400 can also be operated in slightly different manner. For example, unlike the control strategy depicted in FIG. 7, a different control strategy gives equal time to all four switch states. The required voltage rating of the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  is lower than in FIG. 7. However, with this modification the energy buffering ratio of the buffer reduces to 68.4% compared to 72.7% depicted in FIG. 7.

[0069] Referring to FIG. 9, the circuit 400 can be extended to achieve a smaller bus voltage,  $V_{bus}$ , variation or a higher energy buffering ratio,  $\gamma_b$ , by adding more capacitors in parallel to the three upper capacitors,  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$ , shown in the circuit 400 (FIG. 6). For example, a circuit 400' called a 1-m unipolar SSC energy buffer circuit includes a first set of circuitry 402' and the second set of circuitry 404 which includes the capacitor  $C_{11}$  similar to the circuit 400. However, the first set of circuitry 402' includes additional switches and

capacitors than the first set of circuitry 402 in the circuit 400. For example, the first set of circuitry 402' includes m "legs" in parallel (each "leg" consisting of a switch in series with a capacitor), m switches in series with the m capacitors and the switch S<sub>11</sub> in parallel with the m "legs". Each of the m capacitors have equal capacitance. The energy buffering ratio for the circuit 400' is given by:

$$\gamma_b = \frac{[(1+R_v)^2 - (1-mR_v)^2]C_1 + (mR_v)^2}{C_1(1+R_v)^2 + C_2(1+2^2+\dots+m^2)R_v^2}$$

where R<sub>v</sub> is the voltage ripple ratio (= .5 (V<sub>max</sub> - V<sub>min</sub>)/V<sub>nom</sub>), C<sub>1</sub> is the capacitance of the capacitor C<sub>11</sub> and C<sub>2</sub> is the capacitance of one of the m capacitors each (which have equal capacitance).

[0070] Referring to FIG. 10, another type of SSC energy buffer circuit is a circuit 500 called a 1-3 bipolar SSC energy buffer circuit. Film capacitors are bipolar and can be charged in either direction. The circuit 500 takes advantage of this fact and thus improves the topology and operating strategy in order to push the energy buffering ratio, γ<sub>b</sub>, even higher.

[0071] The circuit 500 includes a first set of circuitry 502 and a second set of circuitry 504. The first set of circuitry 502 includes 3 "legs" in parallel and switches S<sub>21</sub>, S<sub>22</sub> and S<sub>23</sub> in series with a respective one capacitor C<sub>21</sub>, C<sub>22</sub>, C<sub>23</sub>, each set forming one leg. The first set of circuitry 502 also includes switches S<sub>h1</sub>, S<sub>h2</sub>, S<sub>h3</sub>, S<sub>h4</sub> (e.g., an H-bridge). The second set of circuitry 504 includes a capacitor, C<sub>11</sub>. The capacitors C<sub>11</sub>, C<sub>21</sub>, C<sub>22</sub>, C<sub>23</sub> have identical capacitance values. The voltage ratings for the capacitors C<sub>11</sub>, C<sub>21</sub>, C<sub>22</sub>, C<sub>23</sub> are 11/8 V<sub>nom</sub>, 3/8 V<sub>nom</sub>, 2/8 V<sub>nom</sub> and 1/8 V<sub>nom</sub>, and respectively. The main difference of this topology compared to unipolar one is that the four supporting capacitors are now put into the H-bridge to enable bi-directional charging. For operating strategy, pre-charging circuitry (not shown) ensures that specified initial voltages are placed on the capacitors C<sub>11</sub>, C<sub>21</sub>, C<sub>22</sub>, C<sub>23</sub> are 5/8 V<sub>nom</sub>, 2/8 V<sub>nom</sub>, 1/8 V<sub>nom</sub>, 0 respectively. At first, switches S<sub>h1</sub> and S<sub>h4</sub> are turned on and switches S<sub>h2</sub> and S<sub>h3</sub> are turned off. Then the circuit 500 operates as a unipolar buffer as described above until the voltage of the four capacitors C<sub>11</sub>, C<sub>21</sub>, C<sub>22</sub>, C<sub>23</sub> reaches 3/8 V<sub>nom</sub>, 2/8 V<sub>nom</sub>, 1/8 V<sub>nom</sub>, and V<sub>nom</sub>, respectively. At this time, the

switches  $S_{h1}$  and  $S_{h4}$  are turned off and the switches  $S_{h2}$  and  $S_{h3}$  are turned on, thus the voltages of the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  seen from the outside are reversed to  $-3/8 V_{nom}$ ,  $-2/8 V_{nom}$  and  $-1/8 V_{nom}$ , while the voltage of the capacitor,  $C_{11}$ , stays the same. After a similar process, the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  are charged back to  $-2/8 V_{nom}$ ,  $-1/8 V_{nom}$  and 0, respectively with the voltage of  $C_{11}$  charged up to  $11/8 V_{nom}$ .

[0072] After this, the discharging process begins and the capacitors  $C_{21}$ ,  $C_{22}$ ,  $C_{23}$  are discharged down, flipped to a positive position and then discharged again while  $C_{11}$  is all the way discharged back to  $5/8 V_{nom}$ .

[0073] Referring to FIG. 11, the waveforms of the voltage of each capacitor during a charging period are shown. As described above, by changing the switch configurations appropriately as energy is delivered to and from the buffer port, the individual capacitors can charge over a wide range (from their initial voltages to rated voltages), while the voltage at the buffer port is maintained within a narrow range (within 12.5% of  $V_{nom}$ ). It can be shown that circuit 500 provides energy buffering of 71.1% of the peak energy storage rating of the capacitors, while providing a buffer port voltage,  $V_{bus}$ , that remains within  $\pm 12.5\%$  of a nominal bus voltage,  $V_{nom}$ . While the energy buffering ratio,  $\gamma_b$ , of the circuit 500 is lower than that of the circuit 400 (i.e., 1-3 unipolar SSC energy buffer), the bipolar SSC energy buffer circuit with a slightly modified control and design methodology (as described further herein) increases its energy buffering ratio,  $\gamma_b$ , to 74%.

[0074] Referring to FIG. 12, the circuit 500 can be extended by adding more capacitors to the first and second of circuitry, 502, 504 as in a circuit 500' called a n-m bipolar SSC energy buffer circuit. Note that the capacitor that does the energy buffering in the circuit 500 is the capacitor  $C_{11}$  in the second set of circuitry 504. Therefore, by replacing  $C_{11}$  alone with a plurality of "legs" in parallel, each "leg" comprising the series connection of a capacitor and switch, better buffering performance can be achieved.

[0075] The circuit 500' includes a first set of circuitry 502' and a second set of circuitry 504'. The first set of circuitry 502' includes capacitors  $C_{21}, C_{22}, \dots, C_{2m}$  (referred herein as m capacitors) and switches  $S_{21}, S_{22}, \dots, S_{2m}$  in series with a respective one capacitor, and the "legs" formed by each switch-capacitor pair in parallel. The first set of circuitry 502' also includes switches  $S_{h1}, S_{h2}, S_{h3}, S_{hn}$  (e.g., an H-bridge). The second set of circuitry 504 includes capacitors  $C_{11}, C_{12}, \dots, C_{1n}$  (referred herein as n capacitors) and switches  $S_{11}, S_{12}, \dots, S_{1n}$  in series with a respective one capacitor, and the "legs" formed by each switch-capacitor pair in parallel.

[0076] The m capacitors in the first set of circuitry 502 in this case have to switch at a higher switching frequency. The energy buffering ratio for this n-m bipolar SSC energy buffer (with n capacitors of equal value  $C_1$  and m capacitors with equal value  $C_2$ ) is given by:

$$\gamma_b = \frac{nC_1 \left[ \left( 1 + 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 - \left( 1 - 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 \right]}{nC_1 \left[ \left( 1 + 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 - C_2 (1 + 2^2 + \dots + m^2) R_v^2 \right]}$$

[0077] Referring to FIG. 13, the variation in energy buffering ratio,  $\gamma_b$ , as a function of the number of n capacitors and number of m capacitors is shown. FIG. 13 indicates that there is an optimal number of m capacitors that should be used for a given number of n capacitors in order to maximize the energy buffering ratio,  $\gamma_b$ . Note that this optimal number of m capacitors depends on the value of allowed voltage ripple ratio,  $R_v$ . In Fig. 13, the voltage ripple ratio,  $R_v$ , is 12.5%.

[0078] FIGS. 14A and 14B show how the optimal number of m capacitors changes as the allowed voltage ripple ratio,  $R_v$ , is changed. FIG. 14A has a voltage ripple ratio,  $R_v$ , of 25%. FIG. 14B has a voltage ripple ratio,  $R_v$ , of 6.25%. If a larger voltage ripple ratio,  $R_v$ , is allowed a higher energy buffering ratio,  $\gamma_b$ , can be achieved with fewer m capacitors. On the other hand, a lower voltage ripple,  $R_v$ , requires a larger number of m capacitors if maximum energy buffering is to be achieved. However, increasing the number of m capacitors

also increases the complexity of the circuit. Therefore the number of  $m$  capacitors to use can be determined by an appropriate trade-off between voltage variation and energy buffering ratio,  $\gamma_b$ .

[0079] Referring now to FIG. 15, one particular example of the circuit 500' is a circuit 500' where  $n=2$  and  $m=6$  also called a 2-6 bipolar stacked switched capacitor energy buffer circuit.

[0080] Exemplary circuit 500' includes a first block of parallel coupled switches and capacitors S11, C11, S12, C12 and a second block of parallel coupled switches and capacitors S21, C21, S22, C22, S23, C23, S24, C24, S25, C25, S26, C26. The first and second blocks are coupled in series across a bus voltage  $V_{bus}$ . Switches Sh1, Sh2, Sh3, Sh4 are disposed in the second block to provide selected signal paths between the first and second blocks.

[0081] As noted above, the capacitors are preferably of a type that can be efficiently charged and discharged over a wide voltage range (e.g., film capacitors). The switches are disposed to selectively couple the capacitors to enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to a buffer port. The switches are cooperatively operated as a switching network such that the voltage seen at the buffer port varies only over a small range as the capacitors charge and discharge over a wide range to buffer energy.

[0082] By appropriately modifying switch states of the SSC energy buffer circuit, the SSC energy buffer circuit absorbs and delivers energy over a wide individual voltage range, while maintaining a narrow-range voltage at the input port. This enables maximal utilization of the energy storage capability.

[0083] The waveforms associated with the circuit 500' are shown in FIG. 16.

[0084] Referring now to FIG. 16, a plot of switching states vs. voltage is shown for the circuit 500" (Fig. 15).

[0085] The bipolar stacked switched capacitor energy buffer circuit (e.g., the circuit 500') previously described can also be controlled in a slightly different manner. Instead of charging the n capacitors only in series with the m capacitors, a state can be introduced by turning S<sub>H3</sub> and S<sub>H4</sub> (or S<sub>H1</sub> and S<sub>H2</sub>) on at the same time in which the n capacitor is charged directly. An example of the modified control is shown in FIG. 5 for the circuit 300 (the 2-4 bipolar SSC energy buffer circuit) of FIG. 4. The modified control is described herein in the section entitled: "Enhanced Bipolar Stacked Switched Capacitor Energy Buffer". With this modified control, and assuming that all m and n capacitors have the same capacitance, the expression for energy buffering ratio,  $\gamma_b$  becomes:

$$\gamma_b = \frac{n[(1+(m+1)R_p)^2 - (1-(m+1)R_p)^2]}{n\{(1+(m+1)R_p)^2 - (2^2+3^2+\dots+(m+1)^2)R_p^2\}}$$

[0086] This is plotted as a function of number of n capacitors and number of m capacitors in FIG. 17. Figure 17 also plots (as dashed lines) the energy buffering ratio without modified control. The modified control achieves higher maximum energy buffering ratio than without the modified control. Furthermore, it achieves this higher maximum with fewer m capacitors than without modified control.

[0087] As discussed above, an SSC energy buffer has two series coupled blocks comprising capacitors and switches. It works on the principle that while the voltage of individual capacitors and the individual blocks can vary over a wide range, the voltage at the buffer port remains constrained to a desired narrow range by having the voltages of the two blocks compensate for each other. There are many possible implementations of the SSC energy buffer architecture. One implementation known as the n-m bipolar SSC energy buffer is described above in conjunction with Fig. 15 with n and m equal to 2 and 6, respectively. In this design all the capacitors have equal capacitance, but

different voltage ratings. Before the buffer starts normal operation the capacitors are precharged to specified initial levels using a precharge circuit. During normal operation, the buffer operates as depicted by the switching patterns and associated voltage waveforms shown in Fig. 15A. In each state, one backbone capacitor and one supporting capacitor are connected in series across the buffer port.

[0088] Important parameters of a switched capacitor energy buffer are the voltage ripple ratio  $R_v$  and the energy buffering ratio  $\Gamma_b$ . The voltage ripple ratio ( $R_v$ ) is defined as the ratio of the peak voltage ripple amplitude to the nominal value of the voltage. The energy buffering ratio ( $\Gamma_b$ ) is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer. Maximizing the energy buffering ratio for a given required voltage ripple ratio is desired because one can make better usage of a given amount of capacitor energy storage. A bipolar SSC energy buffer can be designed with any number of "backbone" capacitors in the lower block ( $n$ ) and any number of "supporting" capacitors in the upper block ( $m$ ). However, for a given voltage ripple ratio requirement and a given number of backbone capacitors there is an optimal number of supporting capacitors that yields the highest energy buffering ratio, and hence the highest effective energy density for the passive components. The energy buffering ratio ( $\Gamma_b$ ) for an  $n$ - $m$  bipolar SSC energy buffer is given by:

$$\Gamma_b = n(1 + mR_v)^2 - (1 - mR_v)^2 / [n(1 + mR_v)^2 + (1 + 2^2 + \dots + m^2)R_v^2] \quad \text{Eq. (10)}$$

[0089] For example, for a 10% bus voltage ripple ratio requirement and with 2 backbone capacitors, the optimal design of a bipolar SSC energy buffer is one with 6 supporting capacitors. This is evident from the plot of Fig. 17.

[0090] The  $n$ - $m$  bipolar SSC energy buffer can also be controlled in a slightly different manner so as to operate as an enhanced bipolar ssc energy buffer. Instead of charging the backbone capacitors only in series with the supporting capacitors, a state can be introduced by turning  $S_{n3}$  and  $S_{n4}$  (or  $S_{n1}$

and  $S_{h2}$ ) on at the same time in which the backbone capacitor is charged directly.

[0091] Referring now to Fig. 18, consider the 2-5 enhanced bipolar SSC energy buffer. Similar to the 2-6 bipolar SSC energy buffer of Fig. 15, the 2-5 enhanced bipolar SSC energy buffer of Fig. 18 is designed for a bus voltage ripple ratio of 10%. Its seven capacitors also have identical capacitance, but different voltage ratings. The pre-charge circuit (not shown in Figs. 15 or 18) ensures that the following initial voltages are placed on the seven capacitors:  $0.4V_{nom}$  on  $C_{11}$ ,  $0.4V_{nom}$  on  $C_{12}$ ,  $0.5V_{nom}$  on  $C_{21}$ ,  $0.4V_{nom}$  on  $C_{22}$ ,  $0.3V_{nom}$  on  $C_{23}$ ,  $0.2V_{nom}$  on  $C_{24}$ , and  $0.1V_{nom}$  on  $C_{25}$ .

[0092] When the energy buffer starts charging up from its minimum state of charge (as shown in Fig. 18A,  $S_{h1}$ ,  $S_{h4}$ ,  $S_{21}$  and  $S_{11}$  are turned on with all the other switches turned off. In this state,  $C_{11}$  and  $C_{21}$  are connected in series and charged until the bus voltage rises from  $0.9V_{nom}$  to  $1.1V_{nom}$ . At this instant the voltage of  $C_{21}$  ( $V_{21}$ ) reaches  $0.6V_{nom}$  and the voltage of  $C_{11}$  ( $V_{11}$ ) reaches  $0.5V_{nom}$ . Then  $S_{21}$  is turned off and  $S_{22}$  is turned on; and the bus voltage drops back down to  $0.9V_{nom}$ . Then, the voltage of  $C_{22}$  rises to  $0.5V_{nom}$  and the voltage of  $C_{11}$  reaches  $0.6V_{nom}$ , and the bus voltage again reaches  $1.1V_{nom}$ . Next,  $S_{22}$  is turned off,  $S_{23}$  is turned on and  $C_{23}$  is charged. This process is repeated until  $C_{25}$  is charged. This charging pattern is identical to the original 2-6 bipolar SSC energy buffer, as can be seen by comparing Figs. 15A and 18A. However, the next two states are different, instead of charging  $C_{11}$  in series with  $C_{26}$ ,  $C_{11}$  is charged directly by turning off  $S_{h1}$  and turning on  $S_{h3}$ . Hence, eliminating the need for capacitor  $C_{26}$  and switch  $S_{26}$  of the original design. This state is maintained until voltage of  $C_{11}$  rises to  $1.1V_{nom}$ . After this  $S_{h4}$  is turned off and  $S_{h2}$  and  $S_{25}$  are turned on. Now  $C_{11}$  can continue to charge up through the now reverse-connected supporting capacitors through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through  $C_{26}$ , then through  $C_{25}$ , and so on until finally through  $C_{21}$ .

[0093] At this stage  $C_{11}$  is fully charged to  $1.6V_{nom}$  and charging of  $C_{12}$  must begin. For this the h-bridge switches are again toggled (i.e.,  $S_{h3}$  and  $S_{h2}$  are turned off, and  $S_{h1}$  and  $S_{h4}$  are turned on),  $S_{11}$  is turned off and  $S_{12}$  is turned on. The charging process for  $C_{12}$  is identical to the charging process for  $C_{11}$ . The switch states, the capacitor voltages and the resulting bus voltages over a complete charge and discharge cycle are shown in Fig. 18A. During the discharge period, the capacitors  $C_{11}$  and  $C_{12}$  are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period.

[0094] Throughout the charging and discharging period of this energy buffer, the bus voltage stays within the  $0.9V_{nom}$ - $1.1V_{nom}$  range. Hence the enhanced 2-5 bipolar SSC energy buffer operated in this matter also has a voltage ripple ratio of 10%. Furthermore, it has an energy buffering ratio of 79.73% which is higher than the energy buffering ratio (79.6%) of the original 2-6 bipolar SSC energy buffer. The original 2-6 bipolar SSC energy buffer has 8 capacitors and 12 switches, while the enhanced 2-5 bipolar SSC energy buffer has 7 capacitors and 11 switches. Hence, the enhanced version achieves the same bus voltage ripple ratio and a slightly better energy buffering ratio with fewer capacitors and switches.

[0095] Assuming that all capacitors have the same capacitance, the energy buffering ratio ( $\Gamma_b$ ) for an enhanced  $n$ - $m$  bipolar SSC energy buffer is given by:

$$\Gamma_b = n[(1 + (m+1)R_v)^2 - (1 - (m+1)R_v)^2] / [n(1 + (m+1)R_v)^2 + (2^2 + 3^2 + \dots + m^2)R_v^2] \quad \text{Eq. (11)}$$

[0096] The energy buffering ratio for the enhanced bipolar SSC energy buffer is plotted as a function of the number of supporting capacitors ( $m$ ) for different number of backbone capacitors ( $n$ ) with 10% voltage ripple ratio in Fig. 17. Fig 17 also plots (as dashed lines) the energy buffering ratio of the original bipolar SSC energy buffer (as given by Eq. (10)). As can be seen from Fig. 17,

the enhanced design achieves a slightly higher maximum energy buffering ratio than the original design. Furthermore, it achieves this higher maximum with fewer supporting capacitors than the original design.

[0097] An exemplary 2-5 enhanced bipolar SSC energy buffer circuit was built and tested with a power factor correction (PFC) circuit powering a dc load. The SSC energy buffer replaces the electrolytic capacitor normally connected at the output of the PFC, as shown in Fig. 3A. The SSC energy buffer is designed to meet a 10% bus voltage ripple ratio requirement on a 320V dc bus with a maximum load of 135W.

[0098] The measured waveforms from the 2-5 enhanced bipolar SSC energy buffer are shown in Fig. 19. Clearly, the enhanced SSC energy buffer maintains the bus voltage within the  $\pm 10\%$  specified range. The roundtrip efficiency of the 2-5 enhanced bipolar SSC energy buffer across a wide load range was also measured and this data is plotted in Fig. 20.

[0099] Fig. 20 also plots the measured roundtrip efficiency of the original 2-6 bipolar SSC energy buffer. As can be seen, the enhanced version has 1% higher roundtrip efficiency. This represents a 20-25% reduction in loss as compared to the original design. The full paper will also provide a more detailed experimental evaluation of the approach.

[00100] A stacked switched capacitor (SSC) architecture for dc-link energy buffering applications, including buffering between single-phase ac and dc has been described. This architecture utilizes the energy storage capability of capacitors more effectively than previous designs, while maintaining the bus voltage within a narrow range. This enables the energy buffer to achieve higher effective energy density and reduce the volume of the capacitors. A prototype 2-6 bipolar SSC energy buffer using film capacitors designed for a 320 V bus with 10% voltage ripple and able to support a 135 W load was built and tested and it is shown that the SSC energy buffer can successfully replace limited-life

electrolytic capacitors with much longer life film capacitors, while maintaining volume and efficiency at a comparable level.

[00101] Also described is an enhanced version of the SSC energy buffer which modifies the control and switching pattern of the buffer switches to yield improved performance. A prototype enhanced SSC energy buffer, designed for a 320V bus and a 135W load, was built and tested. The design rules and experimental results for the enhanced SSC energy buffer are also described. It is shown that the enhanced SSC energy buffer achieves a relatively high effective energy density and round-trip efficiency compared with other designs, while maintaining the same bus voltage ripple ratio. Furthermore, the enhanced design uses fewer capacitors and switches than other designs.

[00102] The techniques described herein are not limited to the specific embodiments described. Elements of different embodiments described herein may be combined to form other embodiments not specifically set forth above. Other embodiments not specifically described herein are also within the scope of the following claims.

[00103] What is claimed is:

1. A stacked switched capacitor (SSC) energy buffer circuit comprising:  
two sub-circuits that are serially coupled during a first operating mode wherein each sub-circuit comprises one or more capacitors, and at least one sub-circuit further comprises a plurality of switches disposed to selectively couple the capacitors to: (a) enable dynamic reconfiguration of how the capacitors are coupled to the terminals of the sub-circuit; and (b) dynamically reconfigure the interconnection among the capacitors within the sub-circuit.
2. The SSC energy buffer circuit of claim 1 wherein the switches in at least one of the two sub-circuits are arranged to dynamically reconfigure a polarity with which at least one capacitor is connected to the terminals of the sub-circuit.
3. The SSC energy buffer circuit of claim 1, further comprising a pre-charge circuit coupled to each of the two sub-circuits said pre-charge circuit operable to charge each of the one or more capacitors in the two sub-circuits to specified initial conditions before entering the first operating mode.
4. The SSC energy buffer circuit of claim 1 wherein at least one subcircuit comprises a plurality of sub-sub-circuits connected in parallel, wherein each sub-sub-circuit comprises a switch serially coupled to a capacitor.
5. The SSC energy buffer circuit of claim 1 wherein the peak energy buffered one of the two sub-circuits is greater than 66% of the total peak energy buffering capability.
6. The SSC energy buffer circuit of claim 1 wherein the capacitors in at least one of the two sub-circuits are of a type that can be efficiently charged and discharged over a wide voltage range.
7. The SSC energy buffer circuit of claim 1 wherein the capacitors in at least one of the first and second blocks are provided as: one of film capacitors, ultra capacitors and electrolytic capacitors.

8. The SSC energy buffer circuit of claim 1 wherein the switches are disposed to selectively couple the capacitors to enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to a buffer port.

9. The SSC energy buffer circuit of claim 1 wherein the switches are cooperatively operated as a switching network such that the voltage seen at a buffer port varies only over a small range as the capacitors charge and discharge over a wide voltage range to buffer energy.

10. A circuit comprising:  
a first set of circuitry comprising:  
m capacitors; and  
m switches, each m switch serially coupled to a corresponding one of the m capacitors; and  
a second set of circuitry comprising:  
n capacitors; and  
n switches, each n switch serially coupled to a corresponding one of the n capacitors;  
wherein a voltage across the first set of circuitry and the second set of circuitry is a bus voltage,  
wherein the circuit is configured to maintain the bus voltage within a predetermined range of a nominal value, and  
wherein n and m are integers greater than zero.

11. The circuit of claim 10 wherein the first set of circuitry includes an H-bridge switch and wherein said H-bridge switch is disposed to allow at least some of said m capacitors to be charged in a bipolar fashion.

12. The circuit of claim 10 wherein  $n = 2$  and  $m = 4$ , and wherein the circuit has an energy buffering ratio,  $\gamma_b$  of 81.6%.

13. The circuit of claim 10 wherein  $n = 1$  and  $m = 3$ , and

wherein the circuit has an energy buffering ratio of:

$$\gamma_b = \frac{nC_1 \left[ \left( 1 + 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 - \left( 1 - 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 \right]}{nC_1 \left[ \left( 1 + 2mR_v \frac{C_2}{C_1 + C_2} \right)^2 - C_2 (1 + 2^2 + \dots + m^2) R_v^2 \right]}$$

where  $R_v$  is the voltage ripple ratio,  $C_1$  is the capacitance of the  $n$  capacitor and  $C_2$  is the capacitance of one of the  $m$  capacitors which are equal in capacitance.

14. The circuit of claim 10 wherein the circuit has an energy buffering ratio of:

$$\gamma_b = \frac{n \left[ (1 + (m + 1)R_v)^2 - (1 - (m + 1)R_v)^2 \right]}{n \left[ (1 + (m + 1)R_v)^2 - (2^2 + 3^2 + \dots + (m + 1)^2) R_v^2 \right]}$$

where  $R_v$  is the voltage ripple ratio,  $C_1$  the capacitance of the  $n$  and  $m$  capacitors are equal.

15. The circuit of claim 10 wherein the  $m$  and  $n$  capacitors are film capacitors.

16. The circuit of claim 10 wherein the  $m$  capacitors have the same capacitance.

17. The circuit of claim 10 wherein the  $n$  capacitors have the same capacitance.

18. The circuit of claim 10 wherein the  $m$  and  $n$  capacitors have the same capacitance.

19. The circuit of claim 10, further comprising a switch coupled to said  $m$  capacitors, and wherein  $m = 3$  and  $n = 1$ , and wherein the circuit has an energy buffering ratio,  $\gamma_b$  of about 72.7%.

20. The circuit of claim 10 wherein  $n = 1$ , and wherein an energy buffering ratio is equal to:

$$\gamma_b = \frac{[(1 + R_v)^2 - (1 - mR_v)^2] C_1 + (mR_v)^2}{C_1 (1 + R_v)^2 + C_2 (1 + 2^2 + \dots + m^2) R_v^2}$$

where  $R_v$  is the voltage ripple ratio,  $C_1$  is the capacitance of the  $n$  capacitor and  $C_2$  is the capacitance of one of the  $m$  capacitors which are equal in capacitance.

21. A grid interface power converter system comprising:  
a stacked switched capacitor (SSC) energy buffer circuit coupled between a DC-DC converter and an AC-DC converter, said stacked switched capacitor (SSC) energy buffer circuit comprising:

two sub-circuits that serially coupled during a first operating mode wherein each sub-circuit comprises one or more capacitors, and at least one sub-circuit further comprises a plurality of switches disposed to selectively couple the capacitors to: (a) enable dynamic reconfiguration of how the capacitors are coupled to the terminals of the subcircuit; and (b) dynamically reconfigure the interconnection among the capacitors within the subcircuit.

22. The circuit of claim 21 said SSC energy buffer circuit comprises:

a first set of circuitry comprising:

$m$  capacitors; and

$m$  switches, each  $m$  switch serially coupled to a corresponding one of the  $m$  capacitors; and

a second set of circuitry comprising:

$n$  capacitors; and

$n$  switches, each  $n$  switch in series with a corresponding one of the  $n$  capacitors;

wherein a voltage across the first set of circuitry and the second set of circuitry is a bus voltage.

23. The circuit of claim 21 wherein the SSC energy buffer circuit is configured to maintain the bus voltage within  $\pm 12.5\%$  of a nominal value.

24. The SSC energy buffer circuit of claim 21 wherein the switches in at least one of the two sub-circuits are arranged to dynamically reconfigure a polarity with which at least one capacitor is connected to the terminals of the sub-circuit.

25. The SSC energy buffer circuit of claim 21, further comprising a pre-charge circuit coupled to each of the two sub-circuits said pre-charge circuit operable to charge each of the one or more capacitors in the two sub-circuits to specified initial conditions before entering the first operating mode.

26. The SSC energy buffer circuit of claim 21 wherein at least one subcircuit comprises a plurality of sub-sub-circuits connected in parallel, wherein each sub-sub-circuit comprises a switch serially coupled to a capacitor.

27. The SSC energy buffer circuit of claim 21 wherein the peak energy storage capability of one of the two sub-circuits is greater than 66% of the total peak energy storage capability.

28. A stacked switched capacitor (SSC) energy buffer circuit having first and second terminals, the SSC energy buffer circuit comprising:

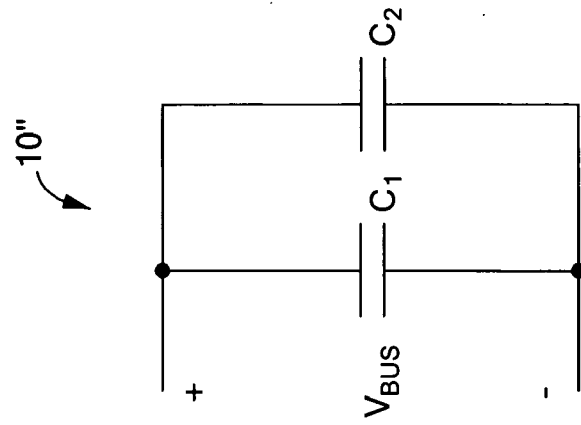
a first sub-circuit comprising one or more capacitors;

a second sub-circuit comprising one or more capacitors; and

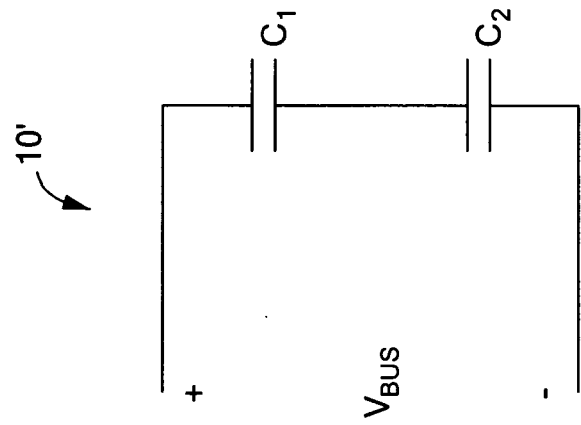
one or more switches disposed in at least one of said first and second sub-circuits to selectively couple said one or more capacitors and wherein said first and second sub-circuits are serially coupled during a first operating mode and wherein said one or more switches are operable to enable dynamic reconfiguration of how the capacitors are coupled to the terminals of the sub-circuit;

29. The SSC energy buffer circuit of claim 28 wherein said one or more switches are operable to dynamically reconfigure the interconnection among the capacitors within at least one of said first and second sub-circuits.

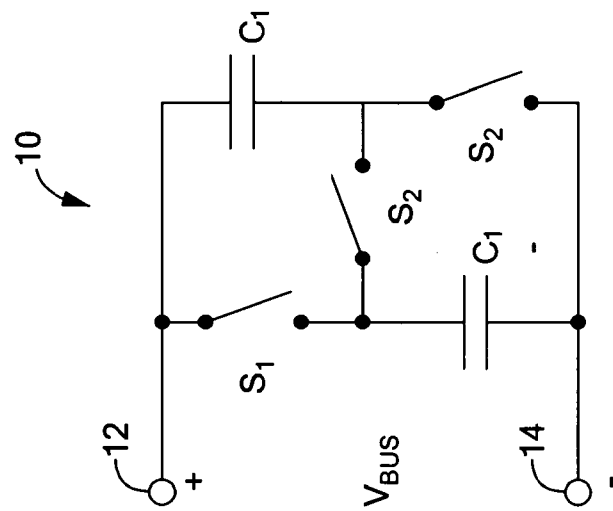
30. The SSC energy buffer circuit of claim 29 wherein in at least some operating modes, said one or more switches are operable to prevent the capacitors from ever being connected together at both terminals.



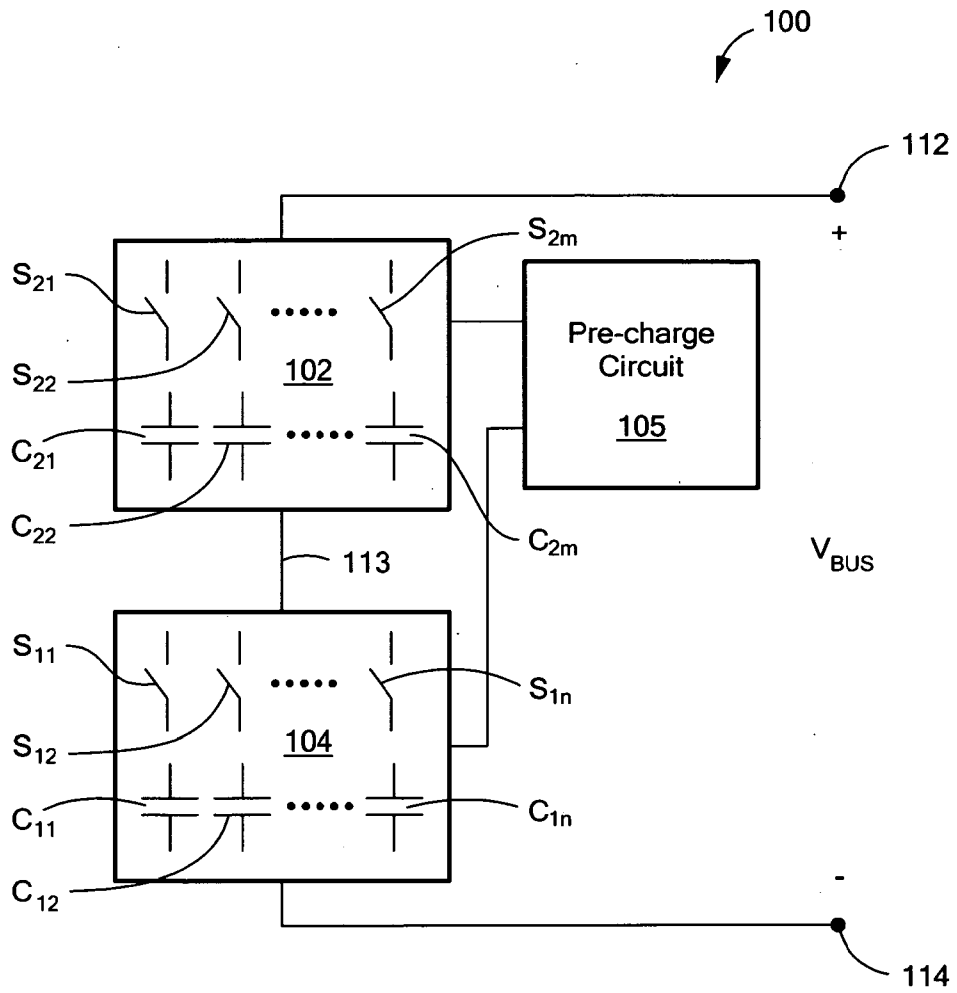
**FIG. 1C**



**FIG. 1B**



**FIG. 1A**



**FIG. 2**

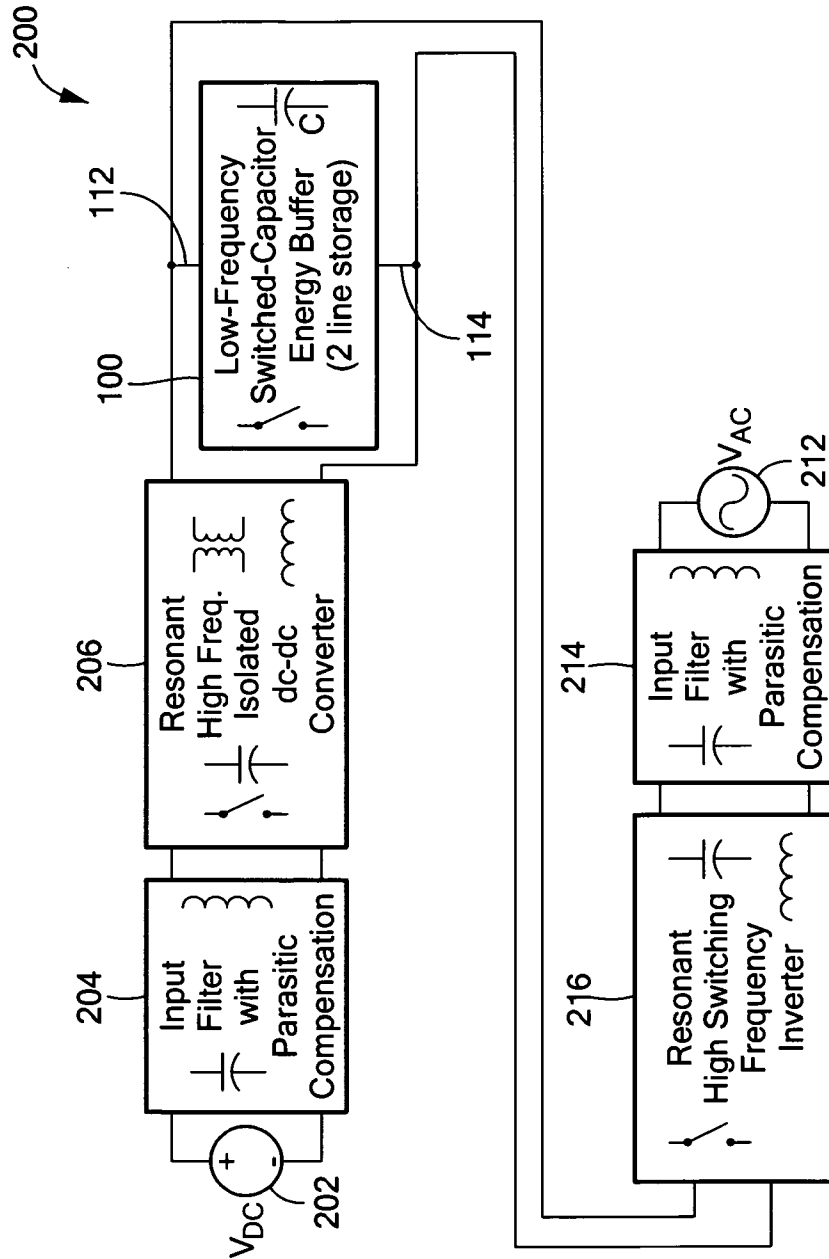
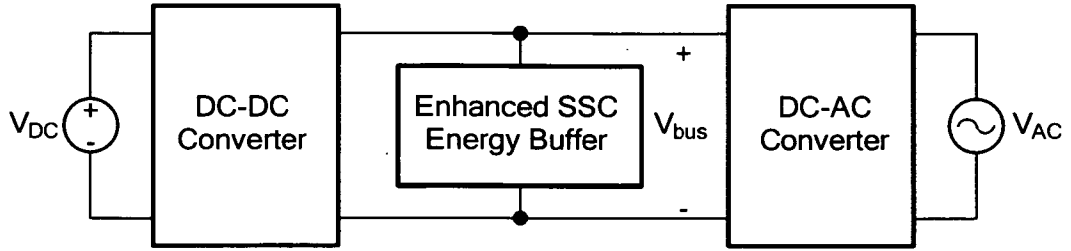
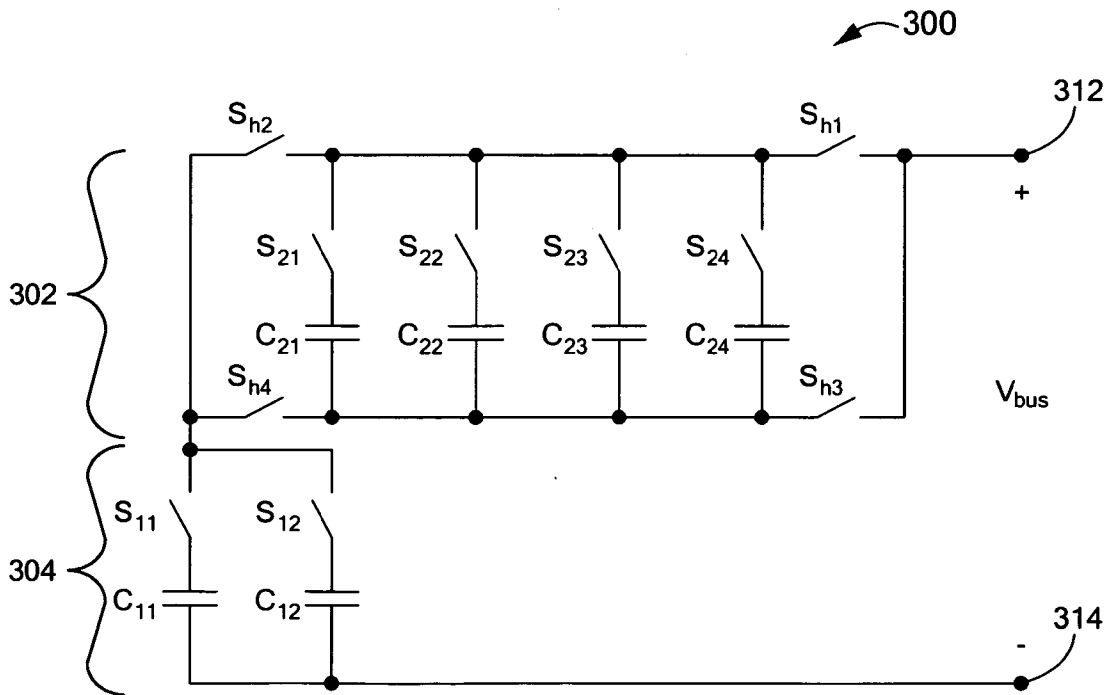


FIG. 3



**FIG. 3A**



**FIG. 4**

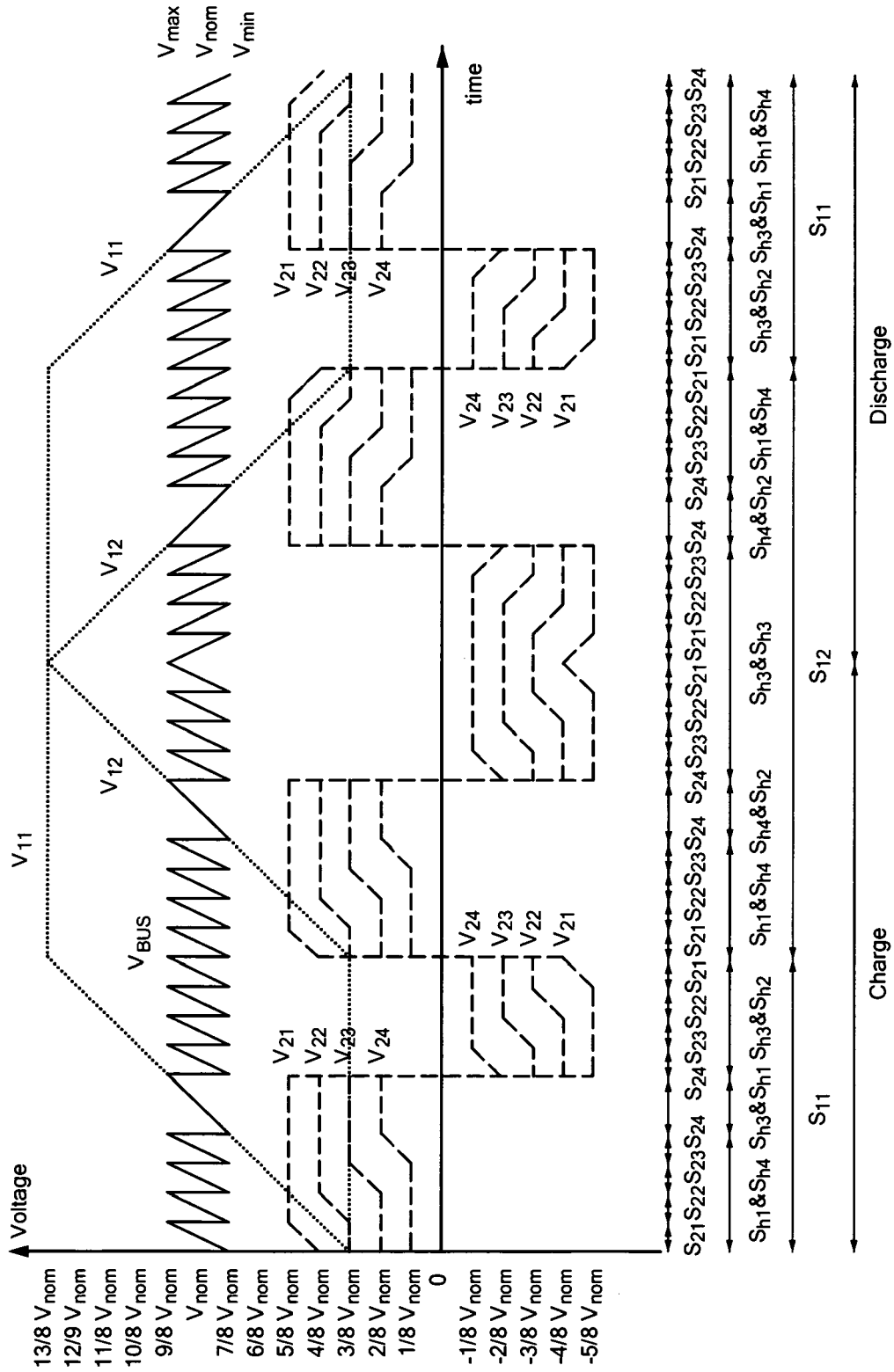


FIG. 5

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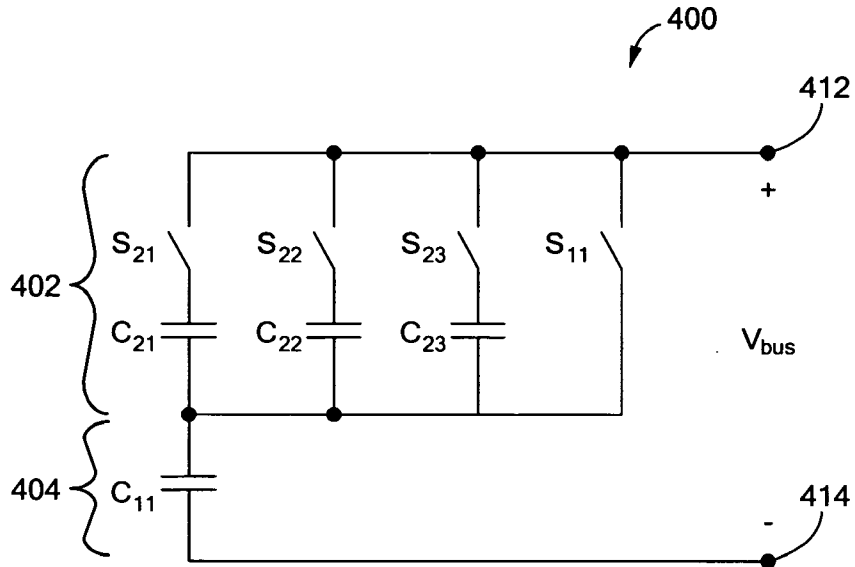


FIG. 6

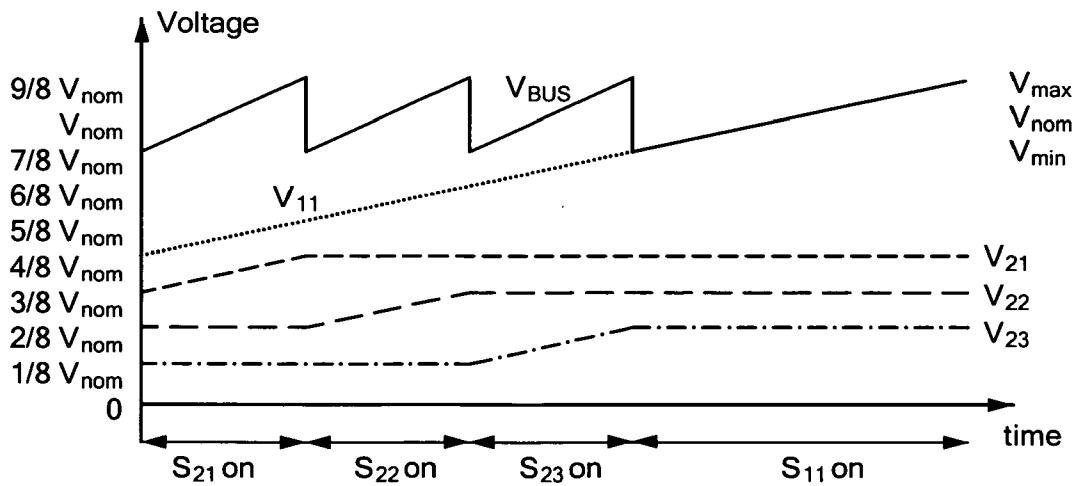
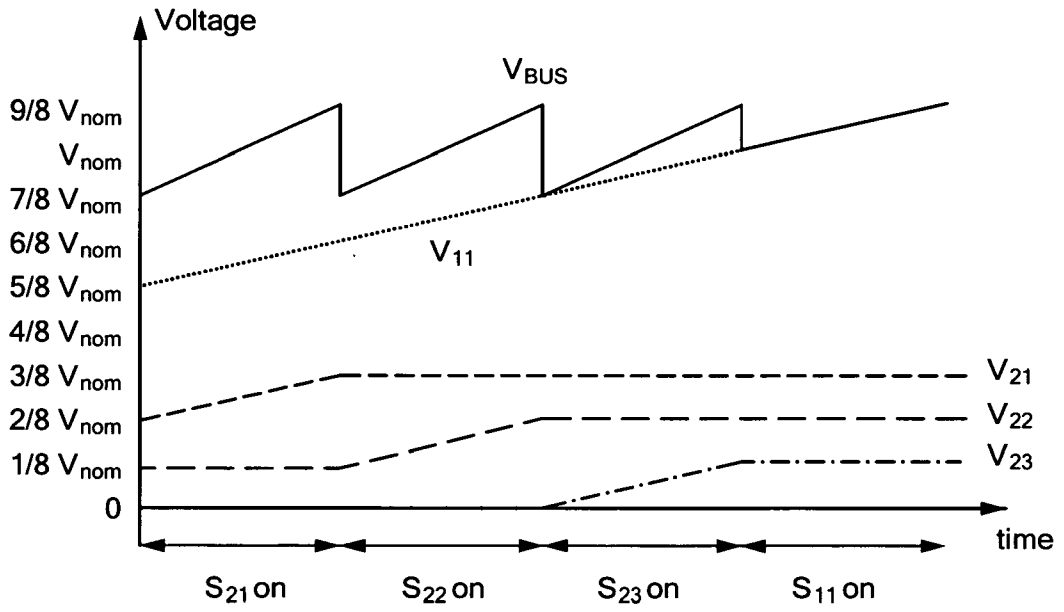


FIG. 7



**FIG. 8**

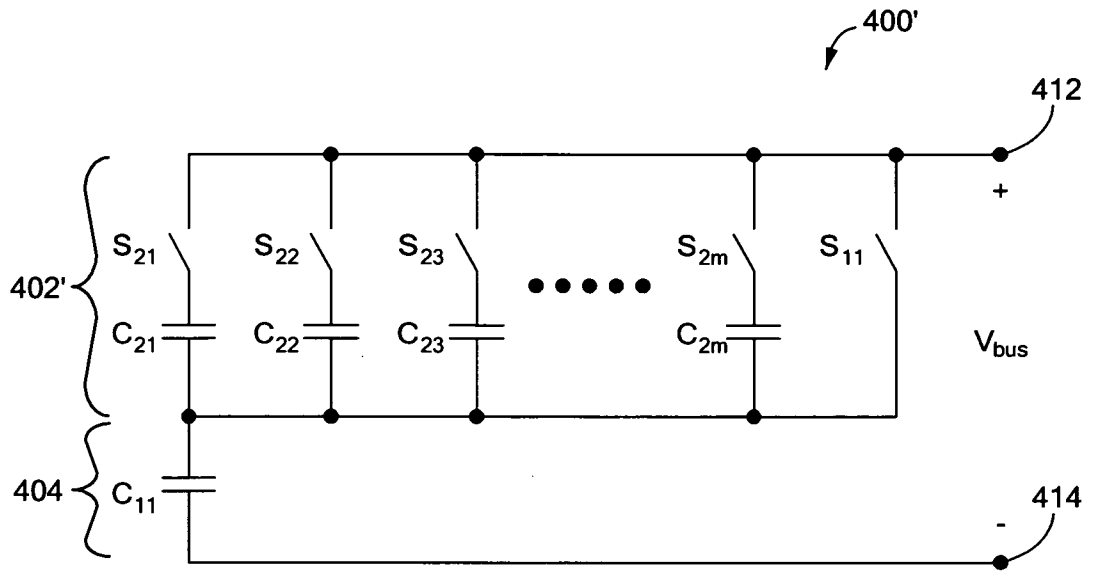


FIG. 9

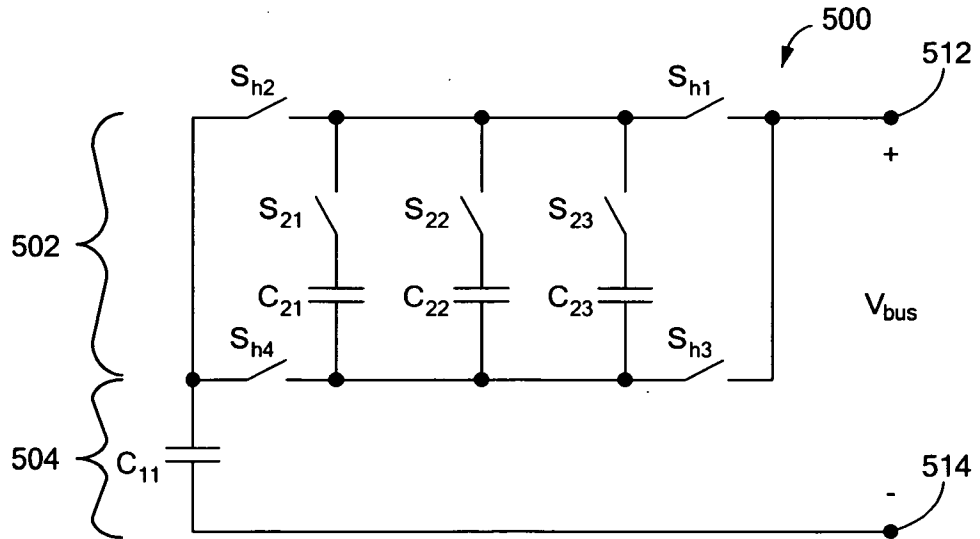


FIG. 10

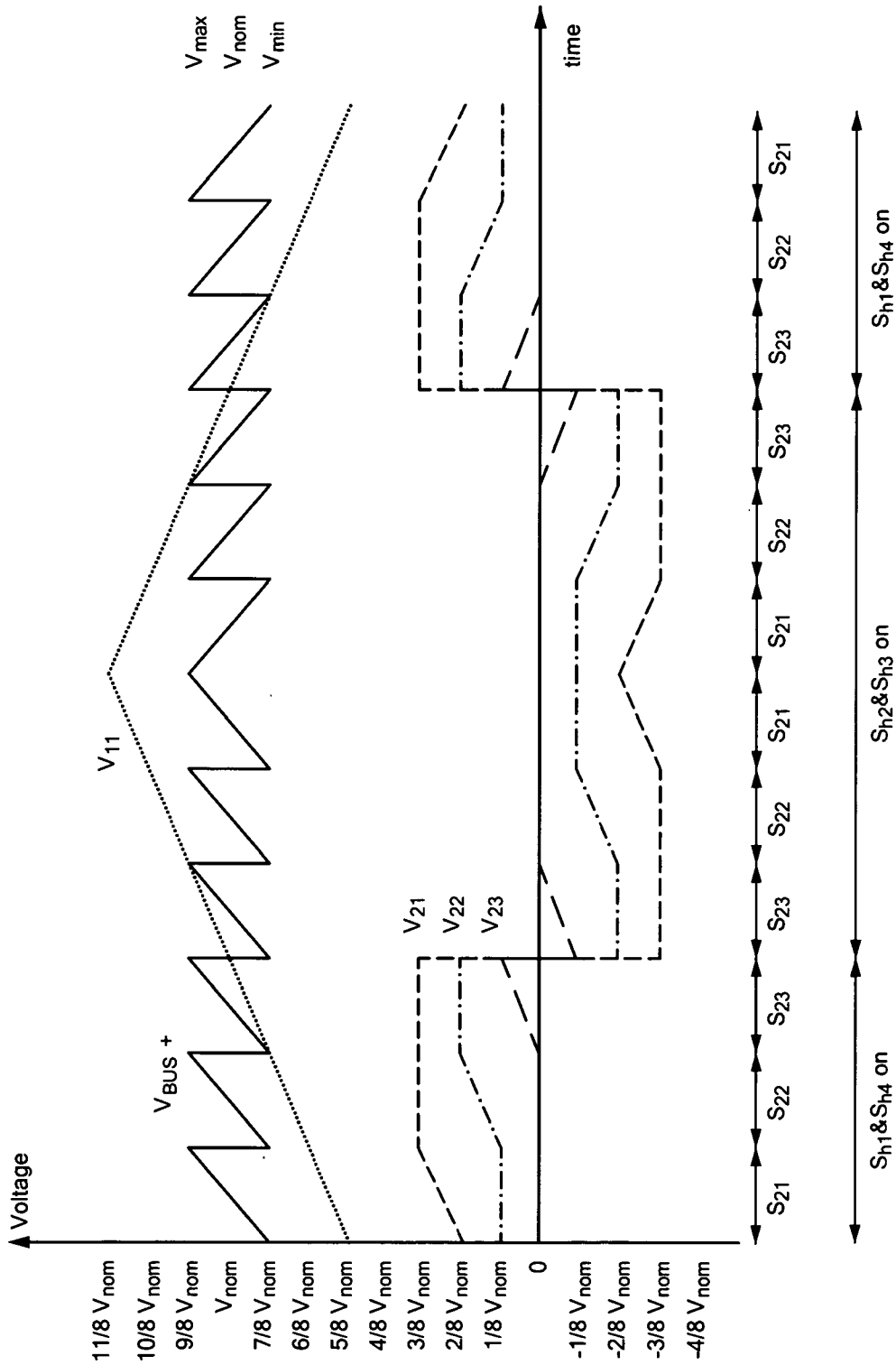


FIG. 11

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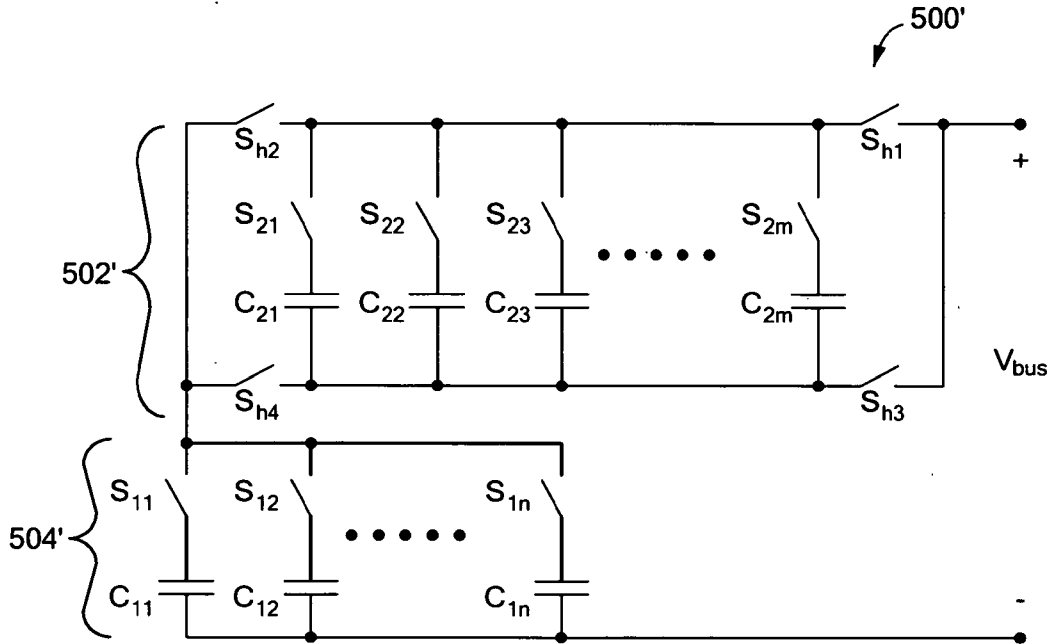


FIG. 12

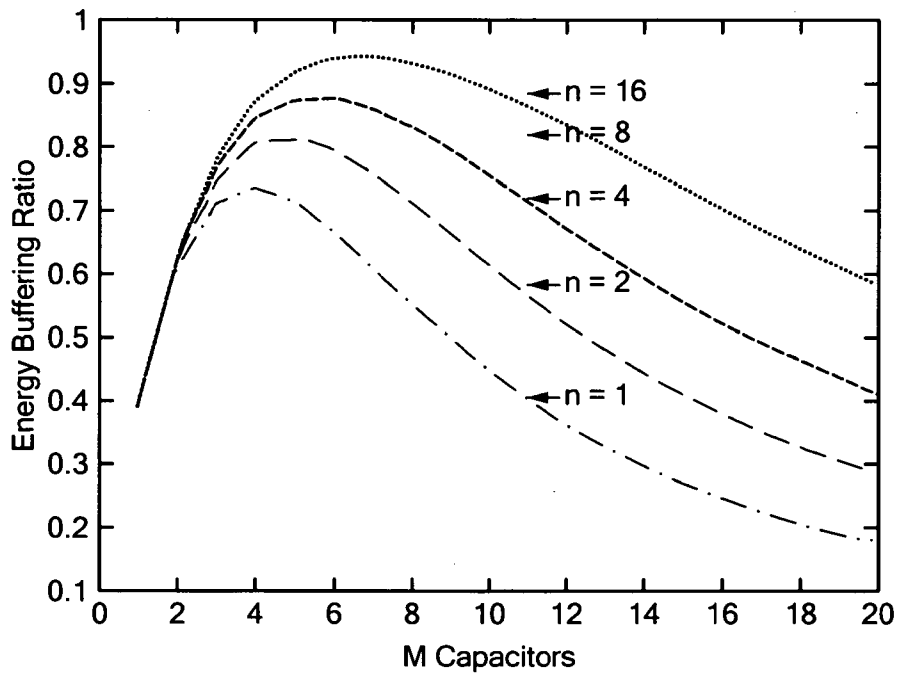
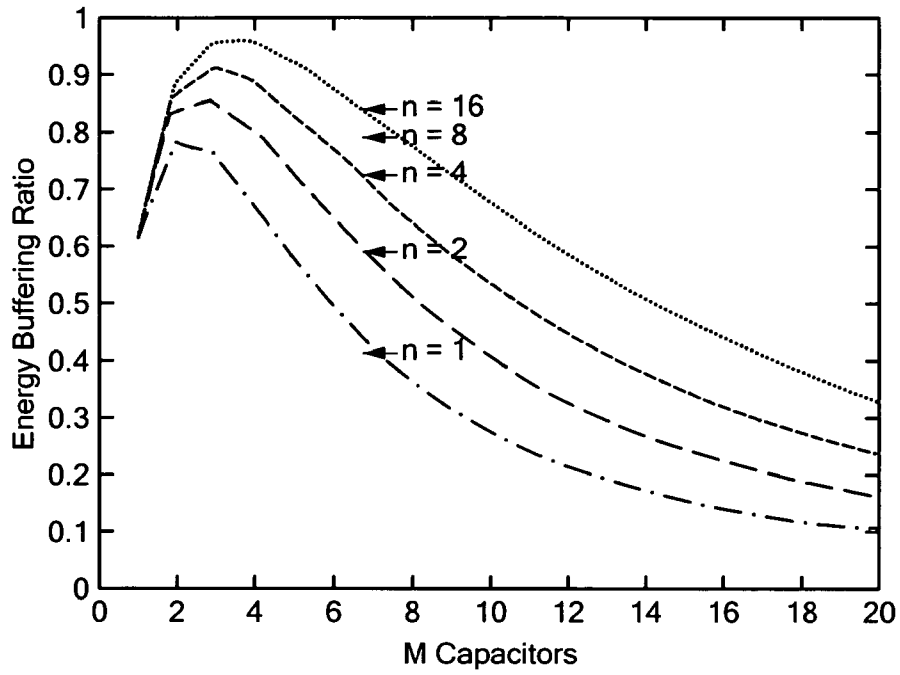
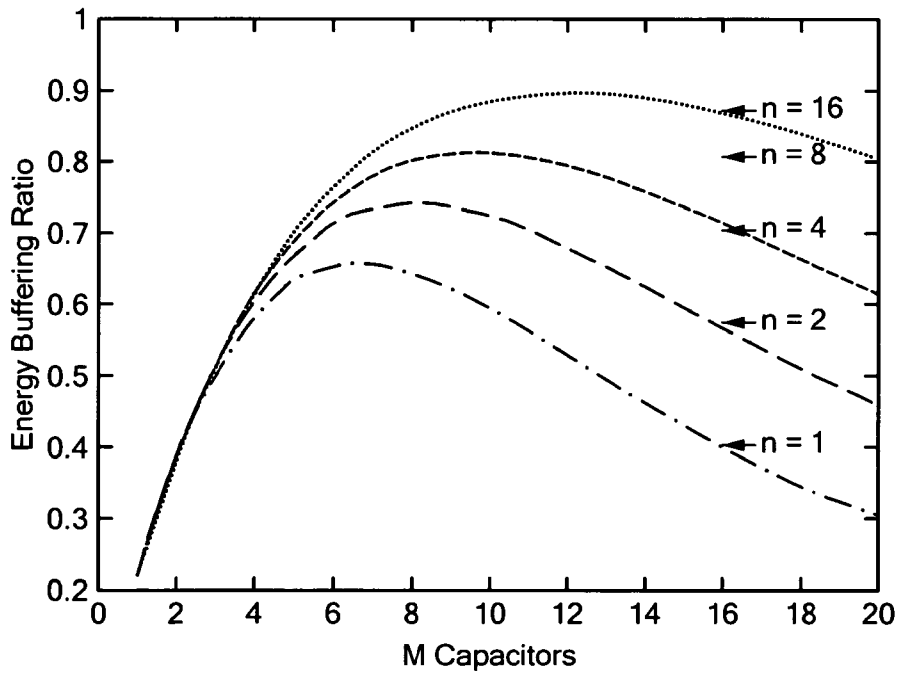


FIG. 13

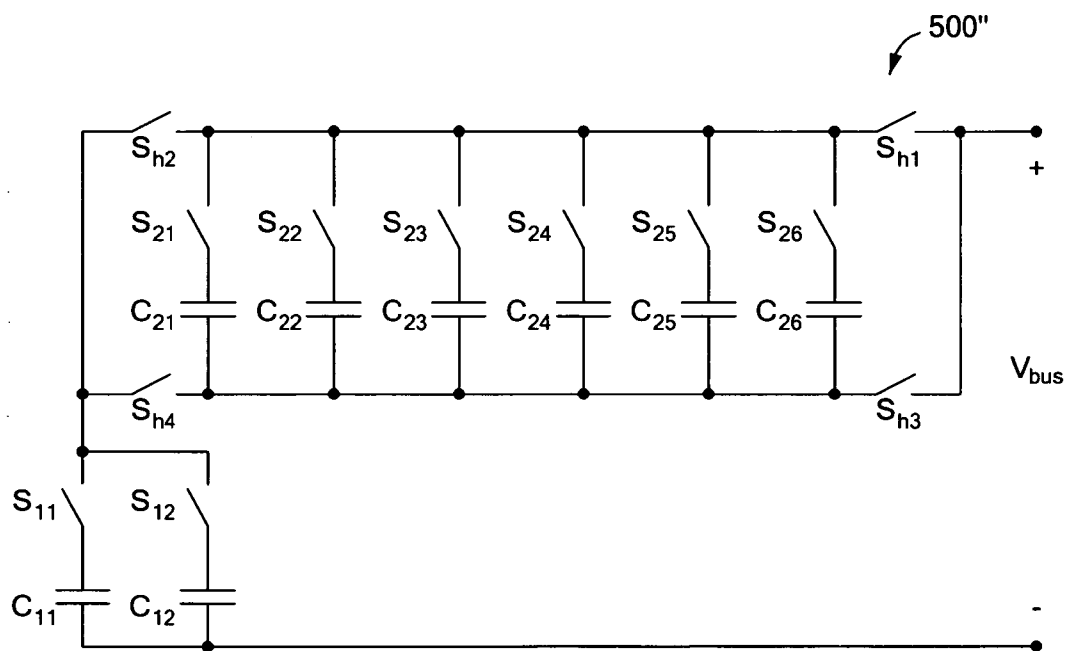
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**FIG. 14A**



**FIG. 14B**



**FIG. 15**



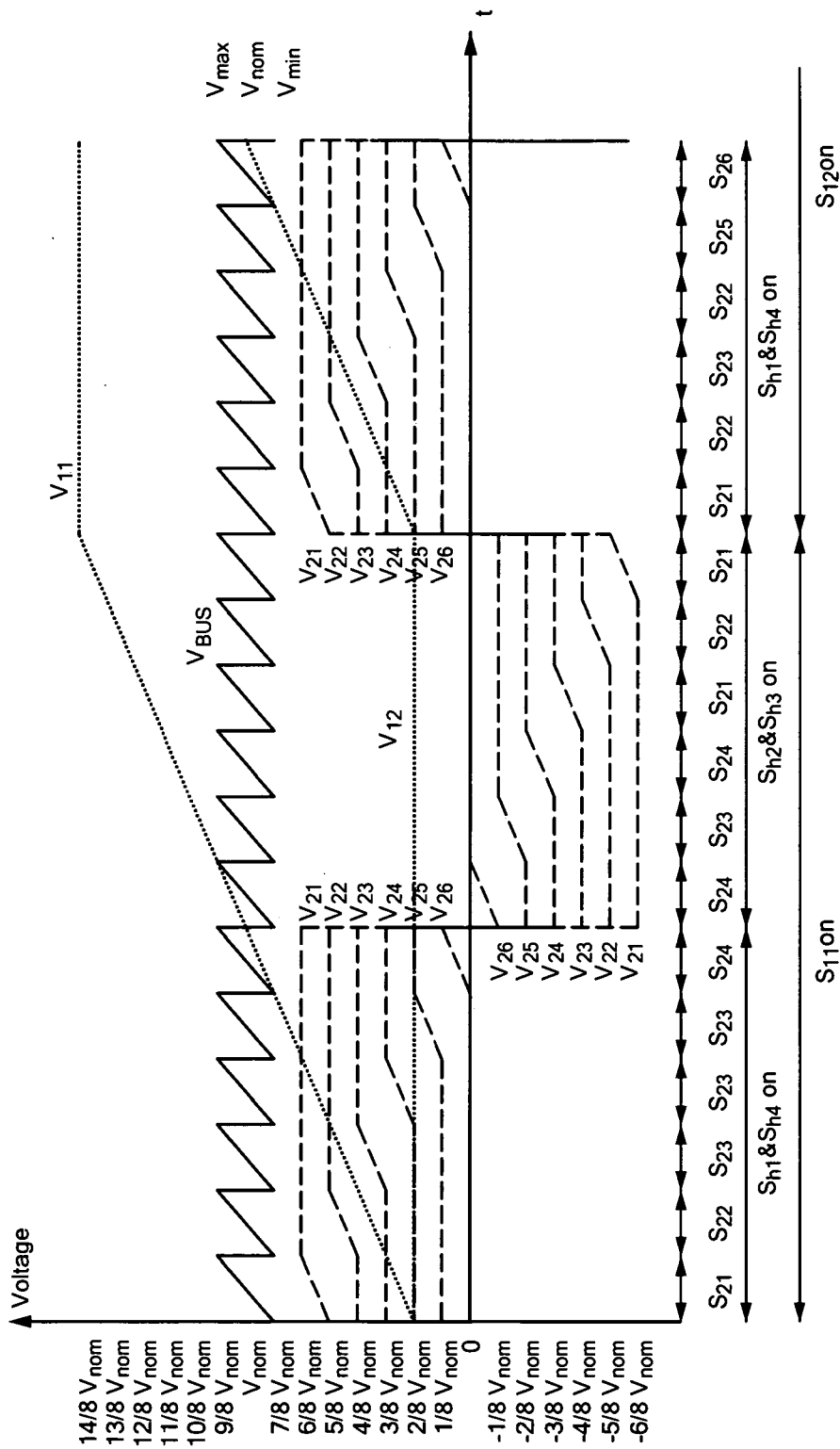


FIG. 16

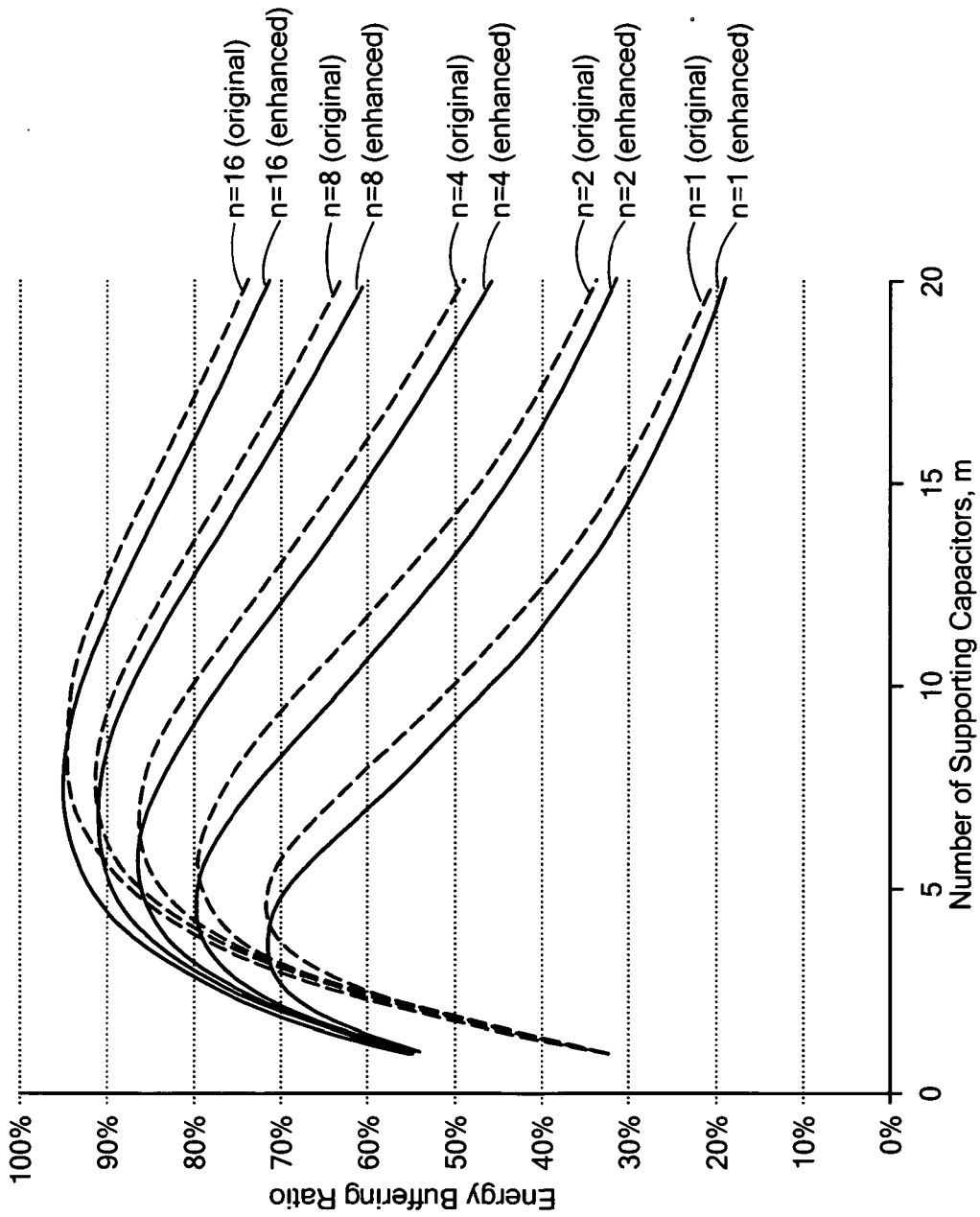
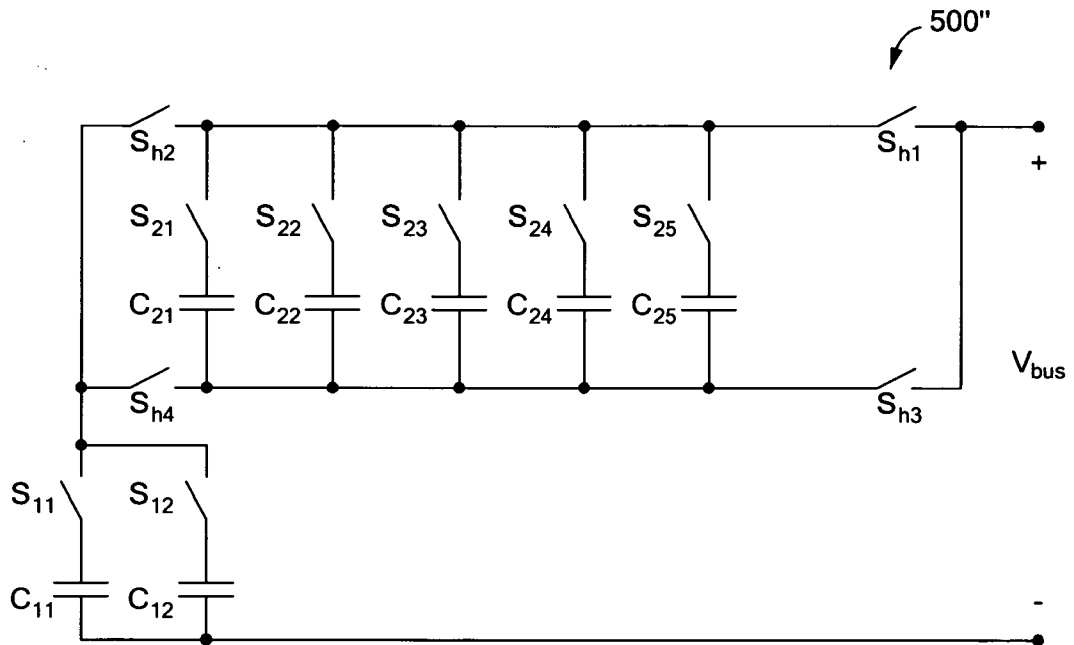


FIG. 17



**FIG. 18**

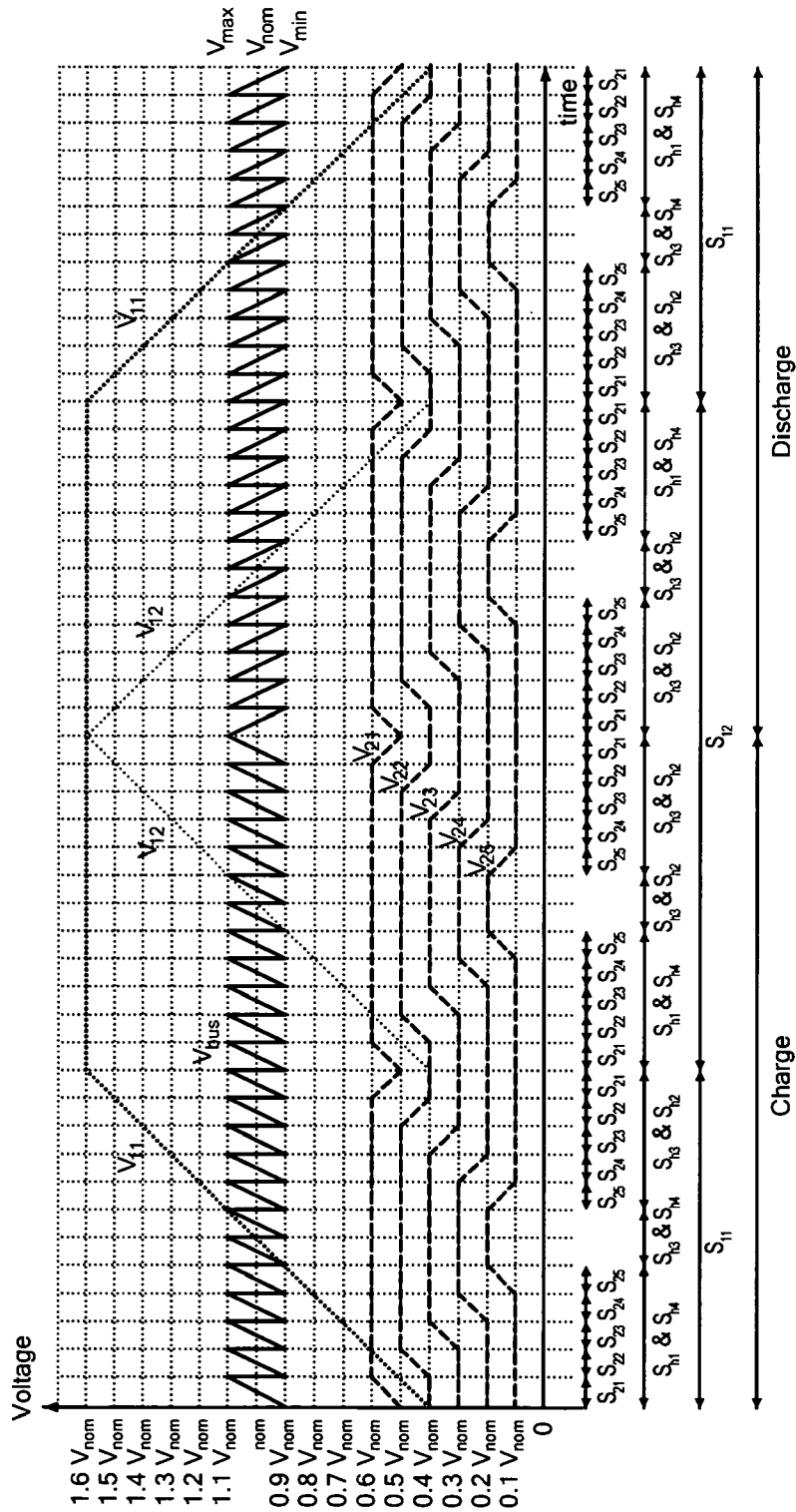
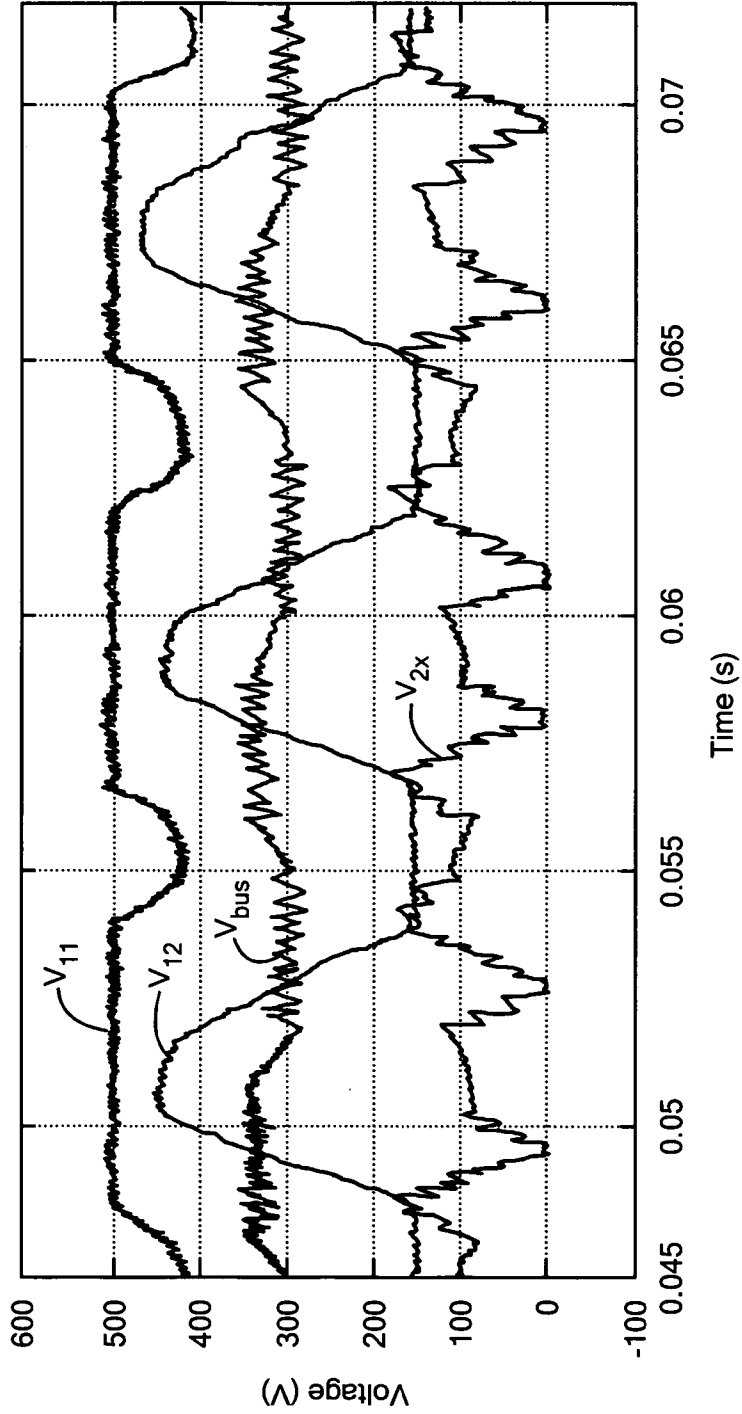


FIG. 18A



**FIG. 19**

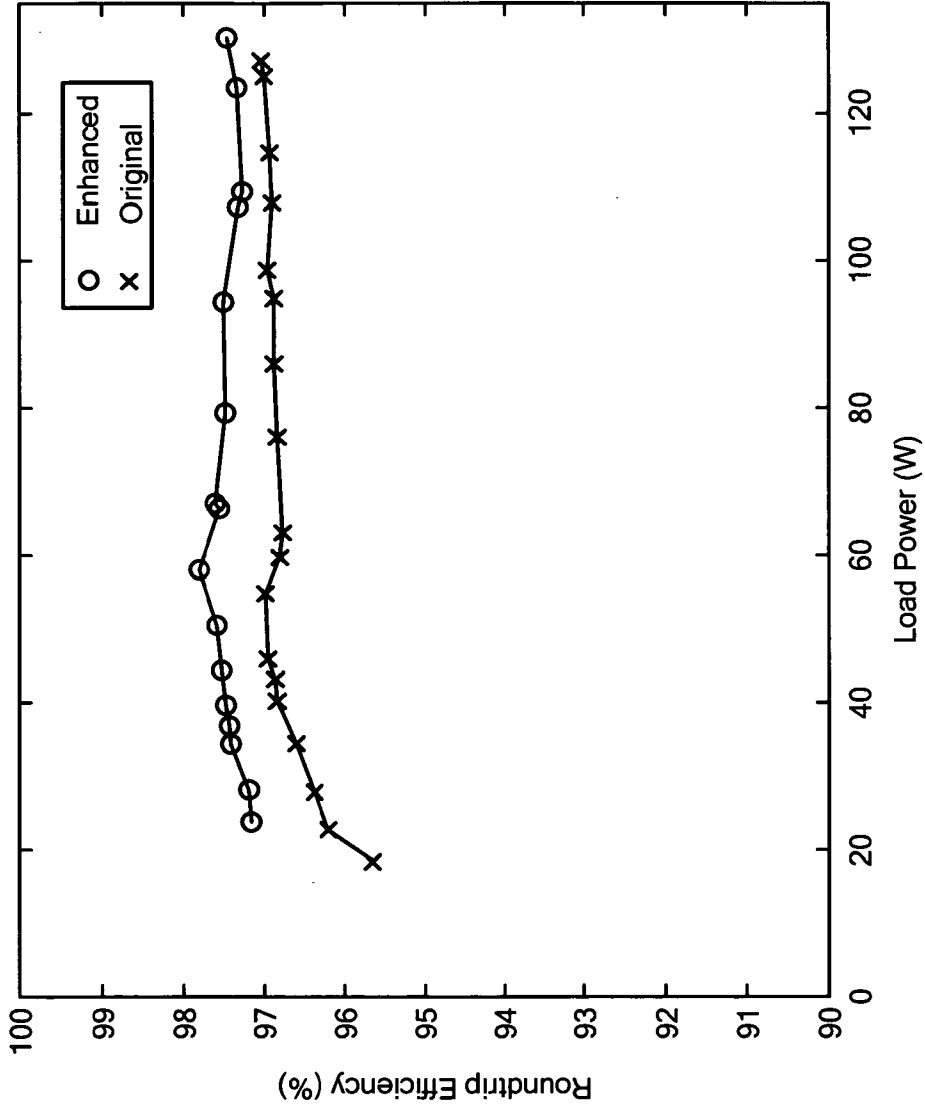


FIG. 20

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US 13/22001

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC(8) - H01G 4/30 (2013.01) USPC - 361/301.4 According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) USPC: 361/301.4		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched USPC: 361/500, 502, 522, 523, 301.1, 301.4; 362/81, 83, 86, 87; 327/524, 541, 100, 108, 109 (keyword limited - see search terms below)		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatBase; Google; Google Scholar Terms: converter, conversion, power, ac, dc, capacitor, switch, transistor, stacked, energy, buffer, storage, bridge, voltage, charge, discharge, efficiency, ratio, capacity, peak, maximum, density, node, reconfigure, select, film, ultra, ripple.		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y --- A	US 2009/0059630 A1 (Williams) 05 March 2009 (05.03.2009), entire document, especially abstract, Figs. 5C, 13A, para [0051], [0053], [0054], [0070], [0146], [0160], [0204], [0205], [0240], [0241], [0270].	1-12, 15-19, 21-30 ----- 13-14, 20
Y --- A	US 2005/0162144 A1 (Kernahan) 28 July 2005 (28.07.2005), entire document, especially abstract, para [0003], [0004], [0283], [0284]	1-12, 15-19, 21-30 ----- 13-14, 20
Y	US 2004/0125618 A1 (De Rooij et al.) 01 July 2004 (01.07.2004), entire document, especially abstract, para [0001], [0002], [0025].	7, 15
A	US 2008/0265586 A1 (Like et al.) 30 October 2008 (30.10.2008), entire document.	1-30
A	US 2011/0026281 A1 (Chapman et al.) 03 February 2011 (03.02.2011), entire document.	1-30
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/>		
* Special categories of cited documents:		
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family	
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search 08 April 2013 (08.04.2013)	Date of mailing of the international search report <div style="font-size: 24pt; font-weight: bold; text-align: center;">03 MAY 2013</div>	
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: <div style="text-align: right;">Lee W. Young</div> PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774	