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(54) CHARGE-COUPLED DEVICE

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94042, United States of America, a corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a charge-coupled device (often referred to as a CCD) having at least one semiconductor cell.

Charge-coupled devices are well known in the integrated circuit arts. As gate structures, they operate to move charge in a semiconductor material in response to application of selected potentials to various electrodes disposed near the semiconductor materials. The direction of charge movement is controlled by barriers implanted in the semiconductor material beneath portions of the electrodes. The theory of operation, manner of fabrication, and the resulting structures of CCD devices have been the subject of various patents, for example, U.S. Patent 3,931,674 entitled "Self Aligned CCD Element Including Two Levels of Electrodes and Method of Manufacture Therefore."

A conventional CCD gate structure is shown in Fig. 1 of the drawings accompanying the present specification. The device includes a wafer 11; implanted barriers 12a, 12b, 12c, and 12d, insulating layers 15, 16, 21a, 21b, and 21c; and electrically conductive regions 18a, 18b, 18c, 28a, 28b, 28c and 28d. In a typical two-phase CCD gate structure, conductive region 18a and 28b will be electrically connected to form a first two-phase gate and region 18b will be electrically connected to region 28c to form a second two-phase gate. Similarly, regions 18c and 28d will be connected to form a first gate of an adjacent structure.

The structural design and manner of fabrication of the CCD gate structure shown in Fig. 1 impose what have now been discovered to be unnecessary limitations upon the minimum size such CCD structures may occupy. The compactness of CCD structures in particular, and integrated circuits in general, is limited by, among other things, the alignment and etching tolerances of existing masking technology. Such tolerances normally expressed as one set of "design rules", in effect mandate some minimum separation between any two noncontiguous regions of a given structure which are not to be electrically connected. For example, utilizing a "three micron design rule" a two-phase CCD gate cell such as that shown in Fig 1 will typically consume approximately 20 microns of wafer surface. This results from the necessity of separating the edges of each electrode from an adjacent but non-contiguous electrode formed during the same process step by the amount of whatever design rule is invoked in the example, three microns. Thus, the left edge of electrode 28d must be situated at least three microns from the right edge of electrode 28c, as in conventional structures these are formed in the same process step and must not be electrically connected. Additionally, it is well known to those skilled in the semiconductor arts that the same or other sets of "design rules" will influence other aspects of the semiconductor structure. That is, certain design rules are applied to insure the formation of the structure shown in Fig. 1 without gaps, for example, so electrode 28b is disposed over barrier 12b.

The present invention accordingly provides a charge-coupled device having at least one semiconductor cell, the cell comprising

a layer of an insulating material on a surface of a semiconductor substrate;

two barrier regions formed in the substrate adjacent to the layer of insulating material, each barrier region having a dopant concentration different from that of the substrate;

two regions of a first electrically conductive material disposed on the layer of the insulating material except on those portions thereof over the barrier regions;

a region of second electrically conductive material disposed on that portion of the layer of the insulating material over one of the barrier regions and overlying selected portions of the regions of the first electrically conductive material;

a region of third electrically conductive material disposed on that portion of the layer of the insulating material over the other of the barrier regions and overlying selected portions of the regions of the first and second electrically conductive material; and

means electrically connecting together selected regions of the first, the second, and the third electrically conductive materials.

The invention also provides a charge-coupled device having at least one semiconductor cell, the cell comprising

a semiconductor substrate formed from a selected semiconductor material of one conductivity type;

a layer of a first insulating material formed on a surface of the substrate;

two regions of a first electrically conductive material disposed apart from each other at selected intervals on the layer of first insulating material;

two regions of second insulating material formed on all surface portions of the regions of the first electrically conductive material not in contact with the first insulating material.

two barrier regions formed apart from each other in the substrate adjacent to the first insulating material in regions of the substrate not overlaid by the regions of the electrically conductive material and the regions of the second insulating material, each barrier region being of the same conductivity type as the substrate but having a dopant concentration different from that of the substrate;

a region of a second electrically conductive material disposed on that portion of the layer of the first insulating material over one barrier region and disposed on selected portions of the regions of the second insulating material overlying the regions of the first electrically conductive material;

a region of third insulating material formed on all surface portions of the second electrically conductive material not in contact with the first and the second insulating materials;

a region of third electrically conductive material disposed on that portion of the first insulating material over the other barrier region and disposed on selected portions of the second and the third insulating materials;

means for connecting the remaining region of the first electrically conductive material to the region of the second electrically conductive material; and

means for connecting the remaining region of the first electrically conductive material to the region of the third electrically conductive material.

The invention moreover provides a method of fabricating a charge-coupled device having at least one semiconductor cell, the method comprising the steps of

forming an insulating layer on a semiconductor substrate;

forming barrier regions in the subtrate adjacent the insulating layer, each barrier region having a dopant concentration different from that of the substrate;

forming regions of a first electrically contive material everywhere on the layer of the insulating material except for those portions of the layer of the insulating material over barrier regions;

forming regions of a second electrically conductive material over one of the barrier regions and over selected portions of the regions of the first electrically conductive material, the second electrically conductive material being electrically isolated from the first electrically conductive material;

forming regions of a third electrically conductive material over the remaining barrier region and over selected portions of the first and second electrically conductive materials, the third electrically conductive material being electrically isolated from the first and second electrically conductive materials; and

electrically connecting selected regions of the first, second, and third electrically conductive materials.

The invention additionally provides a method of fabricating a charge-coupled device having a plurality of semiconductor cells, the method comprising the steps of

forming a layer of a first insulating material on a semiconductor substrate of one conductivity type;

forming a series of regions of a first electrically conductive material spaced apart from one another on the first insulating material;

forming a series of regions of a second electrically insulating material on all surface portions of the first electrically conductive material not in contact with the first insulating material;

forming a series of barrier regions spaced apart from one another in the substrate adjacent to the layer of the first insulating material in regions of the substrate not overlaid by the first electrically conductive material and by the second insulating material, each barrier region having a dopant of same conductivity type as the substrate but having a dopant concentration different from that of the substrate;

forming a series of regions of a second electrically conductive material on those portions of the layer of the first insulating material lying above alternate barrier regions and on selected portions of the second insulating material overlying the first electrically conductive material;

forming a series of regions of a third insulating material on all surface portions of the second electrically conductive material not in contact with the first and second insulating materials;

forming a series of regions of a third electrically conductive material on those portions of the layer of the first insulating material lying over the remaining barrier regions and on selected portions of the second and third insulating materials;

electrically connecting each alternate region of the first electrically conductive material to the corresponding region of the second electrically conductive material nearest the alternate region of the first electrically conductive material; and

electrically connecting each remaining region of the second electrically conductive material to the corresponding region of the third electrically conductive material nearest the remaining region of the first electrically conductive material.

This invention overcomes several disadvantages of conventional CCD gate structure by providing a more compact structure capable of operating at higher speeds. The separate formation of the second set and third set of electrodes according to one embodiment of this invention eliminates the limitations imposed upon the dimensions of the CCD gate structure by the alignment tolerances associated with simultaneously forming electrodes over all barrier regions.

A charge-coupled device of this invention, if fabricated according to the same design rules as conventional structures, can be made in approximately seven-tenths the wafer surface area of such structures. This reduction in size allows more structures to be formed within a given area, thereby increasing the speed of operation of both individual CCD gate structures and arrays of structures. Conversely a device of this invention can be formed according to less stringent design rules to create new CCD gate structures of the same size as existing structures but said new structures thereby having increased manufacturing tolerances to allow their fabrication with lower-quality equipment at a lower cost. Of course compactness and speed of operation each may be "traded off" to create a wide range of intermediate sized CCD gate structures which are somewhat more compact and faster than existing structures, but which may be fabricated with larger manufacturing tolerances than existing CCD gate structures.

In the accompanying drawings:

Fig. 1, to which reference has already been made, shows a cross-section of a typical prior-art charge-coupled device gate structure; and

Figs. 2a to 2d similarly show successive stages of a process by which an illustrative charge-coupled device may be fabricated in accordance with the present invention, Fig. 2d showing the completed charge-coupled device of the invention.

The charge-coupled device shown in Fig. 2d will be described below in conjunction with Figs. 2a, 2b and 2c.

On a semiconductor substrate 30, typically P conductivity type silicon, shown in Fig. 2a, a thin layer of insulating material 32 is formed. Insulating material 32 is typically thermally grown silicon dioxide but may be any suitable nonconductive material. A second layer of insulating material 33 is then formed on the surface of insulating material 32. Layers 33 may be any insulating material, but typically will be silicon nitride because thereby thermal oxide growth will be inhibited. During later processing steps associated with one method of fabricating the structure of Fig. 2d, layer 33 will prevent further growth of insulating material 32, if layer 32 is formed of silicon dioxide. Other materials performing an equivalent function to silicon nitride layer 33 may be substituted for silicon nitride. Following formation of insulating layer 33, a first layer of conductive material 35 is formed on the surface of silicon nitride layer 33. First conducting material 35 will typically be polycrystalline silicon, although other conductive material may also be used. Polycrystalline silicon material 35 can be deposited as doped polycrystalline silicon, or, in some embodiments, undoped polycrystalline silicon, may be deposited which is later doped. The appearance of the wafer following formation of insulating material 32, silicon nitride layer 33, and polycrystalline silicon layer 35, is shown in Fig. 2a.

Utilizing processing techniques well known in the semiconductor manufacturing arts, polycrystalline silicon layer 35 is masked and etched, or otherwise selectively removed, to create individual electrodes 35a, 35b, 35c and 35d (See Fig. 2b). After electrodes 35a, 35b, 35c, and 35d are formed, a second layer of insulating material 37 is formed on the wafer surface. This insulating material is shown in Fig. 2b as regions 37a, 37b, 37c, and 37d. Insulating material 37 will typically be an oxide of silicon, for example, silicon dioxide. When silicon nitride is utilized to form layer 33, and silicon dioxide is utilized as insulating material 37, no insulating material will be formed upon the surface of silicon nitride layer 33, for example, in the region between any two adjacent electrodes. Silicon nitride layer 33 will also prevent layer 32, if it is silicon dioxide, from growing during the formation of insulating material 37. Following formation of insulating material 37, barrier regions 38a, 38b, and 38c are formed in substrate 30. Barrier regions 38 typically will be formed from P type semiconductor materialy, and may be formed in any well-known manner. Utilization of well-known ion implantation technology, however, has been found particularly useful in the formation of barrier regions 38a, 38b, and 38c, because the lateral position of the ions may be precisely controlled relative to that of the gate electrodes. The doping concentration of the other semi-conductor materials in which the ions may lodge will be sufficiently great so the implanted ions will not have a significant effect upon the function of said other materials. The implanted barrier regions 38a, 38b, and 38c establish the directionality of charge transfer in the gate structure of this invention. The appearance of the semiconductor structure following the previously-described processing steps is shown in Fig. 2b.

Additional processing steps will now be described in conjunction with Fig. 2c. A second layer of electrically conductive material 40 is formed on the surface of the semiconductor structure. Typically conductive layer 40 will be formed from polycrystalline silicon or deposited as undoped polycrystalline silicon and then doped. In the manner previously described in conjunction with layer 35, polycrystalline silicon layer 40 will be selectively etched to create electrodes overy every other barrier region. Such electrodes 40a and 40b are depicted in Fig. 2c over barrier region 38a and 38c. The polycrystalline silicon material deposited over barrier regions 38b has been removed. After polycrystalline silicon layer 40 is selectively etched to create electrodes 40a and 40b, insulating material 42a and 42b is formed on the surface of the polycrystalline silicon material 40a and 40b. Typically insulating material 42a will be silicon dioxide, and as previously set forth, it will not form on the surface of silicon nitride layer 33. See, for example, the region immediately above barrier region 38b. The appearance of the semiconductor structure following formation of oxide 42a and 42b is shown in Fig. 2c.

The remaining fabrication steps necessary to complete the two-phase charge-coupled-device gate structure of this invention are described in conjunction with Fig. 2d. Next, a third layer of conductive material 45 is formed across the surface of the wafer. As with the first and second layers of conductive material 35 and 40, conductive material 45 typically will be polycrystalline silicon desposited either already doped, or doped in a subsequent step following its deposition. Similarly, as previously discussed in conjunction with the second layer of polycrystalline silicon 40, polycrystalline silicon layer 45 will be masked and etched to create separate electrodes 45a, 45b, and 45c, as shown in Fig. 2d. The appearance of the semiconductor structure following removal of the undesired portions of polycrystalline silicon layer 45 is shown in Fig. 2d.

One of the two-phase gates will be formed by electrically connecting electrode 35a with electrode 40a, while the second two-phase gate will be formed by electrically connecting electrode 35b with electrode 45b. The semiconductor fabrication processes and technology to accomplish these electrical connections, or other connections if other structures are desired, are well known and are therefore not shown in the drawings. Typically, however, an additional layer of insulating material will be formed across the entire surface of the structure shown in Fig. 2d. Openings through this layer of insulating material will be made to allow ohmic contact to the underlying regions of polycrystalline silicon from the surface of the underlying insulating material. Metallic contacts may then be formed across the surface of the overlapping insulating material to provide any desired electrical connections between the various regions of the semiconductor structure shown in Fig. 2d. The combined assembly of electrodes and barrier regions necessary to make a two-phase charge-coupled-device is designated as "one cell" in Fig. 2d. Of course, a second cell may be formed by connecting electrode 35c to electrode 40b, and by connecting electrode 35d to electrode 45c. Additional cells are not shown in Fig. 2d. The electrical connections between cells can be made at any desired cross-sectional location of the structure shown in Fig. 2d.

One of the primary advantages of the structure of this invention is illustrated by comparing Fig. 1 with Fig. 2d. These two Figures, drawn to approximately the same scale, clearly show the reduction in cell size which accompanies the structure of this invention. Typical prior-art cells such as shown in Fig. 1 consume about 20 microns of wafer surface, while the embodiment of this invention shown in Fig. 2d can be fabricated in 14 microns. Thus the cell shown in Fig. 2d is 30% shorter than the cell shown in Fig. 1. This reduction in cell size allows the charge-coupled device to function faster and therefore increases the limit of high frequency performance. Of course, as previously discussed, if a compact cell geometry is not desired, the structure shown in Fig. 2d can be fabricated in a longer embodiment, which will therefore be designed with more generous alignment tolerances. For example if the structure depicted in Fig. 2d is limited by both etching and alignment tolerances, fabrication of the structure shown in Fig. 2d in 20 microns will result in a structure which is limited only by etching tolerances, and is therefore easier to construct.

Although the structure of one charge-coupled-device of this invention has been described in conjunction with specific conductivity types and semiconductor material, it will be evident to those skilled in the semiconductor arts that complementary conductivity types and other semiconductor materials may be used to fabricate the device of this invention.

WHAT WE CLAIM IS:—

1. A charge-coupled device having at least one semiconductor cell, the cell comprising:

a layer of an insulating material on a surface of a semiconductor substrate;

two barrier regions formed in the substrate adjacent to the layer of insulating material, each barrier region having a dopant concentration different from that of the substrate;

two regions of a first electrically conductive material disposed on the layer of the insulating material except on those portions thereof over the barrier regions;

a region of second electrically conductive material disposed on that portion of the layer of the insulating material over one of the barrier regions and overlying selected portions of the regions of the first electrically conductive material;

a region of third electrically conductive material disposed on that portion of the layer of the insulating material over the other of the barrier regions and overlying selected portions of the regions of the first and second electrically conductive material; and

means electrically connecting together selected regions of the first, the second, and the third electrically conductive materials.

2. A charge-coupled device as claimed in claim 1 wherein each of the first, second, and third electrically conductive materials is polycrystalline silicon.

3. A charge-coupled device as claimed in claim 2 having at least one region of silicon dioxide disposed between adjacent regions of the first, the second, and the third electrically conductive materials.

4. A charge-coupled device having at at least one semiconductor cell, the cell comprising:

a semiconductor substrate formed from a selected semiconductor material of one conductivity type;

a layer of a first insulating material formed on a surface of the substrate;

two regions of a first electrically conductive material disposed apart from each other at selected intervals on the layer of first insulating material;

two regions of second insulating material formed on all surface portions of the regions of the first electrically conductive material not in contact with the first insulating material;

two barrier regions formed apart from each other in the substrate adjacent to the first insulating material in regions of the substrate not overlaid by the regions of the electrically conductive material and the regions of the second insulating material, each barrier region being of the same conductivity type as the substrate but having a dopant concentration different from that of the substrate;

a region of a second electrically conductive material disposed on that portion of the layer of the first insulating material over one barrier region and disposed on selected portions of the regions of the second insulating material overlying the regions of the first electrically conductive material;

a region of third insulating material formed on all surface portions of the second electrically conductive material not in contact with the first and the second insulating materials;

a region of third electrically conductive material disposed on that portion of the first insulating material over the other barrier region and disposed on selected portions of the second and the third insulating materials;

means for electrically connecting one region of the first electrically conductive material to the region of the second electrically conductive material; and

means for connecting the remaining rel gion of the first electrically conductive material to the region of the third electrically conductive material.

5. A charge-coupled device as claimed in claim 4 wherein the two regions of the first electrically conductive material have lower surfaces in contact with the layer of the first insulating material and the region of the second electrically conductive material has a lower surface in contact with the first and second insulating materials.

6. A charge-coupled device as claimed in claim 4 or 5 wherein the first, second and third electrically conductive materials are polycrystalline silicon.

7. A charge-coupled device as claimed in claim 4, 5 or 6 wherein the second and the third insulating materials are silicon dioxide.

8. A charge-coupled device as claimed in claim 4, 5, 6 or 7 wherein the region of the third electrically conductive material completely overlies at least all of one region of the first electrically conductive material.

9. A charge-coupled device as claimed in any preceding claim wherein the layer of the insulating material comprises a first layer on the substrate and a second layer on the first layer.

10. A charge-coupled device as claimed in claim 9 wherein the substrate is silicon, the first layer of insulating material is silicon dioxide, and the second layer of insulating material is silicon nitride.

11. A charge-coupled device as claimed in any preceding claim wherein the barrier regions are formed in the substrate by ion implantation.

12. A charge-coupled device as claimed in any preceding claim wherein the substrate and the barrier regions are P conductivity type.

13. A charge-coupled device as claimed in claim 1 to 11 wherein the substrate and the barrier regions are N conductivity type.

14. A charge-coupled device as claimed in any preceding claim having a plurality of the semiconductor cells, the barrier regions being periodically spaced in the substrate.

15. A charge-coupled device substantially as herein described with reference to Figure 2D of the accompanying drawings.

16. A method of fabricating a charge-coupled device having at least one semiconductor cell, the method comprising the steps of

forming an insulating layer on a semiconductor substrate;

forming barrier regions in the subtrate adjacent the insulating layer, each barrier region having a dopant concentration different from that of the substrate;

forming regions of a first electrically contive material everywhere on the layer of the insulating material except for those portions of the layer of the insulating material over the barrier regions;

forming regions of a second electrically conductive material over one of the barrier regions and over selected portions of the regions of the first electrically conductive material, the second electrically conductive material being electrically isolated from the first electrically conductive material;

forming regions of a third electrically conductive material over the remaining barrier region and over selected portions of the first and second electrically conductive materials, the third electrically conductive material being electrically isolated from the first and second electrically conductive materials; and

electrically connecting selected regions of the first, second, and third electrically conductive materials.

17. A method as claimed in claim 16 wherein the insulating layer is formed by forming a first layer on the substrate and then forming a second layer on the first layer.

18. A method as claimed in claim 17 wherein the semiconductor substrate is silicon, the first layer is silicon dioxide, and the second layer is silicon nitride.

19. A method of fabricating a charge-coupled device having a plurality of semiconductor cells, the method comprising the steps of

forming a layer of a first insulating material on a semiconductor substrate of one conductor substrate of one conductivity type;

forming a series of regions of a first electrically conductive material spaced apart from one another on the first insulating material;

forming a series of regions of a second electrically insulating material on all surface portions of the first electrically conductive material not in contact with the first insulating material;

forming a series of barrier regions spaced apart from one another in the substrate adjacent to the layer of the first insulating material in regions of the substrate not overlaid by the first electrically conductive material and by the second insulating material, each barrier region having a dopant of same conductivity type as the substrate but having a dopant concentration different from that of the substrate;

forming a series of regions of a second electrically conductive material on those portions of the layer of the first insulating material lying above alternate barrier regions and on selected portions of the second insulating material overlying the first electrically conductive material;

forming a series of regions of a third insulating material on all surface portions of the second electrically conductive material not in contact with the first and second insulating materials;

forming a series of regions of a third electrically conductive material on those portions of the layer of the first insulating material lying over the remaining barrier regions and on selected portions of the second and third insulating materials;

electrically connecting each alternate region of the first electrically conductive material to the corresponding region of the second electrically conductive material nearest the alternate region of the first electrically conductive material; and

electrically connecting each remaining region of the second electrically conductive material to the corresponding region of the third electrically conductive material nearest the remaining region of the first electrically conductive material.

20. A method as claimed in claim 19 wherein the regions of the first electrically conductive material have lower surfaces contacting the layer of the first insulating material and the region of the second electrically conductive material has a lower surface contacting the first and second insulating materials.

21. A method as claimed in claim 19 or 20 wherein the layer of the first insulating material is formed by forming a first layer on the substrate and then forming a second layer on the first layer.

22. A method as claimed in claim 21 wherein the semiconductor substrate is silicon, the first layer is a silicon dioxide, and the second layer is silicon nitride.

23. A method of fabricating a charge coupled device substantially as herein described with reference to Figures 2A to 2D.

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1575690 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

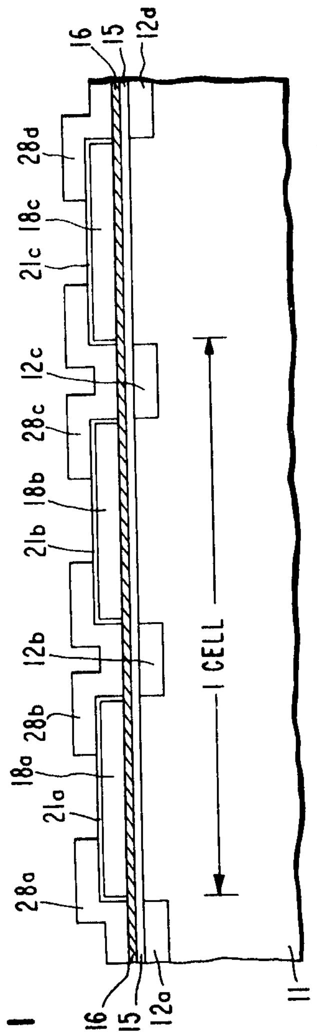

FIG.1

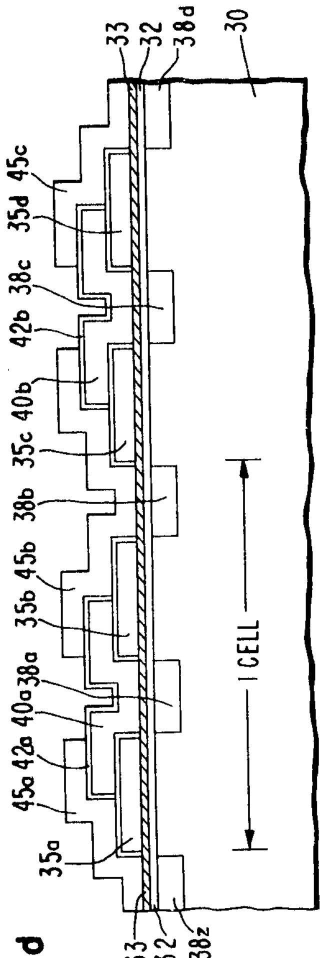

FIG.2d

FIG. 2a

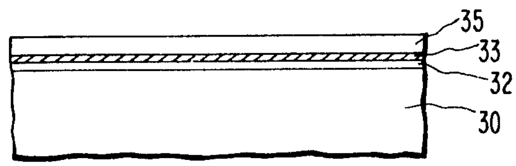

FIG. 2b

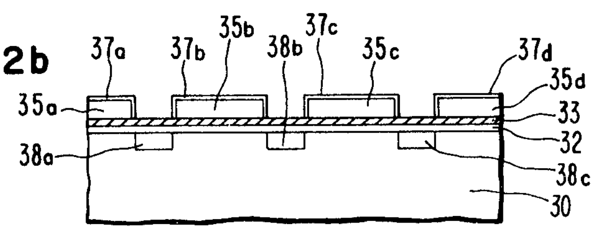

FIG. 2c