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(54) **Title:** COMPUTATIONAL PIXEL IMAGER WITH IN-PIXEL HISTOGRAM ACQUISITION

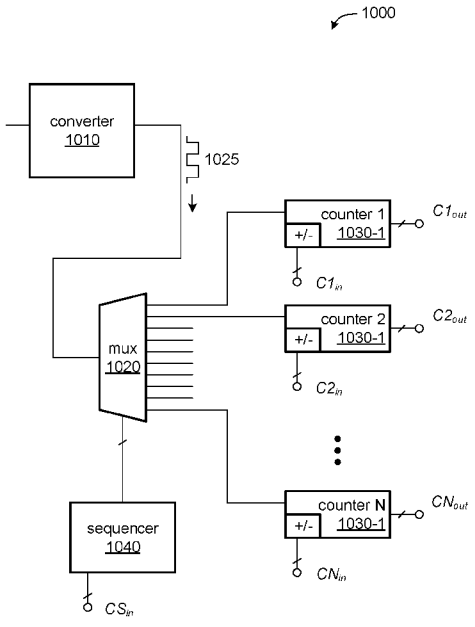


FIG. 10

(57) **Abstract:** A computational pixel imaging device can include multiple counters per pixel that can be used to acquire in-pixel histogram data representative of a signal detected by a pixel's detector. Multiple pixel counters can also be used to execute simultaneous signal-processing threads on acquired image data. The imaging device can also include infinite dynamic range sensing and perform signal down-sampling.

WO 2020/163342 A1

Computational Pixel Imager with In-Pixel Histogram Acquisition

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U. S. provisional application No. 62/800,685 filed on February 4, 2019 and titled "Multi-Function Time Multiplexed Camera." This application also claims priority to U. S. provisional application No. 62/807,683 filed on February 19, 2019 and titled "Event-Based Vision and Inter-Frame Video Compression." The entire contents of these applications are incorporated herein by reference.

FIELD

[0002] The described apparatus and methods relate to imaging arrays that include integrated circuitry for in-pixel data-processing.

BACKGROUND

[0003] The majority of conventional integrated-circuit imaging arrays are either charge-coupled devices (CCDs) or complementary metal-oxide semiconductor (CMOS) devices. In such imaging arrays, photocurrent generated by illumination of a photodiode accumulates charge on a capacitor at each pixel of the array. At the end of an exposure period, the amount of charge stored on the pixel's capacitor is read out of the array for subsequent image processing.

[0004] Recently, digital focal plane arrays have been developed as a different approach to imaging. These arrays include pixel circuitry that can digitize detected signals and perform some signal processing operations within the array pixels.

SUMMARY

[0005] The present invention relates to advanced imaging arrays that include integrated circuits within each pixel to digitize detected signals and to perform advanced signal-processing functions. According to some embodiments, a computational pixel imager includes a detector at each pixel and integrated circuitry that digitizes signals acquired by the detector. The integrated circuitry can include two or more counters at each pixel that are independently controlled to perform different image-processing functions concurrently. In some embodiments, the counters are configured for in-pixel histogram acquisition. Histogram acquisition may be used to determine, for example, time-of-arrival of photons at each pixel in response to pulsed

illumination of objects in a field of view. Additionally, the counters can be configured for infinite dynamic range sensing. For some applications, pixel detectors can be modulated to perform digital down-sampling of received modulated signals.

[0006] Some embodiments relate to a pixel integrated circuit in an array of pixel integrated circuits. The pixel integrated circuit can comprise a signal converter, wherein the signal converter is arranged to receive a signal from a detector, a multiplexer connected to an output of the signal converter, and two or more counters connected to outputs of the multiplexer.

[0007] Some embodiments relate to a method of acquiring in-pixel histograms. The method can include acts of converting, with a signal converter located in a pixel integrated circuit of an array of pixel integrated circuits, an analog signal received from a detector to an output signal; and directing the output signal to different counters included in the pixel integrated circuit at different times during an exposure period for the detector.

[0008] Some embodiments relate to a computational pixel imager having an array of pixels. one or more of the pixels in the array can include a detector, a signal converter connected to receive a signal from the detector, a multiplexer connected to an output of the signal converter, and two or more counters connected to outputs of the multiplexer.

[0009] The foregoing and other aspects, embodiments, and features of the present teachings can be more fully understood from the following description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The skilled artisan will understand that the figures, described herein, are for illustration purposes only. It is to be understood that in some instances various aspects of the invention may be shown exaggerated or enlarged to facilitate an understanding of the invention. In the drawings, like reference characters generally refer to like features, functionally similar and/or structurally similar elements throughout the various figures. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the teachings. The drawings are not intended to limit the scope of the present teachings in any way.

[0011] **FIG. 1A** depicts a computational pixel imaging device, according to some embodiments;

[0012] **FIG. 1B** depicts a computational pixel imaging device, according to some embodiments;

[0013] **FIG. 2** depicts an imaging system that may include a computational pixel imaging device, according to some embodiments;

[0014] **FIG. 3A** depicts an example of pixel circuitry for a computational pixel imaging

device, according to some embodiments;

[0015] **FIG. 3B** depicts an example of pixel circuitry for a computational pixel imaging device, according to some embodiments;

[0016] **FIG. 4** depicts additional data-handling circuitry that may be used with a computational pixel imaging device, according to some embodiments;

[0017] **FIG. 5A** depicts an example of counter connections across pixels, according to some embodiments;

[0018] **FIG. 5B** depicts another example of counter connections across pixels, according to some embodiments;

[0019] **FIG. 6** illustrates acts associated with multi-thread processing of image data acquired by multiple counters, according to some embodiments;

[0020] **FIG. 7A** depicts example circuitry for infinite dynamic range sensing in a pixel, according to some embodiments;

[0021] **FIG. 7B** illustrates further details of an embodiment of circuitry for infinite dynamic range sensing in a pixel;

[0022] **FIG. 8** plots examples of most significant bit read rates for counters adapted for infinite dynamic range sensing in a pixel, according to some embodiments;

[0023] **FIG. 9** depicts an example of a pixel integrated circuit that is adapted for digital down sampling, according to some embodiments; and

[0024] **FIG. 10** depicts an example of a pixel integrated circuit that is adapted for in-pixel histogram acquisition, according to some embodiments.

[0025] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings.

DETAILED DESCRIPTION

[0026] Imaging arrays that include in-pixel digitization circuitry are emerging as useful alternatives to conventional CMOS and CCD imaging arrays for some applications. An example of a computational pixel imaging device 100 is depicted in **FIG. 1A**. According to some embodiments, a computational pixel imaging device 100 can include a substrate 104 on which is formed an array of detectors 110 and an array of pixel integrated circuits 120 that are arranged to receive signals from the corresponding detectors. A detector 110 and its corresponding pixel integrated circuit 120 can form a pixel of a computational pixel imaging device 100, and may both be located on a same substrate 104 in some embodiments. The arrays depicted in **FIG. 1A** are two-dimensional and may comprise tens, hundreds, thousands, or even millions of pixels when implemented in a device. In some cases, the arrays may be one-

dimensional (*e.g.*, for a device that is scanned).

[0027] **FIG. 1B** depicts an embodiment of a computational pixel imaging device 102 in which the detectors 110 are formed on a first substrate 106 in a detector array and the pixel integrated circuits 120 are formed on a second substrate in a pixel integrated circuit array. In some embodiments, the detectors 110 on the first substrate 106 can be directly connected to receiving pixel integrated circuits 120 on the second substrate 108 (*e.g.*, by flip-chip or bump-bonding processes that may include solder bumps or posts). In some implementations, the detectors 110 on the first substrate 106 may be connected to receiving pixel integrated circuits 120 on the second substrate 108 through an interposer located between the substrates and not shown in the drawing. The interposer may provide some signal rerouting so that the array of pixel integrated circuits 120 on the second substrate may be larger than the array of detectors 110 on the first substrate. However, in some cases the pixel size for a pixel integrated circuit 120 may be the same or smaller than a pixel size for a detector 110.

[0028] The first substrate 106 may be made from a first material that can be the same or different from a second material used to form the second substrate 108. For example, the first substrate 106 may be made from a first semiconductor material (*e.g.*, indium phosphide (InP)) and the second substrate may be made from a second semiconductor material (*e.g.*, silicon (Si)). Other materials from which the substrates in **FIG. 1A** and **FIG. 1B** may be formed and/or that may be included on the substrates include, but are not limited to, II-VI semiconductors such as cadmium telluride (CdTe) and mercury-cadmium telluride (HgCdTe), III-V semiconductors such as gallium nitride (GaN) and compositions including GaN, gallium arsenide (GaAs) and compositions including GaAs, and group IV semiconductors such as Si, germanium (Ge), or silicon-germanium (SiGe).

[0029] Various types of detectors 110 may be used in a computational pixel imager 100, 102. In some embodiments, the detectors 110 may comprise *p-n* or *p-i-n* junction photodiodes or phototransistors or photoconductors. Barrier detectors (*e.g.*, barrier photodiodes, barrier phototransistors, *etc.*) may also be used in some cases and provide high detection sensitivity. In some cases, the detectors 110 may comprise avalanche photodiodes for sensing low light levels. In yet other embodiments, the detectors 110 may comprise microbolometers. According to some embodiments, the detectors 110 may be cooled to reduce background noise and/or to enhance responsivity of the detectors. For example, the computational pixel imager 100, 102 may be mounted on a thermoelectric cooler or placed in thermal contact with a chilled heat sink or located in a dewer.

[0030] A computational pixel imager 201 may be included in an imaging system 200 as illustrated in **FIG. 2**, according to some embodiments. An imaging system 200 can include a

camera 202 that may house collection optics 210 and a computational pixel imager 201. The imaging system 200 may also include a controller 250 that can connect to the camera 202 and computational pixel imager 201 by a wired or wireless data-communication link. The collection optics 210 may include one or more lenses and/or mirrors that act to form an image of a viewed scene on detectors 110 in the computational pixel imager 201. The detectors 110 may be located in an imaging plane of the collection optics 210 and an array of pixel integrated circuits 120 may be located in the imaging plane or adjacent to the imaging plane. In some embodiments, some component(s) of the collection optics 210 may be moved controllably and automatically, the imager 201 may be moved controllably and automatically, and/or the entire camera 202 may be moved controllably and automatically (*e.g.*, rotated by motors or actuators) to scan and image a large field of view.

[0031] The imaging system 200 may be adapted as a visible imaging system, an infrared imaging system (*e.g.*, a night-vision system), an ultraviolet imaging system, or an x-ray imaging system. The choice of detector design and material can determine the responsivity of the detector to various wavelengths of radiation. For example, Si-based photodiodes can be used for a visible imaging system (*e.g.*, wavelengths from about 380 nm to about 740 nm), whereas CdTe photodiodes may be used for ultraviolet or x-ray imaging systems. As another example, indium arsenide or HgCdTe photodiodes may be used for an infrared imaging system. In some cases, strained-layer superlattice detectors formed from III-V materials can be used for infrared imaging. In some cases, detector design and material can be chosen to detect radiation within a spectral range that lies within a portion of an infrared wavelength range between 750 nm or approximately 750 nm and 5 microns or approximately 5 microns. For example and in some implementations, a detector can be selected to detect radiation in an infrared spectral range between 0.75 micron and 3 microns or between approximately these end values. In some implementations, a detector can be selected to detect radiation in an infrared spectral range between 3 microns and 5 microns or between approximately these end values.

[0032] In some implementations, the controller 250 can be implemented in various ways and forms. For example, the controller 250 may be embodied as a field programmable gate array (FPGA), a mainframe computer, or anything in between such as a microcontroller, a microprocessor, one or more application-specific integrated circuits, a digital signal processor, a laptop computer or desktop computer, a tablet computer, a smart phone, *etc*. In some cases, the controller 250 can be embodied as combinations of different controlling devices. Part of the control components can include code as software and/or firmware that adapts the controller 250 to execute functionalities that control operation of the imaging system 200 and receive, store, transmit, and process image data acquired by the camera 202. Controller components may also

include custom logic and/or analog circuitry as well as memory that can be used by the computational pixel imager. The controller 250 may be configured to initiate the transfer of digital signals from the pixel integrated circuits 120 and to control the shifts, counts, and accumulation times that can permit the pixel integrated circuits 120 to perform digital-signal-processing functions on-chip. In some cases, some control functions may be incorporated into the pixel integrated circuits 120 (*e.g.*, hardwired or implemented as firmware). Such an integration may permit an array of pixel integrated circuits 120 to operate autonomously and perform on-chip, digital-signal-processing functions relatively free of external control.

[0033] An imaging system 200 in accordance with the present embodiments may be used, for example, in industrial inspection, surveillance, process control, biological research, chemical research, pharmaceuticals, medical imaging, remote sensing, and astronomy. An implementation that comprises a computational pixel imager 201 and single-chip controller 250 may be incorporated in a variety of cameras, including portable, consumer, still and motion cameras, for example. A camera may be configured to operate in the visible region of the optical spectrum or in other wavelength regions by selecting appropriate detectors 110. In some embodiments, a computational pixel imager 201 and controller 250 may be incorporated into a vision system for autonomous vehicles or robotic instruments.

[0034] In the infrared range, an imaging system 200 may be adapted for operation as an infrared camera and used for industrial sensing (*e.g.*, monitor heat emission from industrial components and/or machines), security, or firefighting, for example. An infrared camera may also be employed to provide an infrared image of a scene ahead of and/or around a vehicle. In some implementations, the imaging capability of the camera can extend beyond the human visible range of a scene illuminated by vehicle headlights. An acquired infrared image may be displayed, for example in a "heads up" display or overlaid on a windscreen of the vehicle to assist the vehicle operator. Potential hazards that are not visible to the unaided eye can become visible to a human operator through the camera and display.

[0035] In some implementations, an imaging system 200 can include a cryogenically cooled infrared detector array, with connections between the detector array and the pixel integrated circuit array made via indium bump bonding, for example. In such an embodiment, the detector array may be suitable for low-light-level, low noise sensing in the infrared region of the spectrum (2-20 microns). Cooling may also be employed for detectors used in the visible and ultraviolet regions of the optical spectrum.

[0036] An example of a pixel integrated circuit 120 is depicted in **FIG. 3A**. According to some embodiments, a pixel integrated circuit 120 can include a first transistor 306, a capacitor C_0, which may be included in a current-to-frequency converter 310, and at least one digital

counter 330-1. In some cases, a second transistor 307 may be included between the first transistor 306 and current-to-frequency converter 310. The second transistor 307 can provide additional isolation between node 308 or input to the current-to-frequency converter 310 and the source of the first transistor 306. The second transistor 307, connected in cascade, can help dampen noise arising from reset actions performed on node 308. In some implementations, there can be two or more counters 330-1, 330-2, ... 330-M as illustrated in the drawing. The current-to-frequency converter 310 can be arranged to receive as input an analog signal and output a pulse every time a current exceeds a threshold value. The pulses can be counted by the counters 330-1, 330-2, ... 330-M. When located above or below a detector 110 in a pixel, an area occupied by a pixel integrated circuit 120 may be approximately the same size or smaller than an area occupied by the detector. In some implementations, a voltage-to-frequency converter may be used instead of a current-to-frequency converter. For example, a voltage-to-frequency converter may sense a voltage appearing on a node 308 of a capacitor C_0 and output a pulse every time a voltage exceeds a threshold value.

[0037] In further detail, a detector (which may be embodied as a photodiode 305) can generate a photocurrent I_p when exposed to radiation. In some embodiments, the detector (photodiode 305) may receive a stable bias from a bias source. For example, biasing circuity can be included to apply a bias the photodiode 305 from a voltage source. The circuitry may include a large inductor on a bias line to block time-varying signals from the photodiode and pass a DC bias voltage. It may be advantageous to maintain a stable bias on the detector, and the second transistor 307 can help reduce bias variations that might otherwise occur due to resetting action at node 308.

[0038] In some implementations, passage of the photocurrent I_p to a capacitor C_0 of the current-to-frequency converter 310 may be controlled by the first transistor 306 (and/or second transistor 307) with the application of a digital control signal D_{in} (and/or B_{in}), for example. According to some embodiments, the control signal D_{in} (and/or B_{in}) may determine an exposure period for a pixel of the computational pixel imager. For example, when the control signal D_{in} (and B_{in}) is at a logic "HIGH" or "1" level, photocurrent I_p can flow and accumulate charge on capacitor C_0 raising the voltage at node 308. Toggling the first transistor 306 and/or second transistor 307 to a logic "LOW" or "0" level can block further photocurrent flow to the capacitor C_0, and can terminate an exposure period. The exposure period can be repeated for video imaging and can be any suitable duration. In some embodiments, the exposure period may be any duration of time between 1 nanosecond (1 ns) for high levels of radiation on the detector and tens of minutes for low levels of radiation or for high-dynamic range sensing. Each exposure period can form an image frame with signals received from all pixels in the imager's array.

[0039] In other implementations, the first transistor 306 (or transistors as described further below) may be used to provide gain and at least one of the transistors 306, 307 may be biased to operate in a sub-threshold region. In such embodiments, the first transistor(s) may or may not be used to shutter an exposure period. In some cases, shutter action for exposure periods can be accomplished by control signals (or clock signals) provided to the counters 330-1, 330-2, ... 330-M that instruct one or more counters when to start and stop accumulating counts.

[0040] Although the input transistor(s) 306, 307 can be arranged as a switch (as in **FIG. 3A**) for direct photocurrent injection, in some cases the input transistor(s) may be arranged in other configurations and two or more transistors may be used to receive photocurrent from the photodiode 305. For example, one or more transistors may be arranged to amplify a signal from the photodiode 305. Input transistor(s) may be connected as a source-follower, a transimpedence amplifier, or configured for buffered direct injection of the photocurrent I_p. In some implementations, a current mirror circuit may be included in an input transistor arrangement, wherein the current mirror circuit provides current gain in a circuit branch that runs parallel to the branch containing the photodiode 305 and first transistor 306. The amplified current can be provided to the capacitor C_0 and current-to-frequency converter 310. Although the input transistor(s) 306, 307 are depicted as a field-effect transistor (FET), bipolar junction transistors (BJTs) and other types of transistors may be used in some embodiments.

[0041] The capacitor C_0 may have one terminal connected to an output of the first transistor 306 (or second transistor 307, if present) and a second terminal connected to a reference potential (*e.g.*, ground as illustrated). The capacitance of capacitor C_0 can be small (*e.g.*, between 1 femtoFarad (1 fF) and 1 nanoFarad (1 nF). Higher or lower capacitance values may be used in other embodiments. In some cases, capacitor C_0 can be embodied as parasitic capacitance of a discrete circuit device (*e.g.*, parasitic drain capacitance of the first transistor 306 or second transistor 307, if present), and may not be a separate discrete component in the integrated pixel circuit 120. The capacitor C_0 can determine the least significant bit value for a signal level from a pixel. Although **FIG. 3A** depicts one polarity for applying (sourcing) current to the current-to-frequency converter 310, in some cases it may be beneficial to reverse the orientation of the photodiode 305 or detector and sink current from the current-to-frequency converter 310. The use of appropriate types (*n*-MOS or *p*-MOS) of transistors can allow a pixel integrated circuit to accommodate a current source or current sink photodetection strategy. Current applied to the current-to-frequency converter 310 may charge or discharge a capacitor C_0. For example, in some cases a reset of the capacitor may comprise applying a non-zero voltage to node 308, which can leave a potential across the capacitor C_0 that is discharged, at least in part, by subsequent exposure of the photodiode 305.

[0042] The current-to-frequency converter 310 can include comparator circuitry 315 and reset circuitry 320, according to some embodiments. Comparator circuitry 315 can be embodied as a Schmitt trigger, comparator, or high-gain amplifying transistor that toggles between two output states: for example, from a low level to high, or high level to low, when an input voltage exceeds (or falls below) a reference voltage V_{ref}. In some implementations, the reference voltage may be hardwired to a fixed value or may be a threshold voltage of a transistor. In other cases, the reference voltage V_{ref} may be programmable by an external control signal to two or more values. For example, an integrated pixel circuit 120 may further include transistors (and resistive elements in some cases) arranged to provide programmable voltage values. Reset circuitry 320 may be embodied as one or more transistors arranged to discharge the capacitor C_0 (*e.g.*, shunt the capacitor's terminal connected to node 308 to the reference voltage connected to the other terminal of the capacitor. For example, a toggling of an output from the comparator circuitry 315 can activate the reset circuitry 320 to discharge the capacitor C_0, which can cause the comparator circuitry 315 to toggle back to a prior state of the two states. In some implementations, the current-to-frequency converter 310 may be embodied as described in connection with figure 3 of U.S. patent No. 10,348,993, the entire contents of which is incorporated herein by reference.

[0043] As a result of toggling of the comparator circuitry 315 and resetting of the capacitor C_0, an output of pulses 325 can be provided to one or more counters 330-1, 330-2, ... 330-M during an exposure period. The number of pulses during an exposure period will depend upon and be proportional to an amount of radiation incident on the detector (photodiode 305 in the illustrated embodiment). A higher level of radiation will produce a larger number of pulses during the exposure period. One or more of the counters 330-1, 330-2, ... 330-M can accumulate counts for the pulses received during the exposure period. At the end of the exposure period, the number of counts can be read out of a counter as a digital signal level for the pixel. The digital signal level will be indicative of an intensity of radiation received by the detector at the pixel.

[0044] The counters 330-1, 330-2, ... 330-M can be implemented with transistors arranged as logic gates, according to some embodiments. For example, a counter can be formed from flip-flop logic circuits and embodied as an N-bit ripple counter. Other types of counters, such as synchronous counters may also be used in some implementations. Accumulated counts may be output over parallel digital data lines $C1_{out}$, $C2_{out}$, ... CM_{out}. In some implementations, count values from the counters can be provided to shift registers that are connected to each counter. The shift registers may also be located in the pixel and form part of the pixel integrated circuit 120. In some cases, the counters themselves are configured for additional use as shift registers.

A counter's bit size can determine the most significant bit limit on signal values from a pixel.

[0045] According to some embodiments, the counters 330-1, 330-2, ... 330-M are programmable over digital input lines $C1_{in}$, $C2_{in}$, ... CM_{in}. For example, the counters may be programmed to increment or decrement counts at the start of each exposure period. In some implementations, counting direction may be changed by a programmable control signal at any time during an exposure period. Additionally or alternatively, the counters may be programmed with an initial count value for the start of each exposure period.

[0046] Embodiments described herein are not limited to one current-to-frequency (or voltage-to-frequency) converter per pixel. Two or more converters may be used per pixel integrated circuit 122, as illustrated in the example of **FIG. 3B**. According to some embodiments, one or more pixels of a computational pixel imager can include two or more current-to-frequency converters 310-1, 310-2, ... 310-N arranged to receive an output from the pixel's detector (photodiode 305 in the illustrated example). In some cases, there can be N second transistors 307-1, 307-2, ... 307-N, where N is a positive integer. The N second transistors can be used to provide added isolation of the pixel's detector from resetting actions occurring in the current-to-frequency (or voltage-to-frequency) converters. Additionally, the N second transistors 307-1, 307-2, ... 307-N can be used to select one or more of the converters 310-1, 310-2, ... 310-N for processing of the signal from the photodiode 305. The converters can be as described above in connection with **FIG. 3A**, and their description need not be repeated.

[0047] According to some embodiments, outputs from the converters 310-1, 310-2, ... 310-N may connect to a multiplexer 340 that can be controlled with a digital input signal M_{in} applied to a control port. The control signal M_{in} can select which input port connects to an output port of the multiplexer. In some implementations, the multiplexer 340 can be a N:1 multiplexer. **FIG. 3B** illustrates an example case in which the pixel's counters 330-1, 330-2, ... 330-M can be shared by (*e.g.*, dynamically assigned to) any of the converters 310-1, 310-2, ... 310-N. In some cases, a multiplexer 340 may not be used for some or all converters and one or more of the converters may have separate counter(s) that are dedicated or statically assigned to each converter. Other circuit arrangements are also possible. For example, a first group of counters or a single counter in a pixel may be dedicated to one converter or shared by a first group of converters, and a second group of counters or a second single counter in a pixel may be dedicated to one converter or shared by a second group of converters.

[0048] Adding additional converters can provide redundancy in pixels and improve fabrication yields. For example, if one of the converters fails in a pixel due to microfabrication processes, another converter can be selected for the pixel so that all pixels in the array of pixel integrated circuits can be used. In some implementations, the converters 310-1, 310-2, ... 310-

N within a pixel can be configured differently (to exhibit different gain, frequency characteristics, power consumption, capacitance value for capacitor C_0, *etc.* This can provide improved coverage with the same computational pixel imager for different signal conditions and operating conditions including but not limited to gain, noise, power, and maximum detectable frequency modulations.

[0049] Adding additional converters and counters can also support multi-thread processing operations described herein. For example, a signal from a pixel's detector (*e.g.*, photodiode 305) can be processed by one, two, or more converters and two or more counters (which may be in separate groups of counters), such that different functional operations are performed on parallel computational threads with the pixel's counters. Some of the functional operations can include bit operations such as, but not limited to, add, subtract, complement, shift, compare, and rotate.

[0050] **FIG. 4** depicts some additional data-handling circuitry that can be included with a computational pixel imager. A computational pixel imager 100, 102 may include circuitry that permits the orthogonal transfer of accumulated counts on counters throughout the array 406 of pixel integrated circuits. The orthogonal transfer of count values can be accomplished by shifting count values from a pixel's counter(s) to any one of the pixel's four nearest-neighbor pixels' counters, as described further below. For illustrative purposes, each shaded rectangle 402 within the array 406 depicts approximately an area occupied by a pixel, though in an actual device there can be thousands to millions of pixels. According to some implementations, digital counts can be transferred through column-transfer data lines 420 and/or through row-transfer data lines 430 to other pixels or to the data handlers 410, 412, 414, 416. In some implementations, multiplexers can be included to serialize data from multiple column-transfer data lines 420 and/or row-transfer data lines 430 that is sent to the data handlers 410, 412, 414, 416 and/or off chip. For example, one or more M:1 multiplexers (where M can be any integer value of 2 or greater) can be used to serialize data from multiple row-transfer data lines 430 onto single data lines that provides pixel data to one or more of the data handlers.

[0051] By shifting data along rows or columns, any result or count value from a counter within the array 406 may be transferred to another counter in a different pixel within the array 406 or to the data handlers. Such transfer capability along with programmability of the counters (increment, decrement) and control of count accumulation times can allow digital signal processing operations to be performed within the array 406. Digital signal processing operations that may be performed within the array can include, but are not limited to, threshold filtering, high-pass filtering, low-pass filtering, edge-detection filtering, match filtering, spatial filtering, temporal filtering, or spatio-temporal filtering, smoothing, differentiation, data compression, time-domain integration, image correlation, and convolution.

[0052] For example, match filtering may be implemented by developing a filter kernel for cross correlation with objects in an imaged scene (*e.g.*, a person's iris in a personal identity system, a facial image, a target object). Convolution of a kernel with an image can be implemented as a series of count accumulations (which may increment and decrement counts) and counter value orthogonal transfers. A correlated or convolved image can then be thresholded by compare logic for detections (*e.g.*, detection of an iris or target object). Data transmitted from the array could be raw cross-correlation or convolution results, or may be only data associated with the detections alone which could reduce the amount of data transmitted and subsequently processed. In another aspect, a signal from a steering and/or motion-sensing mechanism may be used to shift accumulated counts in an array synchronously with the overall motion of an imaging system to enable time-domain integration. Similar control of shifting counts can also enable image stabilization for environments where the imaging system may undergo unwanted vibrations. In some embodiments, non-uniformity correction for an imaging array may be performed by counting down for a frame period while viewing a flat, extended source (*e.g.*, a mechanical shutter). After the background scene is acquired, the counters can be configured to count up while the scene data is acquired. After a frame period, only signal and noise data will be present and any systematic non-uniformity of the imager will be cancelled. Non-uniformity correction may employ a 50% duty cycle for scene and background image acquisition.

[0053] In some embodiments, there may be more than one column-transfer data line 420 and more than one row-transfer data line 430 per pixel so that data from multiple counters within a pixel can be transferred in parallel to multiple counters in adjacent pixels. For example, a count value from a first counter in a first pixel can be transferred to a first counter in an adjacent pixel while a count value from a second counter in the first pixel can be transferred to a second counter in an adjacent pixel. In some cases, data serializers may be included in each pixel integrated circuit to send count values from multiple counters within the pixel serially over a signal row and/or column-transfer data line.

[0054] Data handlers 410, 412, 414, 416 may comprise additional transistor circuitry that is configured to provide additional data-processing operations and/or control of data transfer and programming of the pixel integrated circuits 120. For example, data handlers 410, 412, 414, 416 may include additional registers and data serializers to read data from and onto row and column data-transfer lines 430, 420. Data handlers 410, 412, 414, 416 may also include logic gates to enable control of the exposure period duration, counter direction, and/or threshold voltage reference V_{ref}. In some implementations, data handlers can be configured to perform threshold detection, compare, match filtering, and data selection functions. In some cases, data handlers

can be configured to determine a read-out time for selected rows and/or columns (as may be used in connection with infinite dynamic range pixels described below, for example). Data handlers 410, 412, 414, 416 may also include input/output data lines I/O_1, I/O_2, I/O_3, and I/O_4 that can be used to send processed or unprocessed signals, for example, to an external analyzer or processor for further data processing and analysis. In some implementations, one or more of the data handlers 410, 412, 414, 416 may be located on a same chip as the array 406 of pixel integrated circuits. In other embodiments, one or more of the data handlers 410, 412, 414, 416 can be located on a different chip that is connected to the chip containing the array 406 of pixel integrated circuits. According to some embodiments, the array 406 of pixel integrated circuits and data handlers 410, 412, 414, 416 can be manufactured using complimentary metal-oxide-semiconductor (CMOS) microfabrication processes.

[0055] **FIG. 5A** illustrates one example of how multiple counters 530-1, 530-2 in one pixel 502 of a computational pixel imager may be connected to counters in adjacent pixels. Although only two counters are illustrated within the pixel 502, a pixel can include more than two counters in some implementations. Additional counters can be connected in a same way to counters in adjacent pixels. In some implementations, the counters can be ripple counters, though other types of counters can be used in other embodiments. In some cases, counters may be implemented with D flip-flops for each bit and the flip-flops can be connected in series with an output of one flip-flop connected to an input of a next flip-flop. Further details of counters and associated circuitry that can be used in the implementations depicted in **FIG. 5A** and **FIG. 5B** can be found in U.S. patent No. 9,768,785 as described in connection with Figure 3 and Figure 4 in that patent, which is incorporated herein by reference in its entirety.

[0056] According to some embodiments, multiple counters are connected to neighboring counters in a way such that counters operated in a particular manner for image acquisition or performing a signal-processing function can shift count values to other counters anywhere in the array that are operated in the same manner. In some implementations, the shifting of counter values may be through nearest neighbor shifts. For example, a first counter 530-1 operated in a first manner in a first pixel 502 may shift its count value to a first counter operated in a same manner in a first nearest neighbor pixel, whereas a second counter 530-2 operated in a second manner in a first pixel 502 may shift its count value to a second counter operated in a same manner in a second nearest neighbor pixel. The first nearest neighbor pixel can be the same or different than the second nearest neighbor pixel. An example of a first manner of counter operation may be raw image acquisition where the corresponding first counters continuously count up during an exposure period. An example of a second manner of counter operation may be temporal filtering to detect changes in pixel values by modulated signals or moving objects

where a count value is incremented for half an exposure period and then decremented for half an exposure period. Other manners of counter operation are possible as described above and below. By repeated nearest neighbor shifts, along rows and columns, a value on one counter can be shifted to another corresponding counter anywhere in the array.

[0057] For the example depicted in **FIG. 5A**, the counters can be configured to function as both counters and shift registers. Further counter values from multiple counters 530-1, 530-2 in a pixel 502 can be passed over separate data lines (*e.g.*, row data-shift lines 551-2, 552-2) to multiple corresponding counters in an adjacent pixel. Counter values can be passed to adjacent pixels in either direction within a row or column along different data-shift lines (*e.g.*, data-shift lines 551-1, 551-2, 551-3, 551-4). The data-shift lines may also be referred to as row or column buses. Additionally, counter values for pixels at an edge of the array can be passed to edge logic for read-out and/or data processing via the data-shift lines. The data-shift lines may be parallel data lines (such that count values are passed in parallel) or serial data lines. For serial transmission of count values, b:1 multiplexers for b-bit counters may be included in the pixel after the counter output to place count values serially onto data-shift lines. In some embodiments, shift multiplexers 540-1, 540-2 can be included in each pixel, connected to counter outputs, and controlled by signals applied to inputs $M1_{in}$, $M2_{in}$ from edge logic to direct counter values to one of the neighboring pixels. Similarly, input multiplexers 510-1, 510-2 can be connected to data inputs of the counters 530-1, 530-2 to receive and place count values from neighboring pixels' counters on counters 530-1, 530-2 within the pixel. Input multiplexers 540-1, 540-2 may also be controlled by signals applied to inputs $M3_{in}$, $M4_{in}$ from edge logic.

[0058] Another example of inter-pixel counter connections is illustrated in **FIG. 5B**. In some embodiments, values from multiple counters within a pixel can be multiplexed onto a same row or column data-shift line with counter-output multiplexers 560. The counter-output multiplexers 560 can be M:1 multiplexers, where M is an integer value of 2 or greater and corresponds to the number of independently controlled counters within the pixels. Additionally, data received from adjacent pixels can be received by a single input multiplexer 510. The input multiplexer 510 can be a 4:M multiplexer, where M is an integer value of 2 or greater and corresponds to the number of independently controlled counters within the pixels.

[0059] **FIG. 6** illustrates an example method of multi-thread processing 600 that can be performed with an array 406 of pixel integrated circuits having multiple programmable counters in each pixel and arranged to shift values to counters in adjacent pixels as described above. According to some embodiments, a method 600 can include acts of initiating (act 610) an exposure of a detector array of a computational pixel imager to generate image data. During an exposure period (*e.g.*, a signal acquisition period that can be used to form an image frame),

multiple counters in each of a plurality of pixels can accumulate (act 620) count values. The count values for at least some of the counters can be accumulated independently of count values accumulated by other counters and can differ from count values accumulated by other counters, even within a same pixel. In some implementations, the counters within a same pixel can be programmed to operate differently. For example, two counters within a pixel may be programmed to increment and decrement counts periodically at a same frequency but with phases shifted by 90 for in-phase and quadrature (I-Q) detection of a modulated optical signal whereas a third counter can be programmed to increment counts for one-half of an exposure period and to decrement counts for one-half of an exposure period to detect non-stationary objects in an imaged scene. Accumulation of counts in counters can terminate when and exposure is terminated (act 630) ending the exposure period. In some cases, one or more counters within a pixel can be programmed to accumulate counts in response to exposure of the pixel's detector, whereas one or more other counters within the pixel can be programmed to perform other operations on data previously accumulated or provided to the counter(s) (*e.g.*, shift operations, bit rotation operations, ones complement, addition, subtraction, compare, read-out, data receive, *etc.*) Such different in-pixel operations on the counters can be in response to multiple threads that execute simultaneously on the system.

[0060] After counts have been accumulated in multiple counters, two or more independent data-processing operations can be executed on multiple threads simultaneously with the pixel integrated circuit array. For example, first image data (first counter values) acquired with first counters from the pixels can be processed (act 640-1) using shift operations and/or any of the above counter operations to perform a first signal-processing function (*e.g.*, spatial filtering). Additionally, second image data (second counter values) acquired with second counters from the pixels can be processed (act 640-2) using shift operations and/or any of the above counter operations to perform a second signal-processing function (*e.g.*, temporal filtering). In some implementations, the different signal-processing functions can be performed, at least in part, while count values are being accumulated in a subsequent exposure period (as may be the case for convolution, correlation, time domain integration for a deterministically moving camera, or image stabilization functions). In some cases, raw count values may be accumulated as new image data on one or more counters in a pixel while signal processing operations are being performed with other counters, such that the computational pixel imager has essentially no dead time in imaging a scene or successive scenes.

[0061] As indicated in **FIG. 6**, the multiple execution threads (acts 640-1, 640-2, … 640-N) can execute simultaneously. For imaging systems in which outputs and inputs of multiple counters are connected across pixels with separate, parallel data-shift lines (*e.g.*, lines 551-2,

552-2) as illustrated in **FIG. 5A**, at least some signal-processing operations for different counters performing different functions can occur at a same time (*e.g.*, on same clock cycles that drive data transfer or arithmetic operations). For imaging systems in which outputs and inputs of multiple counters are connected across pixels using multiplexers to serialize counter data onto shared data-shift lines as illustrated in **FIG. 5B**, at least some signal-processing operations for different counters performing different functions may be interleaved in time and occur on alternating clock cycles. In either case, multiple execution threads (acts 640-1, 640-2, ... 640-N) can execute concurrently on a pixel integrated circuit chip. When one or more of the multiple execution threads are completed, data for the corresponding counters can be read out of the array 406 of pixel integrated circuits over column-transfer data lines 420 and/or row-transfer data lines 430 for display, analysis, storage, and/or further signal processing.

[0062] In some embodiments, a computational pixel imaging device 100 of the above-described embodiments can include counters that are configured for infinite dynamic range sensing. The dynamic range of an image sensor describes the difference between the brightest and dimmest object that can be detected and discerned in an image. Conventional digital imaging approaches typically cannot achieve high dynamic ranges over three or four orders of magnitude, for example. Digitizing in-pixel, as is done for a computational pixel imaging device 100, can improve the dynamic range capability over conventional digital imaging sensors. However, digitizing in the pixel for high dynamic ranges presents challenges when trying to implement with small pixel sizes. To achieve a high dynamic range, the size of counters must be increased. An advanced CMOS process node may be used to reduce transistor and counter size, but such advanced microfabrication processes may be prohibitively expensive in some instances. Other approaches to reducing the size of digital-pixels (*e.g.*, to the 10 μm size or smaller) is desirable to reduce the size, weight, and power (SWaP) of imaging sensors and imaging devices. The inventors have recognized and appreciated the finite-bit counters (*e.g.*, an 8-bit counter) can be configured for unlimited dynamic range.

[0063] An example of circuitry for an infinite dynamic range counter 710 is depicted in **FIG. 7A**, according to some embodiments. As depicted in the drawing, circuitry for an infinite dynamic range counter 710 can include a *b*-bit counter, read/store logic 730 that is in communication with the counter, and memory 750. The counter 710 can comprise any type of counter described above, such as a ripple counter or synchronous counter or other types of counters. The read/store logic 730 may be embodied as processing logic that could be located on-chip or off-chip and that is configured to determine when to read the most significant bit or group of most significant bits of one or more counters of a computational pixel imaging device 100 and store in memory 750 information indicating that counters have rolled-over in count

value one or more times. In some cases, read/store logic 730 can be implemented as on-chip logic gates or field-programmable gate arrays located within each pixel, or located at an edge of an array 406 of pixel integrated circuits (*e.g.*, in one or more of data handlers 410, 412, 414, 416 referring to **FIG. 4**).

[0064] According to some embodiments, an infinite dynamic range counter 710 can comprise a *b*-bit counter in which the most significant bit (MSB) 720-b is interrogated differently than the lower bits 720-1, 720-2, ... 720-a. The size of the counter (value of b) can be any integer value of 2 or greater. In some implementations, the size of the counter is between 3 bits and 25 bits, though larger counters may be used in some cases. In various embodiments, the MSB 720-b is interrogated at a higher read-out rate than the lower bits. For long exposure periods and/or high signal levels, counters in some pixels can reach their maximum count value and roll-over to a value of 0 and continue counting up. If the roll-over is undetected, signal information is lost. By reading out the MSB or group of MSBs value(s) at a higher rate than the lower bits, roll-over events can be detected and recorded, so that subsequent image data read out for all bits of counters can be corrected to reflect accurate signal levels. A group of MSBs may be a counter's MSB and the next N lower bits (*e.g.*, bits *b*, *b*-1, *b*-2, ... *b*-N) where N is a positive, non-zero integer.

[0065] In some implementations, outputs from counters can be connected in parallel across corresponding counters in an array 406 of pixel integrated circuits, as described above in connection with **FIG. 5A** or **FIG. 5B**. In some cases, bit values for counters may be connected in parallel across corresponding counters in an array 406. For example, the data-shift lines may comprise parallel data lines 730, 740 with the number of parallel data lines equaling the number of counter bits. Additional multiplexers may be used for each of the parallel data lines. As such, a MSB from each counter in a row or column may be connected to a same data-shift line. In some cases, values of MSBs can be read from shared data-shift lines using a synchronous cadence read-out, for example. In other embodiments, the counter may be configured to pass bits between each counter unit that is used to record a bit, as depicted in **FIG. 7B**, for example, for as described in U.S. patent No. 9,768,785. In such cases, bit values for counters may not be connected in parallel across corresponding counters in an array 406. Instead, bit values may be shifted sequentially onto a same data-shift line.

[0066] In operation and according to some embodiments, an infinite dynamic range counter can work as follows. While counters accumulate count values during an exposure period, the values (logic levels) of the counters' MSBs (or groups of MSBs) can be read and monitored by read/store logic 730 over MSB data lines 740. In some implementations, when a counter's MSB toggles to a logic 1 state (or group of MSBs toggle to a predetermined value), the value may be

signaled to and/or detected by read/store logic 730 by placing the value on one or more data lines (*e.g.*, placing a MSB's value on data line 740). In some cases, a bit's value may be placed on a data line 740 by in-pixel logic, such as an AND gate, for example). In some cases, all MSB bit values (or groups of MSBs values) for all counters in the array 406 may then be destructively read out so that the MSB values that have toggled to 1 (or a predetermined value) are read and reset to 0. A toggling of the MSB (or group of MSBs) can indicate a roll-over of the *b-1* bits (or *b-N*-1) and an upcoming roll-over for the *b*-bit counter. A record of a counter's toggling or roll-over and address can be stored in memory 750 by the read/store logic 730. The address can be determined from the read address used to access the counter when all counters in the array are read or all counters in a row or column are read. In some cases, the address may be determined based upon clock cycles used to read counters in a row and/or column. Read/store logic may reset counters' MSB value(s) over control lines (*e.g.*, control line 742). The counters are then allowed to continue accumulating count values until a next MSB or group of MSBs toggles. The number of togglings or roll-overs for each counter can be accumulated in memory 750, where each toggling represents a count of $2^{(b-1)}$ (or $2^{(b-N-1)}$). For count down operation, roll-over events may be detected by detecting a logic 0 level, or by inverting the MSB output and detecting a logic 1 level.

[0067] In some embodiments, in-pixel logic or edge logic may be configured to detect, for example, a falling edge or negative edge of the b^{th} bit. For example, a monitor flip-flop may be configured to latch a logic 1 value to its output when the MSB value rolls over from 1 to 0. Additional in-pixel logic may assert output of the monitor flip-flop on a data line that can be detected and read. The monitor flip-flop can then be reset to detect a next falling edge of the MSB. In such embodiments, each detected logic 1 level from the monitor flip-flop indicates 2^b counts and the MSB does not need to be reset.

[0068] In some embodiments, instead of reading the entire array of counters after detecting a logic 1 on an MSB data line 740, only MSB values of counters (or monitor flip-flop outputs) in a row and/or column containing the counter that has toggled may be destructively read. Such a strategy may reduce read-out times and avoid reading of counters that have not yet had an MSB toggle. In yet other embodiments, time-gated row and column monitoring may be performed by read/store logic to detect and determine the location and address in the array 406 of a counter whose MSB value has toggled, and only that counter (or monitor flip-flop) will be destructively read.

[0069] In alternative embodiments, read-out times of counters' MSB values may be predicted based on prior count accumulations. For example, a first exposure over a first time period may be performed for a short duration in which none of the counters' MSB values roll over. First

count values can accumulate on the counters during this exposure period. In some cases, times for reading and resetting MSB values from one or more counters may be determined from the $(b\text{-}1)^{th}$ bit value (or other bit's value) of a relevant counter in the array. For example, when the $(b\text{-}1)^{th}$ bit value (or other bit value) of a first counter in the array toggles to a logic 1 level and the duration of the exposure period is known, a count rate for the counter can be determined. The count rate can be used to predict, on a subsequent longer exposure, when the counter's MSB value will toggle to a logic 1 level, *e.g.*, and must be read (*e.g.*, accumulate a roll-over count in memory 750) and/or reset. Accordingly, the count rates for all counters in an array 406 can be determined and used to predict when one or more counter's in the array will roll over. The information can then be used to determine, for longer exposures of a same scene, when to read the MSBs of the counters, either globally (reading all counters' MSBs sequentially in a read-out) or individually.

[0070] In some embodiments, the duration of the first exposure may be estimated based on prior images, or several exposure periods may be tried and linearity of increasing counts between at least two successive exposures checked to determine whether any of the counters have rolled over. If all counters have increased linearly or nearly-linearly in two successive exposures, then either exposure results may be used to estimate when roll-overs could occur.

[0071] In some implementations, a first exposure's duration may be determined and terminated automatically. For example, a counter's MSB value may be asserted on a row or column data-shift line as soon as the MSB toggles to a logic 1 level. The value may be asserted by in-pixel logic. Edge logic may detect the logic level and terminate the exposure period. Read/store logic 730 may then read-out all counters and process their count values to determine count-accumulation rates for each counter. The count-accumulation rates can then be used to determine when to read MSB values from one or more counters during a subsequent longer exposure period of a scene during which at least some counters' values would roll over.

[0072] In yet further embodiments of an infinite dynamic range counter, each counter may be divided equally or unequally into two bit groupings and each grouping may be used to accumulate counts. In such embodiments, the bit groupings may be read at different times and total counts accumulated in memory located outside the array of pixels. For example, a first of the two bit groupings (*e.g.*, bit 1 to bit $(b\text{-}N\text{-}1)$) can be read and reset at a first time, and subsequently the second of the bit groupings (bit $b\text{-}N$ to bit b) can be read and reset a second time, and the process repeated multiple times during an exposure period for an image. In some cases, the reading and resetting may alternate between the two bit groups for each successive read. In other cases, the read and reset rates may differ for the two groups. The read and reset rate for a bit group may be determined by any of the above-described methods for an infinite

dynamic range counter.

[0073] For computational pixel imagers that employ infinite dynamic range counting, additional operations may be executed on count accumulations that have been recorded in memory 750. For example, when on-chip data processing or data-shift operations occur (such as for filtering), then such operations can be mirrored or complied with using the count accumulation data in memory. For example, if counter values are shifted in the array 406 of a computational pixel imager, then addresses associated with off-array count accumulations may be updated to reflect the on-array shift of counter data.

[0074] Further details of example circuitry for a counter configured for infinite dynamic range operation are illustrated in **FIG. 7B**. In some implementations, a *b*-bit counter 710 may be configured as series-connected D or JK flip-flops 725-1, 725-2, ... 725-a, 725-b with reconfigurable data inputs D and reconfigurable clock inputs CLK. Each flip-flop can be used to store one bit. For count accumulation corresponding to a received signal, the flip-flop clock inputs can be reconfigured on-the-fly, so that the series of flip-flops operates as a ripple counter. For example, pulses 325 from the current-to-frequency converter 310 (referring to **FIG. 3A**) can be applied to the clock input of the first flip-flop 725-1 (least significant bit) and used to toggle the output of that flip-flop. The output of each flip-flop may then drive the clock of the next flip-flop to form a ripple counter. For read-out, the clocks of each flip-flop may be connected to a same read-out clock and the data inputs D connected to the data outputs Q of the preceding flip-flop, so that data can be shifted across and out of the counter 710.

[0075] For any of the above-described embodiments of counters, a tri-state buffer 770 may be used to place the output value Q of the flip-flop 725-b corresponding to the MSB on a data line 740, as illustrated in **FIG. 7B**. In some cases, additional tri-state buffers may be used for other flip-flops. For configurations where a counter is adapted for infinite dynamic range counting and wherein a toggling of the MSB to a logic 1 level can be automatically sensed, an AND gate 775 (or analogous logic circuitry) can be used to monitor the output of the MSB flip-flop 725-b and activate the tri-state buffer 770 when the MSB toggles to a logic 1 level. An advantage of using the tri-state buffer 770 is that a flip-flop's output Q can be isolated from the data line when the output Q is at a logic 0 level. In some implementations, the data line 740 may be a separate and dedicated data line for monitoring only the value of the MSB (*e.g.*, separate from a data line that is used to read out the entire counter value or to provide orthogonal shifting of counter values in the array 406). In other implementations, the data line 740 may be a same data line that is used to read out the entire counter value or to provide orthogonal shifting of counter values.

[0076] Counters configured for infinite dynamic range counting may be included in

computational pixel imagers having multiple counters in each pixel as described above (*e.g.*, for multi-thread signal processing). Counters configured for infinite dynamic range counting may also be included in computational pixel imagers configured for down-sampling of modulated signals, as described below in connection with **FIG. 9**.

[0077] Example read-out rates for MSB values are plotted in **FIG. 8** for various count accumulations rates from 1 MHz to 20 MHz and counter bit depths. The plotted MSB read-out rates correspond to rates required to avoid missing a roll-over event. The lines of count accumulations rates are, from top to bottom, 20 MHz, 10 MHz, 5 MHz, 2 MHz, and 1 MHz.

[0078] By monitoring, reading out MSB values of counters, and recording roll-over events in memory 750, long exposure durations can be performed and/or scenes with high intensity sources can be viewed and captured with high dynamic range. Counters may roll over multiple times during a high-dynamic range exposure period, and the number of roll-over events for a counter accumulated in memory 750. The number of roll-over events stored in memory 750 are in quanta of $2^{(b-1)}$ counts. At the end of a high-dynamic range exposure period, the number of counts for a counter indicated in memory 750 are combined with the final count value for the counter to obtain the total number of counts. By using the above approach for predicted read rates, the inventors have shown in simulations that total counts in excess of 10^6 can be accurately recorded for an 8-bit counter used in a pixel. The count accumulation rate was 10 MHz and the MSB read-out rate was 80 kHz. In this way, the dynamic range of a sensor can be increased to essentially any value, which is limited by the exposure duration or size of off-array memory 750. Memory 750 may be off chip in some cases or on-chip in circuitry located around an edge of the array 406.

[0079] Additional aspects are possible with a computational pixel imaging device 100. For example, pixel integrated circuits 120 (which can include multiple counters as describe above and/or infinite dynamic range counter circuitry) can be configured for digital pixel down-sampling in some implementations. For some applications, it can be desirable to detect the frequency or measure the phase of an intensity-modulated light source that is present in a scene or used to illuminate objects in a scene viewed by a computational pixel imaging device 100. For example, the phase of amplitude-modulated light returned from an object can contain information regarding the distance of the object from the observer. In-pixel digitization with two counters may be used to determine phase of amplitude-modulated light. For example, the two counters can be controlled to cyclically count up and down at a same frequency as the modulated source, but one counter's phase is shifted by 90º with respect to the other counter (*e.g.*, in-phase and quadrature detection). A limitation of using amplitude-modulated light to measure distance is that relatively high modulation frequencies (*e.g.*, MHz to GHz frequencies)

may be needed to achieve high distance resolution. The use of high modulation frequencies can challenge the ability of current-generation, up/down counting, digital-pixel electronics. In addition, the power requirements for detecting high-frequency modulations can be unacceptably high for some embodiments. The inventors have recognized and appreciated that apparatus and methods can be employed to adapt sensors of computational pixel imaging devices to down-sample the modulated signals so that relatively low frequency up/down counters can be used to detect phases of modulated signals at much higher frequencies.

[0080] **FIG. 9** illustrates an example of a pixel integrated circuit 920 adapted for digital down-sampling. The pixel integrated circuit may be used in pixels of a computational pixel imager and contain the same components as for the pixel integrated circuit 120 described above in connection with **FIG. 3A**, which will not be described again and are given same reference numbers. In some embodiments, a detector 905 of a computational pixel imager may be adapted to be biased with a modulated supply 910 that can provide, for example, a modulated bias or supply voltage to the detector. The modulated supply 910 may be located off-chip and provided to one or more pixels' detectors via bias lines. The detector 905 may be a *p-n* junction photodiode in some embodiments or may be a phototransistor, as illustrated in the drawing.

[0081] For digital down-sampling, the modulation of the supply 910 can be at a first frequency f_1 that differs from a second modulation frequency $f_2 = f_1 + \Delta f$ that is used to modulate the amplitude of a light source 902 that illuminates an object 904. The object 904 can be in a field of view that is imaged onto an array of detectors in a computations pixel imager. In some implementations, the light source 902 may comprise a laser, one or more laser diodes, one or more light-emitting diodes, *etc.* that is (are) driven by a second modulated supply 912. Modulated light can be returned (scattered or reflected) from the object 904 and detected by the modulated detector 905.

[0082] According to some implementations, one or both of the modulated supplies 910, 912 can be included with either or both of an array of pixel integrated circuits 120 or an array of detectors 110. In some implementations, one or both of the modulated supplies 910, 912 can be included in a computational pixel imaging system. In some cases, a computational pixel imaging system may be provided without the supplies 910, 920, but may have modulation inputs configured to receive one or both of the modulation signals from modulated supplies 910, 920.

[0083] In some embodiments, one of the frequencies f_1 or f_2 may be derived from the other (*e.g.*, by using a mixer that mixes f_1 with a signal from a source operating at the difference frequency Δf). In such embodiments, a computational pixel imager may include one or both of the difference-frequency source and high-frequency source. Further, an output from the difference-frequency source can be used to drive count-up and count-down cycles of one or

more counters instead of an output from a mixer.

[0084] The difference (Δf) between the two modulation frequencies f_1, f_2 can be significantly smaller than the value of either frequency. For example, the difference can be tens or hundreds of kilohertz (*e.g.*, between 10 kHz and 500 kHz) whereas the modulation frequencies can be in the megahertz to multi-gigahertz range. Modulation of the bias on the detector can change the sensitivity of the detector and/or effectively gate the detector on and off. The detector 910 can then act as a mixer and demodulate the received modulated optical signal so that the counters 330-1, 330-2, ... 330-M can detect at the difference frequency Δf. Using this technique, no loss of information from the modulated light source 902 will occur, and high-resolution distance determination and depth imagery can be achieved with low-frequency counters in pixel integrated circuits. For example, digital up-down counting during an exposure period can be performed at the difference frequency for in-phase/in-quadrature phase determination as described above. In some cases, the first and second frequencies f_1, f_2 can be provided to a mixer 915 (which may be included with a computational pixel imaging system). An output from the mixer can be used to generate a clock signal with clock generation circuitry 917. The generated clock signal may determine the periodicity of count-up and count-down cycles of one or more of the counters 330-1, 330-2, ... 330-M. A benefit to this technique is that pixel and device power can remain low while still measuring the return phase of a reflected signal.

[0085] In some implementations, an optical element (lens, diffractive optical element, *etc.*) can be placed in front of the optical source 902 to project a pattern of light onto the object. The pattern may be, for example, an array of spots or lines. Distortion of the pattern and/or distances to each portion of the pattern can be detected with a computational pixel imager, even though returned light from the pattern may be dim or not visible to the naked eye due to other illumination of a field of view. Analysis of the pattern distortion can be used to determine three-dimensional geometry of the object as well as one or more distances to the object.

[0086] A pixel integrated circuit can be embodied in different configurations. Example configurations include combinations of configurations (1) through (12) as described below.

[0087] Multiple counters can be included in one or more pixel integrated circuits of an array of pixel integrated circuits, and may not be included in every pixel of an array 406 (referring to **FIG. 4**. In some cases, the counters can be arranged in different configurations in one or more pixels of an array. In some implementations, the counters can be included in different configurations within a same pixel. **FIG. 10** depicts a pixel integrated circuit that includes an alternate configuration for multiple counters 1030-1, 1030-2, ... 1030-N. The illustrated configuration of counters can be included in one or more pixels of a computational pixel imager additionally or alternatively to the above-described configurations of counters.

[0088] In some applications, such as light detection and ranging (LIDAR), it is desirable to analyze the statistical properties of the received light. In LIDAR, for example, the time of arrival of photons returned from one or more objects, after a source has illuminated the object with a pulse of radiation, contains information about the distance to objects in the scene. However, the detection of unwanted background light, multiple reflections, or clutter photons can produce noise in detected photons that obscures the true distance to objects. The inventors have recognized and appreciated that examining a histogram of arrival times of received photons can aid in determining the true distance to object(s) of interest in an imaged scene. The inventors have further recognized and appreciated that calculating histograms may require a large amount of data to be read from conventional imaging devices which can lead to negative sensor size weight and power (SWaP) consequences. In some cases, it may not be possible to read data from an imager fast enough to calculate a meaningful histogram.

[0089] The pixel integrated circuit 1000 in **FIG. 10** illustrates an example configuration of multiple counters in a pixel integrated circuit that can allow acquisition of histogram data within a pixel and on chip. Such a pixel integrated circuit may include a multiplexer 1020 connected to an output of a signal converter 1010, a sequencer 1040 connected to the multiplexer 1020, and two or more counters 1030-1, 1030-2, ... 1030-N, connected to outputs of the multiplexer 1020. The signal converter 1010 can be a current-to-frequency converter (such as described in connection with **FIG. 3A**), a voltage-to-frequency converter, or a photon-to-frequency converter described further below that is arranged to receive a signal from the pixel's detector. In some implementations, the multiplexer 1020 is a 1:N multiplexer, where N is an integer greater than 1. The sequencer 1040 can be configured to connect, for periods of time, each counter to an output of the signal converter 1010 in a sequence so that each of the connected counters can receive an output signal 1025 for a period of time during an exposure period. According to some embodiments, the functionality of the multiplexer 1020 may be included in sequencer 1040 circuitry and a separate multiplexer may not be present.

[0090] According to some implementations, an output signal 1025 from a signal converter 1010 such as a current-to-frequency converter 310 (or voltage-to-frequency converter) can be provided to an input of a controllable multiplexer 1020. Output ports of the multiplexer can connect to two or more counters 1030-1, 1030-2, ... 1030-N. The counters can be implemented as any of the above-described counters, and their description need not be repeated. A sequencer 1040 can connect to a control input of the multiplexer 1020 and be used to issue signals (e.g., multi-bit control signals) to the multiplexer 1020 that determines to which counter the signal 1025 is routed. The sequencer 1040 may be located in the pixel or at the edge of an array of pixel integrated circuits. The sequencer 1040 may be activated or otherwise controlled by an

input signal CS_{in}, which can be received from on-chip or off-chip control logic. In some embodiments, the sequencer may be activated based on a signal issued to one or more counters (*e.g.*, a signal for a counter to start counting), and the sequencer may execute a sequence of commands (*e.g.*, an incrementing count) automatically in response to a received clock signal, for example.

[0091] According to some embodiments, a sequencer may comprise a counter that cycles through counts at a clock rate provided to the sequencer, though other logic circuitry may be used to generate sequence commands. The count values may select an output port of the multiplexor to which the received signal 1025 is routed. For example, a first counter 1030-1 may connect to an output port addressable with the bit sequence [0000], a second counter 1030-2 may connect to an output port addressable with the bit sequence [0001], a third counter may connect to an output port addressable with the bit sequence [0010], and so on. A sequencer 1040 that issues increasing bit counts to the multiplexer 1020 can then distribute the received signal 1025 in a sequential scan to the counters 1030-1, 1030-2, ... 1030-N. In some implementations, by rapidly scanning the received signal 1025 (or connection to the output of the signal converter 1010) across the counters, counts can be accumulated in the counters that depend upon the amount of intensity (or number of photons) received in a time window or bin during which the counter is selected by the multiplexer 1020 and sequencer 1040. The resulting counts in the counters 1030-1, 1030-2, ... 1030-N can then be representative of a histogram of photon arrival times at the pixel's detector, according to some implementations. In a photon counting mode (or Geiger mode) described further below, the counts in each counter can be representative of a number of photons detected during a time interval for which the counter is selected.

[0092] The sequence of scanning the output signal 1025 from the signal converter 1010 to the counters 1030-1, 1030-2, ... 1030-N need not be in a sequence as illustrated and described above. For example, the sequencer 1040 may be programmed to select counters in a reverse order (*e.g.*, from counter N to counter 1) or any other sequence (*e.g.*, counter 1, counter N, counter 2, ...). Further, the dwell time for each counter selected need not be equal.

[0093] With an appropriate detector element used to detect single photons, the CPI architecture can be adapted for photon counting, in some implementations. Additionally or alternatively, the CPI architecture may be adapted for time-of-arrival of received photons. Advantageously, the pixel front-end of a pixel integrated circuit can support high voltage bias, avalanche detection, and fast reset. For photon counting mode, counters 1030-1, 1030-2, ... 1030-N can be driven by avalanche resets of the voltage at node 308. For example, with a biased and high-sensitivity detector, a detected photon can produce an avalanche of carriers

leading to a large current pulse delivered to the signal converter 1010. The current pulse can produce an avalanche reset of a capacitor C_0 in the converter 1010. As such, each pulse of the output signal can correspond to one detected photon and avalanche reset of the capacitor, *e.g.*, at node 308 referring to **FIG. 3A**. In such embodiments, the number of counts in each counter can then indicate the number of photons detected during the time the counter was selected. In this photon counting mode, the signal converter acts as a photon-to-pulse converter. For time-of-arrival measurements, the selection of counters in a sequence can be driven by fast clock edges. In such embodiments, the number of counts in each counter can indicate a time of arrival and amount of intensity received during the time the counter was selected.

[0094] As an example, time-of-arrival histograms can be acquired in one or more pixels having counters configured as shown in **FIG. 10**. To acquire an N-bin histogram, N counters are used in a pixel. The size of the counter will determine the number of events that can be counted in each bin of the histogram. For example, a *b*-bit counter can accumulate *b* occurrences (e.g., single photon detections) within a bin, or more if the *b*-bit counter is configured for infinite dynamic range counting as described above. The multiplexer 1020 and sequencer 1040 can cycle the signal 1025 and connection to converter 1010 through all counters in a sequence. The dwell time at each counter (the time during which the counter is enabled or selected by the sequencer 1040 and multiplexer 1020) determines a time bin for the counter and the number of counts accumulated by a counter is representative of a number of photons (or intensity) received during the time bin. In some embodiments, the counts in the counters 1030-1, 1030-2, … 1030-N can be read out after a single sequence. In other cases, the counts may be read out after multiple sequences to increase the number of accumulated counts in the counters and improve the signal-to-noise ratio (SNR). By looking at the number of counts recorded by each counter and knowing the times at which the counters were active, it is possible to determine the time-of-arrival of an optical pulse. The time of arrival may be based on count values from two or more of the counters. Any suitable metric may be used as time-of-arrival, *e.g.*, peak of histogram (which can correspond to a peak intensity of the detected optical pulse) or rising half-value of histogram (which can correspond to a rising half-intensity point of a detected pulse).

[0095] In a system configuration, a pulsed light source may be included with the computational pixel imager in a camera. The sequencer 1040 may be triggered to begin issuing one or more sequences of commands to the multiplexer 1020 (with or without a delay) when the light source is pulsed to illuminate objects in an imaged scene.

[0096] In some implementations, background signal may be removed from the detected signal. For example, a background count (down count if image is acquired using up counts) can be collected on each counter for an equivalent time period to that used for histogram acquisition

on each counter. The background count can be acquired in the absence of a pulse of light from the pulsed illumination source. The background count could be collected, for example, just before or just after each laser pulse. The resulting count in each bin after acquiring the background count and performing a histogram acquisition represents only counts generated due to the return pulse and random noise. As such, in-pixel background removal can be performed prior to read-out of image data and/or histogram data.

[0097] Histogram acquisition may be performed in other ways with a computational pixel imager. For example and referring again to **FIG. 3B**, a sequencer and/or multiplexer may be arranged to sequentially activate the second transistors 307-1, 307-2, ... 307-N for sequential periods of time. In such embodiments, the outputs of the different signal converters 310-1, 310-2, ... 310-N may connect to separate counters or groups of counters and an output multiplexer 340 may not be present. Further, the signal converters may all be configured to operate in the same way. The separate counters can then acquire histogram data that is representative of, for example, photon arrival time or number of detected photons.

[0098] A pixel integrated circuit can be embodied in different configurations. Example configurations include combinations of configurations (1) through (12) as described below.

(1) A pixel integrated circuit in an array of pixel integrated circuits, the pixel integrated circuit comprising: a signal converter, wherein the signal converter is arranged to receive a signal from a detector; a multiplexer connected to an output of the signal converter; and two or more counters connected to outputs of the multiplexer.

(2) The pixel integrated circuit of configuration (1), further comprising a sequencer connected to a control input of the multiplexer.

(3) The pixel integrated circuit of configuration (2), wherein the sequencer sends digital signals to the multiplexer to select a first of the two or more counters to connect to the output of the signal converter for a first period of time and to select a second of the two or more counters to connect to the output of the signal converter for a second period of time.

(4) The pixel integrated circuit of configuration (2) or (3), wherein the sequencer comprises a counter that issues count values to the multiplexer.

(5) The pixel integrated circuit of any one of any one of configurations (1) through (4), wherein the signal converter is a current-to-frequency signal converter.

(6) The pixel integrated circuit of any one of any one of configurations (1) through (5), wherein the signal converter is a photon-to-pulse signal converter.

(7) The pixel integrated circuit of any one of any one of configurations (1) through (6), wherein a first counter of the two or more counters comprises a plurality of flip-flops.

(8) The pixel integrated circuit of configuration (7), wherein an output of a flip-flop corresponding to the most significant bit for the first counter connects to a tri-state buffer.

(9) The pixel integrated circuit of configuration (8), further comprising: data input multiplexers connected to a data inputs of the plurality of flip-flops; and clock input multiplexers connected to the clock inputs of the plurality of flip-flops.

(10) The pixel integrated circuit of any one of configurations (7) through (9), wherein the first counter can be configured as a counter and as a shift register.

(11) The pixel integrated circuit of any one of any one of configurations (1) through (10), wherein a counter of the two or more counters comprises: a *b*-bit counter; a data line arranged to transmit a value of a most significant bit of the *b*-bit counter; and read-out circuitry configured to read the most significant bit at a higher read-out rate than a read-out rate for other bits of the *b*-bit counter.

(12) The pixel integrated circuit of any one of any one of configurations (1) through (11), wherein the array is located adjacent to an imaging plane of an optical assembly.

[0099] Methods for operating a pixel integrated circuit of any of the above or below configurations can include various processes. Example methods include combinations of processes (13) through (20) as described below.

(13) A method of acquiring in-pixel histograms, the method comprising: converting, with a signal converter located in a pixel integrated circuit of an array of pixel integrated circuits, an analog signal received from a detector to an output signal; and directing the output signal to different counters included in the pixel integrated circuit in a sequence of different times during an exposure period for the detector.

(14) The method of (13), wherein the converting comprises current-to-frequency conversion.

(15) The method of (13) or (14), wherein the converting comprises photon-to-pulse conversion.

(16) The method of any one of (13) through (15), wherein the directing is performed, at least in part, with a multiplexer.

(17) The method of (16), wherein the directing further comprises providing a sequence of commands, with a sequencer, to the multiplexer that connects an output from the signal converter to a first counter of the different counters for a first period of time and connects an output from the signal converter to a second counter of the different counters for a second period of time.

(18) The method of (17), wherein the first period had a duration that is different from the second period.

(19) The method of any one of (13) through (18), further comprising determining a number of photons detected by at least one of the different counters.

(20) The method of any one of (13) through (19), further comprising determining a time of arrival of an optical pulse based on count values from two or more of the different counters.

[0100] A computational pixel imager can be embodied in different configurations. Example configurations include combinations of configurations (21) through (28) as described below. Any of these configurations may include features from configurations (1) through (12) above.

(21) A computational pixel imager having an array of pixels, one or more of the pixels comprising: a detector; a signal converter connected to receive a signal from the detector; a multiplexer connected to an output of the signal converter; and two or more counters connected to outputs of the multiplexer.

(22) The computational pixel imager of configuration (21), further comprising a sequencer connected to a control input of the multiplexer.

(23) The computational pixel imager of configuration (21) or (22) wherein the signal converter is a current-to-frequency signal converter.

(24) The computational pixel imager of any one of configurations (21) through (23), wherein the signal converter is a photon-to-pulse signal converter.

(25) The computational pixel imager of any one of configurations (21) through (24), wherein a first counter of the two or more counters comprises a plurality of flip-flops.

(26) The computational pixel imager of configuration (25), wherein the first counter can be configured as a counter and as a shift register during operation of the computational pixel imager.

(27) The computational pixel imager of any one of configurations (21) through (26), wherein a counter of the two or more counters comprises: a b-bit counter; a data line arranged to transmit a value of a most significant bit of the b-bit counter; and read-out circuitry configured to read the most significant bit at a higher read-out rate than a read-out rate for other bits of the b-bit counter.

(28) The computational pixel imager of any one of configurations (21) through (27) included in a camera.

CONCLUSION

[0101] Unless stated otherwise, the terms "approximately" and "about" are used to mean within ± 20% of a target value in some embodiments, within ± 10% of a target value in some embodiments, within ± 5% of a target value in some embodiments, and yet within ± 2% of a

target value in some embodiments. The terms "approximately" and "about" can include the target value. The term "essentially" is used to mean within ± 3% of a target value.

[0102] The technology described herein may be embodied as a method, of which at least some acts have been described. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be implemented in which acts are performed in an order different than described, which may include performing some acts simultaneously, even though described as sequential acts in illustrative embodiments. Additionally, a method may include more acts than those described, in some embodiments, and fewer acts than those described in other embodiments.

[0103] Having thus described at least one illustrative embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

CLAIMS

What is claimed is:

1. A pixel integrated circuit in an array of pixel integrated circuits, the pixel integrated circuit comprising:

a signal converter, wherein the signal converter is arranged to receive a signal from a detector;

a multiplexer connected to an output of the signal converter; and

two or more counters connected to outputs of the multiplexer.

2. The pixel integrated circuit of claim 1, further comprising a sequencer connected to a control input of the multiplexer.

3. The pixel integrated circuit of claim 2, wherein the sequencer sends digital signals to the multiplexer to select a first of the two or more counters to connect to the output of the signal converter for a first period of time and to select a second of the two or more counters to connect to the output of the signal converter for a second period of time.

4. The pixel integrated circuit of claim 2, wherein the sequencer comprises a counter that issues count values to the multiplexer.

5. The pixel integrated circuit of any one of claims 1 through 4, wherein the signal converter is a current-to-frequency signal converter.

6. The pixel integrated circuit of any one of claims 1 through 4, wherein the signal converter is a photon-to-pulse signal converter.

7. The pixel integrated circuit of any one of claims 1 through 4, wherein a first counter of the two or more counters comprises a plurality of flip-flops.

8. The pixel integrated circuit of claim 7, wherein an output of a flip-flop corresponding to the most significant bit for the first counter connects to a tri-state buffer.

9. The pixel integrated circuit of claim 8, further comprising:

data input multiplexers connected to a data inputs of the plurality of flip-flops; and

clock input multiplexers connected to the clock inputs of the plurality of flip-flops.

10. The pixel integrated circuit of claim 7, wherein the first counter can be configured as a counter and as a shift register.

11. The pixel integrated circuit of any one of claims 1 through 4, wherein a counter of the two or more counters comprises:

a *b*-bit counter;

a data line arranged to transmit a value of a most significant bit of the *b*-bit counter; and

read-out circuitry configured to read the most significant bit at a higher read-out rate than a read-out rate for other bits of the *b*-bit counter.

12. The pixel integrated circuit of any one of claims 1 through 4, wherein the array is located adjacent to an imaging plane of an optical assembly.

13. A method of acquiring in-pixel histograms, the method comprising:

converting, with a signal converter located in a pixel integrated circuit of an array of pixel integrated circuits, an analog signal received from a detector to an output signal; and

directing the output signal to different counters included in the pixel integrated circuit in a sequence of different times during an exposure period for the detector.

14. The method of claim 13, wherein the converting comprises current-to-frequency conversion.

15. The method of claim 13, wherein the converting comprises photon-to-pulse conversion.

16. The method of claim 13, wherein the directing is performed, at least in part, with a multiplexer.

17. The method of claim 16, wherein the directing further comprises providing a sequence of commands, with a sequencer, to the multiplexer that connects an output from the signal converter to a first counter of the different counters for a first period of time and connects an output from the signal converter to a second counter of the different counters for a second period of time.

18. The method of claim 17, wherein the first period had a duration that is different from the second period.

19. The method of any one of claims 13 through 18, further comprising determining a number of photons detected by at least one of the different counters.

20. The method of any one of claims 13 through 18, further comprising determining a time of arrival of an optical pulse based on count values from two or more of the different counters.

21. A computational pixel imager having an array of pixels, one or more of the pixels comprising:

a detector;

a signal converter connected to receive a signal from the detector;

a multiplexer connected to an output of the signal converter; and

two or more counters connected to outputs of the multiplexer.

22. The computational pixel imager of claim 21, further comprising a sequencer connected to a control input of the multiplexer.

23. The computational pixel imager of claim 21 or 22, wherein the signal converter is a current-to-frequency signal converter.

24. The computational pixel imager of claim 21 or 22, wherein the signal converter is a photon-to-pulse signal converter.

25. The computational pixel imager of claim 21 or 22, wherein a first counter of the two or more counters comprises a plurality of flip-flops.

26. The computational pixel imager of claim 15, wherein the first counter can be configured as a counter and as a shift register during operation of the computational pixel imager.

27. The computational pixel imager of claim 21 or 22, wherein a counter of the two or more counters comprises:

a b-bit counter;

a data line arranged to transmit a value of a most significant bit of the b-bit counter; and

read-out circuitry configured to read the most significant bit at a higher read-out rate than a read-out rate for other bits of the b-bit counter.

28. The computational pixel imager of claim 21 or 22 included in a camera.

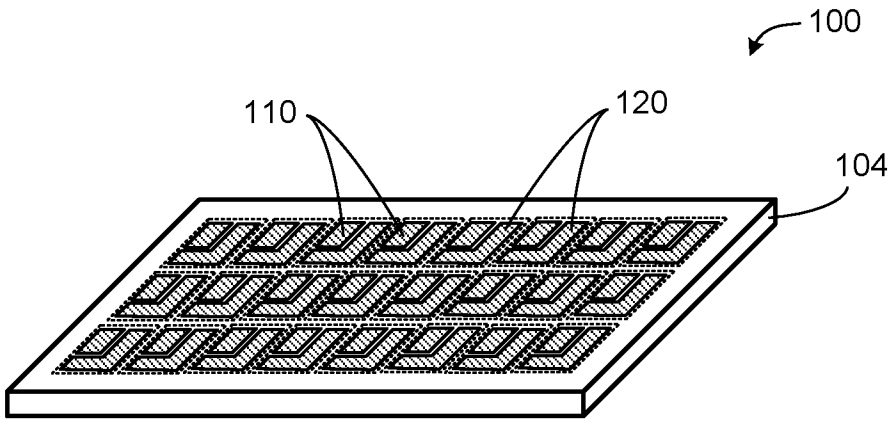


FIG. 1A

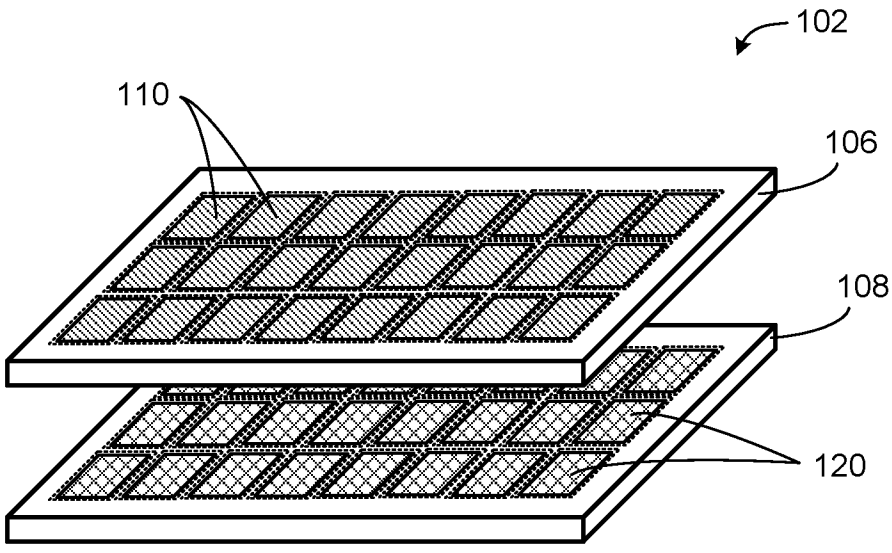


FIG. 1B

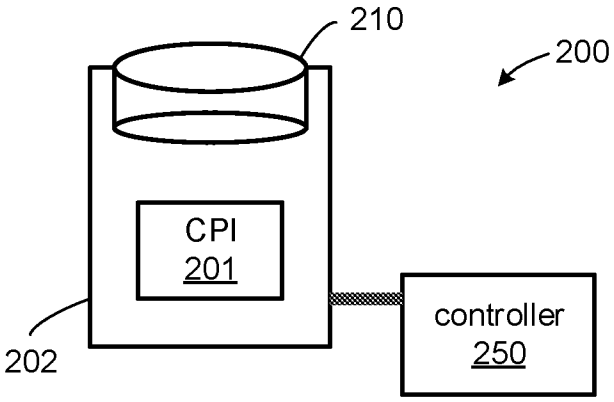

210
200
CPI
201
controller
250
202

FIG. 2

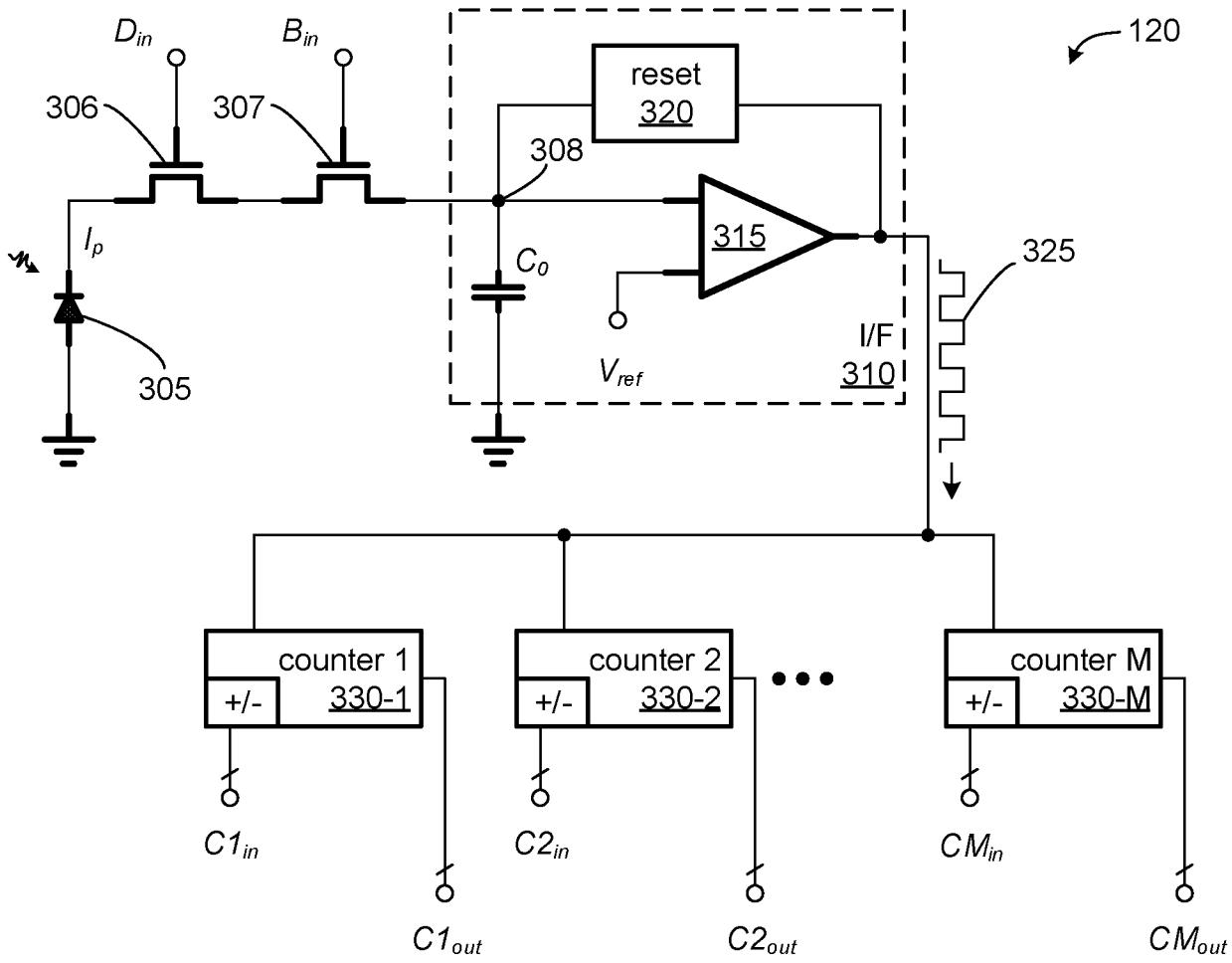

D_{in}
B_{in}
120
306
307
reset
320
308
I_p
315
325
C_0
V_{ref}
I/F
310
305
counter 1
+/-
330-1
counter 2
+/-
330-2
counter M
+/-
330-M
$C1_{in}$
$C2_{in}$
CM_{in}
$C1_{out}$
$C2_{out}$
CM_{out}

FIG. 3A

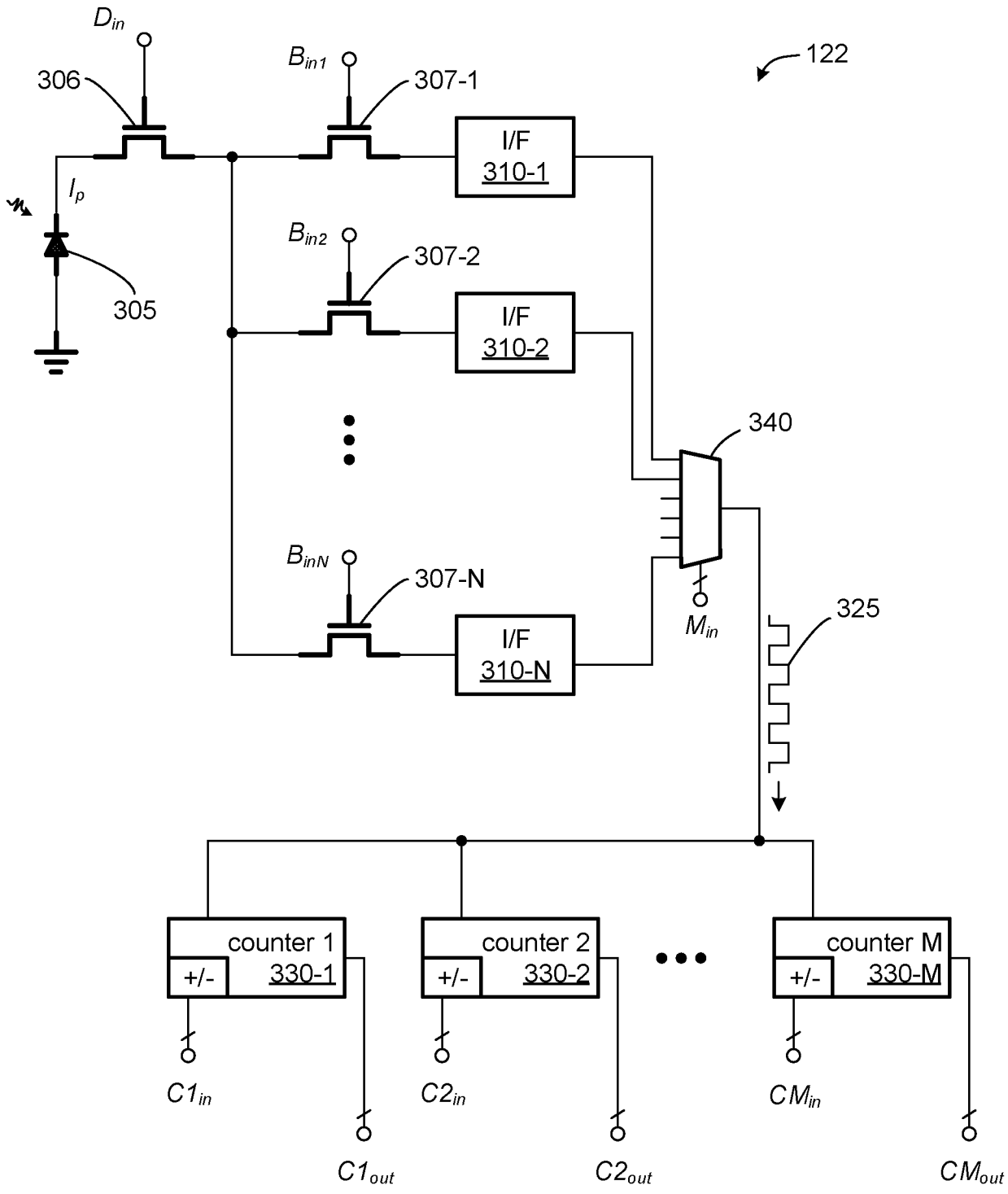

D_{in}
306
B_{in1}
307-1
122
I/F
310-1
I_p
B_{in2}
307-2
305
I/F
310-2
340
B_{inN}
307-N
M_{in}
325
I/F
310-N
counter 1
+/-
330-1
counter 2
+/-
330-2
counter M
+/-
330-M
$C1_{in}$
$C2_{in}$
CM_{in}
$C1_{out}$
$C2_{out}$
CM_{out}

FIG. 3B

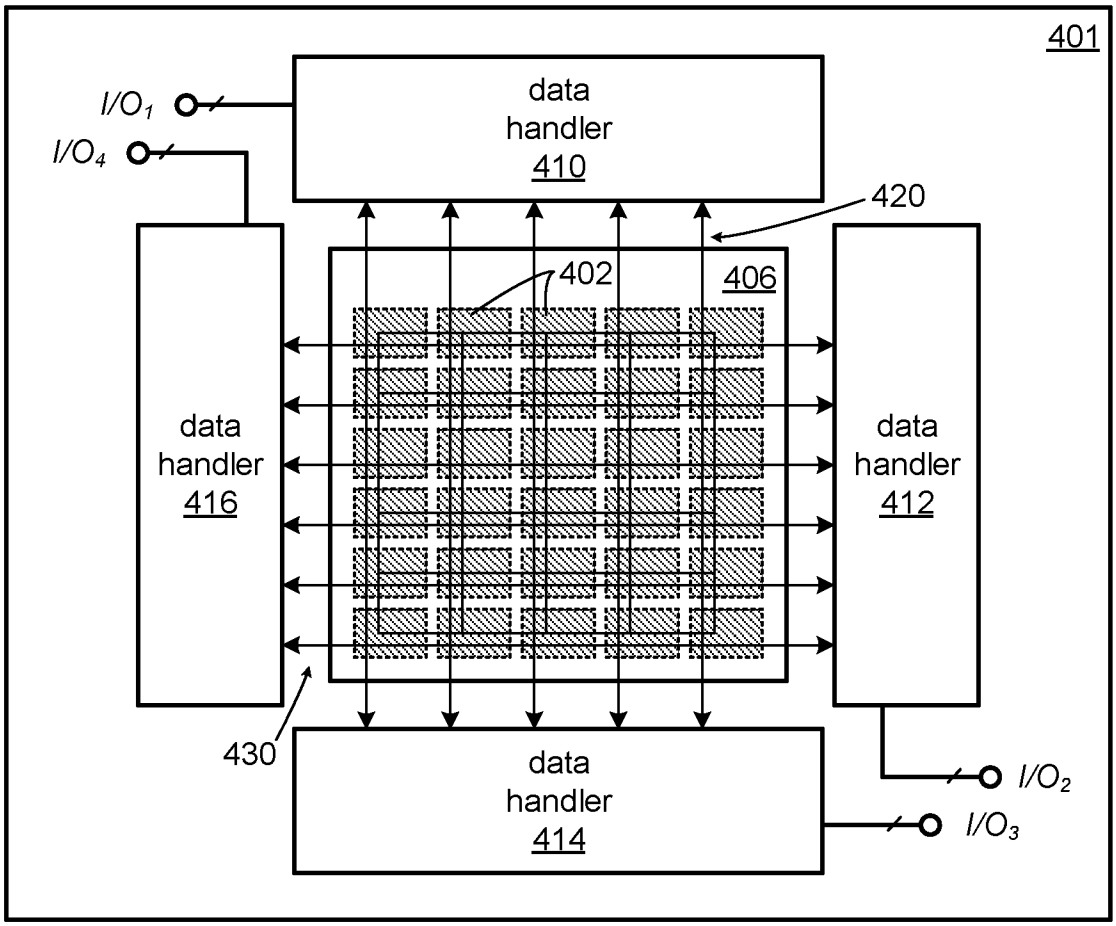

401
I/O1
I/O4
data handler 410
420
402
406
data handler 416
data handler 412
430
data handler 414
I/O2
I/O3

FIG. 4

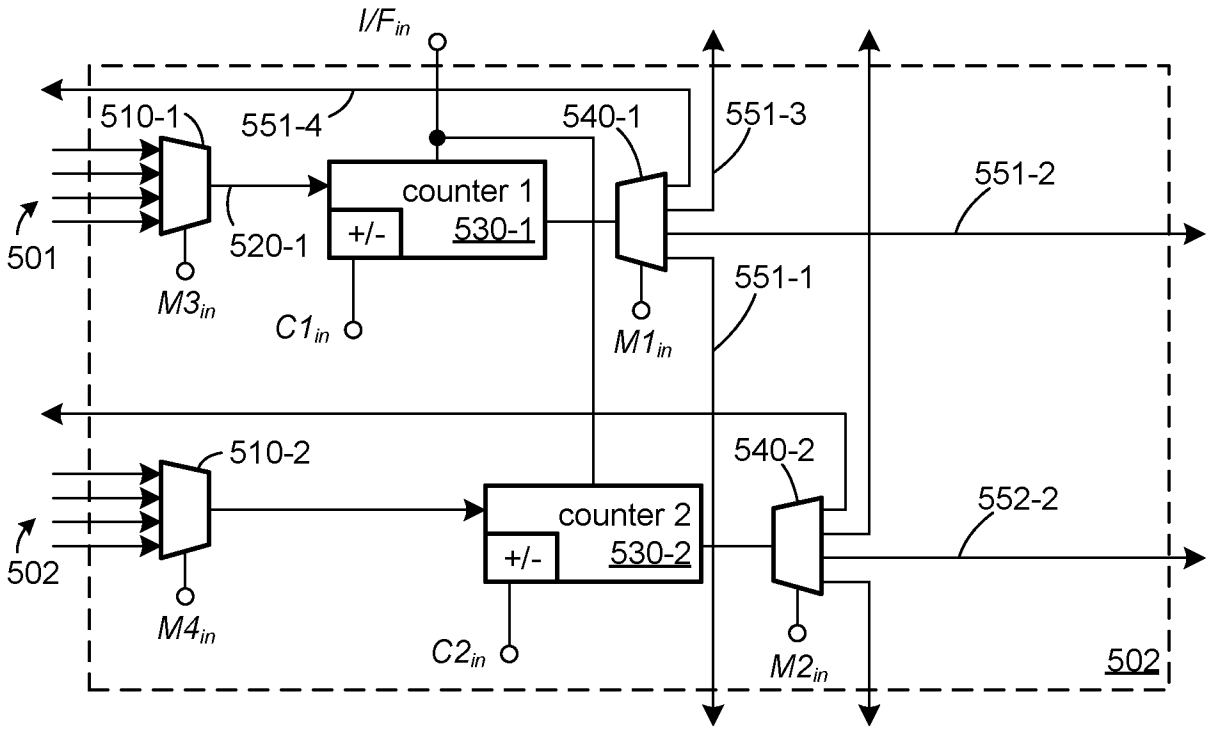

I/Fin
510-1
551-4
540-1
551-3
551-2
counter 1
+/-
530-1
501
520-1
M3in
C1in
M1in
551-1
510-2
540-2
552-2
counter 2
+/-
530-2
502
M4in
C2in
M2in
502

FIG. 5A

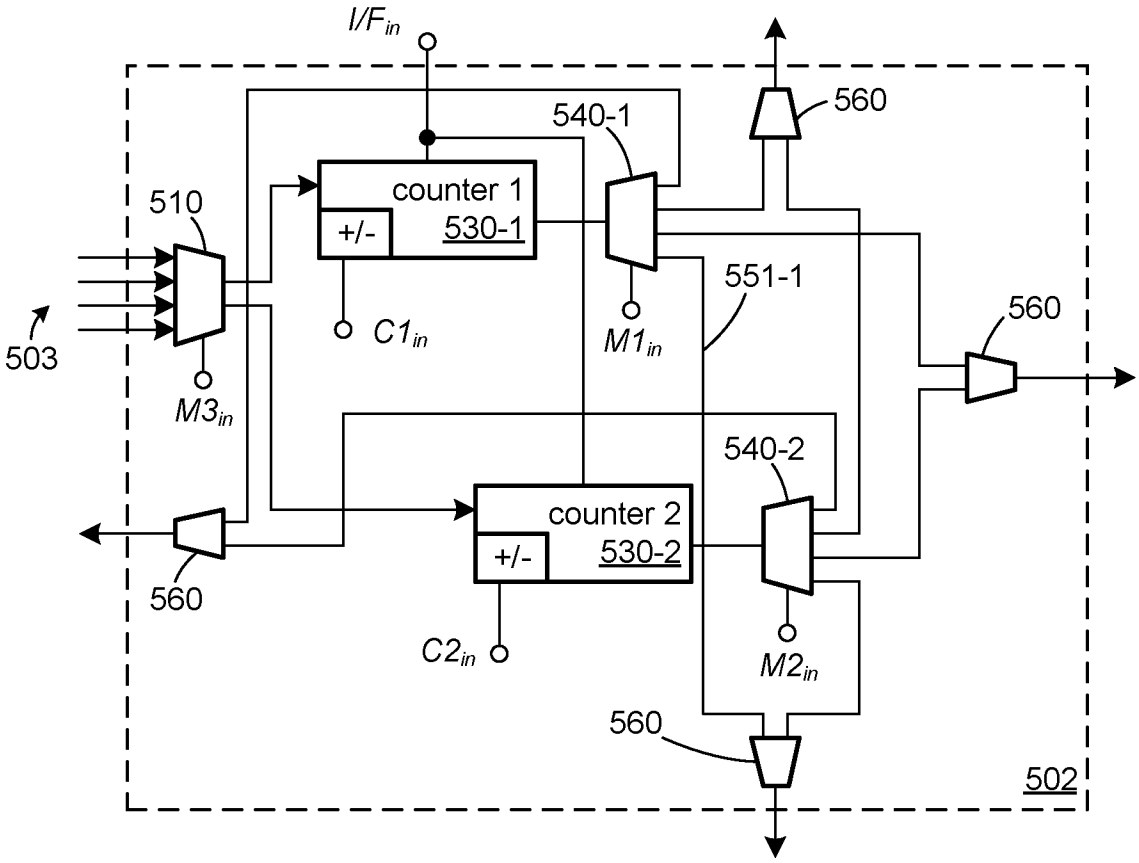

I/F_in
540-1
560
counter 1
+/-
530-1
510
551-1
560
503
C1_in
M1_in
M3_in
540-2
counter 2
+/-
530-2
560
C2_in
M2_in
560
502

FIG. 5B

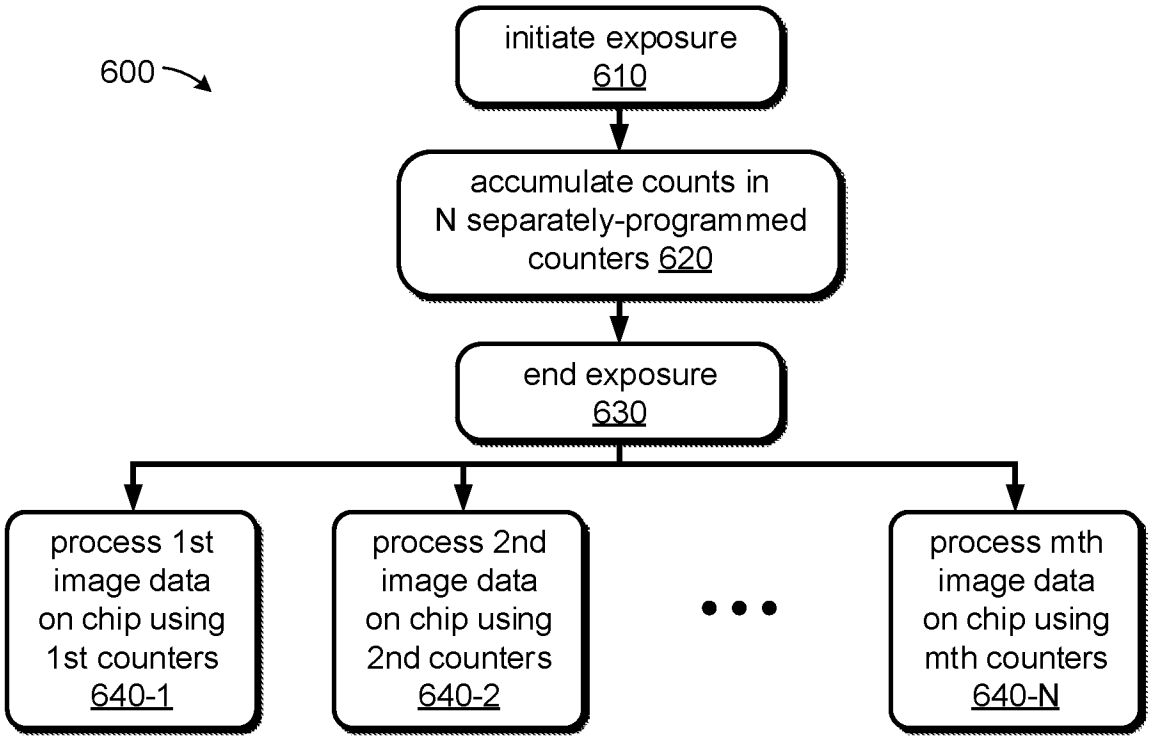

600
initiate exposure
610
accumulate counts in
N separately-programmed
counters 620
end exposure
630
process 1st
image data
on chip using
1st counters
640-1
process 2nd
image data
on chip using
2nd counters
640-2
• • •
process mth
image data
on chip using
mth counters
640-N

FIG. 6

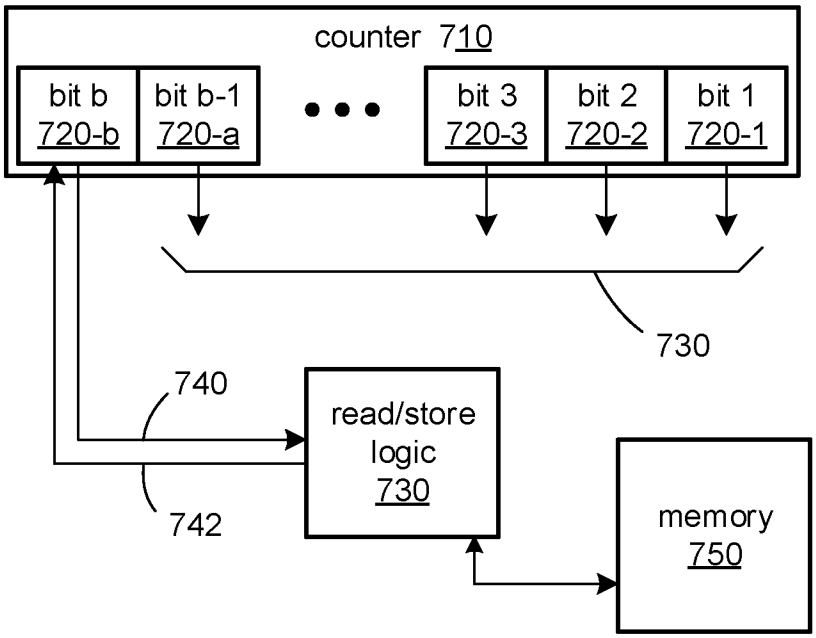

counter 710
bit b
720-b
bit b-1
720-a
bit 3
720-3
bit 2
720-2
bit 1
720-1
730
740
742
read/store
logic
730
memory
750

FIG. 7A

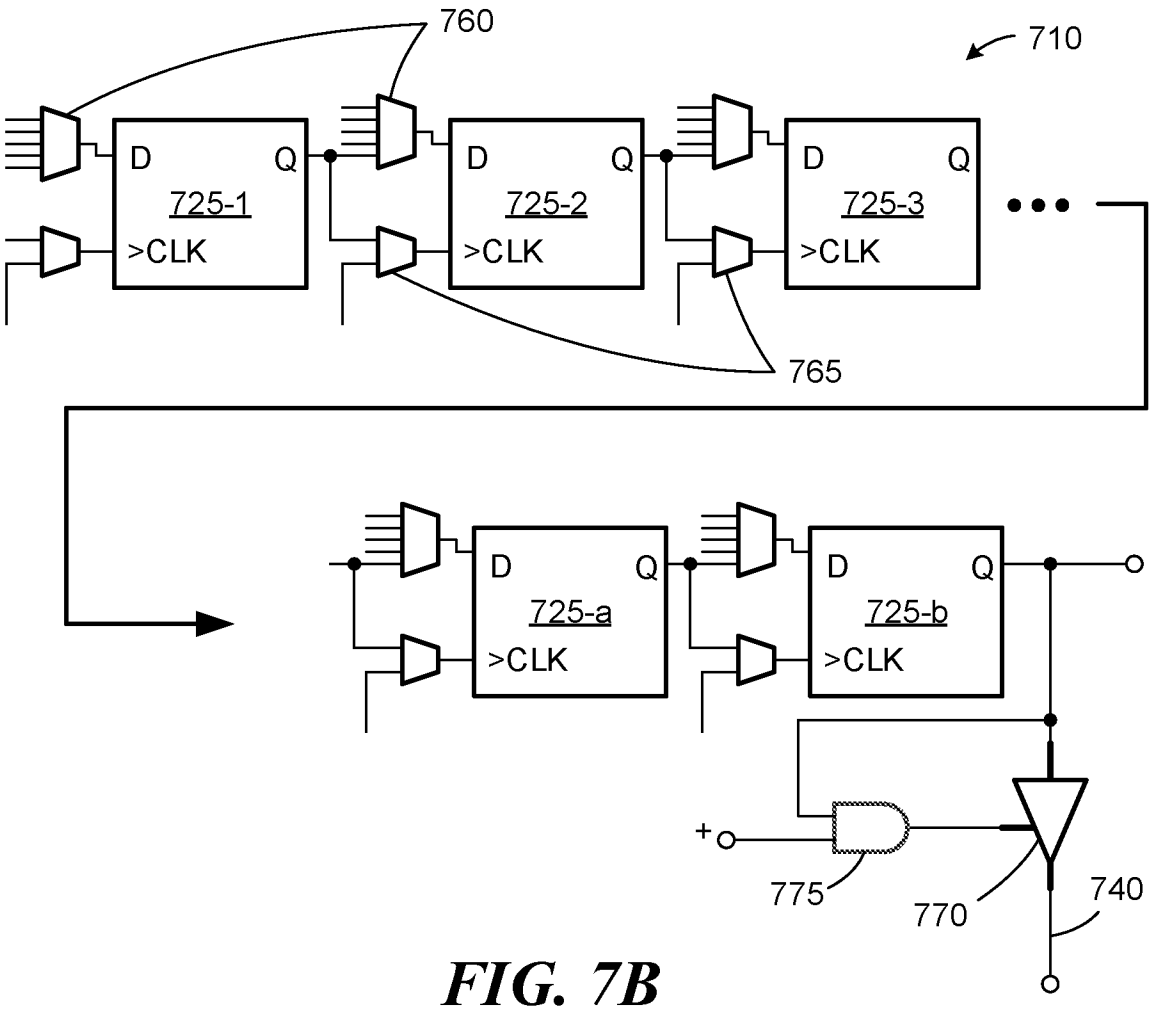

760
710
D
Q
725-1
>CLK
725-2
725-3
765
725-a
725-b
775
770
740

FIG. 7B

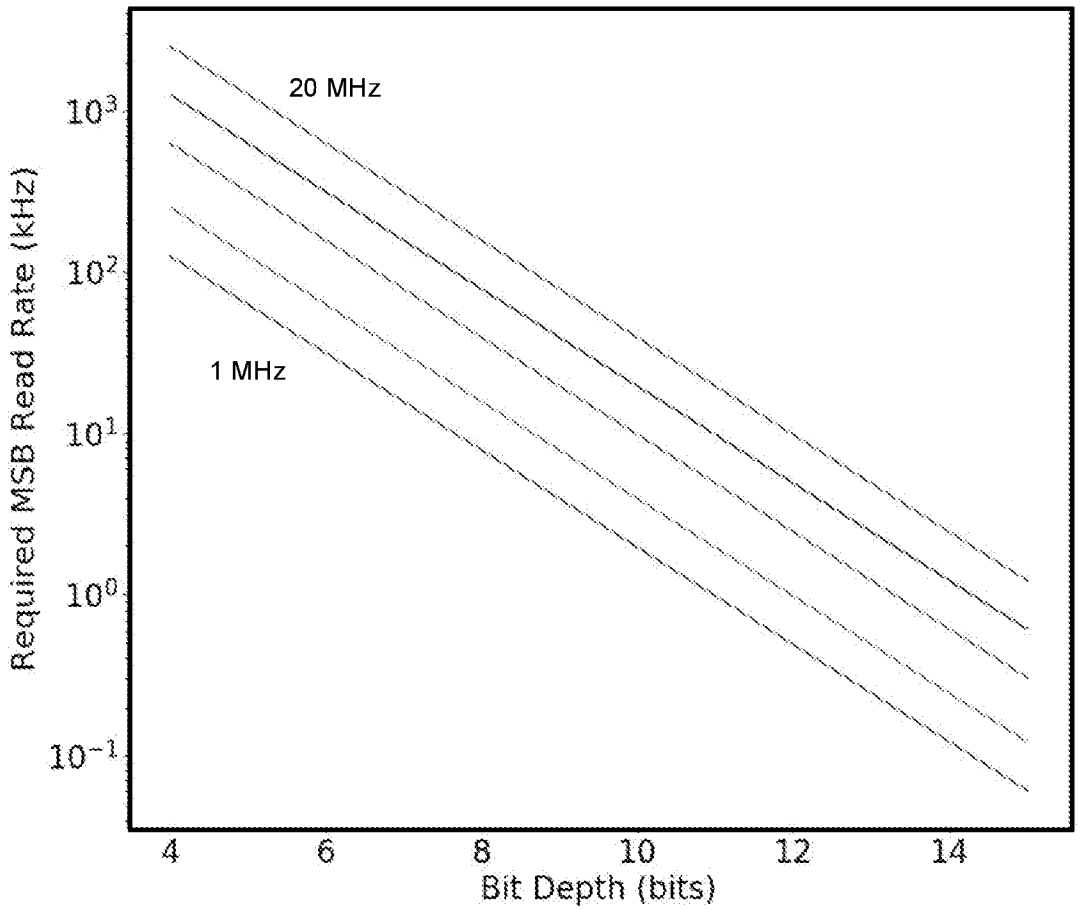

20 MHz
1 MHz
Required MSB Read Rate (kHz)
10^3
10^2
10^1
10^0
10^{-1}
4
6
8
10
12
14
Bit Depth (bits)

FIG. 8

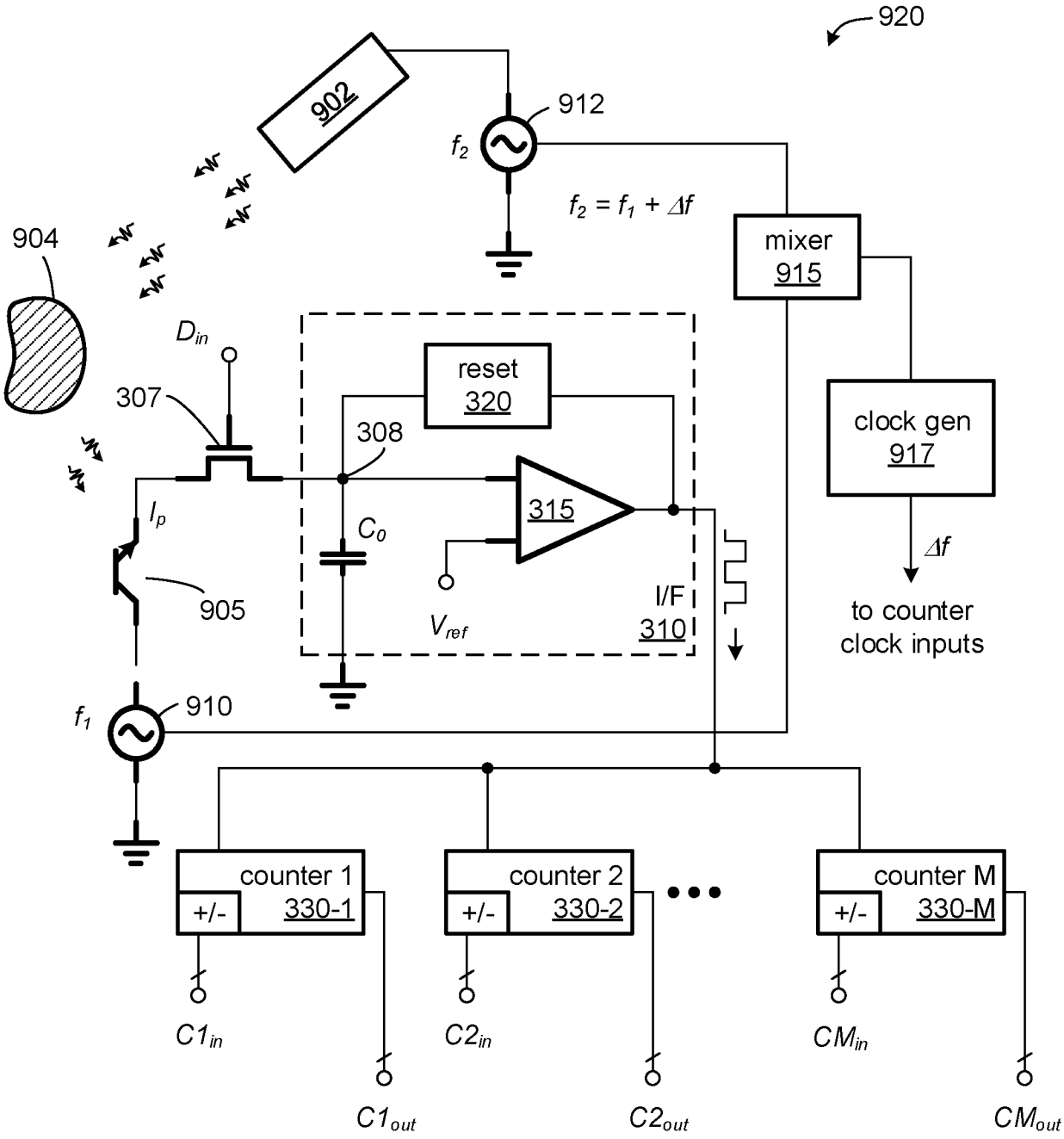

920
902
912
f_2
$f_2 = f_1 + \Delta f$
mixer
915
904
D_{in}
307
reset
320
308
clock gen
917
315
I_p
C_0
Δf
905
V_{ref}
I/F
310
to counter
clock inputs
f_1
910
counter 1
+/-
330-1
counter 2
+/-
330-2
counter M
+/-
330-M
$C1_{in}$
$C2_{in}$
CM_{in}
$C1_{out}$
$C2_{out}$
CM_{out}

FIG. 9

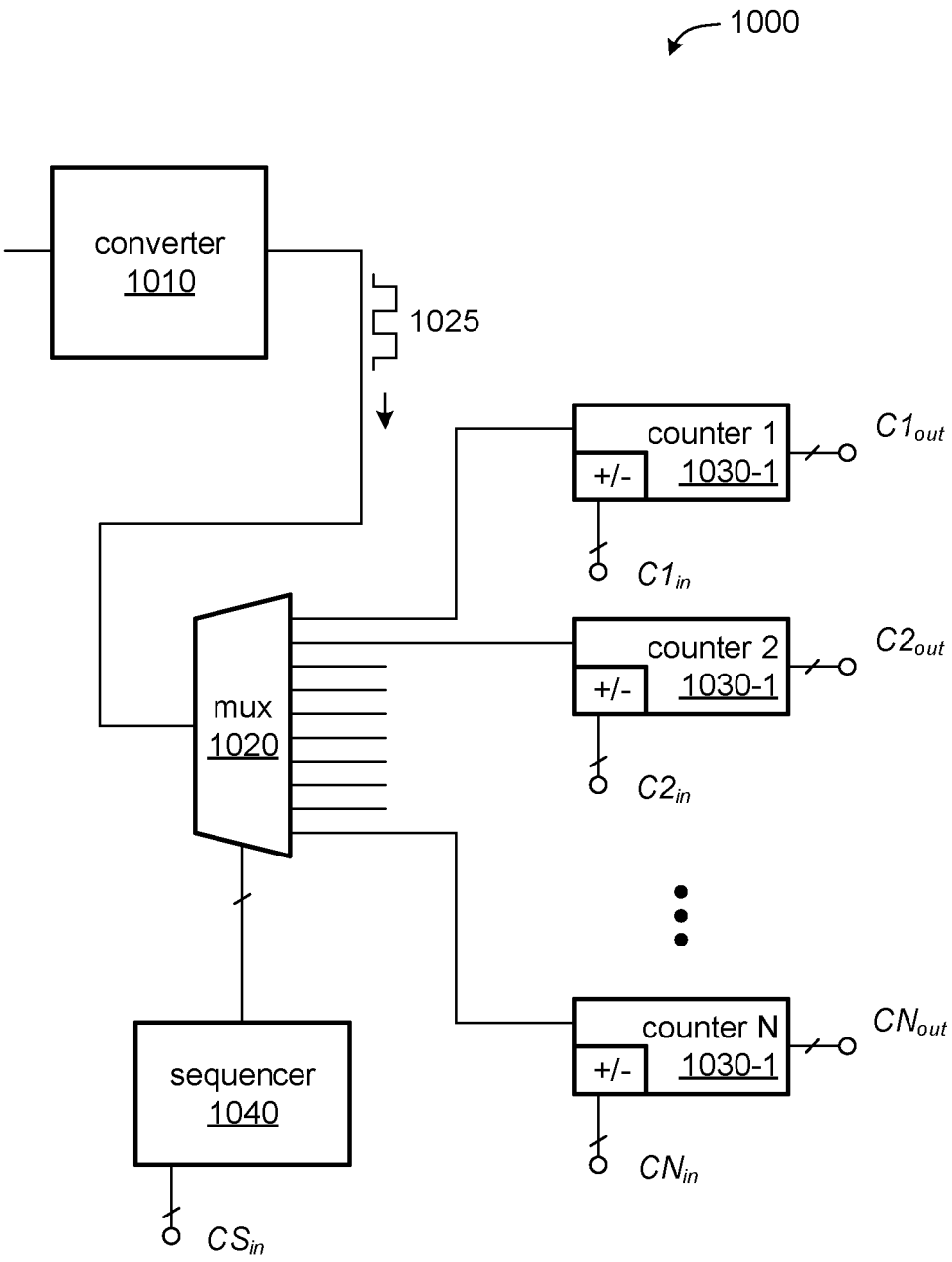

1000
converter
1010
1025
counter 1
+/-
1030-1
$C1_{out}$
$C1_{in}$
mux
1020
counter 2
+/-
1030-1
$C2_{out}$
$C2_{in}$
counter N
+/-
1030-1
CN_{out}
CN_{in}
sequencer
1040
CS_{in}

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/016593

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01S7/4865 G01S17/894
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007/182949 A1 (NICLASS CRISTIANO [CH]) 9 August 2007 (2007-08-09) paragraph [0045] - paragraph [0064] -----	1-7, 12-28 8-11
Y	US 2013/003911 A1 (SCHULTZ KENNETH I [US] ET AL) 3 January 2013 (2013-01-03) paragraph [0041] - paragraph [0046]; figures 2-4 -----	8-10
Y	US 2011/235771 A1 (AULL BRIAN F [US] ET AL) 29 September 2011 (2011-09-29) paragraph [0027] ----- -/--	11

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 April 2020	11/05/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Penchev, Petyo

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2020/016593

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CRISTIANO NICLASS ET AL: "Single-Photon Synchronous Detection", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE, USA, vol. 44, no. 7, 1 July 2009 (2009-07-01), pages 1977-1989, XP011263252, ISSN: 0018-9200, DOI: 10.1109/JSSC.2009.2021920 page 1978 - page 1979; figures 2,3 -----	1-7, 12-28

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2020/016593

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO 2013006188 A1	10-01-2013
US 2011235771 A1	29-09-2011	US 2011235771 A1	29-09-2011
		WO 2011119306 A1	29-09-2011