

[54] CATHODE RAY TUBE CONTROL
APPARATUS FOR DISPLAYING UPPER
AND LOWER CASE CHARACTERS USING A
SINGLE MATRIX

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[22] Filed: Jan. 2, 1973

[21] Appl. No.: 320,039

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Reiling

[52] U.S. Cl. 340/324 AD, 178/15, 178/30,
354/6

[51] Int. Cl. G06f 3/14

[58] Field of Search..... 340/324 A, 324 AD, 336;
315/18, 19, 22, 29; 178/6.8, 15, 30; 95/4.5
R, 4.5 J; 354/6

[56] References Cited

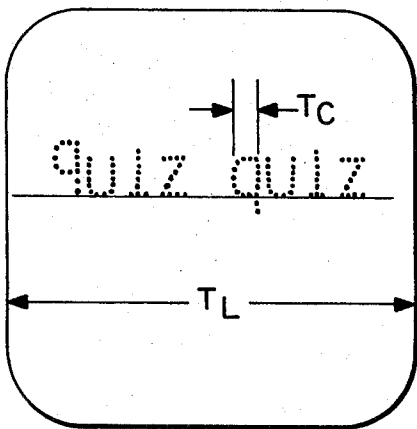
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[57] ABSTRACT

A low cost cathode ray tube display system includes apparatus for providing incremental vertical movement of the character raster of a cathode ray tube display circuit in a desired direction from a given line of reference in response to signals derived from decoding special character codes included within the number of characters being displayed by the system.

18 Claims, 13 Drawing Figures



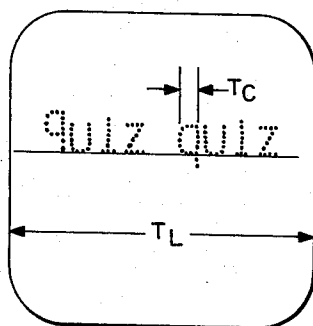


Fig. 1.

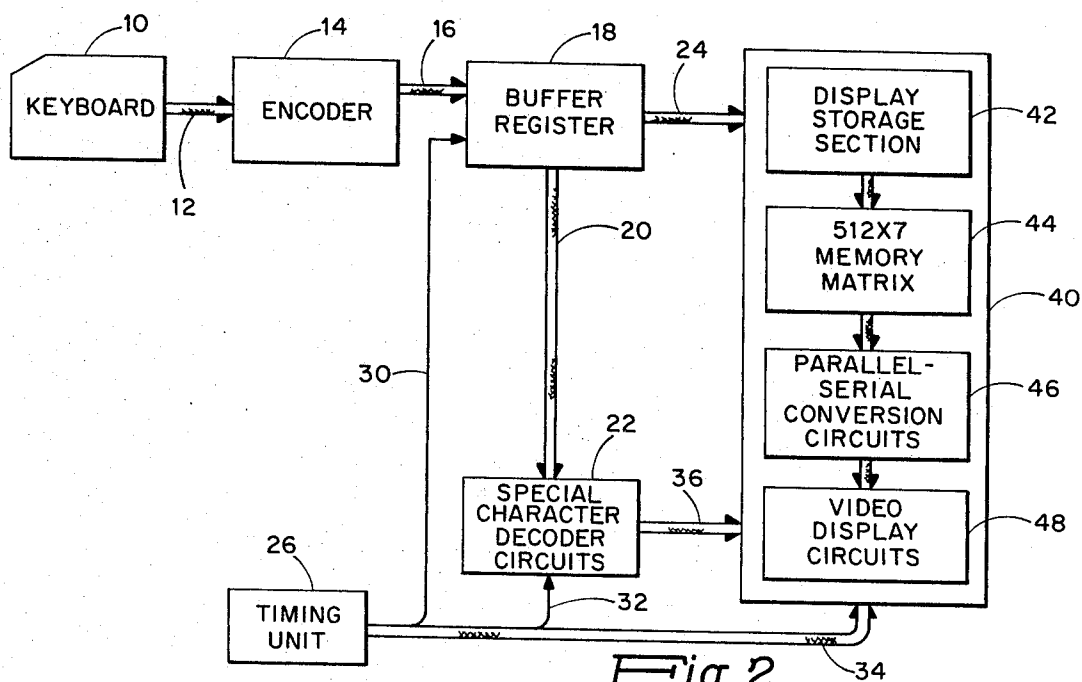


Fig. 2.

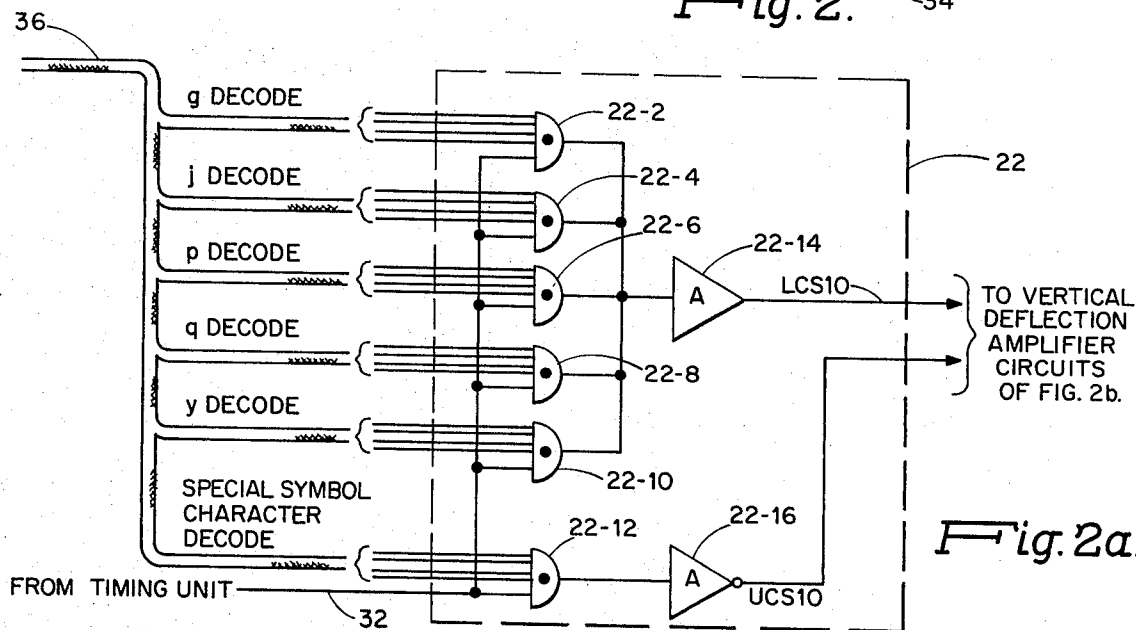


Fig. 2a.

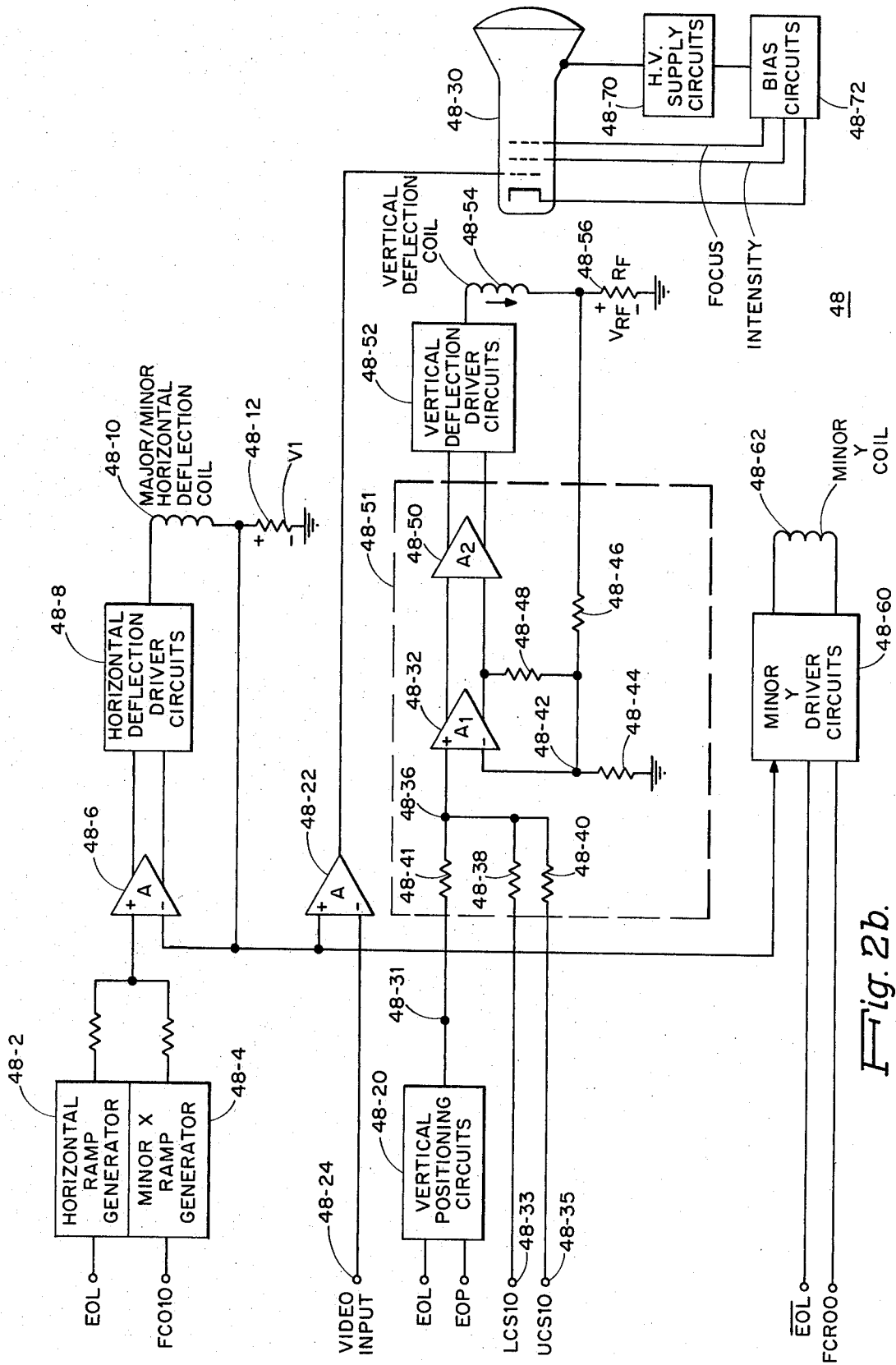


Fig. 2b.

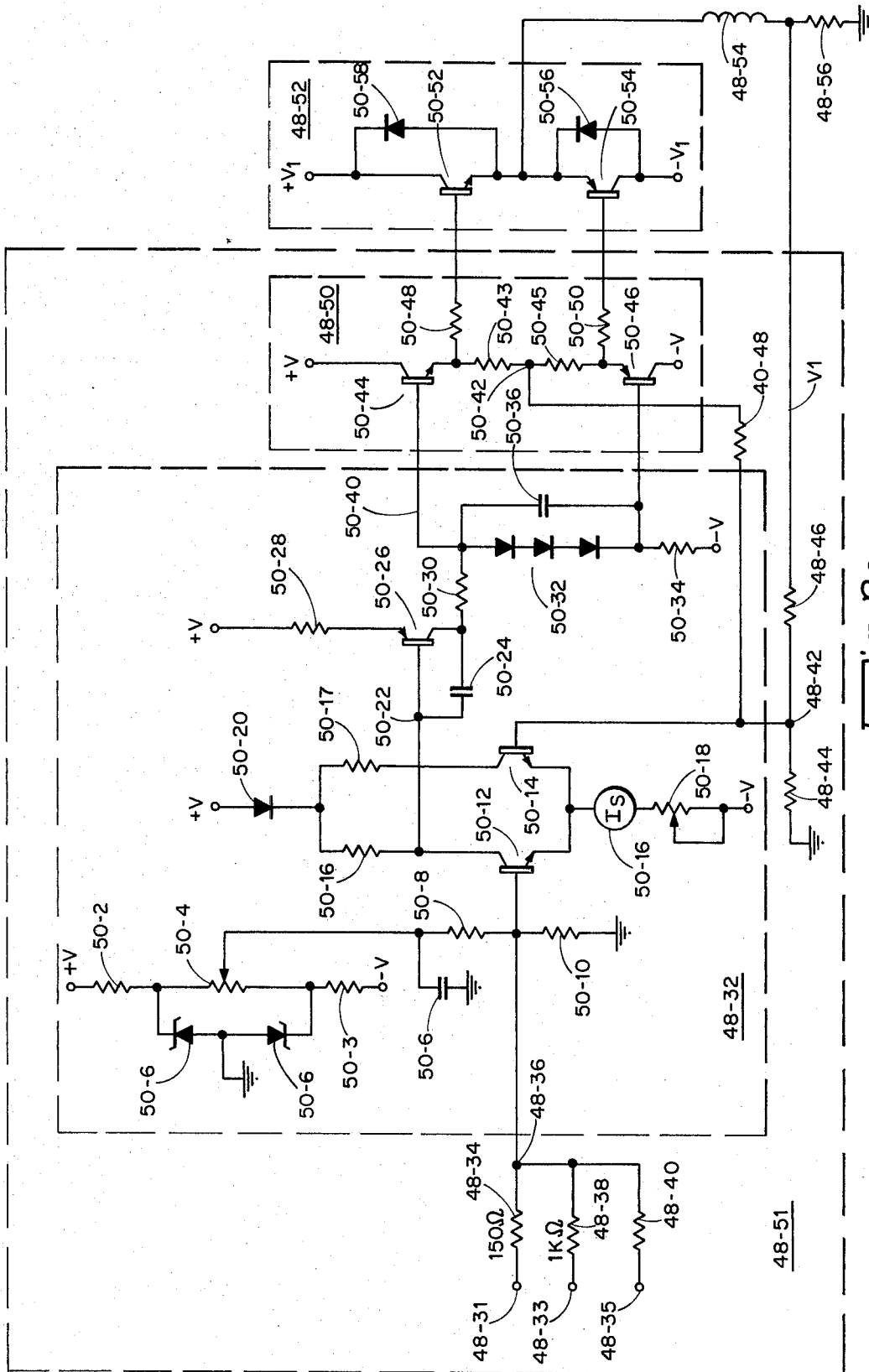


Fig. 2c.

Fig. 3.

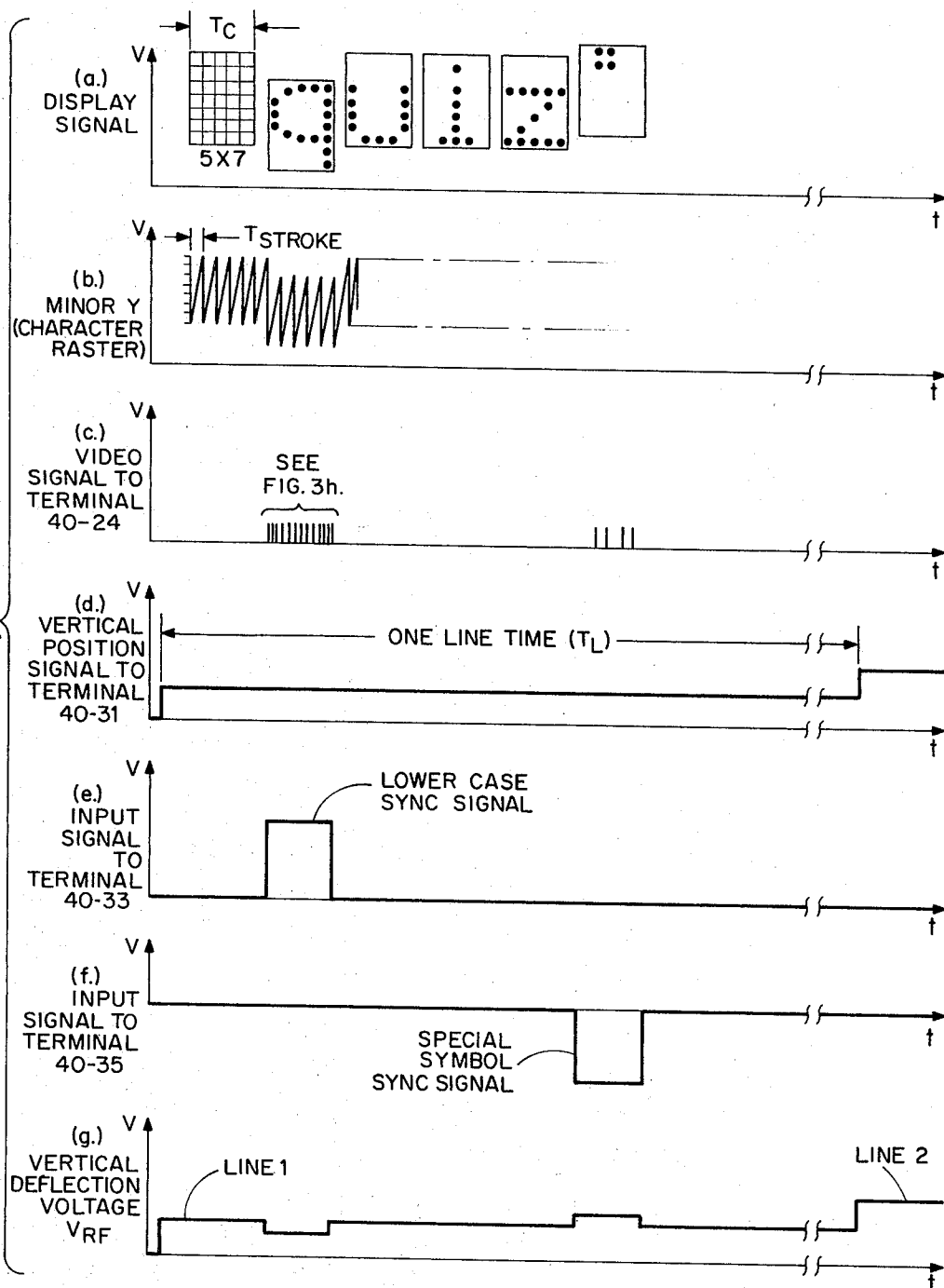
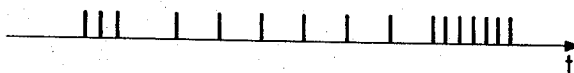


Fig. 3h.



CATHODE RAY TUBE CONTROL APPARATUS FOR DISPLAYING UPPER AND LOWER CASE CHARACTERS USING A SINGLE MATRIX

BACKGROUND OF THE INVENTION

1. Field of Use

This invention relates to cathode ray tube display systems and more particularly to apparatus for displaying upper and lower case characters using a single matrix.

2. Prior Art

Some prior art publications suggest the inclusion of additional apparatus within character generator systems to allow the positioning of subscripts and lower case letters. One such publication is titled, "Static ROM Row Scan Character Generator, EA4004," dated March, 1971, published by Electronic Arrays, Inc. In accordance with the system described, additional apparatus which includes a counter and adder circuit is arranged to alter the normal sequence of the line decode inputs to a read only memory character generator and at the same time blank the output of the generator during specific time intervals.

In the arrangement suggested, the positioning of lower case characters is required to be accomplished by delaying the occurrence of the character information so as to give the appearance of having the lower case character written below the line.

U.S. Pat. No. 3,500,327 illustrates another type display character system in which positions of characters of a small matrix are shifted within a larger matrix area by delaying transmission to the CRT display.

The type of prior art arrangements described above require the timing of the various signals be very accurate for proper positioning of the characters being displayed. This could necessitate additional circuits for attaining increased timing accuracy thereby increasing the cost of the system. Further, the systems require larger size matrices and additional apparatus for delaying the information signals which also increase the cost of the display system. A further disadvantage is that even with the introduction of such apparatus, the modifications to such apparatus as well as the system to accommodate different directions of positioning when required would be quite extensive and would increase greatly the complexity of the system.

Accordingly, it is an object of the present invention to provide a low cost CRT display system which can display upper and lower case characters using a single matrix.

It is a further object of the present invention to provide apparatus for incrementally moving the raster of a CRT display circuit in response to manually generated predetermined character codes to be displayed.

It is still a further object of the present invention to provide improved vertical positioning apparatus for displaying information on a CRT display system in a manner to facilitate the reading of the information being displayed.

SUMMARY OF THE INVENTION

The foregoing objects are achieved in a preferred embodiment of the present invention which provides positioning apparatus operative in response to specially coded characters occurring within a given line of characters to produce an incremental change in a vertical direction for positioning the characters so as to be more easily read.

In greater detail, the apparatus in accordance with the present invention includes decoding means operative to sense the specially coded characters to be shifted from their normal position along a given line of characters. The decoding means provides a control signal directing the vertical deflection amplifier circuits to produce an incremental shift in a given direction for a predetermined time interval which results in moving the character matrix raster from its normal position by an incremental amount. Thus, when the character is written on the matrix area, it appears displaced from the normal line of characters.

In accordance with the invention, a desired amount of change in incrementally positioning the characters with respect to the remainder of the characters of a line is accomplished by selecting a desired value of input voltage to be applied to one input terminal of the deflection amplifier circuits. This voltage is summed with the normal line position voltage applied to another input terminal of the vertical deflection amplifier circuits. The selection of voltages is arranged to permit the incremental positioning signal to be compatible with the voltage levels corresponding to binary ONE and ZERO states of the logic circuits utilized in the system. The arrangement of the present invention also permits the specifying of a variety of incremental changes simply by adding additional input terminals for applying different voltages to the input of the vertical deflection amplifier circuits.

Because of the above arrangement, the invention minimizes the need for additional circuits. Further, the arrangement of the invention requires minimal changes to be made to a conventional CRT display system.

The above and other objects of this invention are achieved in an illustrative embodiment described hereinafter. The novel features which are believed to be characteristic of the invention both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description considered in connection with the accompanying drawings. It is to be expressly understood, however, that these drawings are only for the purpose of illustration and description and are not intended as the definition of the limits of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the difference in appearance of in the characters of a word being displayed with and without employing the present invention.

FIG. 2 illustrates in block diagram form a CRT display system incorporating the improved positioning apparatus of the present invention.

FIG. 2a shows in greater detail the logic circuits included within the decoder circuit block of FIG. 2.

FIG. 2b illustrates in greater detail the display storage and control circuit block of FIG. 2.

FIG. 2c illustrates in greater detail the stages of the vertical deflection amplifier circuit of FIG. 2.

FIGS. 3a-3h illustrate waveforms used in describing the operation of the system of FIG. 1 including the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 2 shows in block diagram form a cathode ray tube (CRT) display system arranged to include the po-

sitioning apparatus of the present invention. The system, exclusive of the apparatus of the invention, is conventional in design. In particular, the system includes a keyboard 10 which applies signal inputs along a plurality of conductors 12 to an encoder 14. The encoder produces a predetermined 7 bit character code in response to each key selection. The code employed by the system is the American Standard Code for Information Interchange (ASCII).

The keyboard generated character code is applied via conductors 16 to a buffer register 18 and stored temporarily. The same character code is later applied via conductors 24 to a display storage section 42 of the display section 40 where it is used to select the appropriate sequence of signals from a character generation 44. A parallel to serial conversion circuit 46 converts the matrix signals into a serial pulse train which is applied to the video display circuits of the section 40 resulting in the display of a character on a CRT included as part of the circuits 48. In a preferred arrangement, the character generator 44 includes a read only memory (ROM) which is constructed from a 512 by 7 diode memory matrix. The matrix stores groups of dot matrix patterns corresponding to the character set. The set includes both upper and lower case characters in addition to special symbols. Since each character is displayed within a 5 by 7 area, five groups of 7 bit patterns are required, as explained herein.

As seen from FIG. 2, the signals stored in buffer register 18 from the encoder 14 are also applied via a second set of conductors 20 to special character decoder circuits 22. These circuits, shown in greater detail in FIG. 2a, are operative to generate control signals in response to a keyboard selection of any one of a group of special characters. The decoder control signals are applied along conductors 36 to the video display circuits which are shown in greater detail in FIG. 2b. A timing unit 26 provides the basic timing for the system of FIG. 2. For example, the unit 26 times the storage information coded signals in buffer register 18 by applying enabling and clear signals to conductor 30 at appropriate time intervals. The timing unit 26 also provides via a conductor 32 timing signals which establish the time duration of the signals produced by the decoder circuits 22. Additionally, the timing unit 26 applies the requisite timing and control signals to the various sections of the display storage and control circuits 40 via a set of conductors 34. The timing unit 26 is conventional in design and may, for example, take the form of timing circuits disclosed in U.S. Pat. No. 3,214,695, to Keith M. Betz, assigned to the assignee of the present invention.

The decoder circuits 22, as illustrated by FIG. 2a, include a plurality of AND gates 22-2 through 22-12 arranged as shown. Each of the AND gates receives a timing signal from timing unit 26 along conductor 32. Additionally, each AND gate receives via the set of conductors 36 certain ones of the output terminals of the storage devices which comprise the buffer register 18. The terminals applied to each gate are selected to decode a different one of the character codes which correspond to the characters indicated in the Figure (i.e., lower case characters g, j, p, q, y, and a special symbol). Upon the decoding of any one of these character codes, the AND gate associated therewith conditions an amplifier circuit 22-14 to force a lower case output signal, LCS10, from a binary ZERO to a binary

ONE state. In a similar fashion, the AND gate 22-12 is operative to condition an inverter circuit 22-6 to force a special symbol signal, USC10, from a binary ONE state to a binary ZERO state.

Both the lower case signal LCS10 and special symbol signal USC10 are applied to the vertical deflection amplifier circuits of FIG. 3. The duration of these signals, as seen from FIG. 2a, is established by the timing signals generated by timing unit 26. The duration of each timing signal corresponds to a character interval; that is, the interval it takes the video circuits 48 to write a character on the CRT.

FIG. 2b shows in block diagram form the video display circuits of block 40. As shown, the system includes horizontal ramp generating circuits 48-2 and minor horizontal ramp generator circuits 48-4 which provide horizontal sweep ramp waveform signals and horizontal character ramp positioning signals respectively which are applied as inputs to a horizontal deflection summing amplifier circuit 48-6.

The amplifier circuit 48-6 is a direct coupled amplifier connected in a feedback arrangement and converts the voltage signals applied to its input current signals which are applied to the horizontal deflection coil 48-10 via transistor driver circuits of block 48-8. As explained in greater detail herein, voltage to current conversion is accomplished by the amplifier circuit 48-6 which compares a voltage, V1, applied to its negative or inverting input terminal with the value of input voltage applied to the amplifier's positive or non-inverting input terminal by the generators 48-2 and 48-4. The amplifier circuit 48-6 produces an output signal until the difference between the two values of voltages being compared is zero volts. As seen from FIG. 2b, the voltage V1 is derived from the horizontal sweep voltage and is developed across a resistor 48-12 which connects in series with the horizontal deflection yoke coil 48-10 which functions as both a minor and major coil.

The timing unit 26 of FIG. 2 provides the digital control timing signals EOL and FC010 which time the operation of generator circuits 48-2 and 48-4 respectively. The timing signal EOL is a negative going digital signal arranged to switch state at the end of a complete line of characters thereby conditioning the horizontal ramp generator circuit 48-2 to return to an initial voltage level during an interval corresponding to the retrace portion of the horizontal ramp waveform. The timing signal FC010 is a positive going digital signal arranged to switch state at the end of every character stroke as explained herein. Thus, the signal EOL conditions the generator circuits 48-2 to provide ramp waveforms for deflecting the beam of the CRT in a horizontal direction for a line of characters. The signal FC010 conditions the generator circuits 48-4 to provide ramp waveforms for deflecting the CRT display beam in a horizontal direction for each character position. The time intervals associated with the signals EOL and FC010 respectively correspond to the time intervals defined by the signals TL and TC IN, FIGS. 1 and 3.

The vertical positioning circuits 48-20 generate line positioning staircase waveforms which move the display beam to selected vertical line positions on the face of the cathode ray tube 48-30. The minor vertical driver circuits 48-60 provide ramp waveforms for rapid vertical trace and retrace deflection of the CRT beam within a character position. The vertical positioning circuits 48-20 apply the ramp waveforms to a vertical

summing amplifier circuit **48-51**. The amplifier circuit **48-51** like the horizontal deflection amplifier circuit **48-6** is operative to convert the voltage applied to a summing junction **48-36** into a current which is applied via driver circuits of the vertical deflection driver circuits **48-52** vertical deflection coil **48-54** for deflecting the beam in a vertical direction.

The operation of the vertical positioning circuits of block **48-20** and the operation of the minor Y driver circuits **48-60** are controlled by the EOL control signal and its complement, $\overline{\text{EOL}}$, each of which change state at the end of each line interval (TL), an end of page (EOP) control signal which switches state at the end of a predetermined number of lines (i.e., every page) and a control signal, FCR00 which switches state at the end of each character stroke. As seen from FIG. 2b, the voltage VI developed across resistor **48-12** occurs in synchronism with the horizontal sweep signal applied to the horizontal deflection coil **48-10**. The voltage VI is used to synchronize the operation of the minor Y driver circuits **40-68**.

Also, as seen from FIG. 2b, the video display circuits include a video amplifier circuit **48-22**, conventional in design, which applies the video signals applied to its negative or inverting input terminal to the control grid of the cathode ray tube **48-30**. The voltage V1 applied to the non-inverting or positive input terminal of the amplifier circuit **48-22** serves as an erasing voltage for the amplifier circuit. When enabled by the voltage V1, the video amplifier circuit **40-22** responds to the video pulses applied to the video input which in turn unblanks the CRT display to produce the characters of a given horizontal line during the interval TL designated in FIG. 1. Bias circuits **48-72** and high voltage supply circuits **48-70**, conventional in design, are arranged to supply intensity, focus and anode voltage for operating the tube **48-30**.

The major deflection coils **48-10** and **48-54** are arranged so that the minor vertical (y) coil is located at the rear of these deflection coils. As indicated, the minor Y driver circuits **48-60** drive the minor Y coil **48-62** which produces a magnetic field for modulating the electron beam of the tube as it moves across the screen horizontally in tracing out the necessary strokes of each character. Character spacing is controlled by varying the speed of the electron beam as it is deflected a selected number of times for each character. The area of the screen which includes the number of strokes for tracing the character, is termed "character raster." in the present embodiment, as described herein, the number of strokes defining the raster for a character is six, five for tracing out the character and one for character space. The strokes which define the character raster are blanked out and do not appear except at the time during which the video signals are applied to the CRT. The video signals produce a series of dots on the face of the tube which forms the character. This arrangement will be described in greater detail with reference to the waveforms of FIG. 3.

Vertical deflection amplifier circuits (FIGS. 2b and 2c)

As mentioned, this amplifier circuit, as seen from FIGS. 2b and 2c, includes an input amplifier circuit **48-32** arranged to drive a current amplifier circuit **48-50** which in turn drives the vertical deflection driver circuits **48-52**. The amplifier circuit **48-32** provides an output voltage some of which is fed back to its inverting or negative input terminal by a resistor **48-48** to pro-

vide the amplifier circuit with AC stability. Each of the amplifier circuits **48-50** and **48-52** is a unity voltage gain, current amplifier which includes a pair of complementary type transistors. As seen from FIG. 2c, the pair of driving transistors supply current to the vertical deflection coil **48-54** and sensing resistor **48-56**. The voltage, VRF, developed across sensing resistor **48-56** is fed back via a voltage divider network including a resistor **48-46** and resistor **48-42** and then applied to the inverting input terminal of the input amplifier circuit **48-32**.

The amplifier circuit **48-51** is shown in greater detail in FIG. 2c. This amplifier circuit is the most pertinent with respect to the invention. As seen from FIGS. 2b and 2c, the input amplifier circuit **48-32** has three input terminals **48-31**, **48-33**, and **48-35** which connect respectively through resistors **48-34**, **48-38**, and **48-40**. The resistors connect in common as shown to form the summing junction **48-36**.

The input voltage signal applied to terminal **48-31** by vertical positioning circuits **48-20**, as mentioned, determines the line position by providing a staircase waveform whose amplitude determines the line positioning of the electron beam. The voltage signal applied to input terminal **48-33** is the lower case sync signal LCS10 which is summed with the vertical line positioning signal applied to terminal **48-31**. The value of resistance for resistor **48-38** is selected to deflect the electron beam in a vertical direction by a predetermined amount.

In the present embodiment, as described herein, the value or resistance **48-38** as compared to the resistance value of resistor **48-34** is of a ratio which causes the voltage level at summing junction **48-36** to decrease by a predetermined amount from the voltage level which corresponds to the normal line position. In the present embodiment, a 10:1 ratio in values of resistances is selected. The ratio drops down the value of voltage at summing junction **48-36** by an amount equal to two spaces out of the possible seven spaces defining the character raster.

The signal applied to the input terminal **48-35** is the special symbol sync signal USC10 which is summed with the vertical line positioning signal applied to input terminal **48-34**. This signal is opposite in polarity to the lower case sync signal LCS10 and deflects the electron beam of the display in a vertical direction by a predetermined amount. This signal in contrast to the lower case sync signal LCS10 increases the level of the voltage at summing junction **48-36** which deflects the beam up from its normal line position. The exact incremental change depends upon the type of the symbol being generated. As for example, if the special symbol corresponded to an exponent, the incremental change could correspond to four spaces.

Considering the amplifier circuit **48-51** and driver circuits **48-52**, reference is made to FIG. 2c. As seen from the Figure, the input amplifier **48-32** includes a differential input stage having a pair of transistors **50-12** and **50-14** which connect via their emitter electrodes to a current source **50-16**, a variable resistor **50-18** and a supply voltage, $-V$ as shown. The collector electrodes of transistors **50-16** and **50-18** connect to the supply voltage, $+V$ via temperature compensating diode **50-20** through load resistors **50-16** and **50-17** respectively.

A variable resistor 50-4 is adjusted to compensate for variations in tube and circuit characteristics and provides a desired value of voltage to input transistor 50-12 for vertical centering the electron beam under dynamic operating conditions. The voltage is derived from the circuit including resistors 50-2, and 50-3, zener diodes 50-6 and sources of supply voltages +V and -V. The centering voltage is applied to the base electrode of transistor 50-12 via a voltage divider including resistor 50-8 and 50-10. The feedback voltage, V₁, is applied to the base electrode of transistor 50-14. A capacitor 50-6 decouples any noise signals from the supply voltages.

An amplified and inverted difference voltage signal developed across load resistor 50-16 of transistor 50-12 is applied to the base electrode of a second voltage amplifying transistor 50-26. The transistor 50-26, as shown, has its emitter electrode connected to biasing supply voltage +V via emitter resistor 50-28. The transistor inverts and amplifies by a factor of 15 the input difference signal producing an output signal across load resistor 50-30. The output signal is applied to the base electrodes of current driver transistors 50-44 and 50-46. The signal applied to the base electrode of transistor 50-46 is shifted in level by a level shifting network including diodes 50-32 and capacitor 50-36 which eliminates cross-over distortion during switching and provides thermal stability for the driver circuits. A resistor 50-34 connected to supply voltage, -V, provides the proper biasing voltage to the driver circuits.

The transistors 50-44 and 50-46 are connected in an emitter follower configuration with resistors 50-43 and 50-45 and supply voltages +V and -V as shown. The resistors 50-43 and 50-45 establish current flowing through transistors 50-44 and 50-46. The resistor 40-48 which connects to a junction 50-42 provides negative feedback signal to transistor 50-14. The transistors 50-44 and 50-46 provide complementary output signals for driving a pair of power transistors 50-52 and 50-54 of the circuits 48-52. The power transistors are connected as shown to supply current to coil 48-54. Each transistor supplies currents for one half of an operating cycle so as to reduce the power dissipation requirements of each transistor. The diodes 50-56 and 50-58 provide short circuit protection for their respective transistors.

DESCRIPTION OF OPERATION OF THE PREFERRED EMBODIMENT

With specific reference to FIGS. 1, 2, 2a through 2c, and 3, the operation of the positioning apparatus of the present invention will now be described. FIG. 1 illustrates the difference in appearance the word "quiz" has when it is written by the system of FIG. 2 employing the positioning apparatus of the present invention. It is seen from FIG. 1 that the second occurrence of the word "quiz" is much easier to read when the "q" is positioned so that its tail extends below the horizontal line of characters.

FIG. 3 illustrates the relationship between the various waveforms of the system of FIG. 2b which result in the positioning apparatus providing the proper positioning of special characters in accordance with the present invention.

Referring to FIG. 3, the first waveform (a) illustrates the manner in which the word "quiz" appears along a horizontal line of characters when written in accordance

with the subject invention. The symbol "q" is recognized by the special decoder circuits 22 of FIG. 2a which are operative to force the lower case signal LCS10 to a binary ONE state in response to a timing signal from timing unit 26. As illustrated by waveform e, this results in the generation of the sync signal LCS10 which endures for a character interval as shown. During this interval, signals derived from the memory matrix of FIG. 2 are generated and provide the sequence of video pulses illustrated by waveform c. As seen by the expanded drawing of this waveform in FIG. 3h, each pulse produces a dot by unblanking the CRT at a position defined by the character strokes of waveform b which are produced by the minor Y coil. As shown by waveform a, the first dot pattern causes two dots to be written during a first character interval, the next three dot patterns cause two dots to be written during character intervals 2 through 4, and the last dot pattern causes seven dots to be written during the fifth character interval resulting in the formation of the letter "q."

The lower case character sync LCS10 signal applied to the input terminal 48-33 of the vertical deflection amplifier 48-51 of FIG. 2b causes a net decrease in the vertical deflection voltage as illustrated by waveform g of FIG. 3. This voltage decrease causes the "q" character to be shifted down from the normal line position of a line of characters. Because the remaining characters of the word "quiz" are not designated as special characters, they are written along the normal line position for line 1.

FIG. 3 also indicates the manner in which the area provided for a special symbol appears. Here, the special symbol is a quotation mark symbol. When the special character symbol is decoded by the special character decoder circuits 22, it results in the AND gate 22-12 of FIG. 2a causing the generation of a special symbol sync signal, USC10, as illustrated by waveform f of FIG. 3. This signal when applied to terminal 48-35 of the vertical deflection amplifier 48-51 of FIG. 2b produces an increase in the voltage at summing junction 48-36 which produces an increase in the vertical deflection voltage as illustrated by waveform g of FIG. 3. Accordingly, when the video signals from the character generator are applied to video terminal 48-24, the special symbol is written in the area shown by waveform a of FIG. 3.

It will be appreciated that by simply adding other inputs and resistors to summing junction of vertical deflection amplifier, other symbols such as subscripts and superscripts can be easily positioned as required. Thus, the positioning apparatus of the present invention can be easily incorporated into a conventional cathode ray tube display system with little modification to the system. It will also be appreciated that many modifications can be made to the system shown without departing from the invention.

While in accordance with the provision and statutes, there has been illustrated and described the best form of the invention known, certain changes may be made to the various elements described without departing from the spirit of the invention as set forth in the appended claims, and that in some cases, certain features of the invention may be used to advantage without the corresponding use of other features.

Having described the invention, what is claimed as new and novel is:

1. A cathode ray tube display system including a cathode ray tube, keyboard entry and storage means coupled to said tube, said keyboard entry and storage means including means for generating predetermined binary coded signals designating which character included in a set of characters is to be displayed along a horizontal line starting from a normal line position, said tube having major and minor vertical deflection generation means operative to generate major and minor positioning waveforms respectively for conditioning major and minor driver circuits for driving major and minor vertical coils in a vertical direction, said minor vertical deflection driver circuit means being operative to generate a high frequency pulse waveform for producing a predetermined number of character writing strokes for each of the characters to be written along said line, each of said strokes having a height corresponding to a number of spaces, said system further including improved positioning apparatus, coupled to said vertical deflection driver circuit means, said positioning apparatus comprising:

decoder circuit means coupled to said keyboard entry and storage means, said decoding circuit means including logic circuit means for generating a control signal in response to any one of a predetermined number of characters comprising a special group of characters within said set which have a similar characteristic; and,

amplifier circuit means including input means and output means, said input means being coupled to said logic circuit means and to said major vertical generation circuit means, and said output means being coupled to said vertical deflection driver circuit means, said amplifier circuit means being responsive to the joint application of said control signal and said positioning waveform to said input means to condition said amplifier circuit output means to apply an output signal to said deflection driver circuit means which produces an incremental vertical shift in said one of said predetermined number of characters from said normal line position.

2. Positioning apparatus for use in a cathode ray tube display system including data entry and storage means for generating coded signals representative of a different ones of the characters included in a set of characters to be displayed along a horizontal line starting from a normal line position, a cathode ray tube coupled to said entry and storage means, said tube having major and minor horizontal deflection and vertical deflection generation circuit means operative to generate major and minor positioning waveforms to condition major and minor deflection driver circuits respectively for driving a horizontal coil and major vertical coil and a minor vertical coil coupled to said tube for deflecting the electron beam along said horizontal line and in a vertical direction, said minor vertical deflection driver circuit means being operative to generate a high frequency pulse waveform for producing character writing strokes for the characters to be written along said line, each stroke having a height corresponding to a number of spaces, said positioning apparatus comprising:

decoder circuit means coupled to said data entry and storage means, said decoder circuit means being operative to generate a control signal upon decod-

ing each one of a group of special characters included within said set; and,

vertical deflection amplifier circuit means coupled to said major vertical deflection driver circuit means and to said decoder circuit means, said vertical deflection amplifier circuit means including:

amplifier circuit means having at least one input terminal and an output terminal; and

a plurality of input impedance means, each of said plurality of impedance means having an input and an output terminal, said output terminals of each of said input impedance means being connected in common to said input terminal of said amplifier circuit means, said input terminal of a predetermined first one of said plurality of impedance means being coupled to receive said major vertical positioning voltage waveform from said vertical deflection generation circuit means for driving said major vertical coil establishing said normal line position along which characters are to be written, said input terminal of a predetermined second one of said plurality of impedance means being coupled to receive said control signal,

said amplifier circuit means being conditioned by the joint application of said major vertical positioning voltage waveform and said control signal to produce a first predetermined voltage level at said output terminal to condition said major vertical driver circuit means to change the deflection current in said vertical major coil by a first incremental amount during a character interval so as to shift vertically said each one of said group of special characters by an incremental amount from said normal line position so that each of said characters can be more easily read.

3. The positioning apparatus of claim 2 wherein said decoding circuit means includes a plurality of first gating circuit means, each of said gating circuit means being connected to said data entry and storage means and arranged to decode a different one of said group of special characters and each of said gating circuit means including means for receiving a timing signal having a predetermined duration corresponding to said character interval, each of said plurality of gating circuits being operative to generate said control signal in response to receiving signals coded to represent a different one of said group of special characters from said data entry and storage means.

4. The positioning apparatus of claim 3 wherein said decoding circuit means further includes output logic circuit means coupled to each of said plurality of gating circuit means, each of said plurality of gating means upon decoding said different one of said group of special characters being operative to condition said output logic circuit means to generate said control signal having a predetermined voltage level.

5. The positioning apparatus of claim 4 wherein said output logic circuit means includes an amplifier circuit operative to produce said predetermined voltage level of said control signal so as to correspond to a voltage level representative of a binary ONE in said system.

6. The positioning apparatus of claim 3 wherein each of said plurality of gating circuit means include an AND gate and wherein each of said plurality of gating circuit means is connected to decode signals coded to represent a different one of said group of special char-

acters corresponding to lower case characters *g, j, p, q* and *y*.

7. The positioning apparatus of claim 2 wherein said predetermined first and second ones of said impedance means selected to have first and second values of impedance respectively, said first and second values of impedance being selected to be a predetermined ratio so as to cause the voltage level applied to said input terminal of said amplifier circuit means to be decreased by a predetermined amount from the voltage produced by said major vertical positioning voltage waveform.

8. The positioning apparatus of claim 7 wherein said predetermined ratio corresponds to a 10 to 1 ratio.

9. The positioning apparatus of claim 7 wherein said first and second ones of said impedance means are resistances said ratio for said first and second resistances being selected to decrease said voltage level applied to said input terminal by a predetermined amount which corresponds to a shift in said character of two spaces out of said number of spaces.

10. The positioning apparatus of claim 7 wherein said major vertical positioning voltage waveform and control signals are of the same polarity.

11. The positioning apparatus of claim 2 wherein said decoder means further includes second gating means for generating a special symbol signal upon decoding at least one other type of special character and wherein said input terminal of a third one of said impedance means is connected to receive said special symbol signal, said vertical amplifier circuit means being conditioned by the joint application of said major vertical positioning voltage waveform and said special symbol signal to produce a second predetermined voltage level at said output terminal to condition said major vertical driver circuit means to change said deflection current by a second incremental amount different from said first incremental amount so as to shift vertically said other type of special character by a predetermined amount from said normal line position so as to position said other type of special character in a predetermined manner.

12. The positioning apparatus of claim 11 wherein said first, second and third ones of said impedance means are resistances and each having a predetermined value, said first and third values being selected to be of a predetermined ratio so as to cause the voltage level applied to said input terminal of said amplifier circuit means to increase by a predetermined amount from the voltage applied to said input terminal produced by said major vertical positioning voltage waveform.

13. The positioning apparatus of claim 11 wherein said major vertical positioning voltage waveform and said special symbol signal are of the opposite polarity.

14. The positioning apparatus of claim 11 wherein said gating means including means for receiving a timing signal having a predetermined duration corresponding to said character interval and inverter circuit means coupled to said gating means, said gating means being operative in response to receiving signals coded to represent said special character to condition said inverter circuit means to generate said special symbol signal.

15. The positioning apparatus of claim 2 wherein said vertical amplifier means further includes a differential amplifier circuit means having a non-inverting terminal and an inverting input terminal, said input terminal being connected to said non-inverting terminal of said amplifier means and said inverting input terminal being

coupled to said major vertical deflection coil for receiving a feedback voltage and said differential amplifier circuit means being operative in response to signals applied to said non-inverting and inverting terminals to produce a difference voltage for application to said output terminal.

16. The positioning apparatus of claim 15 wherein said vertical amplifier further includes current amplifier circuit means having an input circuit and an output circuit, said input circuit being coupled to receive said difference voltage from said differential amplifier circuit means and said output circuit being coupled to said output terminal, said current amplifier circuit means being operative to connect said difference voltage into a current waveform for driving said deflection circuit means.

17. The positioning apparatus of claim 16 wherein said current amplifier circuit means and said deflection circuit means each include a pair of complementary type transistors connected in an emitter follower configuration for producing said current waveform.

18. In a cathode ray tube display system including a cathode ray tube, keyboard input means, an encoder coupled to said keyboard input means, said encoder being operative in response to a key selection to produce output binary code signals representative of a character within a set of upper and lower case characters to be displayed on said tube along a horizontal line, storage register means coupled to receive said output binary code signals from said encoder means for coupling said cathode ray tube to said register storage means, said tube having major and minor horizontal deflection and vertical deflection generation circuit means operative to generate major and minor positioning waveforms to condition major and minor deflection driver circuit means respectively to drive major horizontal coil and major vertical coil and a minor vertical coil coupled to said tube for deflecting the electron beam along said horizontal line and in a vertical direction, said minor vertical deflection driver circuit means being operative to generate a high frequency pulse waveform for producing character writing strokes, a number of which define a character raster for each of the characters to be written along said line, each stroke having a height corresponding to a number of spaces, said display system further including positioning apparatus comprising:

decoder circuit means coupled to said storage register, said decoder circuit means including means for generating a control signal upon sensing when said register storage means stores binary code signals which correspond to any one of a plurality of characters each of which can be written below said horizontal line and included within said set of characters; and,

vertical deflection amplifier circuit means including input means and output means, said input means being coupled to receive said control signal and said major vertical positioning voltage waveform, said output means being coupled to said vertical deflection driver circuit means and said input means being responsive to the joint application of said control signal and said positioning voltage waveform to condition said amplifier circuit output means to apply an output signal to said deflection circuit means which produces an incremental vertical shift in the character raster for a character interval so that the character written during said character interval is displaced from said line enabling it to be more easily read.

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