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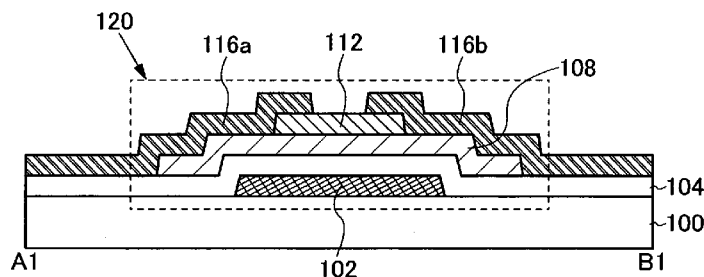
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(54) Title: SEMICONDUCTOR DEVICE INCLUDING A TRANSISTOR, AND MANUFACTURING METHOD OF SEMI-
CONDUCTOR DEVICE

FIG. 1B



(57) Abstract: An object is to prevent contamination of a semiconductor film in a transistor or a semiconductor device including the transistor. Another object is to suppress variation in electrical characteristics and deterioration. A transistor including: a gate electrode layer provided over a substrate; a gate insulating film provided over the gate electrode layer; a semiconductor layer which is provided over the gate insulating film and which overlaps the gate electrode layer; a carbide layer provided over and in contact with a surface of the semiconductor layer; and a source electrode layer and a drain electrode layer which are electrically connected to the semiconductor layer is provided.

DESCRIPTION

**SEMICONDUCTOR DEVICE INCLUDING A TRANSISTOR, AND
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE**

5

TECHNICAL FIELD

[0001]

The present invention relates to a transistor, a semiconductor device including
10 the transistor, and methods for manufacturing the transistor and the semiconductor
device. Further, the present invention relates to a display device including the
transistor. For example, the present invention relates to an electro-optic device typified
by a liquid crystal display device or the like and an electronic appliance including such
a display device as a component.

15

BACKGROUND ART

[0002]

In recent years, a technique for forming thin film transistors using a
20 semiconductor thin film (with a thickness of several tens to several hundreds of
nanometers) formed over a substrate having an insulating surface has attracted attention.
Thin film transistors have been widely applied to electronic devices such as ICs or
display devices. In particular, development as a switching element of a display device
typified by a liquid crystal display device has been urgently developed.

25 [0003]

In display devices such as liquid crystal display devices, amorphous silicon
thin film transistors have been in practical use as switching elements. Channel-etched
inversed staggered (or bottom-gate) TFTs including a channel formation region formed
using amorphous silicon have been used in many cases.

30 [0004]

A back-channel portion of an inversed staggered thin film transistor is exposed
to a variety of work environment during the manufacture of the thin film transistor.

For example, due to dry etching in a process for manufacturing the thin film transistor, plasma damage is caused or a fixed charge is generated in some cases. Further, moisture or an impurity adheres to or penetrates the back-channel portion after the manufacture of the thin film transistor in some cases. Change in qualities or contamination of the back-channel portion of the thin film transistor increases off current, leading to variation in characteristics and deterioration of the thin film transistor.

[0005]

In order to reduce in off current of the thin film by removing an impurity of the back-channel portion, a technique in which the impurity adhered to the surface of back-channel portion is removed by surface treatment which i-type layer amorphous silicon in the back-channel portion between a source electrode and a drain electrode is subjected to plasma discharge under an atmosphere gas containing H₂ or He has been disclosed (see Patent Document 1).

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. H11-274504

DISCLOSURE OF INVENTION

[0007]

However, the characteristics of the thin film transistor cannot be sufficiently stabilized by only surface treatment of the back-channel portion of the thin film transistor. This is because a chemically and thermally stable surface cannot be formed by only plasma treatment or the like performed on the surface of the semiconductor film. Although it is known that a silicon oxide film or a silicon nitride film is used as a protection film on the back-channel side of the thin film transistor, such a protection film adversely affects a semiconductor film that is easily damaged by plasma in some cases.

[0008]

In view of the above-described problems, it is an object of one embodiment of

the present invention to suppress change in semiconductor characteristics in a transistor or a semiconductor device including the transistor. It is another object of one embodiment of the present invention to improve the reliability of the semiconductor device.

5 [0009]

In order to solve the above-described problems, one embodiment of the present invention has a structure in which a carbide layer that is chemically or thermally stable and dense is formed over and in contact with a surface of a semiconductor layer. Specifically, one embodiment of the present invention is a transistor including: a gate
10 electrode layer provided over a substrate; a gate insulating film provided over the gate electrode layer; a semiconductor layer which is provided over the gate insulating film and which overlaps the gate electrode layer; a carbide layer provided over and in contact with a surface of the semiconductor layer; and a source electrode layer and a drain electrode layer which are electrically connected to the semiconductor layer. The
15 carbide layer serves as a protective layer which prevents atoms or the like that causes change in semiconductor characteristics from being in contact with or entering the semiconductor layer. The carbide layer also serves as a protective layer of a semiconductor layer in the manufacturing process. Further, deterioration, change in qualities or the like of the carbide layer can be suppressed even when the carbide layer
20 is exposed to various chemical solutions or the like in the manufacturing process because the carbide layer is a chemically stable film. Furthermore, the carbide layer is also a thermally stable film; thus, at the interface between the semiconductor layer and the carbide layer, change in semiconductor characteristics can be suppressed when the carbide layer is heated.

25 [0010]

In the above structure, the carbide layer is provided over and in contact with part of the surface of the semiconductor layer, and the source electrode layer and the drain electrode layer are provided over and in contact with the surfaces of the semiconductor layer where the carbide layer is not provided. Alternatively, in the
30 above structure, a first low resistance layer serving as a source region is provided in a region where the semiconductor layer is in contact with the source electrode layer; and a second low resistance layer serving as a drain region is provided in a region where the

semiconductor layer is in contact with the drain electrode layer.

[0011]

One embodiment of the present invention is a transistor including: a gate electrode layer provided over a substrate; a gate insulating film provided over the gate electrode layer; a semiconductor layer provided over the gate insulating film; a source electrode layer and a drain electrode layer which are electrically connected to the semiconductor layer; and a carbide layer provided in contact with the semiconductor layer, the source electrode layer, and the drain electrode layer.

[0012]

One embodiment of the present invention is a transistor including: a gate electrode layer provided over a substrate; a gate insulating film provided over the gate electrode layer; a source electrode layer and a drain electrode layer provided over the gate insulating film; a semiconductor layer which is provided over the source electrode layer and the drain electrode layer and over the gate electrode layer with the gate insulating film provided therebetween; and a carbide layer provided over and in contact with the surface of the semiconductor layer.

[0013]

In the above structures, a first low resistance layer serving as a source region is provided in a region where the semiconductor layer is in contact with the source electrode layer; and a second low resistance layer serving as a drain region is provided in a region where the semiconductor layer is in contact with the drain electrode layer.

[0014]

In the above structures, the carbide layer is formed using at least one of materials of silicon carbide, silicon nitride carbide, germanium carbide, n-type silicon carbide, and p-type silicon carbide.

[0015]

One embodiment of the present invention provides a method for manufacturing a transistor, including the steps of: forming a gate electrode layer over a substrate; forming a gate insulating film over the gate electrode layer; forming a semiconductor layer over the gate insulating film so as to overlap the gate electrode layer; forming a carbide film so as to cover the semiconductor layer; forming a carbide layer by etching the carbide film; forming a conductive film over the carbide layer and the

semiconductor layer; and forming a source electrode layer and a drain electrode layer by etching the conductive film.

[0016]

One embodiment of the present invention provides a method for manufacturing a transistor, including the steps of: forming a gate electrode layer over a substrate; forming a gate insulating film over the gate electrode layer; forming a semiconductor layer over the gate insulating film so as to overlap the gate electrode layer; forming a conductive film over the semiconductor layer; forming a source electrode layer and a drain electrode layer by etching the conductive film; and forming a carbide film so as to cover the semiconductor layer, the source electrode layer, and the drain electrode layer.

[0017]

One embodiment of the present invention provides a method for manufacturing a transistor, including the steps of: forming a gate electrode layer over a substrate; forming a gate insulating film over the gate electrode layer; forming a conductive film over the gate insulating film; forming a source electrode layer and a drain electrode layer by etching the conductive film; forming a semiconductor layer over the source electrode layer and the drain electrode layer with the gate insulating film provided therebetween; and forming a carbide layer over the surface of the semiconductor layer.

[0018]

Examples of a semiconductor layer in this specification include a semiconductor material formed of a Group 14 element such as silicon, germanium, or silicon germanium, a compound semiconductor material such as InGaAs, InGaP, or InGaN, and an oxide semiconductor material including zinc oxide, tin oxide, or indium oxide. The crystallinity of the semiconductor layer may be either single crystal or non-single-crystal (e.g., polycrystalline, microcrystalline, or amorphous). Note that the semiconductor layer may include two or more crystal structures among the above crystal structures (e.g., an amorphous structure and a microcrystalline structure (or a polycrystalline structure)).

[0019]

In this specification, a semiconductor device refers to any device which can function by utilizing semiconductor characteristics, and a display device, a semiconductor circuit, and an electronic appliance are all included in the category of the

semiconductor device. In addition, in this specification, a display device includes a light-emitting device and a liquid crystal display device in its category. The light-emitting device includes a light-emitting element, and the liquid crystal display device includes a liquid crystal element. A light-emitting element includes, in its category, an element whose luminance is controlled by current or voltage, and specifically includes an inorganic electroluminescent (EL) element, an organic EL element, an LED element, and the like.

[0020]

In one embodiment of the present invention, a carbide layer is provided in contact with a semiconductor layer, so that change in semiconductor characteristics of a semiconductor device can be suppressed. Further, the reliability of the semiconductor device can be increased.

BRIEF DESCRIPTION OF DRAWINGS

[0021]

In the accompanying drawings:

FIGS. 1A to 1C illustrate a structure of a transistor according to Embodiment 1;

FIGS. 2A and 2B illustrate a structure of a transistor according to Embodiment

1;

FIGS. 3A and 3B each illustrate a structure of a transistor according to Embodiment 1;

FIGS. 4A and 4B illustrate models which are used in simulation;

FIGS. 5A and 5B show calculation results of diffusion coefficients of hydrogen obtained by simulation;

FIGS. 6A to 6D illustrate an example of a manufacturing method of a transistor according to Embodiment 1;

FIGS. 7A and 7B illustrate an example of a manufacturing method of a transistor according to Embodiment 1;

FIG. 8 illustrates a structure of a transistor according to Embodiment 1;

FIGS. 9A to 9C illustrate structures of a transistor according to Embodiment 2;

FIGS. 10A to 10D illustrate an example of a manufacturing method of a

transistor according to Embodiment 2.

FIGS. 11A to 11C illustrate structures of a transistor according to Embodiment 3;

FIGS. 12A to 12E illustrate an example of a manufacturing method of a transistor according to Embodiment 3.

FIGS. 13A and 13B illustrate a structure of a transistor according to Embodiment 3;

FIGS. 14A-1, 14A-2, and 14B illustrate examples of a semiconductor device according to Embodiment 4;

FIGS. 15A and 15B illustrate an example of a semiconductor device according to Embodiment 5;

FIG. 16 illustrates an example of a semiconductor device according to Embodiment 6; and

FIGS. 17A to 17F illustrate examples of semiconductor devices according to Embodiment 7.

BEST MODE FOR CARRYING OUT THE INVENTION

[0022]

Embodiments of the present invention are described in detail below with reference to the accompanying drawings. The present invention is not limited to the following description of the embodiments. It is easily understood by those skilled in the art that modes and details of the present invention can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be limited to the descriptions of the embodiment modes and the embodiment below. Further, structures according to different embodiments can be implemented in combination as appropriate. In the structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals, and repetitive description thereof is omitted.

[0023]

(Embodiment 1)

In this embodiment, structures and manufacturing methods of semiconductor

devices according to one embodiment of the present invention are described with reference to FIGS. 1A to 1C, FIGS. 2A and 2B, FIGS. 3A and 3B, FIGS. 4A and 4B, FIGS. 5A and 5B, FIGS. 6A to 6D, FIGS. 7A and 7B, and FIG. 8.

[0024]

5 FIG. 1A is a top view, FIG. 1B is a cross-sectional view taken along line A1-B1 of FIG. 1A, and FIG. 1C is a cross-sectional view taken along line A2-B2 of FIG. 1A.

[0025]

 First, structures of the transistor of this embodiment are described. A transistor 120 illustrated in FIGS. 1A to 1C includes a gate (including a gate wiring and a gate electrode layer (hereinafter referred to as a "gate electrode layer 102")) provided over a substrate 100, a gate insulating film 104 provided over the gate electrode layer 102, a semiconductor layer 108 provided over the gate insulating film 104, a carbide layer 112 provided over and in contact with a surface of the semiconductor layer 108, and a source (including a source wiring and a source electrode (hereinafter referred to as a "source electrode layer 116a")) and a drain (including a drain wiring and a drain electrode (hereinafter referred to as a "drain electrode layer 116b")) which are electrically connected to the semiconductor layer 108 (see FIGS. 1A to 1C).

[0026]

 The semiconductor layer 108 is provided so that at least part thereof overlaps the gate electrode layer 102 with the gate insulating film 104 provided therebetween, and the semiconductor layer 108 serves as a layer for forming a channel region of the transistor 120 (a channel layer).

[0027]

 For the semiconductor layer 108, a semiconductor formed of a Group 14 element such as silicon, germanium, silicon germanium, or silicon carbide, a compound semiconductor such as InGaAs, InGaP, or InGaN, an oxide semiconductor such as zinc oxide or tin oxide, or the like may be used. The crystallinity of the semiconductor layer 108 may be either single crystal or non-single-crystal (e.g., polycrystalline, microcrystalline, or amorphous). Note that the semiconductor layer 108 may include two or more crystal structures among the above crystal structures (e.g., an amorphous structure and a microcrystalline structure (or the polycrystalline structure)).

[0028]

The carbide layer 112 is provided over and in contact with the surface of the semiconductor layer 108 at least in a region that overlaps the gate electrode layer 102. In addition, the carbide layer 112 can be provided over and in contact with part of the surface of the semiconductor layer 108, and the source electrode layer 116a and the drain electrode layer 116b can be provided in contact with regions of the semiconductor layer 108, over which the carbide layer 112 is not provided. Here, an example where the regions of the semiconductor layer 108, over which the carbide layer 112 is not provided, are provided apart from each other and the source electrode layer 116a and the drain electrode layer 116b are provided in contact with the regions is described.

[0029]

As a formation method of the carbide layer 112, a CVD method, a sputtering method, or the like can be used. The thickness of the carbide layer 112 can be set to greater than or equal to 1 nm and less than or equal to 500 nm, preferably greater than or equal to 10 nm and less than or equal to 100 nm.

[0030]

In the case where the source electrode layer 116a and the drain electrode layer 116b are provided over the semiconductor layer 108, the carbide layer 112 can serve as a channel protective layer (a channel stop layer). In the case where the carbide layer 112 is made to actively serve as a channel protective layer, the carbide layer 112 is preferably formed as a dense film. A dense film can prevent an impurity that causes change in semiconductor characteristics from being in contact with or entering the semiconductor layer 108. Further, deterioration, change in qualities or the like of the carbide layer can be suppressed even when the carbide layer is exposed to various chemical solutions or the like in the manufacturing process because the carbide layer is a chemically stable film. Furthermore, the carbide layer is also a thermally stable film, and thus, change in the state can be suppressed when the interface between the semiconductor layer and the carbide layer is heated. As compared to the case where the carbide layer 112 is not provided in contact with the semiconductor layer 108, change in semiconductor characteristics caused by exposure of the semiconductor layer 108 can be suppressed.

[0031]

The carbide layer 112 may be provided in contact with a surface of at least a

region in which a channel is formed in the semiconductor layer 108. In addition, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, or a silicon nitride oxide film may be formed as a protective insulating film over the carbide layer 112. The protective insulating film over the carbide layer 112 can be formed by a sputtering method or a CVD method.

[0032]

In FIGS. 1A to 1C, the source electrode layer 116a serves as a source of the transistor 120, and the drain electrode layer 116b serves as a drain of the transistor 120. Depending on the driving method of the transistor 120, the source electrode layer 116a might serve as a drain and the drain electrode layer 116b might serve as a source.

[0033]

In the structure illustrated in FIGS. 1A to 1C, a silicon carbide layer can be used as the carbide layer 112 which is provided over and in contact with the surface of the semiconductor layer 108. Silicon nitride carbide, germanium carbide, or the like may be used other than silicon carbide. Alternatively, an impurity imparting one conductivity type may be added to the silicon carbide. For example, n-type silicon carbide including an impurity element imparting n-type conductivity such as phosphorus or arsenic, or p-type silicon carbide including an impurity element imparting p-type conductivity such as boron, aluminum, or gallium can be used. The carbide layer 112 can be formed using one or combination of the above-mentioned materials.

[0034]

The crystallinity of the carbide layer 112 may be either single crystal or non-single-crystal (e.g., polycrystalline, microcrystalline, or amorphous). The carbide layer 112 may include two or more crystal structures among the above crystal structures (e.g., an amorphous structure and a microcrystalline structure (or a polycrystalline structure)). In this specification, the case where the crystallinity of the carbide layer is amorphous is described.

[0035]

Next, the shapes of the semiconductor layer 108 and the carbide layer 112 in the structure illustrated in FIGS. 1A to 1C are described. Note that in the description below, the width of the carbide layer 112 (W_b) and the width of the semiconductor layer

108 (Wc) indicate the length of the carbide layer 112 and the length of the semiconductor layer 108 in the channel width direction, respectively. Further, the length of the carbide layer 112 (Lb) and the length of the semiconductor layer 108 (Lc) indicate the length of the carbide layer 112 and the length of the semiconductor layer 108 in the channel length direction, respectively. Furthermore, the channel length direction indicates the direction which is substantially parallel to the direction in which carriers move in the transistor 120 (the direction in which the source electrode layer 116a and the drain electrode layer 116b are connected to each other), and the channel width direction indicates the direction which is substantially perpendicular to the channel length direction.

[0036]

The transistor illustrated in FIGS. 1A to 1C is a transistor in the case where the width of the carbide layer 112 (Wb) is larger than the width of the semiconductor layer 108 (Wc) and the carbide layer 112 is provided to extend beyond (to cross) both edges of the semiconductor layer 108 in the channel width direction. In addition, the length of the carbide layer 112 (Lb) is smaller than the length of the semiconductor layer 108 (Lc). Further, two regions which are not covered with the carbide layer 112 are provided in the channel length direction, and the source electrode layer 116a and the drain electrode layer 116b are provided over the two regions that are apart from each other so as to be electrically connected. In this manner, leakage current caused by change in semiconductor characteristics at the surface of the semiconductor layer 108 can be reduced.

[0037]

FIGS. 1A to 1C illustrate the transistor 120 in which the length of the semiconductor layer 108 (Lc) is made large so that the semiconductor layer 108 extends beyond edges of the gate electrode layer 102 in the channel length direction; however, the length of the semiconductor layer 108 (Lc) may be made small so that the whole region of the semiconductor layer 108 may be located over the gate electrode layer 102. Note that FIG. 2A is a top view and FIG. 2B is a cross-sectional view taken along line A1-B1 of FIG. 2A.

[0038]

In FIGS. 1A to 1C and FIGS. 2A and 2B, the width of the carbide layer 112

(Wb) is made larger than the width of the semiconductor layer 108 (Wc). The widths of the source electrode layer 116a and the drain electrode layer 116b (Wd) may each be larger than the width of the semiconductor layer 108 (Wc) in regions where the source electrode layer 116a and the drain electrode layer 116b overlap the semiconductor layer 108 (see FIGS. 3A and 3B). With such a structure, regions of the semiconductor layer 108, with which the carbide layer 112 is not in contact, can be covered with the source electrode layer 116a and the drain electrode layer 116b. Accordingly, there is an advantage that the semiconductor layer 108 is protected and the reliability is improved. Further, contact resistance between the semiconductor layer 108 and the source and drain electrode layers 116a and 116b can be reduced by an increase in the contact area between the semiconductor layer 108 and the source and drain electrode layers 116a and 116b.

[0039]

The widths of the source electrode layer 116a and the drain electrode layer 116b (Wd) indicate the lengths of the source electrode layer 116a and the drain electrode layer 116b in the channel width direction.

[0040]

The widths of the source electrode layer 116a and the drain electrode layer 116b (Wd) may be larger than the width of the carbide layer 112 (Wb). Alternatively, only one of the widths of the source electrode layer 116a and the drain electrode layer 116b (Wd) may be larger than the width of the semiconductor layer 108 (Wc) (or the width of the carbide layer 112 (Wb)).

[0041]

In the structures described in this embodiment, a light-blocking portion such as a black matrix may be provided above and/or below the carbide layer 112 to shield the carbide layer 112 from light. Variation in electrical characteristics of the transistor due to irradiation of the carbide layer 112 with light can be suppressed by a structure in which the carbide layer 112 is shield from light. In the case where the gate electrode layer 102 is formed using a light-blocking material, a light-blocking portion such as a black matrix may be provided over the carbide layer 112 (on the side opposite to the gate electrode layer 102).

[0042]

Next, the effectiveness of the carbide layer provided in contact with the semiconductor layer is described on the basis of computation simulation. Note that the effect of silicon carbide (SiC) and amorphous silicon (a-Si) which block hydrogen was researched here.

5 [0043]

〈Calculation method〉

First, motion of atoms was tracked by numerically solving equations of motion for each atom by classical molecular dynamics simulation where the temperature T was set at 25 °C. With the use of mean-square displacement of hydrogen atoms (H atoms) obtained from the calculation results, the diffusion coefficient D of H atoms was calculated from Einstein's relation (Formula 1). As the diffusion coefficient D is larger, diffusion is more likely to be caused.

[0044]

[Formula 1]

15

$$\lim_{t \rightarrow \infty} \left\langle \frac{1}{N} \sum_{i=1}^N |r_i(t) - r_i(0)|^2 \right\rangle_t = 6Dt \quad \dots(\text{Formula 1})$$

20

$$\left(\begin{array}{l} \left\langle \frac{1}{N} \sum_{i=1}^N |r_i(t) - r_i(0)|^2 \right\rangle_t : \text{The mean-square displacement of H atoms} \\ N: \text{the number of H atoms} \\ r_i(t): \text{position of the } i\text{-th H atom in time "t"} \\ \langle \rangle_t : \text{time average} \end{array} \right)$$

25 [0045]

〈Calculation model and calculation conditions〉

FIG. 4A illustrates an a-Si:H model (density: 2.30 g/cm³) in which 60 H atoms (10 at.%) are added into 540 a-Si atoms. FIG. 4B illustrates an a-SiC:H model (density: 3.22 g/cm³) in which 67 H atoms (10 at.%) are added into 600 a-SiC atoms. Here, three-dimensional periodic boundary conditions are used, which allows calculation of a bulk.

[0046]

An empirical potential which characterizes the interaction between atoms is defined in the classical molecular dynamics method which is used in this calculation, so that force that acts on each atom is evaluated. For the a-Si:H model, a Tersoff potential (between silicon atoms) and a Lennard-Jones potential (between a silicon atom and a hydrogen atom, between hydrogen atoms) were used. For the a-SiC:H model, a Tersoff potential (between silicon atoms, between carbon atoms, between a silicon atom and a carbon atom) and a Lennard-Jones potential (between a silicon atom and a hydrogen atom, between a carbon atom and a hydrogen atom, between hydrogen atoms) were used. As a calculation program, simulation software "Materials Explorer 5.0", which is manufactured by Fujitsu Limited, was used.

[0047]

Classical molecular dynamics simulation was performed on each calculation model under the conditions where the number of atoms was fixed, the volume was fixed, and the temperature T was set at 25 °C (time step: 0.2 fsec $\times$ 5 million steps) to obtain the mean-square displacement of hydrogen.

[0048]

〈Calculation results and consideration〉

The mean-square displacement of H atoms in a-Si and the mean-square displacement of H atoms in a-SiC, which were obtained from the calculation, are shown in FIG. 5A. FIG. 5B shows the diffusion coefficients D of H atoms in the calculation models, each of which are obtained from the region where the slope in the graph of FIG. 5A is substantially constant (60 psec to 100 psec). From FIG. 5B, it was found that H in a-SiC are less likely to be diffused than H atoms in a-Si. In other words, it seems that an a-SiC film has a high effect of preventing entry of hydrogen into the semiconductor layer as compared to an a-Si film.

[0049]

Next, an example of a manufacturing method of the transistor illustrated in FIGS. 1A to 1C is described with reference to FIGS. 6A to 6D and FIGS. 7A and 7B.

[0050]

First, the gate electrode layer 102 is formed over the substrate 100 and the gate insulating film 104 is formed over the gate electrode layer 102. Then, a semiconductor

film 106 is formed over the gate insulating film 104 (see FIG. 6A).

[0051]

A substrate having an insulating surface may be used as the substrate 100, and for example, a glass substrate can be used. Alternatively, as the substrate 100, an insulating substrate formed using an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate; a semiconductor substrate which is formed using a semiconductor material such as silicon and whose surface is covered with an insulating material; or a conductive substrate which is formed using a conductor such as metal or stainless steel and whose surface is covered with an insulating material can be used. Further alternatively, a plastic substrate can be used as long as it can withstand heat treatment in a manufacturing process.

[0052]

The gate electrode layer 102 can be formed in the following manner: after a conductive film is formed over an entire surface of the substrate 100, the conductive film is etched by a photolithography method.

[0053]

The gate electrode layer 102 can be formed using a conductive material such as aluminum (Al), copper (Cu), molybdenum (Mo), tungsten (W), or titanium (Ti). Note that when aluminum is used alone for the wiring or the electrode, there are problems in that aluminum has low heat resistance and that aluminum is easily eroded, for example. Therefore, it is preferable to use aluminum in combination with a heat-resistant conductive material.

[0054]

As the heat-resistant conductive material, an element selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc); an alloy containing the above element as its component; an alloy film containing a combination of the above elements; or a nitride containing the above element as its component may be used. A film formed using any of these heat-resistant conductive materials and an aluminum (or copper) film may be stacked, so that the wiring and the electrode may be formed.

[0055]

The gate electrode layer 102 may be formed using a material having high

conductivity and a light-transmitting property. As such a material, indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), organoindium, organotin, zinc oxide (ZnO), or the like can be used, for example. The gate electrode layer 102 can be formed to have a single layer structure or a stacked structure of two or more layers using
5 any of the above-mentioned materials.

[0056]

Note that an insulating film serving as a base film may be provided between the substrate 100 and the gate electrode layer 102. The base film has a function of preventing diffusion of an impurity element from the substrate 100, and can be formed
10 to have a single layer or stacked structure using one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0057]

The gate insulating film 104 can be formed using a silicon oxide film, a silicon
15 oxynitride film, a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, a tantalum oxide film, or the like. Further, any of these films may be stacked. For example, any of these films can be formed by a sputtering method or the like with a thickness of greater than or equal to 10 nm and less than or equal to 500 nm.

[0058]

The semiconductor film 106 can be formed using any of the following
20 materials: a semiconductor material formed of a Group 14 element such as silicon, germanium, or silicon germanium; a compound semiconductor material such as GaAs, InP, or GaN; and an oxide semiconductor material including zinc oxide, tin oxide, or the like. The crystallinity of the semiconductor film 106 may be either single crystal or
25 non-single-crystal (e.g., polycrystalline, microcrystalline, or amorphous). Note that the semiconductor film 106 may include two or more crystal structures among the above crystal structures (e.g., the amorphous structure and the microcrystalline structure (or the polycrystalline structure)).

[0059]

30 As the oxide semiconductor material, an In-Ga-Zn-O-based non-single-crystal film or any of the following oxide semiconductor materials can be used: an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, an

Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, an Sn-Al-Zn-O-based oxide semiconductor, an In-Zn-O based oxide semiconductor, an Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, an In-O-based oxide semiconductor, an Sn-O-based oxide semiconductor, a Zn-O-based oxide semiconductor, and an In-Sn-O-based oxide semiconductor. For example, an oxide semiconductor film is formed by a sputtering method using an In-Ga-Zn-O-based oxide semiconductor target. Alternatively, the oxide semiconductor film can be formed by a sputtering method under a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (typically argon) and oxygen. In the case of using a sputtering method, the film formation may be performed with a target including SiO at greater than or equal to 2 wt% and less than or equal to 10 wt% so that SiO_x ($X > 0$) which inhibits crystallization may be included in the oxide semiconductor film. Thus, crystallization can be suppressed at the time of heat treatment for dehydration or dehydrogenation to be performed in a later process.

[0060]

Next, the semiconductor film 106 is etched to form the island-shaped semiconductor layer 108 (see FIG. 6B). At this time, the semiconductor film 106 is etched so that the island-shaped semiconductor layer 108 remains at least above the gate electrode layer 102.

[0061]

Then, a carbide film 110 is formed so as to cover the semiconductor layer 108 (see FIG. 6C).

[0062]

The carbide film 110 can be formed by a sputtering method. In this case, the carbide film 110 can be formed by a DC or RF sputtering method using a silicon carbide target or a silicon carbide target to which boron is added, under an argon atmosphere at greater than or equal to a room temperature and less than or equal to 400 °C, preferably at greater than or equal to a room temperature and less than or equal to 100 °C. However, without limitation to this, the carbide film 110 may be formed by a CVD method or the like at greater than or equal to 100 °C and less than or equal to the upper temperature limit of the substrate. The thickness of the carbide film 110 can be set to

greater than or equal to 1 nm and less than or equal to 500 nm, preferably greater than or equal to 10 nm and less than or equal to 100 nm.

[0063]

For example, the carbide film 110 is formed by a sputtering method in an atmosphere which does not include hydrogen such as an argon atmosphere or an atmosphere which includes a small amount of hydrogen, whereby the concentration of hydrogen contained in the carbide film 110 can be reduced. Accordingly, change in semiconductor characteristics of the semiconductor layer 108 due to hydrogen contained in the carbide film 110 can be reduced.

[0064]

In the case of using an oxide semiconductor film or an amorphous silicon film as the semiconductor film 106, the semiconductor film 106 and the carbide film 110 can be formed successively by a sputtering method. When the semiconductor film 106 and the carbide film 110 are successively formed, the semiconductor film 106 is not exposed to the atmosphere; thus, entry of impurities between the semiconductor film 106 and the carbide film 110 can be suppressed.

[0065]

Next, the carbide film 110 is etched to form the island-shaped carbide layer 112 (see FIG. 6D). At this time, the carbide film 110 is etched so that the island-shaped carbide layer 112 remains at least in a region that overlaps the gate electrode layer 102. In addition, the carbide film 110 is etched so as to expose at least part of the semiconductor layer 108.

[0066]

As the etching, dry etching with the use of a fluorine-based gas such as CF_4 , SF_6 , or NF_3 can be applied. In the case of using an oxide semiconductor material for the semiconductor layer 108, etching selectivity of the carbide layer 112 with respect to the semiconductor layer 108 can be high and the carbide layer 112 can be favorably etched while the semiconductor layer 108 is hardly etched. Further, damage to the semiconductor layer 108 can be reduced.

[0067]

Note that etching selectivity shows, for example in the case of etching a layer A and a layer B, the difference between etching rates of the layer A and the layer B.

Accordingly, a high etching selectivity means that there is a sufficient difference between the etching rates.

[0068]

At this time, heat treatment may be performed in the case of using an oxide semiconductor material for the semiconductor layer 108. The heat treatment eliminates substances including hydrogen atoms in the oxide semiconductor layer; thus, a structure of the oxide semiconductor layer can be improved and defect level in energy gap can be reduced. The heat treatment is performed under an inert gas atmosphere at greater than or equal to 250 °C and less than or equal to 700 °C, preferably greater than or equal to 450 °C and less than or equal to 600 °C or less than a strain point of the substrate. The inert gas atmosphere is preferably an atmosphere which contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is greater than or equal to 6 N (99.9999 %), preferably greater than or equal to 7 N (99.99999 %) (that is, the concentration of the impurities is greater than or equal to 1 ppm, preferably less than or equal to 0.1 ppm).

[0069]

The heat treatment can be performed in such a way that, for example, an object to be heated is introduced into an electric furnace in which a resistance heating element or the like is used and heated, under a nitrogen atmosphere at 450 °C for an hour. During the heat treatment, the oxide semiconductor layer is not exposed to the atmosphere to prevent the entry of water and hydrogen.

[0070]

The impurities are reduced by the heat treatment, leading to an i-type semiconductor layer (an intrinsic semiconductor layer) or a substantially i-type semiconductor layer. Accordingly, a transistor having extremely excellent characteristics can be realized.

[0071]

The above heat treatment has an effect of removing hydrogen, water, and the like and can be referred to as dehydration treatment, dehydrogenation treatment, or the

like. The heat treatment can be performed at any timing, for example, during the formation of the oxide semiconductor layer, or after the semiconductor layer is processed to have an island shape. Such dehydration treatment or dehydrogenation treatment may be conducted not only once but also plural times.

5 [0072]

Then, a conductive film 114 is formed over the gate insulating film 104, the semiconductor layer 108, and the carbide layer 112 (see FIG. 7A).

[0073]

10 The conductive film 114 can be formed by a sputtering method, a vacuum evaporation method, or the like using metal including an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc); an alloy including the above element as a component; or a material including a nitride or the like in which the above element is included.

15 [0074]

The conductive film 114 may be formed using a material having high conductivity and a light-transmitting property. As such a material, indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), organoindium, organotin, zinc oxide (ZnO), or the like can be used, for example.

20 [0075]

For example, the conductive film 114 can be formed to have a single layer structure of a molybdenum film or a titanium film. The conductive film 114 may be formed to have a stacked structure and, for example, can be formed to have a stacked structure of an aluminum film and a titanium film. Alternatively, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are sequentially stacked may be used. A three-layer structure in which a molybdenum film, an aluminum film, and a molybdenum film are sequentially stacked may be used. As the aluminum films used for these stacked structures, an aluminum film including neodymium (an Al-Nd film) may be used. Further alternatively, the conductive film 25 114 may be formed to have a single layer structure of an aluminum film including silicon. Moreover, the conductive film 114 may be formed to have a stacked structure of an aluminum film and an ITO film. The thickness of the conductive film 114 is set 30

to 1 nm to 200 nm.

[0076]

Next, the conductive film 114 is etched to form the source electrode layer 116a and the drain electrode layer 116b (see FIG. 7B).

5 [0077]

In the above-described step, the carbide layer 112 serves as a channel protective layer (a channel stop layer) which suppresses etching of the semiconductor layer 108 when the conductive film 114 is etched.

[0078]

10 As illustrated in FIG. 7B, the carbide layer 112 is provided in contact with the back channel side (the surface on the side opposite to the gate electrode layer 102) of the semiconductor layer 108, whereby the carbide layer 112 serves as a channel protective layer and entry of an element or the like which causes change in semiconductor characteristics into the semiconductor layer 108 can be suppressed. As
15 a result, change in semiconductor characteristics of the semiconductor layer 108 due to the entry of an element or the like which causes change in semiconductor characteristics can be suppressed; accordingly, variation in electrical characteristics and deterioration of a transistor in which the semiconductor layer 108 is used as a channel layer can be suppressed. Deterioration, change in qualities of the carbide layer can be suppressed
20 when the carbide layer is exposed to various chemical solutions in the manufacturing process because the carbide layer is a chemically stable film. The carbide layer is also a thermally stable film, and thus, change in the state can be suppressed when the interface between the semiconductor layer and the carbide layer is heated. As compared to the case where the carbide layer 112 is not provided in contact with the
25 semiconductor layer 108, change in semiconductor characteristics caused by exposure of the semiconductor layer 108 can be suppressed.

[0079]

Through the above process, the transistor 120 can be manufactured.

[0080]

30 Further, a protective insulating layer may be formed so as to cover the transistor 120. As the protective insulating layer, for example, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a

silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, or an aluminum nitride oxide film may be formed by a CVD method, a sputtering method, or the like. Further, after the source electrode layer 116a and the drain electrode layer 116b are formed, the exposed portion of the carbide layer 112 may be oxidized (including natural oxidation) or nitrided to form a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a silicon nitride oxide film in a region over the carbide layer 112, which is located between the source electrode layer 116a and the drain electrode layer 116b.

[0081]

Then, various electrodes and wirings are formed, whereby a semiconductor device including the transistor 120 is completed.

[0082]

The case where the carbide layer 112 is formed after the semiconductor layer 108 is formed is illustrated in FIGS. 6A to 6D and FIGS. 7A and 7B. However, after the semiconductor film 106 and the carbide film 110 are formed in succession so as to be stacked, they may be patterned into the semiconductor layer 108 and the carbide layer 112, respectively, with a plurality of masks. By forming the semiconductor film 106 and the carbide film 110 in succession in this manner, damage to the surface of the semiconductor film 106 due to plasma or the like can be reduced.

[0083]

Further, in the structure illustrated in FIGS. 1A to 1C, a low resistance layer 115a can be provided between the semiconductor layer 108 and the source electrode layer 116a and a low resistance layer 115b can be provided between the semiconductor layer 108 and the drain electrode layer 116b (see FIG. 8). The low resistance layers 115a and 115b have resistance which is lower than resistance of the semiconductor layer 108. The low resistance layers 115a and 115b are provided, so that contact resistance between the source electrode layer 116a and the semiconductor layer 108 and contact resistance between the drain electrode layer 116b and the semiconductor layer 108 can be reduced. In FIG. 8, after the formation of the carbide layer 112, a low resistance film and a conductive film are formed over the entire surface of the substrate, and then the low resistance layers 115a and 115b, the source electrode layer 116a, and the drain electrode layer 116b are formed.

[0084]

In the case of using silicon for the semiconductor layer 108, a material in which an impurity element imparting one conductivity type is added to silicon may be used for the low resistance layers 115a and 115b. For example, an n-type silicon film such as an amorphous silicon film including an impurity element imparting n-type conductivity such as phosphorus (P), or the like to can be used. In the case of using an oxide semiconductor for the semiconductor layer 108, oxide conductive layers can be used as the low resistance layers 115a and 115b. As a material of the oxide conductive layer, a conductive material that transmits visible light, for example, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, an Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, an Sn-Al-Zn-O-based metal oxide, an In-Zn-O-based metal oxide, an Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, an In-O-based metal oxide, an Sn-O-based metal oxide, a Zn-O-based metal oxide, or In-Sn-O-based metal oxide can be employed. The thickness of the oxide conductive layer is selected as appropriate, in the range of greater than or equal to 1 nm and less than or equal to 300 nm. In the case of using a sputtering method, the film formation may be performed with a target including SiO₂ at greater than or equal to 2 wt% and less than or equal to 10 wt% so that SiO_x ($X > 0$) which inhibits crystallization may be included in the conductive film which transmits light. Thus, crystallization can be suppressed at the time of heat treatment for dehydration or dehydrogenation to be performed in a later process.

[0085]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0086]

(Embodiment 2)

In this embodiment, structures of a semiconductor device which are different from those described in Embodiment 1 and a manufacturing method thereof are described with reference to FIGS. 9A to 9C and FIGS. 10A to 10D. The structure and the manufacturing method (e.g., applicable materials) described in this embodiment are in common with those of Embodiment 1 in many points. Thus, description of the

common points is omitted and only points different from those of Embodiment 1 are described in detail below.

[0087]

FIG. 9A is a top view and FIG. 9B is a cross-sectional view taken along line
5 A1-B1 of FIG. 9A.

[0088]

First, structures of the transistor of this embodiment are described. A transistor 130 illustrated in FIGS. 9A and 9B includes the gate electrode layer 102 provided over the substrate 100, the gate insulating film 104 provided over the gate
10 electrode layer 102, the semiconductor layer 108 provided over the gate insulating film 104, the source electrode layer 116a and the drain electrode layer 116b which are electrically connected to the semiconductor layer 108, and the carbide film 110 provided so as to cover the semiconductor layer 108, the source electrode layer 116a, and the drain electrode layer 116b (see FIGS. 9A and 9B). In the transistor 130, part of the
15 semiconductor layer 108, which is located between the source and the drain, is removed. Such a transistor is also referred to as a channel-etched transistor.

[0089]

The carbide film is provided so as to cover the semiconductor layer 108, the source electrode layer 116a, and the drain electrode layer 116b of the transistor 130.
20 The carbide film is provided in contact with the back-channel side of the semiconductor layer, whereby the carbide film serves as a protection film, which can prevent moisture or the like from being in contact with or entering the semiconductor layer. As a result, change in semiconductor characteristics of the semiconductor layer 108 due to entry or contact of an impurity such as hydrogen can be suppressed; accordingly, variation and
25 deterioration in electrical characteristics of the transistor in which the semiconductor layer 108 is used as a channel layer can be suppressed.

[0090]

In the structure illustrated in FIGS. 9A to 9C, a silicon carbide film can be used as the carbide film 110 which is provided over and in contact with the surface of the
30 semiconductor layer 108. Silicon nitride carbide, germanium carbide, or the like may be used other than a silicon carbide. Alternatively, an impurity imparting one conductivity type may be added to the silicon carbide. For example, n-type silicon

carbide including an impurity element imparting n-type conductivity such as phosphorus or arsenic, or p-type silicon carbide including an impurity element imparting p-type conductivity such as boron, aluminum, or gallium. The carbide film 110 can be formed using one or combination of the above-mentioned materials.

5 [0091]

Further, the transistor 130 may have a structure in which the low resistance layer 115a is provided between the semiconductor layer 108 and the source electrode layer 116a and a low resistance layer 115b is provided between the semiconductor layer 108 and the drain electrode layer 116b (see the transistor 131 illustrated in FIG. 9C).
10 The low resistance layers 115a and 115b have resistance which is lower than resistance of the semiconductor layer 108. The low resistance layers 115a and 115b are provided, so that contact resistance between the source electrode layer 116a and the semiconductor layer 108 and contact resistance between the drain electrode layer 116b and the semiconductor layer 108 can be reduced.

15 [0092]

In the case of using silicon for the semiconductor layer 108, a material in which an impurity element imparting one conductivity type is added to silicon may be used for the low resistance layers 115a and 115b. For example, an n-type silicon film such as an amorphous silicon film including an impurity element imparting n-type conductivity
20 such as phosphorus (P), or the like to can be used. In the case of using an oxide semiconductor for the semiconductor layer 108, oxide conductive layers can be used as the low resistance layers 115a and 115b. As a material of the oxide conductive layer, a conductive material that transmits visible light, for example, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, an Sn-Ga-Zn-O-based metal oxide, an
25 Al-Ga-Zn-O-based metal oxide, an Sn-Al-Zn-O-based metal oxide, an In-Zn-O-based metal oxide, an Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, an In-O-based metal oxide, an Sn-O-based metal oxide, a Zn-O-based metal oxide, or In-Sn-O-based metal oxide can be employed. The thickness of the oxide conductive layer is selected as appropriate, in the range of greater than or equal to 1 nm and less
30 than or equal to 300 nm. In the case of using a sputtering method, the film formation may be performed with a target including SiO₂ at greater than or equal to 2 wt% and

less than or equal to 10 wt% so that SiO_x ($X > 0$) which inhibits crystallization may be included in the conductive film which transmits light. Thus, crystallization can be suppressed at the time of heat treatment for dehydration or dehydrogenation to be performed in a later process.

5 [0093]

Next, an example of a manufacturing method of the transistor illustrated in FIGS. 9A to 9C is described with reference to FIGS. 10A to 10D.

[0094]

10 First, the gate electrode layer 102 is formed over the substrate 100, and then the gate insulating film 104 is formed over the gate electrode layer 102. The semiconductor layer 108 is formed over the gate insulating film 104 (see FIG. 10A).

[0095]

Next, the conductive film 114 is formed over the gate insulating film 104 and the semiconductor layer 108 (see FIG. 10B).

15 [0096]

Then, a resist mask 117 is formed and the conductive film 114 is selectively etched to form the source electrode layer 116a and the drain electrode layer 116b, while part (part near the surface) of the island-shaped semiconductor layer 108 is removed (channel-etched) to form a recessed portion in the island-shaped semiconductor layer 108. As illustrated in FIG. 10C, part of the semiconductor layer 108 is removed to form a recessed portion 118, whereby the source electrode layer 116a and the drain electrode layer 116b are electrically insulated from each other without fault. Note that the resist mask 117 is removed after the etching.

[0097]

25 Then, the carbide film 110 is formed so as to cover the semiconductor layer and the conductive layers (see FIG. 10D).

[0098]

Through the above-described process, the transistor 130 can be manufactured.

[0099]

30 Note that in FIGS. 10A to 10D, the case where the carbide film 110 is formed so as to cover the transistor 130 is described; however, one embodiment of the present invention is not limited thereto. The carbide film 110 may be provided in contact with

at least a region in which a channel is formed in the semiconductor layer 108.

[0100]

In the case of using an oxide semiconductor for the semiconductor layer 108, dehydration treatment or dehydrogenation treatment is preferably performed. The dehydration treatment or dehydrogenation treatment can be performed at any timing, for example, during the formation of the oxide semiconductor layer, or after the oxide semiconductor layer is processed to have an island shape. Such dehydration treatment or dehydrogenation treatment may be conducted not only once but also plural times.

[0101]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0102]

(Embodiment 3)

In this embodiment, structures of a semiconductor device which are different from those described in Embodiment 1 and a manufacturing method thereof are described with reference to FIGS. 11A to 11C and FIGS. 12A to 12E. The structure and the manufacturing method (e.g., applicable materials) described in this embodiment are in common with those of Embodiment 1 in many points. Thus, description of the common points is omitted and only points different from those of Embodiment 1 are described in detail below.

[0103]

Note that FIG. 11A is a top view and FIG. 11B is a cross-sectional view taken along line A1-B1 of FIG. 11A.

[0104]

A transistor 140 illustrated in FIGS. 11A and 11B includes the gate electrode layer 102 provided over the substrate 100, the gate insulating film 104 provided over the gate electrode layer 102, the source electrode layer 116a and the drain electrode layer 116b provided over the gate insulating film 104, the semiconductor layer 108 provided over the source electrode layer 116a and the drain electrode layer 116b and over the gate insulating film 104 which is located in a region above the gate electrode layer 102 and between the source electrode layer 116a and the drain electrode layer 116b, and the carbide layer 112 provided so as to cover the semiconductor layer 108 (see FIGS. 11A

and 11B).

[0105]

That is, the transistor 140 described in this embodiment have a structure where the position of the source electrode layer 116a and the drain electrode layer 116b and the position of the semiconductor layer 108 (the order of stacking) are interchanged in the structures of the above embodiments. The structures illustrated in FIGS. 11A to 11C are also referred to as a bottom-gate bottom-contact type. Note that FIG. 11A is a top view and FIG. 11B is a cross-sectional view taken along line A1-B1 of FIG. 11A.

[0106]

As illustrated in FIGS. 11A and 11B, the carbide layer 112 is provided in contact with the back channel side (the surface on the side opposite to the gate electrode layer 102) of the semiconductor layer 108, whereby entry of an element or the like which causes change in semiconductor characteristics into the semiconductor layer 108 can be suppressed. As a result, change in semiconductor characteristics of the semiconductor layer 108 due to the entry of an element or the like which causes change in semiconductor characteristics can be suppressed; accordingly, change in electrical characteristics of a transistor in which the semiconductor layer 108 is used as a channel layer can be suppressed.

[0107]

In the structure illustrated in FIGS. 11A to 11C, a silicon carbide layer can be used as the carbide layer 112 which is provided over and in contact with the surface of the semiconductor layer 108. Silicon nitride carbide, germanium carbide, or the like may be used other than silicon carbide. Alternatively, an impurity imparting one conductivity type may be added to the silicon carbide. For example, n-type silicon carbide including an impurity element imparting n-type conductivity such as phosphorus or arsenic, or p-type silicon carbide including an impurity element imparting p-type conductivity such as boron, aluminum, or gallium can be used. The carbide layer 112 can be formed using one or combination of the above-mentioned materials.

[0108]

As in a transistor 141 illustrated in FIG. 11C, the low resistance layer 115a may be provided between the semiconductor layer 108 and the source electrode layer 116a

and the low resistance layer 115b may be provided between the semiconductor layer 108 and the drain electrode layer 116b. The low resistance layers 115a and 115b are provided, so that contact resistance between the source electrode layer 116a and the semiconductor layer 108 and contact resistance between the drain electrode layer 116b and the semiconductor layer 108 can be reduced.

[0109]

Next, an example of a manufacturing method of the transistor 140 illustrated in FIGS. 11A and 11B is described with reference to FIGS. 12A to 12E.

[0110]

10 First, the gate electrode layer 102 is formed over the substrate 100 and the gate insulating film 104 is formed over the gate electrode layer 102. After that, the source electrode layer 116a and the drain electrode layer 116b are formed over the gate insulating film 104 (see FIG. 12A).

[0111]

15 Next, the semiconductor film 106 is formed so as to cover the source electrode layer 116a and the drain electrode layer 116b (see FIG. 12B).

[0112]

20 Then, the semiconductor film 106 is etched to form the island-shaped semiconductor layer 108 (see FIG. 12C). At this time, the semiconductor film 106 is etched so that the island-shaped semiconductor layer 108 remains at least above the gate electrode layer 102.

[0113]

Next, the carbide film 110 is formed so as to cover the semiconductor layer 108 (see FIG. 12D).

25 [0114]

Then, the carbide film 110 is etched to form the island-shaped carbide layer 112 (see FIG. 12E).

[0115]

Through the above process, the transistor 140 can be manufactured.

30 [0116]

Note that a protective insulating layer may be formed so as to cover the transistor 140 after the transistor 140 is formed.

[0117]

In the case where the transistor illustrated in FIG. 11C is manufactured, in FIG. 12A, a conductive film forming the source electrode layer 116a and the drain electrode layer 116b and a low resistance film are stacked in this order over the gate insulating film 104, and then the low resistance film is etched; thus, the low resistance layers 115a and 115b can be formed.

[0118]

In the case of using silicon for the semiconductor layer 108, a material in which an impurity element imparting one conductivity type is added to silicon may be used for the low resistance layers 115a and 115b. For example, an n-type silicon film such as an amorphous silicon film including an impurity element imparting n-type conductivity such as phosphorus (P), or the like to can be used. In the case of using an oxide semiconductor for the semiconductor layer 108, oxide conductive layers can be used as the low resistance layers 115a and 115b. As a material of the oxide conductive layer, a conductive material that transmits visible light, for example, an In-Sn-Zn-O-based metal oxide, an In-Al-Zn-O-based metal oxide, an Sn-Ga-Zn-O-based metal oxide, an Al-Ga-Zn-O-based metal oxide, an Sn-Al-Zn-O-based metal oxide, an In-Zn-O-based metal oxide, an Sn-Zn-O-based metal oxide, an Al-Zn-O-based metal oxide, an In-O-based metal oxide, an Sn-O-based metal oxide, a Zn-O-based metal oxide, or In-Sn-O-based metal oxide can be employed. The thickness of the oxide conductive layer is selected as appropriate, in the range of greater than or equal to 1 nm and less than or equal to 300 nm. In the case of using a sputtering method, the film formation may be performed with a target including SiO_2 at greater than or equal to 2 wt% and less than or equal to 10 wt% so that SiO_x ($X > 0$) which inhibits crystallization may be included in the conductive film which transmits light. Thus, crystallization can be suppressed at the time of heat treatment for dehydration or dehydrogenation to be performed in a later process.

[0119]

Note that in FIGS. 11A to 11C, the case where the island-shaped carbide layer 112 is formed so as to completely cover the semiconductor layer 108 is described; however, one embodiment of the present invention is not limited thereto. The carbide

layer 112 may be provided so as to be in contact with at least a region where a channel is formed in the semiconductor layer 108. For example, the carbide layer 112 can be provided so as to be in contact with part of the semiconductor layer 108. For example, as in the transistor 150 illustrated in FIGS. 13A and 13B, the length of the carbide layer 112 (Lb) is set smaller than the length of the semiconductor layer 108 (Lc). Further, two regions which are not covered with the carbide layer 112 are provided in the channel length direction, and the source electrode layer 116a and the drain electrode layer 116b are provided in the two regions that are apart from each other so as to be electrically connected. When such a structure is employed, the carbide layer 112 may be formed so as to be in contact with part of the semiconductor layer 108 (formed so as not to be in contact with the source electrode layer 116a and the drain electrode layer 116b), and a protective insulating layer 121 may be provided over the carbide layer 112, the semiconductor layer 108, and the source electrode layer 116a and the drain electrode layer 116b. In this manner, leakage current caused by change in semiconductor characteristics of the surface of the semiconductor layer 108 can be reduced.

[0120]

As the protective insulating layer 121, for example, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, or an aluminum nitride oxide film may be formed by a CVD method, a sputtering method, or the like.

[0121]

In the case of using oxide semiconductor for the semiconductor layer 108, dehydration treatment or dehydrogenation treatment is preferably performed. The dehydration treatment or dehydrogenation treatment can be performed at timing, for example, during the formation of the semiconductor layer, or after the semiconductor layer is processed to have an island shape. Such dehydration treatment or dehydrogenation treatment may be conducted not only once but also plural times.

[0122]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0123]

(Embodiment 4)

In this embodiment, an example of a liquid crystal display device is described as a semiconductor device including any of the transistors described in Embodiments 1 to 3. The appearance and the cross section of a liquid crystal display panel in the liquid crystal display device are described with reference to FIGS. 14A-1, 14A-2, and 14B. FIGS. 14A-1 and 14A-2 are each a top view of a panel in which thin film transistors 4010 and 4011 which include a semiconductor layer, and a liquid crystal element 4013, which are formed over a first substrate 4001, are sealed between the first substrate 4001 and a second substrate 4006 with a sealant 4005. FIG. 14B corresponds to a cross-sectional view taken along line M-N of FIGS. 14A-1 and 14A-2.

[0124]

The sealant 4005 is provided so as to surround a pixel portion 4002 and a scan line driver circuit 4004 which are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Thus, the pixel portion 4002 and the scan line driver circuit 4004 as well as a liquid crystal layer 4008 are sealed between the first substrate 4001 and the second substrate 4006 with the sealant 4005. A signal line driver circuit 4003 that is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate which is prepared separately is mounted in a region that is different from the region surrounded by the sealant 4005 over the first substrate 4001.

[0125]

Note that there is no particular limitation on the connection method of a driver circuit which is separately formed, and a COG method, a wire bonding method, a TAB method, or the like can be used. FIG. 14A-1 illustrates an example in which the signal line driver circuit 4003 is mounted by a COG method, and FIG. 14A-2 illustrates an example in which the signal line driver circuit 4003 is mounted by a TAB method.

[0126]

Each of the pixel portion 4002 and the scan line driver circuit 4004 which are provided over the first substrate 4001 includes a plurality of thin film transistors. FIG. 14B illustrates the thin film transistor 4010 included in the pixel portion 4002 and the thin film transistor 4011 included in the scan line driver circuit 4004. Insulating layers 4020 and 4021 are provided over the thin film transistors 4010 and 4011.

[0127]

Any of the structures described in the above embodiments can be applied to the thin film transistors 4010 and 4011.

[0128]

5 A pixel electrode layer 4030 included in the liquid crystal element 4013 is electrically connected to the thin film transistor 4010. A counter electrode layer 4031 included in the liquid crystal element 4013 is formed on the second substrate 4006. A portion where the pixel electrode layer 4030, the counter electrode layer 4031, and the liquid crystal layer 4008 overlap corresponds to the liquid crystal element 4013. Note
10 that the pixel electrode layer 4030 and the counter electrode layer 4031 are provided with insulating layers 4032 and 4033 which function as alignment films, respectively, and the liquid crystal layer 4008 is sandwiched between the pixel electrode layer 4030 and the counter electrode layer 4031 with the insulating layers 4032 and 4033 provided therebetween.

15 [0129]

 The first substrate 4001 and the second substrate 4006 can be formed using glass, metal (typically, stainless steel), ceramic, or plastic. As for plastic, a fiberglass-reinforced plastics (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, or an acrylic resin film can be used. In addition, a sheet with a structure in which
20 an aluminum foil is sandwiched between PVF films or polyester films can be used.

[0130]

 A columnar spacer denoted by reference numeral 4035 is obtained by selective etching of an insulating film and is provided to control a distance (a cell gap) between the pixel electrode layer 4030 and the counter electrode layer 4031. Note that a
25 spherical spacer may also be used. In addition, the counter electrode layer 4031 is electrically connected to a common potential line provided on the same substrate as the thin film transistor 4010. With the use of a common connection portion, the counter electrode layer 4031 and the common potential line can be electrically connected to each other through conductive particles arranged between a pair of substrates. Note
30 that the conductive particles are included in the sealant 4005.

[0131]

 In addition, liquid crystal exhibiting a blue phase for which an alignment film

is unnecessary may be used. The blue phase is one of liquid crystal phases and a phase which appears just before the transition from a cholesteric phase to an isotropic phase when the temperature of cholesteric liquid crystal is increased. Because the blue phase appears only in a small temperature range, a liquid crystal composition in which greater than or equal to 5 wt% of a chiral agent is mixed is used for the liquid crystal layer 4008 in order to improve the temperature range. The liquid crystal composition including liquid crystal exhibiting a blue phase and a chiral agent has a short response time of 10 μ s to 100 μ s and are optically isotropic; therefore, alignment treatment is unnecessary, and viewing angle dependence is small.

10 [0132]

Note that the liquid crystal display device described in this embodiment is an example of a transmissive liquid crystal display device; however, the liquid crystal display device can be applied to either a reflective liquid crystal display device or a semi-transmissive liquid crystal display device.

15 [0133]

The liquid crystal display device described in this embodiment is an example in which a polarizing plate is provided on the outer surface of the substrate (on the viewer side) and a coloring layer and an electrode layer used for a display element are provided on the inner surface of the substrate in this order; however, the polarizing plate may be provided on the inner surface of the substrate. The stacked structure of the polarizing plate and the coloring layer is also not limited to this embodiment and may be set as appropriate depending on materials of the polarizing plate and the coloring layer or conditions of the manufacturing process. In addition, a light-blocking film which functions as a black matrix may be provided.

25 [0134]

In this embodiment, in order to reduce surface unevenness of the thin film transistors and to improve reliability of the thin film transistors, the thin film transistors are covered with the insulating layers (the insulating layer 4020 and the insulating layer 4021) functioning as a protective film or a planarizing insulating film. Note that the protective film is provided to prevent entry of a contaminant impurity such as an organic substance, a metal substance, or moisture floating in the atmosphere and is

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preferably a dense film. As the protective film, a single layer or a stacked layer of any of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, or an aluminum nitride oxide film may be formed by a sputtering method. In this
5 embodiment, an example in which the protective film is formed by a sputtering method is described; however, there is no particular limitation on the method, and a variety of methods may be used.

[0135]

Here, the insulating layer 4020 having a stacked structure is formed as the
10 protective film. Here, a silicon oxide film is formed by a sputtering method, as a first layer of the insulating layer 4020. When the silicon oxide film is used as the protective film, the silicon oxide film has an effect of preventing a hillock of an aluminum film used as a source electrode layer and a drain electrode layer.

[0136]

15 An insulating layer is formed as a second layer of the protective film. Here, a silicon nitride film is formed by a sputtering method, as a second layer of the insulating layer 4020. The use of the silicon nitride film as the protective film can prevent mobile ions of sodium or the like from entering a semiconductor region so that variation in electric characteristics of a TFT can be suppressed.

20 [0137]

After the protective film is formed, annealing (greater than or equal to 200 °C and less than or equal to 400 °C) of the semiconductor layer may be performed.

[0138]

The insulating layer 4021 is formed as the planarizing insulating film. An
25 organic material having heat resistance, such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy can be used for the insulating layer 4021. In addition to such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. Note that the insulating layer 4021 may be formed by
30 stacking a plurality of insulating films formed of these materials.

[0139]

Note that a siloxane-based resin corresponds to a resin formed using a siloxane-based material as a starting material and having the bond of Si-O-Si. As for the siloxane-based resin, an organic group (e.g., an alkyl group or an aryl group) or a fluoro group may be used as a substituent. The organic group may include a fluoro group.

[0140]

There is no particular limitation on the formation method of the insulating layer 4021, and the following method or tool can be used depending on the material of the insulating layer 4021: a sputtering method, an SOG method, a spin coating method, a dip coating method, a spray coating method, a droplet discharge method (e.g., an inkjet method, screen printing, or offset printing), a doctor knife, a roll coater, a curtain coater, a knife coater, or the like. When the insulating layer 4021 is formed using material liquid, annealing (greater than or equal to 200 °C and less than or equal to 400 °C) of the semiconductor layer may be performed in a baking step at the same time. A baking step of the insulating layer 4021 also serves as the annealing of the semiconductor layer, whereby a semiconductor device can be manufactured efficiently.

[0141]

The pixel electrode layer 4030 and the counter electrode layer 4031 can be formed using a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0142]

A conductive composition including a conductive high molecule (also referred to as a conductive polymer) can be used for the pixel electrode layer 4030 and the counter electrode layer 4031. The pixel electrode formed using a conductive composition preferably has a light transmittance of greater than or equal to 70 % at a wavelength of 550 nm. Further, the resistivity of the conductive high molecule included in the conductive composition is preferably less than or equal to 0.1 Ω·cm.

[0143]

As the conductive high molecule, a so-called π -electron conjugated conductive high molecule can be used. As examples thereof, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, and a copolymer of more than two kinds of them can be given.

5 [0144]

Further, a variety of signals and potentials are supplied from an FPC 4018 to the signal line driver circuit 4003 which is formed separately, and the scan line driver circuit 4004 or the pixel portion 4002.

[0145]

10 In this embodiment, a connection terminal electrode 4015 is formed using the same conductive film as the pixel electrode layer 4030 included in the liquid crystal element 4013. A terminal electrode 4016 is formed using the same conductive film as the source and drain electrode layers included in the thin film transistors 4010 and 4011.

[0146]

15 The connection terminal electrode 4015 is electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive film 4019.

[0147]

FIGS. 14A-1, 14A-2, and 14B illustrate an example in which the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001; however, this embodiment is not limited to this structure. The scan line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

20 [0148]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

25 [0149]

(Embodiment 5)

In this embodiment, an example of a light-emitting display device is described as a semiconductor device including any of the transistors described in Embodiments 1 to 3. The appearance and the cross section of a light-emitting display panel (a light-emitting panel) in the light-emitting display device are described with reference to FIGS. 15A and 15B. FIG. 15A is a top view of a panel in which thin film transistors

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4509 and 4510 which include a semiconductor layer formed over a first substrate 4501, and a light-emitting element 4511 are sealed between the first substrate 4501 and a second substrate 4506 with a sealant 4505. FIG. 15B corresponds to a cross-sectional view taken along line H-I of FIG. 15A. Note that an example of using an organic EL element as a light-emitting element is described here.

[0150]

A sealant 4505 is provided so as to surround a pixel portion 4502, signal line driver circuits 4503a and 4503b, and scan line driver circuits 4504a and 4504b which are provided over a first substrate 4501. In addition, a second substrate 4506 is provided over the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b. Accordingly, the pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b are sealed as well as a filler 4507, between the first substrate 4501 and the sealant 4505 with the second substrate 4506. It is preferable that a panel be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the panel is not exposed to the outside air, in this manner.

[0151]

The pixel portion 4502, the signal line driver circuits 4503a and 4503b, and the scan line driver circuits 4504a and 4504b formed over the first substrate 4501 each include a plurality of thin film transistors. In FIG. 15B, a thin film transistor 4510 included in the pixel portion 4502 and a thin film transistor 4509 included in the signal line driver circuit 4503a are illustrated.

[0152]

The thin film transistors 4509 and 4510 can employ any of the structures described in the above embodiments. In this embodiment, the thin film transistors 4509 and 4510 are n-channel thin film transistors.

[0153]

Moreover, reference numeral 4511 denotes a light-emitting element. A first electrode layer 4517 which is a pixel electrode included in the light-emitting element 4511 is electrically connected to a source electrode layer or a drain electrode layer of the thin film transistor 4510. Note that a structure of the light-emitting element 4511 is a

stacked structure of the first electrode layer 4517, the electroluminescent layer 4512, and the second electrode layer 4513, but there is no particular limitation on the structure. The structure of the light-emitting element 4511 can be changed as appropriate depending on the direction in which light is extracted from the light-emitting element 4511, or the like.

[0154]

A partition 4520 is formed using an organic resin film, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition 4520 be formed using a photosensitive material and an opening be formed over the first electrode layer 4517 so that a sidewall of the opening is formed as an inclined surface with continuous curvature.

[0155]

The electroluminescent layer 4512 may be formed with a single layer or a plurality of layers stacked.

[0156]

A protective film may be formed over the second electrode layer 4513 and the partition 4520 in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element 4511. As the protective film, a silicon nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed.

[0157]

In addition, a variety of signals and potentials are supplied to the signal line driver circuits 4503a and 4503b, the scan line driver circuits 4504a and 4504b, or the pixel portion 4502 from FPCs 4518a and 4518b.

[0158]

In this embodiment, a connection terminal electrode 4515 is formed from the same conductive film as the first electrode layer 4517 included in the light-emitting element 4511, and a terminal electrode 4516 is formed from the same conductive film as the source and drain electrode layers included in the thin film transistors 4509 and 4510.

[0159]

The connection terminal electrode 4515 is electrically connected to a terminal included in the FPC 4518a via an anisotropic conductive film 4519.

[0160]

The second substrate 4506 located in the direction in which light is extracted from the light-emitting element 4511 should have a light-transmitting property. In that case, a light-transmitting material such as a glass plate, a plastic plate, a polyester film, or an acrylic film is used for the second substrate 4506.

5 [0161]

As the filler 4507, an ultraviolet curable resin or a thermosetting resin can be used, in addition to an inert gas such as nitrogen or argon. For example, PVC (polyvinyl chloride), acrylic, polyimide, an epoxy resin, a silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used.

10 [0162]

In addition, if needed, an optical film, such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter, may be provided as appropriate on a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film.

[0163]

The signal line driver circuits 4503a and 4503b and the scan line driver circuits 4504a and 4504b may be provided by mounting driver circuits formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared. In addition, only the signal line driver circuits or part thereof, or the scan line driver circuits or part thereof may be separately formed and mounted. This embodiment is not limited to the structure illustrated in FIGS. 15A and 15B.

25 [0164]

Through the above process, a light-emitting display device (a display panel) having high reliability can be manufactured as a semiconductor device.

[0165]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0166]

(Embodiment 6)

In this embodiment, electronic paper is described as an example of semiconductor devices including transistors.

[0167]

FIG. 16 illustrates active matrix electronic paper as an example of the semiconductor device. A thin film transistor 581 used for the semiconductor device can be manufactured in a manner similar to the thin film transistor described in any of Embodiments 1 to 3.

[0168]

The electronic paper in FIG. 16 is an example of a display device using a twisting ball display system. The twisting ball display system refers to a method in which spherical particles each colored in black and white are arranged between a first electrode layer and a second electrode layer which are used for a display element, and a potential difference is generated between the first electrode layer and the second electrode layer to control orientation of the spherical particles, so that display is performed.

[0169]

The thin film transistor 581 provided over a substrate 580 has a bottom gate structure. A source electrode layer or a drain electrode layer is electrically connected to a first electrode layer 587 through a contact hole formed in insulating layers 583, 584, and 585. Between the first electrode layer 587 and a second electrode layer 588, spherical particles 589 each including a black region 590a, a white region 590b, and a cavity 594 filled with liquid around the black region 590a and the white region 590b are provided. The circumference of each of the spherical particles 589 is provided with a filler 595 such as a resin (see FIG. 16). In FIG. 16, the first electrode layer 587 corresponds to a pixel electrode, and the second electrode layer 588 corresponds to a common electrode. The second electrode layer 588 is electrically connected to a common potential line provided on the same substrate as the thin film transistor 581. A common connection portion described in the above embodiment is used, whereby the second electrode layer 588 provided on a substrate 596 and the common potential line can be electrically connected to each other through the conductive particles arranged between a pair of substrates.

[0170]

In that case, a microcapsule having a diameter of approximately 10 μm to 200 μm , in which transparent liquid, positively charged white microparticles, and negatively charged black microparticles are encapsulated, is used. In the microcapsule which is provided between the first electrode layer and the second electrode layer, when an electric field is applied by the first electrode layer and the second electrode layer, the white microparticles and black microparticles move to opposite sides from each other, so that white or black can be displayed. A display element using this principle is an electrophoretic display element, and is called electronic paper in general. Reflectance of the electrophoretic display element is higher than that of a liquid crystal display element, and thus, an assistant light is unnecessary, power consumption is low, and a display portion can be recognized in a dim place. In addition, even when power is not supplied to the display portion, an image which has been displayed once can be maintained. Accordingly, a displayed image can be stored even if a semiconductor device having a display function (which may be referred to simply as a display device or a semiconductor device including a display device) is distanced from an electric wave source.

[0171]

In this manner, highly reliable electronic paper can be manufactured as a semiconductor device.

[0172]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0173]

(Embodiment 7)

In this embodiment, electronic appliances each include any of the display devices described in Embodiments 4 to 6 as part are described.

[0174]

Examples of electronic appliances each manufactured using any of the transistors described in Embodiments 1 to 3 include cameras such as video cameras and digital cameras, goggle type displays, navigation systems, audio reproducing devices (e.g., car audio component or other audio components), computers, game machines,

portable information terminals (e.g., mobile computers, cellular phones, portable game machines, and electronic books), image reproducing devices provided with recording media (i.e., devices that are capable of playing back recording media such as digital versatile discs (DVDs) and equipped with display devices that can display the image), and the like. Specific examples for such electronic appliances are illustrated in FIGS. 17A to 17F.

[0175]

FIG. 17A illustrates a television set according to one embodiment of the present invention, which includes a housing 9101, a supporting base 9102, a display portion 9103, speaker portions 9104, a video input terminal 9105, and the like. In the display portion 9103 of this television set, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the housing 9101. A television set having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0176]

FIG. 17B illustrates a computer according to one embodiment of the present invention, which includes a main body 9201, a housing 9202, a display portion 9203, a keyboard 9204, an external connection port 9205, a pointing device 9206, and the like. In the display portion 9203 of this computer, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the housing 9202. A computer having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0177]

FIG. 17C illustrates a cellular phone according to one embodiment of the present invention, which includes a main body 9401, a housing 9402, a display portion 9403, an audio input portion 9404, an audio output portion 9405, operation keys 9406, an external connection port 9407, an antenna 9408, and the like. In the display portion 9403 of this cellular phone, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the main body 9401 or the housing 9402. A cellular phone having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0178]

FIG. 17D illustrates a camera according to one embodiment of the present invention, which includes a main body 9501, a display portion 9502, a housing 9503, an external connection port 9504, a remote controller receiving portion 9505, an image receiving portion 9506, a battery 9507, an audio input portion 9508, operation keys 9509, an eye piece portion 9510, and the like. In the display portion 9502 of this camera, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the main body 9501 or the housing 9503. A camera having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0179]

FIG. 17E illustrates an example of a digital photo frame. For example, in a digital photo frame 9600, a display portion 9603 is incorporated in a housing 9601. Various images can be displayed on the display portion 9603. For example, the display portion 9603 can display data of an image shot by a digital camera or the like to function as a normal photo frame.

[0180]

Note that the digital photo frame 9600 is provided with an operation portion, an external connection terminal (a USB terminal, a terminal that can be connected to various cables such as a USB cable, or the like), a recording medium insertion portion, and the like. Although they may be provided on the same surface as the display portion, it is preferable to provide them on the side surface or the back surface for the design of the digital photo frame 9600. For example, a memory which stores data of an image shot by a digital camera is inserted in the recording medium insertion portion of the digital photo frame, whereby the image data can be downloaded and displayed on the display portion 9603. In the display portion 9602 of this digital photo frame, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the housing 9601. A digital photo frame having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0181]

The digital photo frame 9600 may have a configuration capable of wirelessly

transmitting and receiving data. Through wireless communication, desired image data can be downloaded to be displayed.

[0182]

FIG. 17F illustrates a cellular phone 9700 which includes a housing 9701, a display portion 9702, and an operation button 9703. In addition, operations such as making calls and composing mails can be conducted when a person touches the display portion 9702 with his/her finger or the like. In the display portion 9702 of this cellular phone, transistors similar to those described in any of Embodiments 1 to 3 are arranged in matrix. The transistors also can be applied to a driver circuit or the like in the main body in the housing 9701. A digital photo frame having high reliability can be obtained with the use of the transistor described in any of Embodiments 1 to 3.

[0183]

There are mainly three screen modes of the display portion 9702. The first mode is a display mode mainly for displaying images. The second mode is an input mode mainly for inputting data such as text. The third mode is a display-and-input mode in which two modes of the display mode and the input mode are combined.

[0184]

For example, in a case of making a call or composing a mail, a text input mode mainly for inputting text is selected for the display portion 9702 so that text displayed on a screen can be input. In that case, it is preferable to display a keyboard or number buttons on almost all area of the screen of the display portion 9702.

[0185]

A detection device including a sensor for detecting inclination, such as a gyroscope or an acceleration sensor, is provided inside the cellular phone 9700, display in the screen of the display portion 9702 can be automatically switched by determining the installation direction of the cellular phone 9700 (whether the cellular phone 9700 is placed horizontally or vertically for a landscape mode or a portrait mode).

[0186]

The screen modes are switched by touching the display portion 9702 or operating the operation button 9703 of the housing 9701. Alternatively, the screen modes may be switched depending on the kind of the image displayed on the display portion 9702. For example, when a signal of an image displayed on the display

portion is a signal of moving image data, the screen mode is switched to the display mode. When the signal is a signal of text data, the screen mode is switched to the input mode.

[0187]

5 Further, in the input mode, when input by touching the display portion 9702 is not performed for a certain period while a signal detected by the optical sensor in the display portion 9702 is detected, the screen mode may be controlled so as to be switched from the input mode to the display mode.

[0188]

10 The display portion 9702 may function as an image sensor. For example, an image of a palm print, a fingerprint, or the like is taken when the display portion 9702 is touched with a palm or a finger, whereby personal identification can be performed. Further, by providing a backlight or a sensing light source which emits a near-infrared light in the display portion, an image of a finger vein, a palm vein, or the like can be
15 taken.

[0189]

As described above, the range of application of the semiconductor device according to one embodiment of the present invention is extremely wide, and the semiconductor device can be applied to electronic appliances in various fields.

20 An electronic appliance having high reliability can be provided with the use of the transistor described in any of Embodiments 1 to 3.

This application is based on Japanese Patent Application serial no. 2009-202449 filed with Japan Patent Office on September 2, 2009, the entire contents of which are hereby
25 incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a gate electrode layer provided over a substrate;

5 a gate insulating film provided over the gate electrode layer;

a semiconductor layer provided over the gate insulating film, the semiconductor layer overlapping with the gate electrode layer;

a carbide layer provided over and in contact with the semiconductor layer;

a source electrode layer electrically connected to the semiconductor layer; and

10 a drain electrode layer electrically connected to the semiconductor layer.

2. The semiconductor device according to claim 1,

wherein the source electrode layer is over and in contact with the semiconductor layer, and

15 wherein the drain electrode layer is over and in contact with the semiconductor layer.

3. The semiconductor device according to claim 1, further comprising a first layer and a second layer,

20 wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

wherein a contact resistance of between the first layer and the source electrode layer is lower than that of between the semiconductor layer and the source electrode layer,

25 wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

wherein a contact resistance of between the second layer and the drain electrode layer is lower than that of between the semiconductor layer and the drain electrode layer.

30

4. The semiconductor device according to claim 1, further comprising a first layer and a second layer,

wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

wherein a resistance of the first layer is lower than that of the semiconductor layer,

5 wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

wherein a resistance of second layer is lower than that of the semiconductor layer.

10 5. The semiconductor device according to claim 1,

wherein the carbide layer comprises a material selected from the group consisting of silicon carbide, silicon nitride carbide, germanium carbide, n-type silicon carbide, and p-type silicon carbide.

15 6. The semiconductor device according to claim 1,

wherein the semiconductor layer includes at least one of indium, zinc, and gallium.

7. A semiconductor device comprising:

20 a gate electrode layer provided over a substrate;

a gate insulating film provided over the gate electrode layer;

a semiconductor layer provided over the gate insulating film;

a source electrode layer electrically connected to the semiconductor layer;

a drain electrode layer electrically connected to the semiconductor layer; and

25 a carbide layer provided in contact with the semiconductor layer, the source electrode layer, and the drain electrode layer.

8. The semiconductor device according to claim 7, further comprising a first layer and a second layer,

30 wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

wherein a contact resistance of between the first layer and the source electrode

layer is lower than that of between the semiconductor layer and the source electrode layer,

wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

5 wherein a contact resistance of between the second layer and the drain electrode layer is lower than that of between the semiconductor layer and the drain electrode layer.

9. The semiconductor device according to claim 7, further comprising a first
10 layer and a second layer,

wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

wherein a resistance of the first layer is lower than that of the semiconductor layer,

15 wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

wherein a resistance of second layer is lower than that of the semiconductor layer.

20 10. The semiconductor device according to claim 7,

wherein the carbide layer comprises from a material selected from the group consisting of silicon carbide, silicon nitride carbide, germanium carbide, n-type silicon carbide, and p-type silicon carbide.

25 11. The semiconductor device according to claim 7,

wherein the semiconductor layer includes at least one of indium, zinc, and gallium.

12. A semiconductor device comprising:

30 a gate electrode layer provided over a substrate;

a gate insulating film provided over the gate electrode layer;

a source electrode layer provided over the gate insulating film;

a drain electrode layer provided over the gate insulating film;

a semiconductor layer provided over the source electrode layer, the drain electrode layer, and the gate electrode layer;

a carbide layer provided over and in contact with the semiconductor layer, and

5 wherein the gate insulating film is interposed between the gate electrode layer and the semiconductor layer.

13. The semiconductor device according to claim 12, further comprising a first layer and a second layer,

10 wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

wherein a contact resistance of between the first layer and the source electrode layer is lower than that of between the semiconductor layer and the source electrode layer,

15 wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

wherein a contact resistance of between the second layer and the drain electrode layer is lower than that of between the semiconductor layer and the drain electrode layer.

20

14. The semiconductor device according to claim 12, further comprising a first layer and a second layer,

wherein the first layer is interposed between the semiconductor layer and the source electrode layer,

25 wherein a resistance of the first layer is lower than that of the semiconductor layer,

wherein the second layer is interposed between the semiconductor layer and the drain electrode layer, and

30 wherein a resistance of second layer is lower than that of the semiconductor layer.

15. The semiconductor device according to claim 12,

wherein the carbide layer comprises from a material selected from the group consisting of silicon carbide, silicon nitride carbide, germanium carbide, n-type silicon carbide, and p-type silicon carbide.

5 16. The semiconductor device according to claim 12,
 wherein the semiconductor layer includes at least one of indium, zinc, and
 gallium.

 17. A method for manufacturing a semiconductor device, comprising the steps
10 of:

 forming a gate electrode layer over a substrate;
 forming a gate insulating film over the gate electrode layer;
 forming a semiconductor layer over the gate insulating film so as to overlap
 with the gate electrode layer;
15 forming a carbide layer over the semiconductor layer;
 forming a source electrode layer so as to be electrically connected to the
 semiconductor layer; and
 forming a drain electrode layer so as to be electrically connected to the
 semiconductor layer.

20 18. The method for manufacturing the semiconductor device according to
 claim 17, further comprising the steps of:

 forming a carbide film so as to cover the semiconductor layer;
 etching the carbide film so as to form the carbide layer;
25 forming a conductive film over the carbide layer and the semiconductor layer;
 and
 etching the conductive film so as to form the source electrode layer and the
 drain electrode layer.

30 19. A method for manufacturing a semiconductor device, comprising the steps
 of:

 forming a gate electrode layer over a substrate;

forming a gate insulating film over the gate electrode layer;

forming a semiconductor layer over the gate insulating film so as to overlap with the gate electrode layer;

5 forming a source electrode layer so as to be electrically connected to the semiconductor layer;

forming a drain electrode layer so as to be electrically connected to the semiconductor layer; and

forming a carbide film so as to cover the semiconductor layer, the source electrode layer, and the drain electrode layer.

10

20. The method for manufacturing the semiconductor device according to claim 19, further comprising the steps of:

forming a conductive film over the semiconductor layer; and

15 etching the conductive film so as to form the source electrode layer and the drain electrode layer.

21. A method for manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode layer over a substrate;

20 forming a gate insulating film over the gate electrode layer;

forming a source electrode layer over the gate insulating film;

forming a drain electrode layer over the gate insulating film;

forming a semiconductor layer over the source electrode layer and the drain electrode layer;

25 forming a carbide layer over the semiconductor layer, and

wherein the gate insulating film is interposed between the gate electrode layer and the semiconductor layer.

30 22. The method for manufacturing the semiconductor device according to claim 21, further comprising the steps of:

forming a conductive film over the gate insulating film;

etching the conductive film so as to form the source electrode layer and the

drain electrode layer;

forming a carbide film so as to cover the semiconductor layer; and
etching the carbide film so as to form the carbide layer.

FIG. 1A

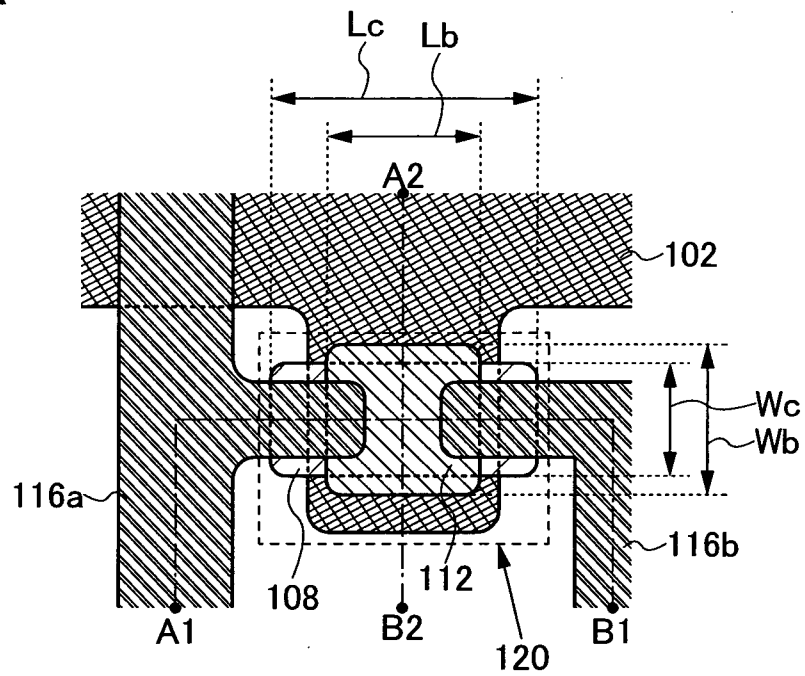


FIG. 1B

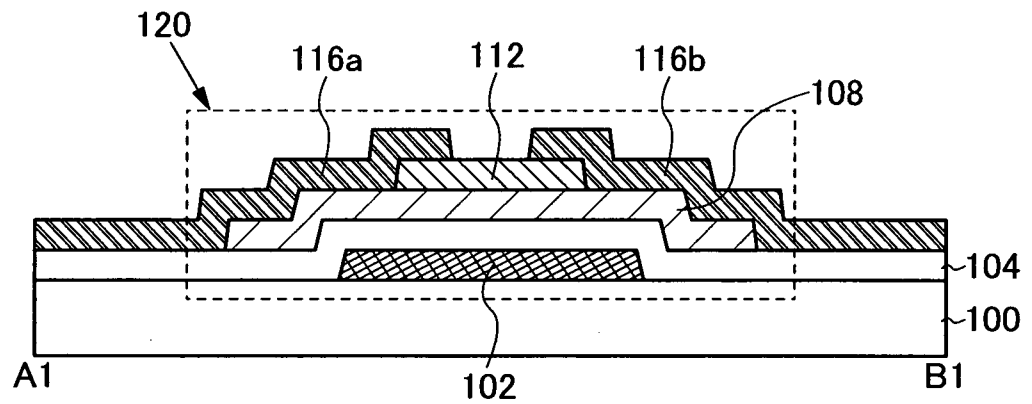


FIG. 1C

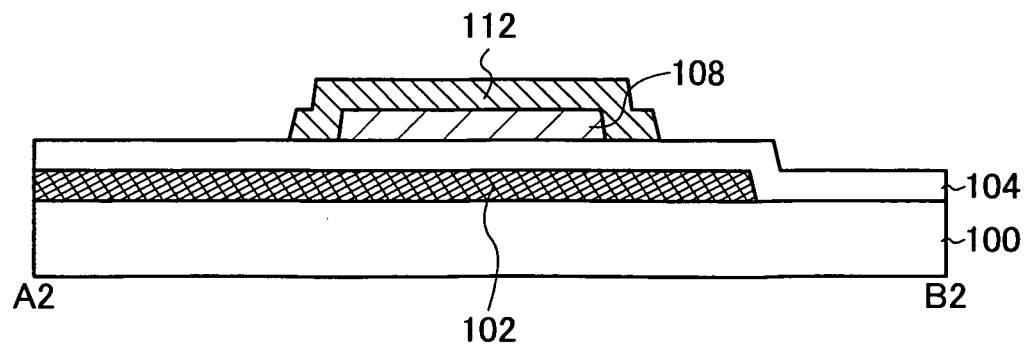


FIG. 2A

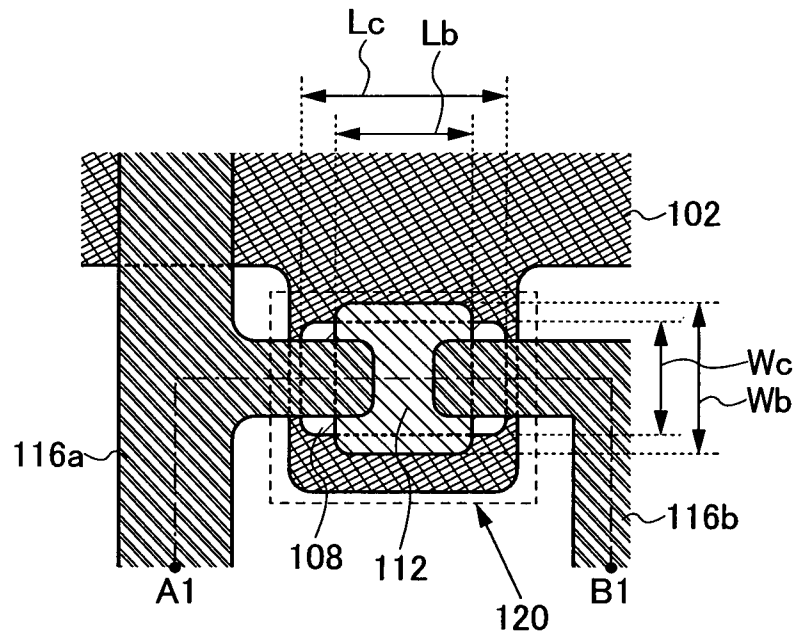


FIG. 2B

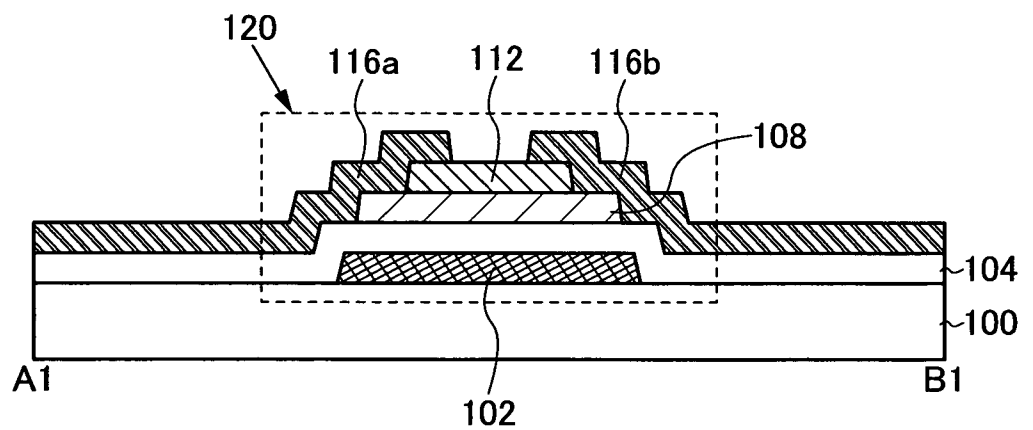


FIG. 3A

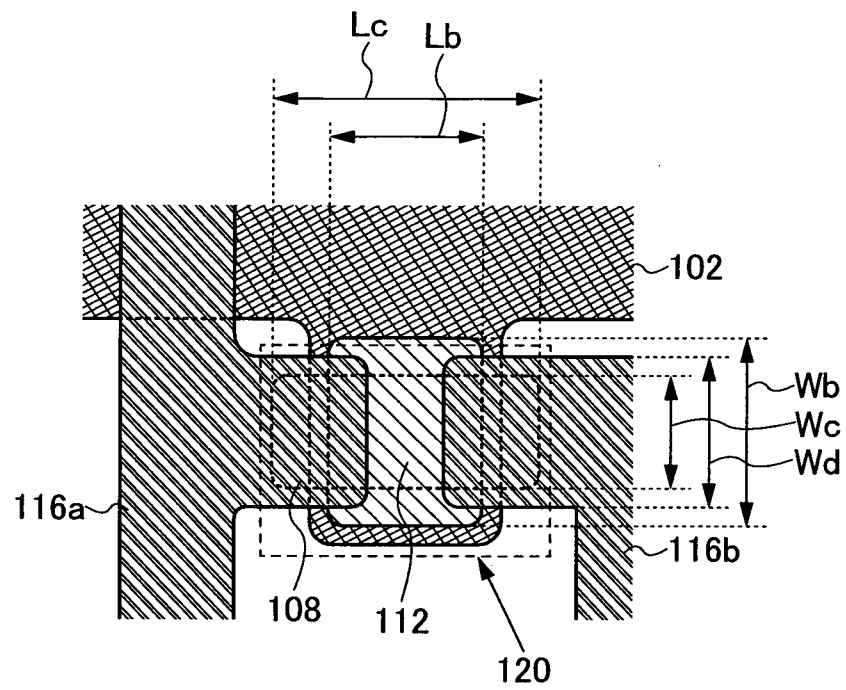


FIG. 3B

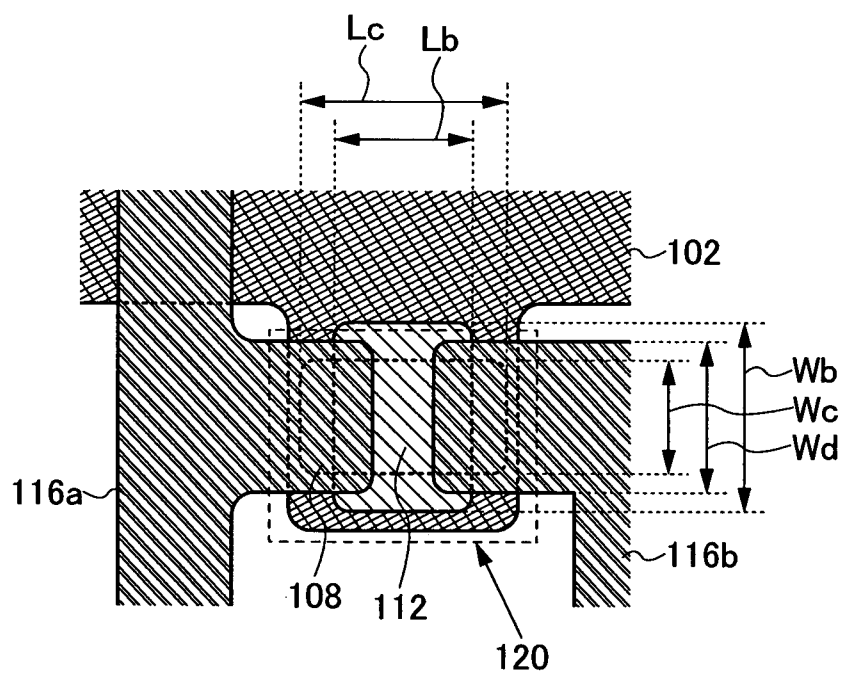


FIG. 4A

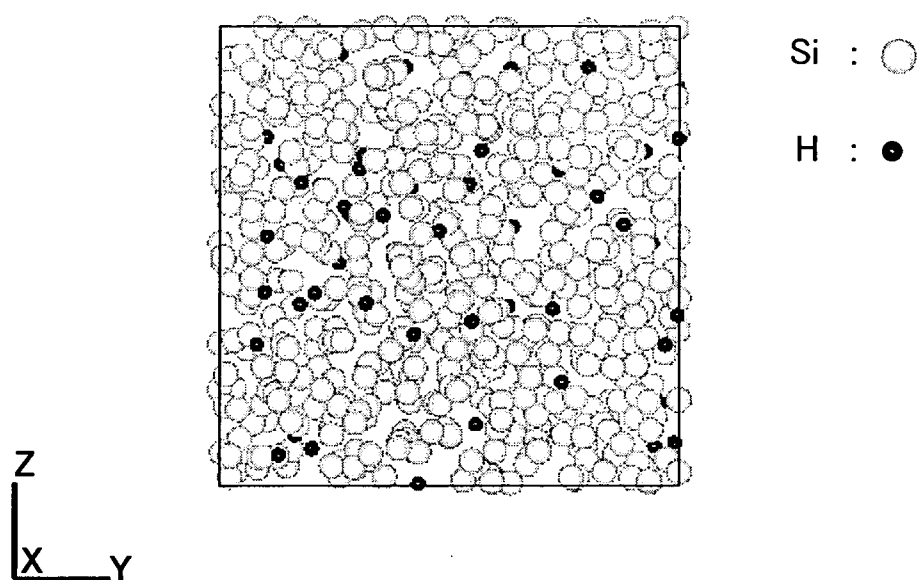


FIG. 4B

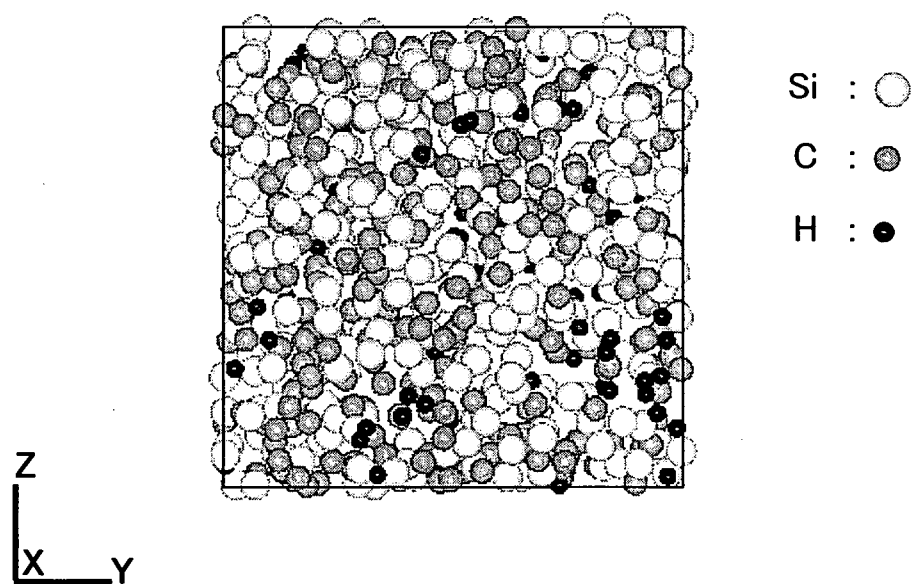


FIG. 5A

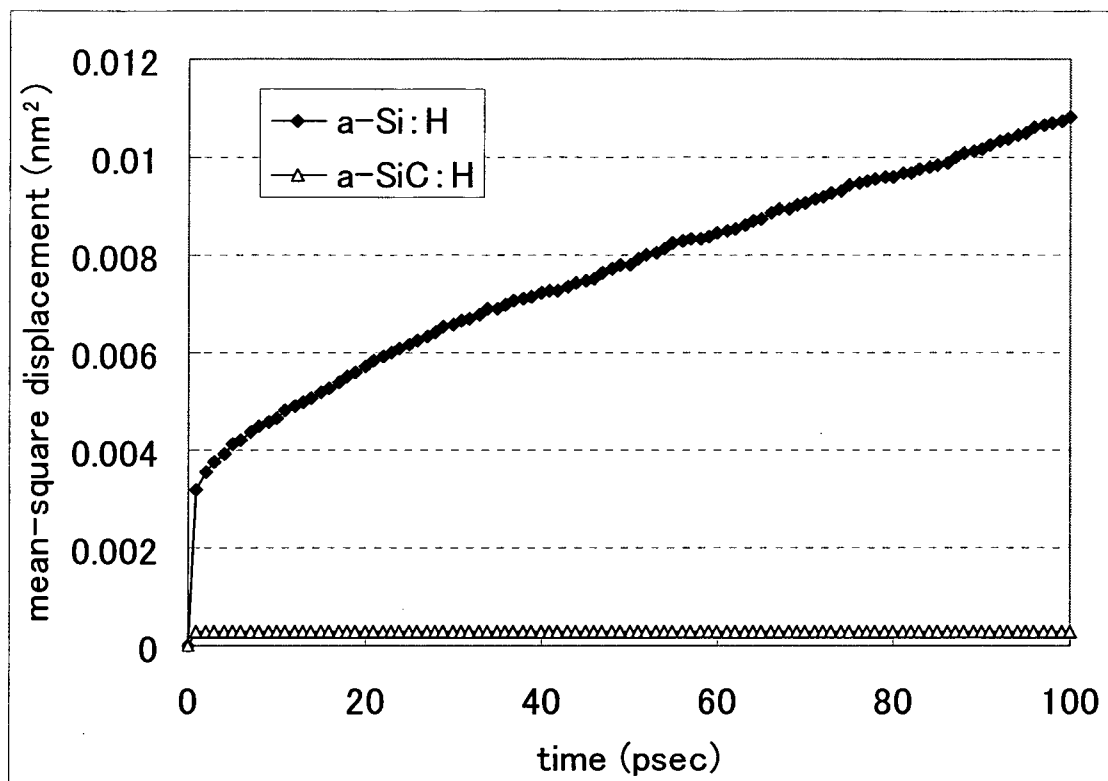


FIG. 5B

Calculation model	D (cm ² /sec)
a-Si:H	9.6×10^{-8}
a-SiC:H	9.5×10^{-11}

FIG. 6A

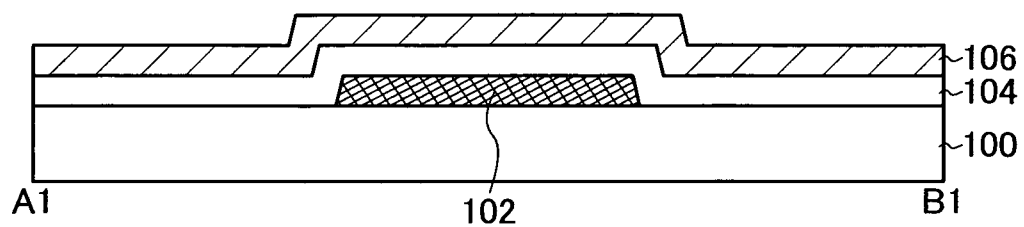


FIG. 6B

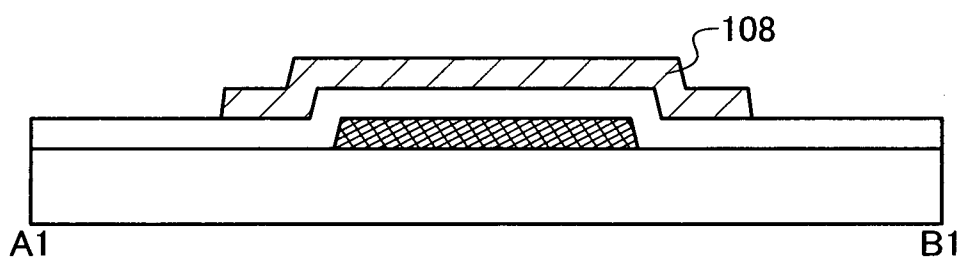


FIG. 6C

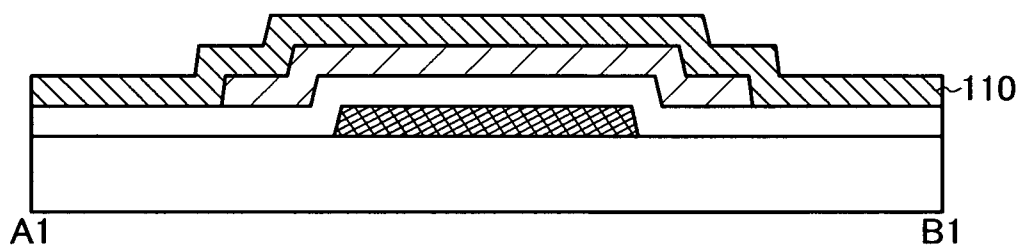


FIG. 6D

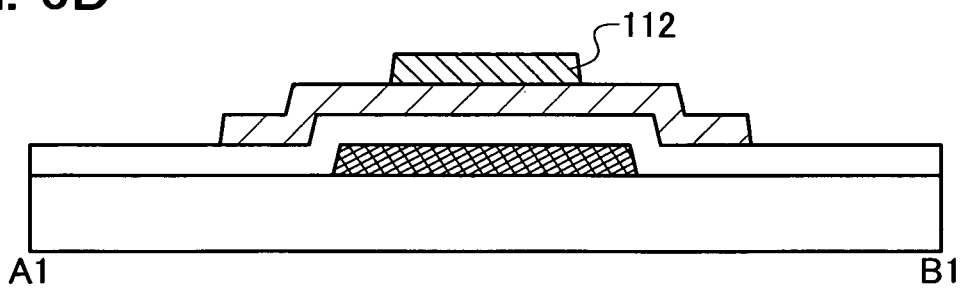


FIG. 7A

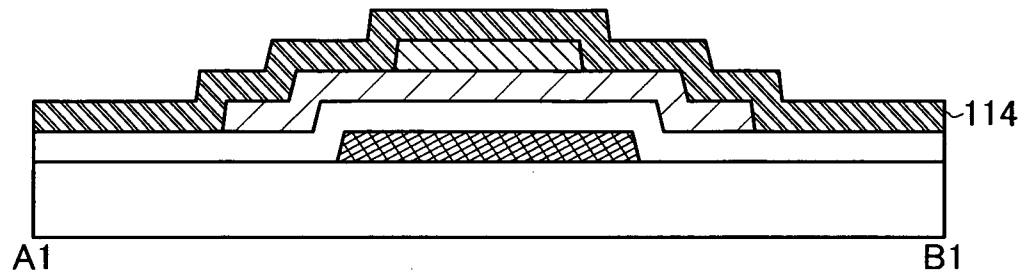


FIG. 7B

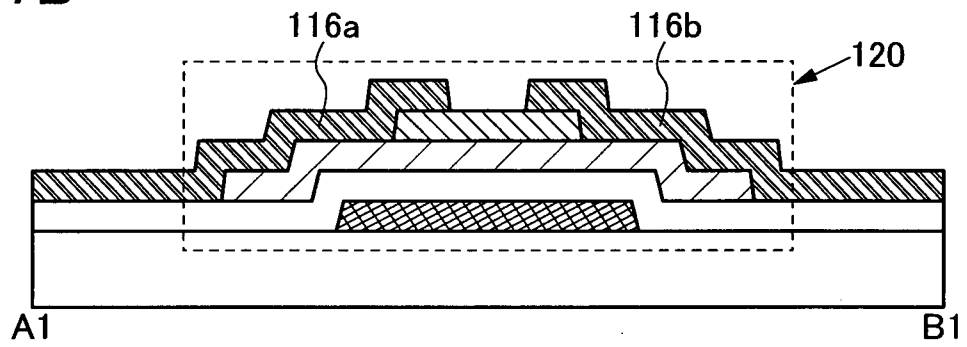


FIG. 8

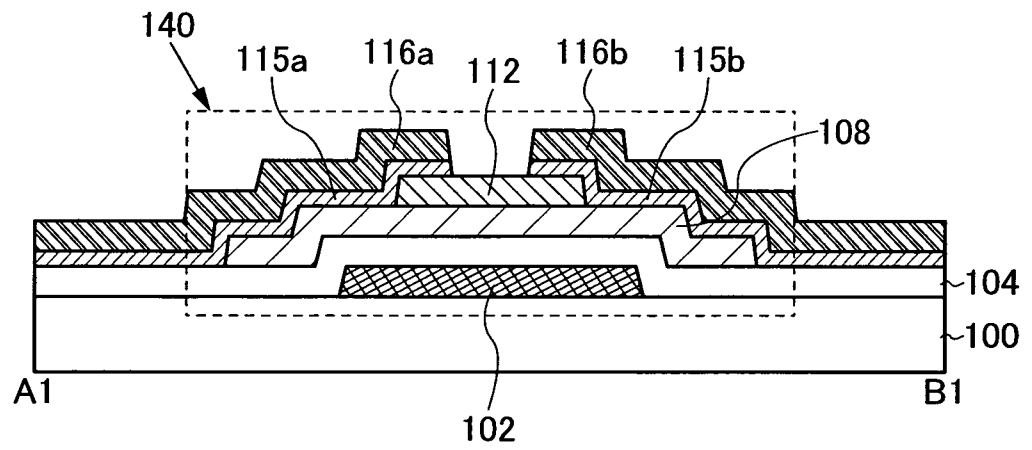


FIG. 9A

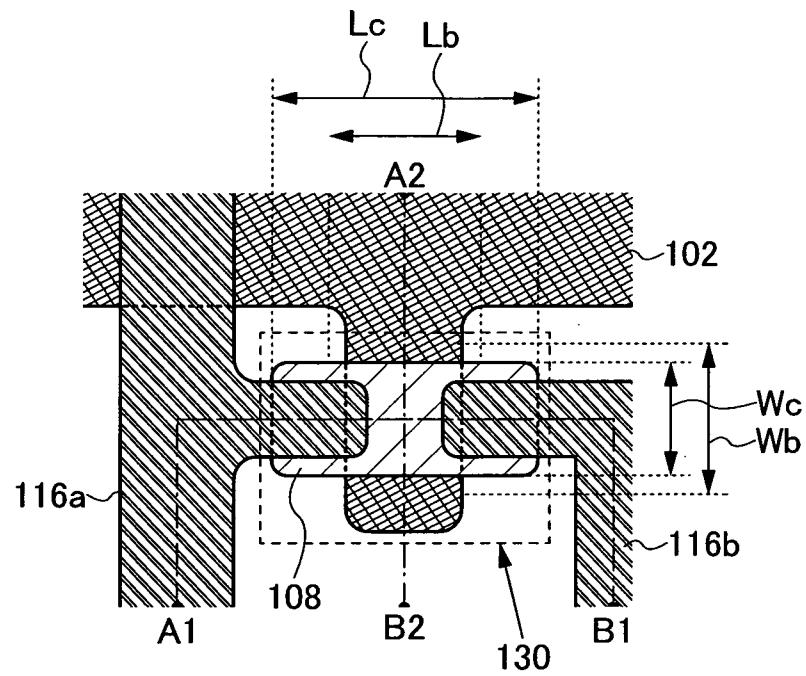


FIG. 9B

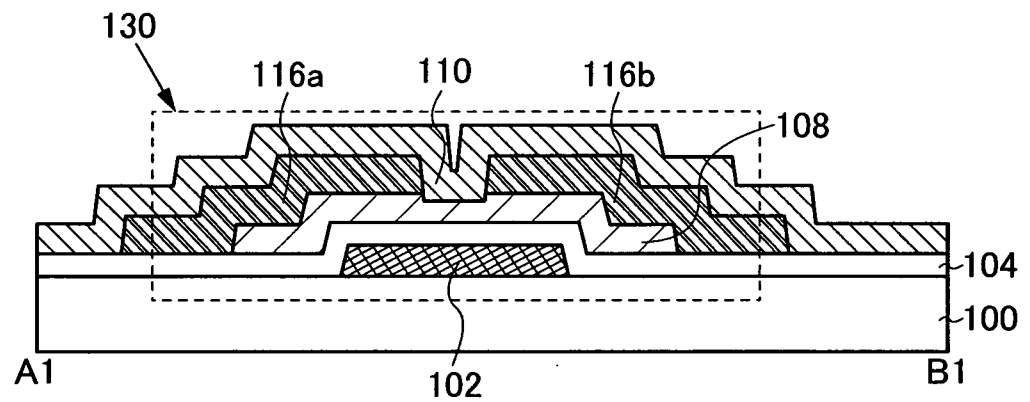


FIG. 9C

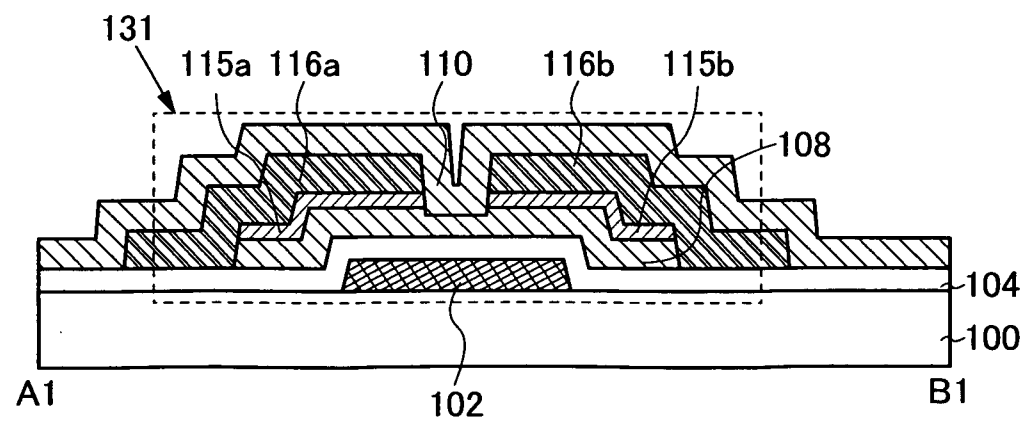


FIG. 10A

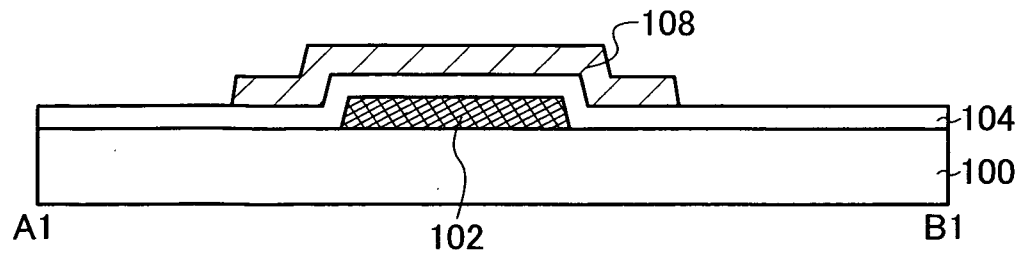


FIG. 10B

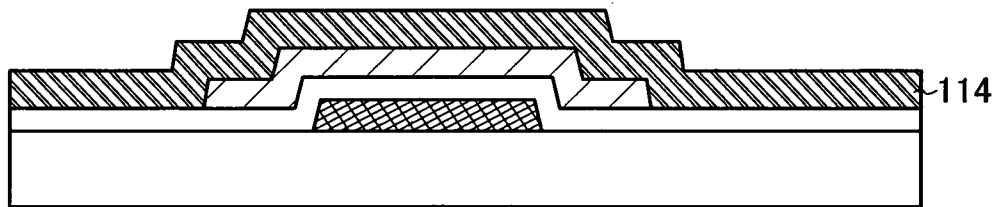


FIG. 10C

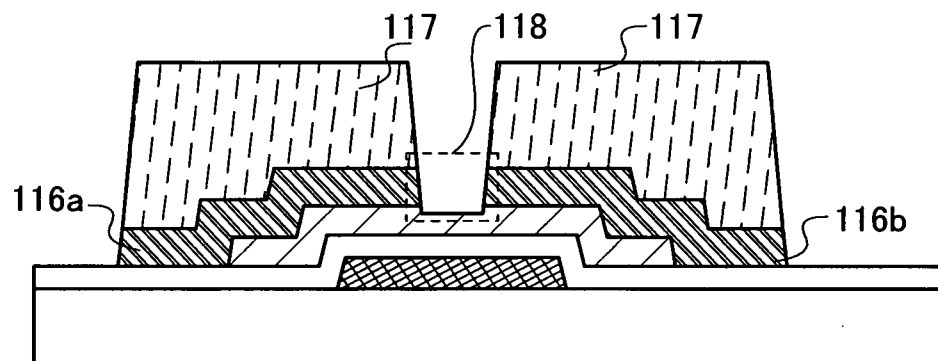


FIG. 10D

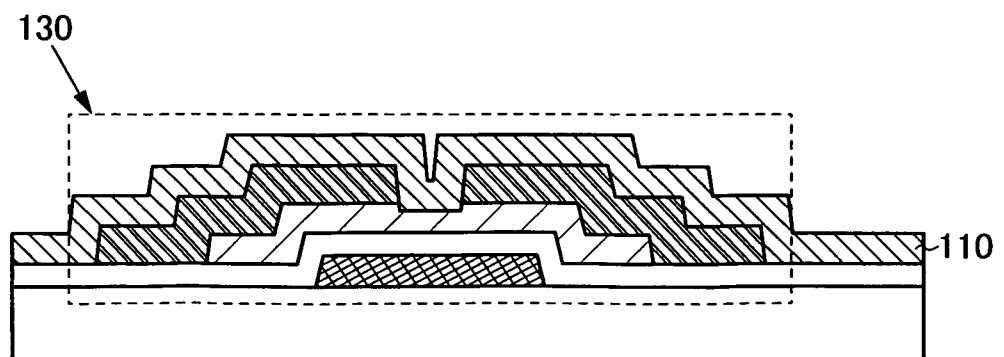


FIG. 11A

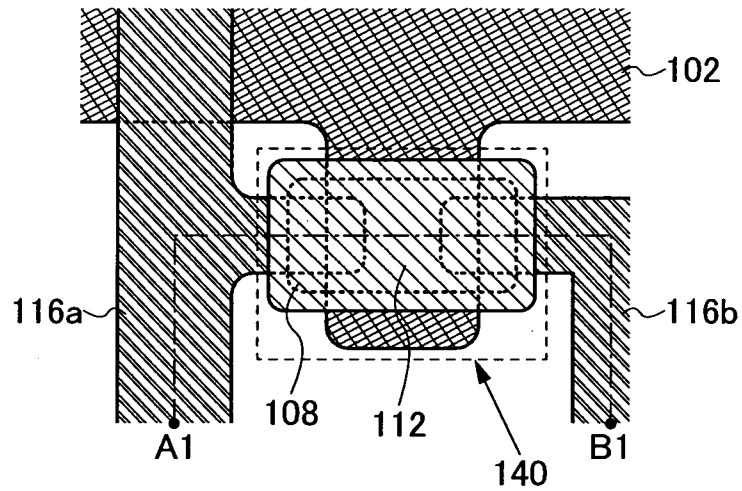


FIG. 11B

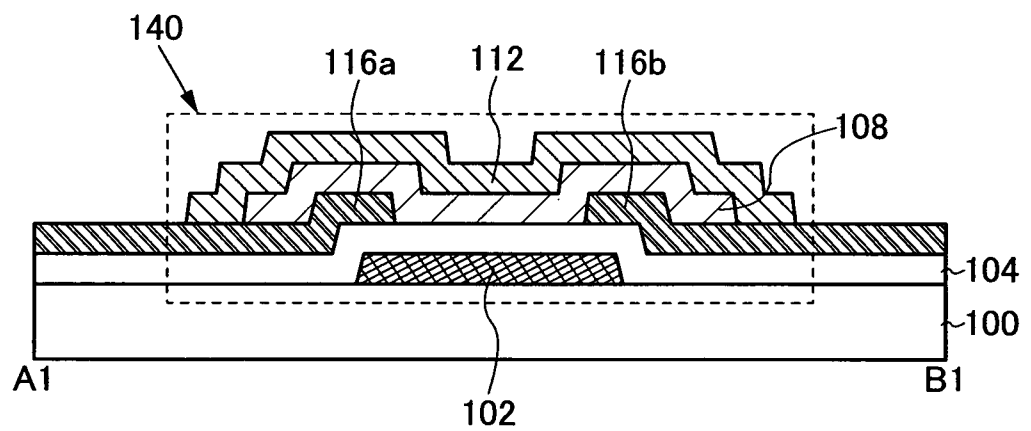


FIG. 11C

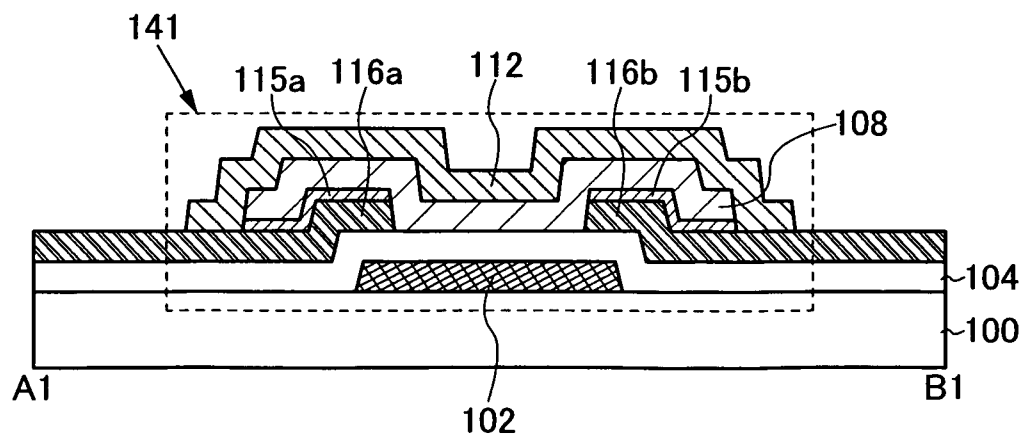


FIG. 12A

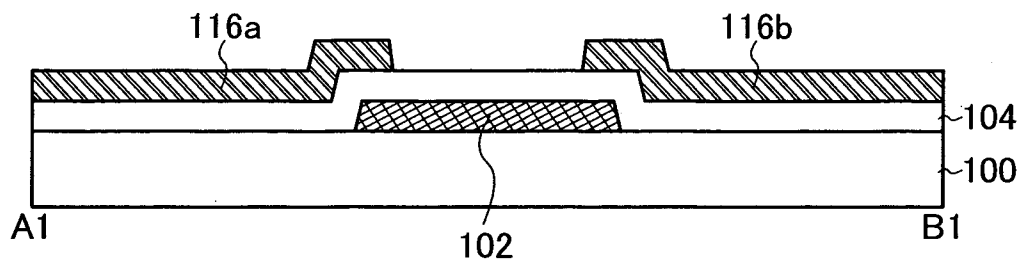


FIG. 12B

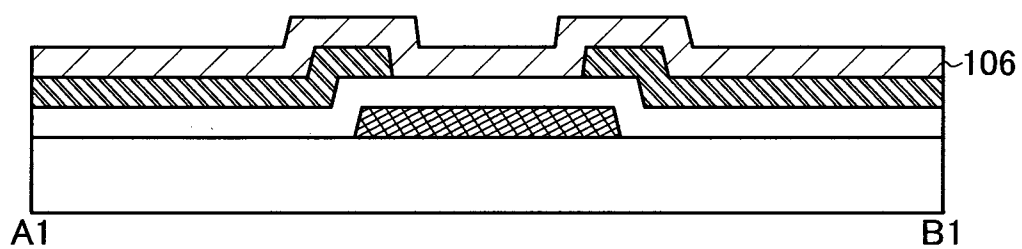


FIG. 12C

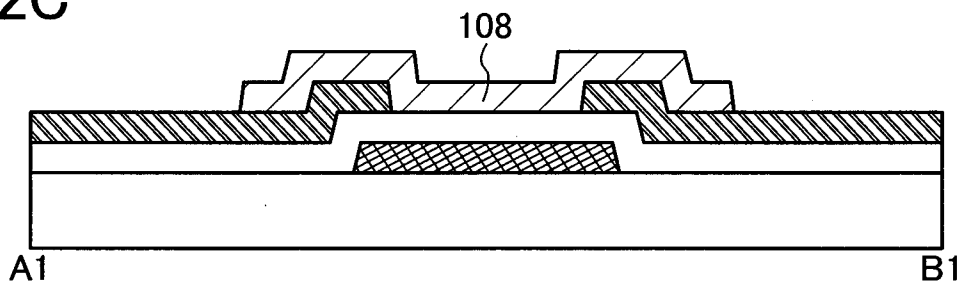


FIG. 12D

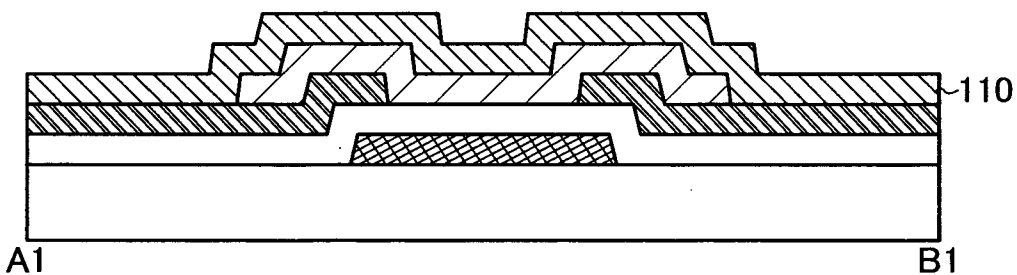


FIG. 12E

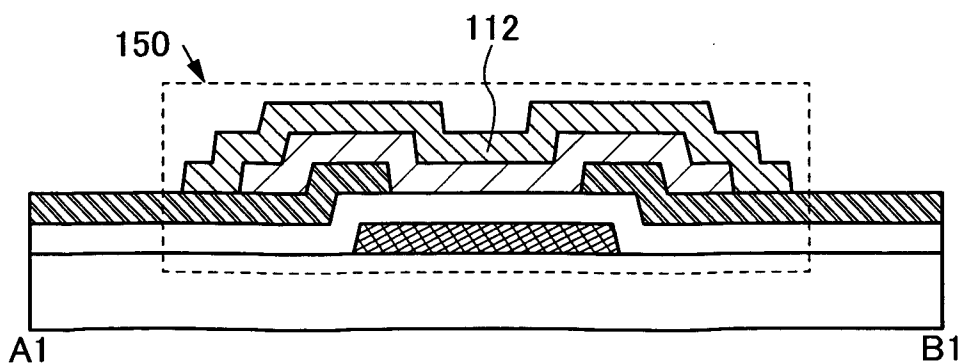


FIG. 13A

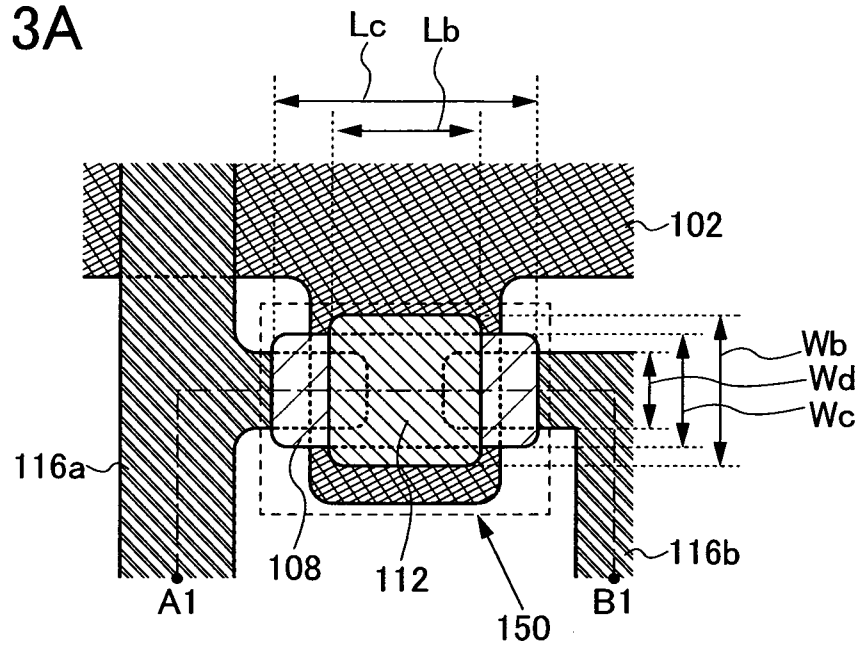


FIG. 13B

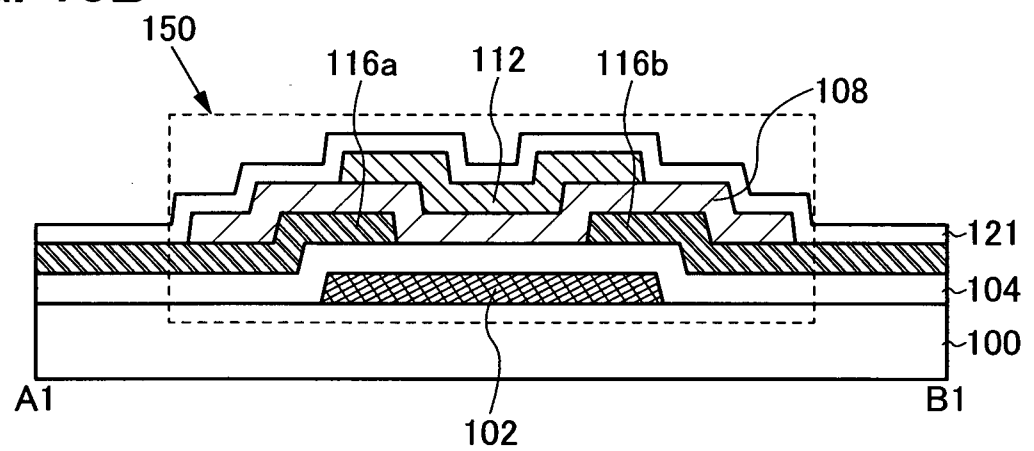


FIG. 14A-1

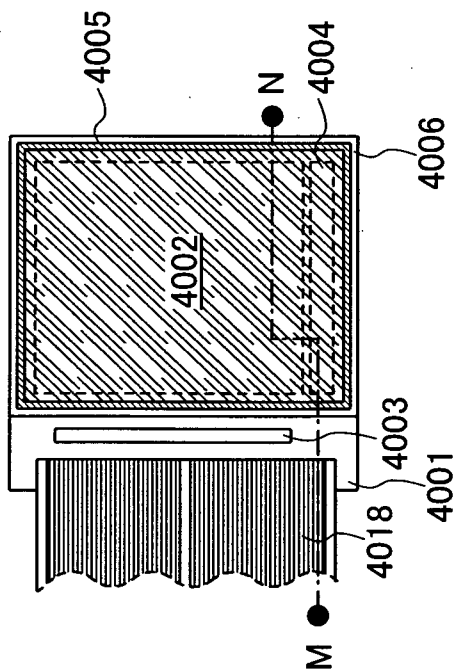


FIG. 14A-2

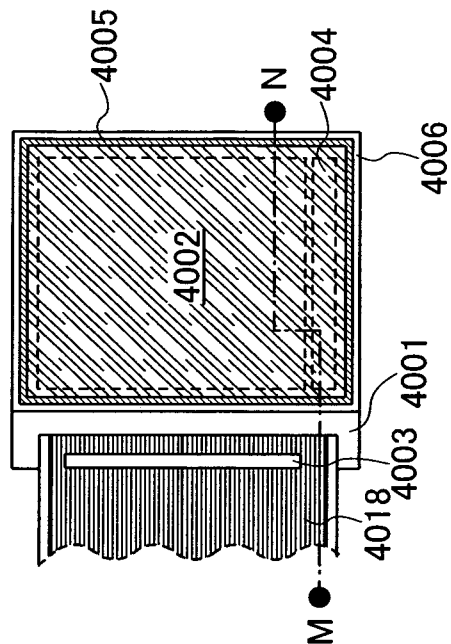


FIG. 14B

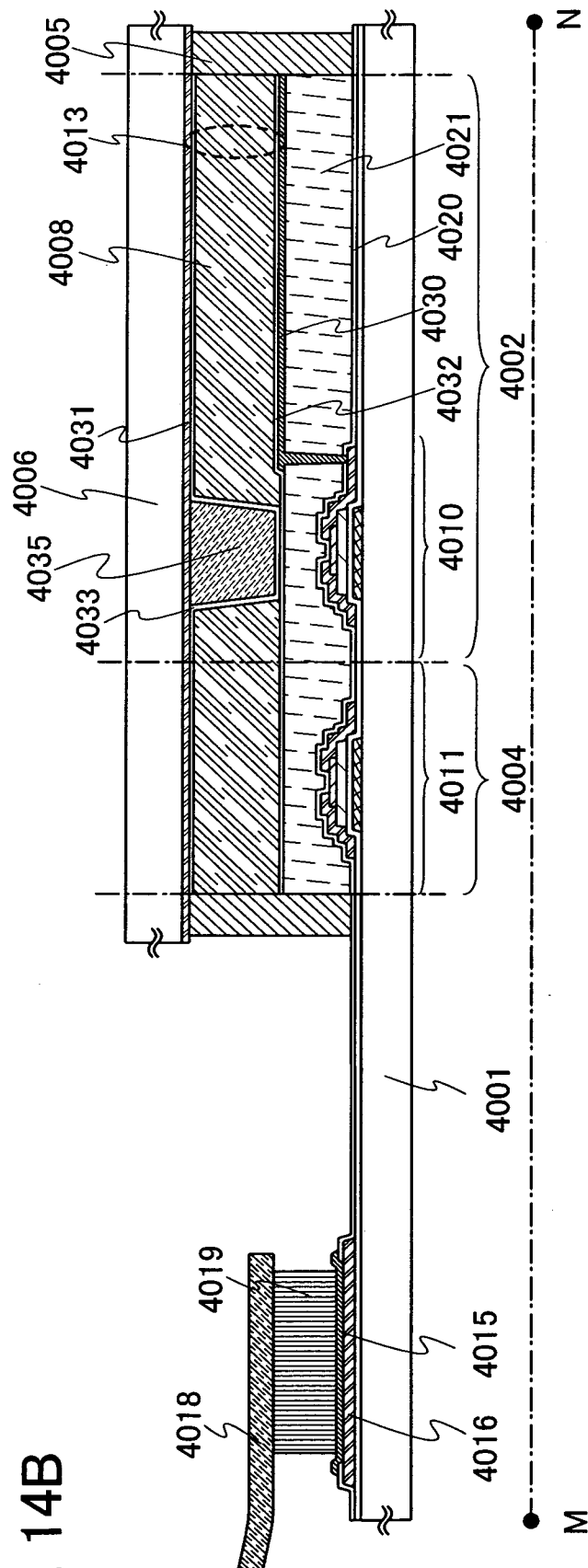


FIG. 15A

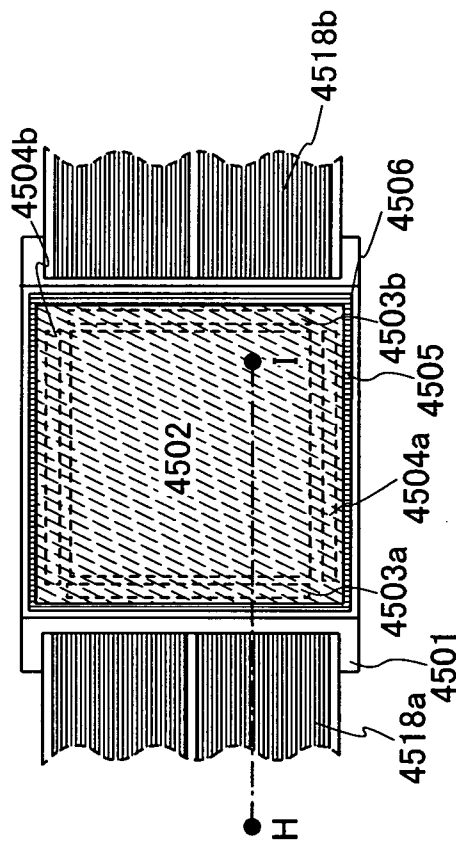


FIG. 15B

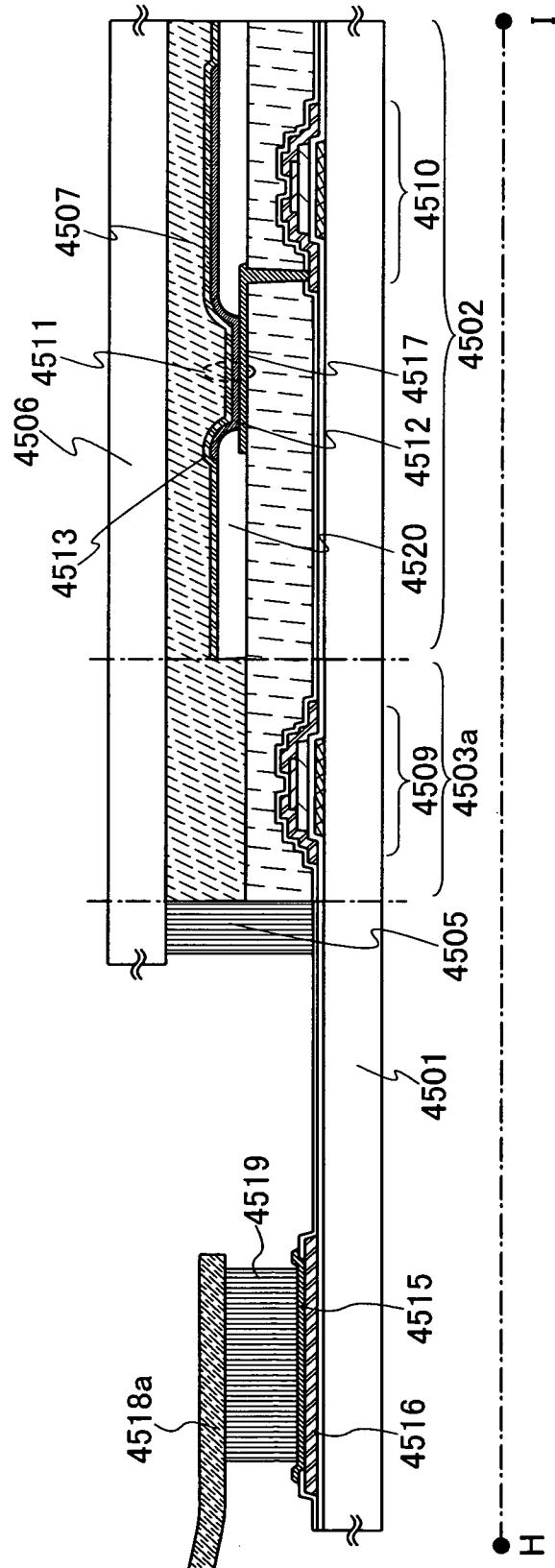


FIG. 16

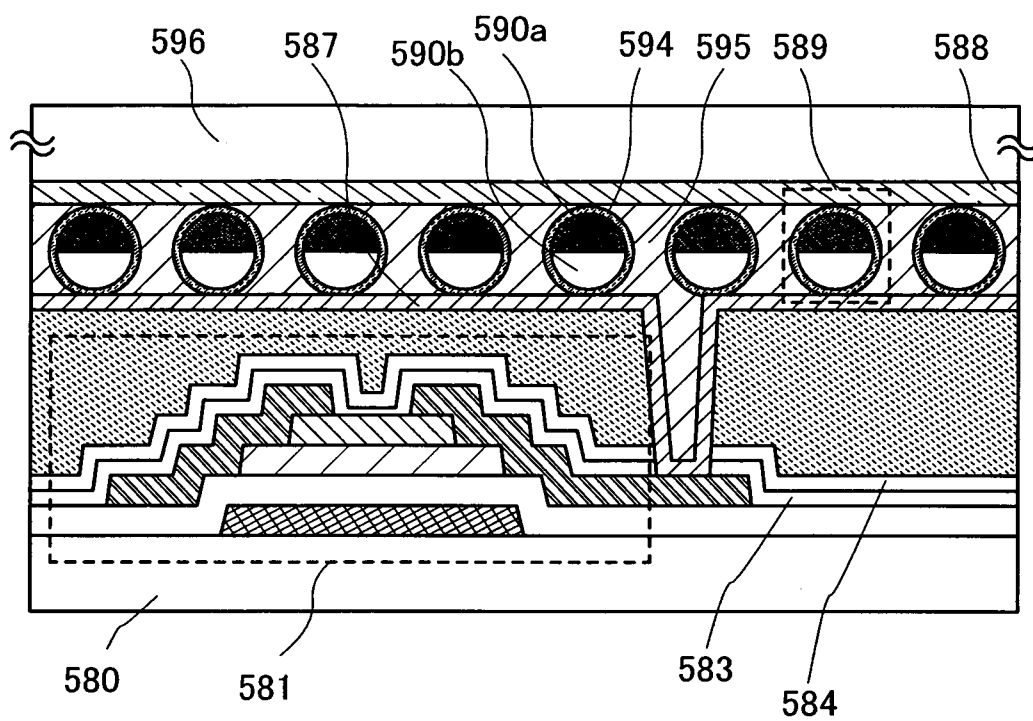


FIG. 17A

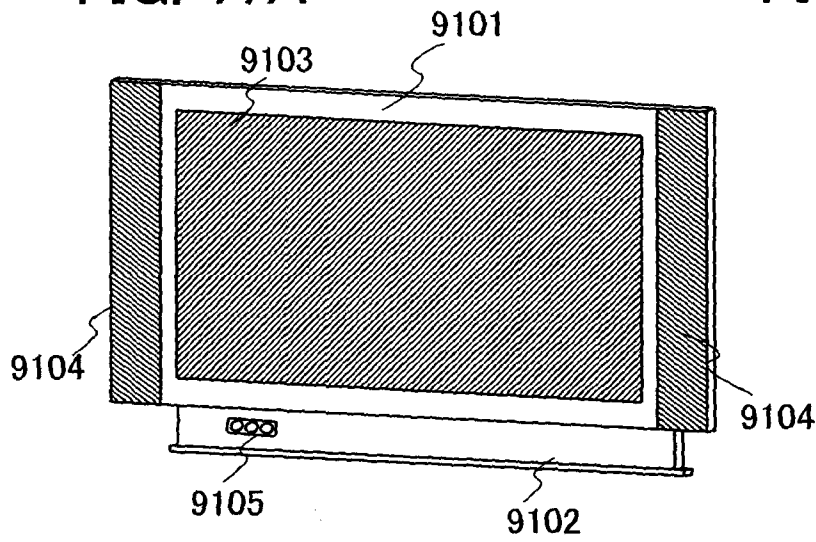


FIG. 17B

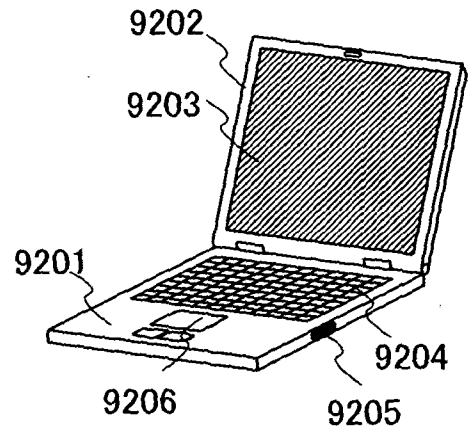


FIG. 17C

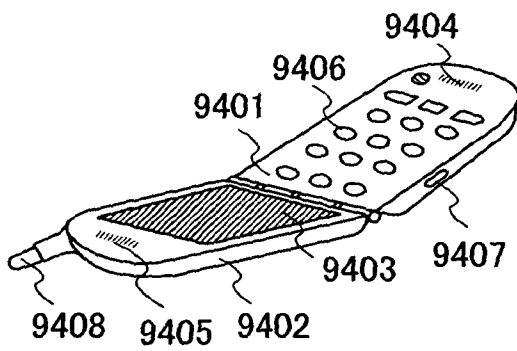


FIG. 17D

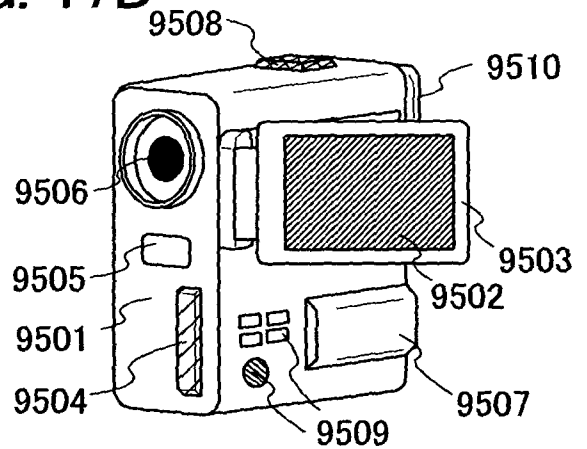


FIG. 17E

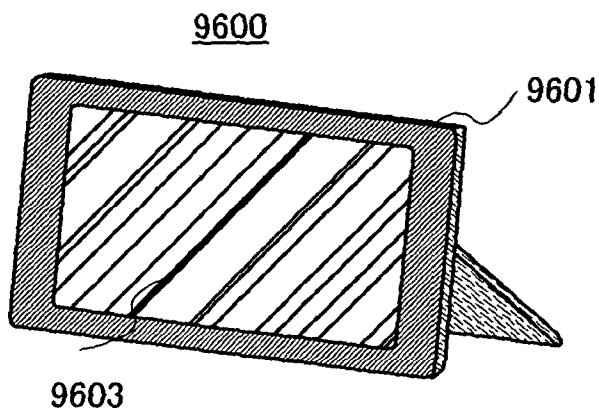
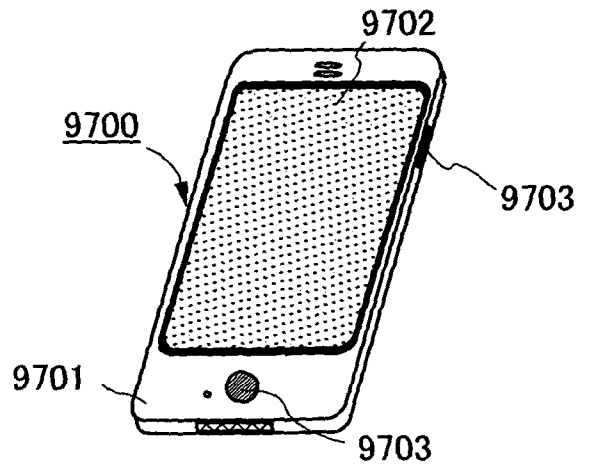


FIG. 17F



EXPLANATION OF REFERENCE

100: substrate, 102: gate electrode layer, 104: gate insulating film, 106: semiconductor film, 108: semiconductor layer, 110: carbide film, 112: carbide layer, 114: conductive film, 115a: low resistance layer, 115b: low resistance layer, 116a: source electrode layer, 116b: drain electrode layer, 117: resist mask, 118: recessed portion, 120: transistor, 121: protective insulating layer, 130: transistor, 131: transistor, 140: transistor, 141: transistor, 150: transistor, 580: substrate, 581: thin film transistor, 583: insulating layer, 587: electrode layer, 588: electrode layer, 589: spherical particle, 594: cavity, 595: filler, 596: substrate, 4001: substrate, 4002: pixel portion, 4003: signal line driver circuit, 4004: scan line driver circuit, 4005: sealant, 4006: substrate, 4008: liquid crystal layer, 4010: thin film transistor, 4011: thin film transistor, 4013: liquid crystal element, 4015: connection terminal electrode, 4016: terminal electrode, 4018: FPC, 4019: anisotropic conductive film, 4020: insulating layer, 4021: insulating layer, 4030: pixel electrode layer, 4031: counter electrode layer, 4032: insulating layer, 4501: substrate, 4502: pixel portion, 4503a: signal line driver circuit, 4504a: scan line driver circuit, 4505: sealant, 4506: substrate, 4507: filler, 4509: thin film transistor, 4510: thin film transistor, 4511: light-emitting element, 4512: electroluminescent layer, 4513: electrode layer, 4515: connection terminal electrode, 4516: terminal electrode, 4517: electrode layer, 4518a: FPC, 4519: anisotropic conductive film, 4520: partition, 590a: black region, 590b: white region, 9101: housing, 9102: supporting base, 9103: display portion, 9104: speaker portion, 9105: video input terminal, 9201: main body, 9202: housing, 9203: display portion, 9204: keyboard, 9205: external connection port, 9206: pointing device, 9401: main body, 9402: housing,

9403: display portion, 9404: audio input portion, 9405: audio output
portion, 9406: operation key, 9407: external connection port, 9408: antenna,
9501: main body, 9502: display portion, 9503: housing, 9504: external
connection port, 9505: remote controller receiving portion, 9506: image
5 receiving portion, 9507: battery, 9508: audio input portion, 9509: operation
key, 9510: eye piece portion, 9600: digital photo frame, 9601: housing,
9603: display portion, 9700: cellular phone, 9701: housing, 9702: display
portion, 9703: operation button

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/063446

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2010
 Registered utility model specifications of Japan 1996-2010
 Published registered utility model applications of Japan 1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 2-27771 A (SUMITOMO METAL INDUSTRIES, LTD.) 1990.01.30, Page 3, left upper column, line 11 to page 5, left upper column, line 16, Figs.1,2 (No Family)	1-5, 17, 18 6-16, 19-22
X Y	US 2009/0076322 A1 (MATSUNAGA et al.) 2009.03.19, Par. Nos. [0089] to [0154] & JP 2009-89351 A	7, 10, 11, 19, 20 1-6, 8, 9, 12-18, 21, 22
X Y	US 2007/0072439 A1 (Akimoto et al.) 2007.03.29, Par. Nos. [0129] to [0167], Figs. 7, 15 & JP 2007-123861 A & EP 1770788 A2 & CN 1941299 A	7-9, 11, 19, 20 1-6, 10, 17, 18



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

06.10.2010

Date of mailing of the international search report

19.10.2010

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

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4M

2934

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/063446

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/0180045 A1 (Yoon et al.) 2009.07.16, Par. No. [0045] & JP 2009-170905 A & KR 10-2009-0078568 A & CN 101487961 A	1-22
Y	WO 2007/058329 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2007.05.24, Par. Nos. [0036] to [0046], [0055] to [0081], Figs. 1 to 4 & JP 2007-165861 A & US 2007/0108446 A1 & KR 10-2008-0070811 A & CN 101283444 A	12-16, 21, 22

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/063446

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Because the subject matter of claim 1 does not appear to be novel with respect to JP 2-27771 A (SUMITOMO METAL INDUSTRIES, LTD.) 1990.01.30, Page 3, left upper column, line 11 to page 5, left upper column, line 16, Fig.1,2 found in search, it would not involve the special technical feature.

Consequently, there would not be a special technical feature common to all the claims.

Therefore, this international patent application is not considered to comply with the requirement of unity of invention.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.