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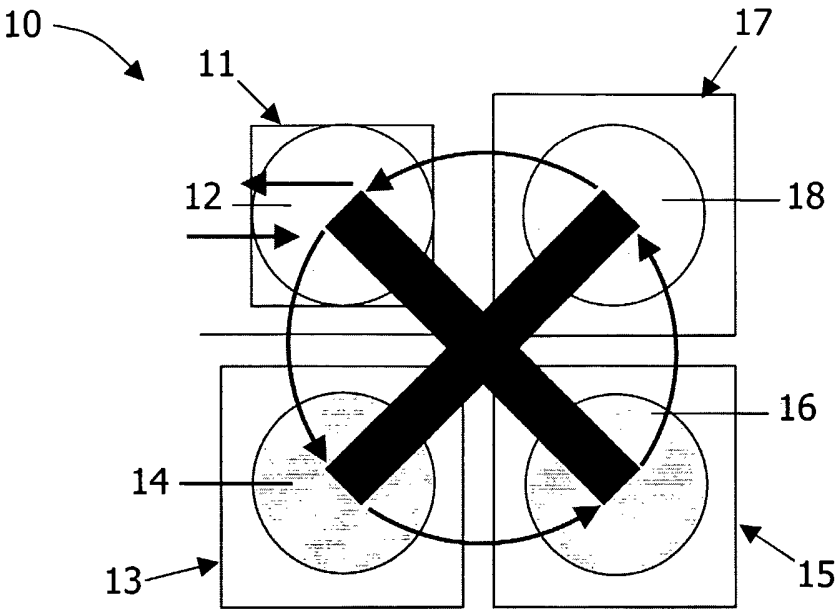
(54) Title: FLEXIBLE RINSING STEP IN A CMP PROCESS



(57) Abstract: The present invention relates to chemical mechanical planarizing (CMP) and to an apparatus for performing such a CMP process. The method and apparatus according to the invention prevent or at least minimize the time during which a wafer is exposed to air in between two subsequent polishing steps during a CMP process by adjusting the time period of the rinsing steps such that each rinsing step ends at substantially the same time. In that way, damage such as corrosion can be avoided or at least minimized and high quality devices can be achieved.

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Flexible rinsing step in a CMP process

The present invention relates to a chemical-mechanical polishing (CMP) tool and process and more particularly to a CMP tool and process in which the exposure of the wafers to air in between subsequent steps of planarization and rinsing is minimized as well as to intermediate semiconductor products or final semiconductor products having been polished by the CMP tool or method.

Chemical-mechanical polishing (CMP) has developed into an important process in the design, development, and processing of e.g. electric or electronic components. CMP technology is essential for the manufacture of cost-effective and leading-edge products. It has become critical to the fabrication of advanced multilevel integrated circuits in the microelectronic industry. The CMP process is commonly used by the semiconductor industry today to polish off high spots on wafers or on films deposited on wafers, in that way flattening the film or wafer to reach required local and/or global planarization of surfaces. This CMP process is therefore often simply referred to as a planarization process.

In the CMP process, both mechanical and chemical forces are utilized to produce a reasonable, required mechanical removal rate of a material, e.g. the wafer or film material, and a precise controllability of the removal rate. The selectivity in removal rate of one material to another is the product of both chemical and mechanical forces. Hence, by tuning these chemical and mechanical forces it is possible to achieve a good selectivity or no selectivity depending on the required application.

The CMP process has been comprehensively described and illustrated by J.M. Steigerwald, S.P. Murarka and R.J. Gutman in 'Chemical Mechanical Planarization of Microelectronic Materials', John Wiley & Sons, New York, 1997. A CMP process comprises moving a sample surface to be planarized or polished against a polishing pad that is used to provide support against the sample surface and to carry slurry between the sample surface and the polishing pad to affect polishing which leads to planarization. The chemical reaction that takes place during CMP modifies the surface properties of the material that is being polished by creating a surface layer, such as e.g. an oxide layer. This surface layer comprises

chemical and mechanical properties that are different from those of the bulk material and often this surface layer can be easily removed by the abrasion of abrasive particles and the polishing pad rubbing against the sample. Chemical force thus serves for two main purposes. Firstly, formation of a surface layer which makes that material can easily be removed and which enables a precise control over the removal rate. Secondly, removal of the abraded materials by dissolving them or by surrounding them with surfactants preventing the abraded materials from being re-deposited onto the sample surface.

Fig. 1 illustrates a schematic representation of a generally known polishing tool. A wafer 1 to be planarized is pressed against a polishing surface 2, also called polishing pad 2, and the wafer 1 and polishing pad 2 are brought into movement, preferably rotational movement, with respect to each other (see Fig. 1). In a preferred embodiment, both the wafer 1 and the polishing pad 2 undergo a rotational movement. A polishing slurry 3, comprising fine abrasive particles suspended in an aqueous medium comprising chemical reagents, is dispensed to a location on the polishing pad 2, e.g. to the center of the polishing pad 2. Centrifugal force generated by the rotational movement and the presence of the wafer 1 very close to the polishing pad 2 distribute the slurry 3 across the polishing pad 2 forming a thin sheet of liquid on the polishing pad 2. Fig. 2 shows in detail a wafer 1 to be polished, the polishing pad 2 and the polishing slurry 3. The combination of mechanical action from the force and velocity applied to the abrasive particles in the slurry 3 and the chemical action from the water and chemical reagents in the slurry 3, results in material removal from the surface of the wafer 1.

For certain applications, a CMP tool may comprise more than one polishing platform, each comprising a polishing pad 2 according to Fig. 1. Hence, the CMP process may comprise more than one polishing step. In between subsequent polishing steps, the wafers are rinsed with deionised (DI) water, which is ultra-pure water used in semiconductor processing, or, more in general, with a cleaning solution. An example of a cleaning solution may be benzotriazole (BTA) with a concentration of between 0.0001 to 0.1 M. During a rinsing step, the polished wafer is immersed in DI water in order to stop chemical reaction initiated during preceding operation and to remove products of this operation from the wafer surface. After a rinsing step, the wafer 1 is lifted up from the polishing platform and moved on to the next polishing platform for a subsequent polishing phase. In a perfectly tuned polishing sequence, the wafer 1 would be directly brought into the successive polishing phase without any waiting moment.

It is, however, a disadvantage of the known systems that rinsing steps in between two subsequent polishing steps have a fixed time duration. Hence, if different polishing steps have different time durations, the wafer that has passed the polishing step with the shortest time duration is immersed in the DI water first, and after the fixed rinsing time duration, it is removed from the DI water and has to wait in air, still being wet, before it can be transferred to a subsequent polishing step, as all wafers are simultaneously moved to a next step. The exposure to air of a wet wafer comprising traces of chemical residues from the slurry, in the highly chemically active environment of a CMP tool, increases the possibility of damage, e.g. corrosion, of the surface of the wafer, which can lead to products and devices which have poor quality.

It is an object of the present invention to provide a CMP tool and a CMP process which minimize the possibility of corrosion or damage of the surface of a substrate such as a semiconductor wafer or a partially processed semiconductor substrate as well as to provide intermediate or final semiconductor products made by the process.

The above objective is accomplished by a method, a device and semiconductor products according to the present invention.

The present invention provides a chemical mechanical planarization apparatus with at least two polishing platforms, each having means for carrying out-processing steps simultaneously, each processing step comprising a polishing step and at least one of said processing steps furthermore comprises a rinsing step after the polishing step. In the method according to the present invention, each processing step has a total processing step time and the apparatus furthermore comprises a control means adapted for setting the total processing step time such that the processing step at each polishing platform ends substantially at the same time. By ending at substantially the same time is meant that the difference between the ending of the processing steps at each polishing platform is not larger than 2 seconds.

According to an embodiment of the present invention, the apparatus may furthermore comprise means for determining the end time of each processing step by the end time of the slowest polishing step and the control means may have means for setting the total processing step time by adjusting the time duration of each of the at least one rinsing step. The apparatus may furthermore also comprise an endpoint detector for determining the end time of the processing steps.

In the apparatus according to the invention, wafers do not have to wait in air before they can be moved to a next polishing platform. Therefore, the chemical mechanical planarization apparatus according to this invention has the advantage that there is no or substantially no wet wafer waiting in the air in between two polishing or polishing + rinsing steps and thus the possibility of damaging, such as e.g. corrosion, can be minimized.

In an embodiment of the invention, each processing step may comprise a polishing step followed by a rinsing step. The control means may be adapted for controlling the duration of each rinsing step so that rinsing is performed during a time period determined by the difference between the end time of the preceding polishing step and the end time of the slowest polishing step, increased with a minimum rinsing time. In one embodiment, the control means may be adapted for controlling the minimum rinsing time to between 1 and 60 seconds, preferably between 8 and 10 seconds.

In the apparatus according to this embodiment of the present invention, an advantage is that no negative effect on the tool throughput occurs. No extra time is added there, which would be the case if for example fixed end times for the rinsing steps were set, as in that case a security margin would have to be built in. Another advantage of this embodiment according to the invention is that polishing and rinsing is performed on the same wafer carrier. In most prior art CMP tools, rinsing may be performed on a different wafer carrier than the wafer carrier where the polishing step is performed. This leads to large tools, which is a disadvantage because it takes up too much space in e.g. a clean room.

In an embodiment according to the invention, the apparatus may comprise a first, a second and a third polishing platform. The first, second and third embodiment may for example be adapted to perform resp. copper CMP, barrier CMP and buffing.

The present invention furthermore provides a method for chemical mechanical planarization of substrates. The method comprises at least two simultaneous processing steps, each processing step comprising a polishing step and at least one of the processing steps furthermore comprises a rinsing step after the polishing step, and wherein all processing steps are controlled so that they end substantially at the same time.

The end time of all processing steps may be determined by the end time of the slowest polishing step and the total processing step time may be set by adjusting the time duration of each of the at least one rinsing step.

In the method according to the invention, wafers do not have to wait in air before they can be moved to a next polishing platform. Therefore, the method for chemical mechanical planarization according to this invention has the advantage that there is no or

substantially no wet wafer waiting in the air in between two polishing or polishing + rinsing steps and thus the possibility of damaging, such as e.g. corrosion, can be minimized.

In one embodiment of the invention, each processing step may comprise a rinsing step after the polishing step and each rinsing step may be performed during a time period determined by the difference between the end time of the preceding polishing step and the end time of the slowest polishing step, increased with a minimum rinsing step.

The method according to this embodiment of the present invention has the advantage that there is no negative effect on the tool throughput. No extra time is added there, which would be the case if for example fixed end times for the rinsing steps were set, as in that case a security margin would have to be built in. Another advantage of this embodiment according to the invention is that polishing and rinsing is performed on the same wafer carrier. In most prior art CMP tools, rinsing may be performed on a different wafer carrier than the wafer carrier where the polishing step is performed. This leads to large tools, which is a disadvantage because it takes up too much space in e.g. a clean room.

In embodiments according to the invention, the substrate may be a semiconductor wafer or a partially processed semiconductor substrate.

The present invention furthermore provides a computer program product for setting a time period for a processing step in a CMP process of a substrate when the computer program product is executed on a processing engine such as a computer, an embedded microprocessor, e.g. in a microcontroller or a programmable gate array such as an FPGA, the computer program containing a code for controlling a process comprising at least two subsequent processing steps, and at least one of the processing steps furthermore comprises a rinsing step after the polishing step, wherein all processing steps end substantially at the same time.

The invention also provides a machine-readable data storage device storing the computer program product according to the invention.

Furthermore, a method of manufacturing an electric or electronic device is provided. The method comprises performing chemical mechanical planarization of a substrate, the chemical mechanical planarization comprises at least two subsequent processing steps, each processing step comprising a polishing step and at least one of the processing steps furthermore comprising a rinsing step after the polishing step, wherein all processing steps end substantially at the same time. The substrate may for example be a semiconductor wafer or a partially processed semiconductor substrate.

The invention furthermore provides a computer system adapted for receiving parameters and sending these parameters to the CMP tool for performing the CMP process according to the present invention.

These and other characteristics, features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention. This description is given for the sake of example only, without limiting the scope of the invention. The reference figures quoted below refer to the attached drawings.

Fig. 1 is a schematic representation of a wafer-polishing tool.

Fig. 2 is a schematic illustration of a wafer-slurry-pad system.

Fig. 3 is a schematic illustration of a CMP tool that may be used for embodiments of the present invention.

Fig. 4A illustrates a wafer that was continuously being processed and did not have to wait in the CMP tool in accordance with an embodiment of the present invention.

Fig. 4B illustrates a wafer that was not continuously being processed and had to wait in the CMP tool during processing.

Fig. 5 illustrates a simplified block diagram of a computer system in which the method of the present invention may be embodied.

In the different Figures, the same reference signs refer to the same or analogous elements.

The present invention will be described with respect to particular embodiments and with reference to certain drawings, but the invention is not limited thereto as it is limited only by the claims. Any reference signs in the claims shall not be construed as limiting the scope. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Where the term “comprising” is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun e.g. "a" or "an", "the", this includes a plural of that noun, unless specifically stated otherwise.

Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

The present invention provides a CMP tool and a CMP process in which the exposure of a substrate to be polished, e.g. semiconductor wafers, to air in between two subsequent steps in the process is avoided or at least minimized. In that way, the substrates such as wafers are less, or even not at all, subject to possible damage such as e.g. corrosion. The substrates may be semiconductor wafers, whether plain or partially processed. This leads to the production of high quality products, such as e.g. electric or electronic devices.

Fig 3 illustrates, as a non-limiting example , a schematic diagram of a CMP tool 10, comprising a load/unload station 11 with a first wafer carrier 12, a first polishing platform 13 with a second wafer carrier 14, a second polishing platform 15 with a third wafer carrier 16 and a third polishing platform 17 with a fourth wafer carrier 18. An example of process allocation to polishing platforms 13, 15, 17 is given hereinafter. It has to be understood that this example is only for the ease of explaining and understanding and is not limiting to the invention.

CMP may, for example, be used during the formation of copper interconnects in the manufacturing process of e.g. electronic devices. Copper CMP (Cu-CMP) is a preferred way of making copper interconnects, as copper cannot be patterned by plasma etching due to the lack of a volatile compound of copper at a relatively low temperature, e.g. below 200°C, which is an essential feature of the plasma etching process. In Cu-CMP, copper metallization for interconnects may, for example, be achieved by combining damascene technique, known by a person skilled in the art, with an appropriate choice of barrier film material like for example tantalum (Ta) or tantalum nitride (TaN).

The damascene process is a way of making metal lines which involves depositing an insulator, e.g. an oxide, etching a trench in the oxide, depositing metal

everywhere and then polishing back with CMP so metal is just left in the trench. This is the opposite of the traditional sequence, which has metal being deposited first, the metal being patterned through etching, and the oxide being deposited to try to fill the gaps between the metal. Damascene processing removes the gap fill problem (getting oxide between the metal lines). It also results in a different distribution of processes used in the fab in that it uses an oxide etch instead of a metal etch, and a metal CMP step instead of an oxide CMP step. Another advantage of the damascene process is that metal lines and vias can be formed in one process cycle, making the process very attractive in terms of electrical performance, reliability of the circuit and product costs.

JP-200144201 describes a damascene structure and its manufacture making use of a barrier film. Use is made of a sacrificial layer that is a modified top part of the dielectric layer and is present under the barrier film. The barrier film acts both as an adhesion promoter between copper and the underlying dielectric and as a diffusion barrier. Excess copper is removed during a first CMP step. The barrier film is removed during a second CMP step. While removing the barrier film, copper is also further removed. After removing the barrier film, the sacrificial film is removed at a higher speed (up to 100 times as high) than the copper. CMP allows the removal of both the excess copper and the barrier film and achieves the required die and wafer-scale planarization.

For the example described hereinabove, the CMP tool 10 may be such that a first wafer can be loaded into the load/unload station 11 and is subsequently moved to the first polishing platform 13, while a second wafer is introduced into the CMP tool 10 through load/unload station 11. On the first polishing platform 13, in the example given, copper CMP may be performed using a slurry such as e.g. EPL2361 obtainable from Rohm and Haas Electronic Materials. Such a copper CMP slurry is used to remove the bulk copper film at a high removal rate. The process should efficiently stop at the barrier film. The process has a high Cu to barrier/oxide selectivity. For a copper layer with a thickness of about 1 μm, for example, the main processing time on this first polishing platform 13 may be between 70 and 90 seconds. The end time of this step may be triggered by an endpoint detector.

Next, the first wafer is moved to the second polishing platform 15, the second wafer is moved to the first polishing platform 13 and a third wafer is introduced into the CMP tool 10 through load/unload station 11. In the second polishing platform 15, for the example given, barrier CMP may be performed using a slurry such as e.g. CUS1351 obtainable from Rohm and Haas Electronic Materials. The function of the barrier CMP process is to remove the barrier film material, such as e.g. Ta or TaN. The slurry used for

barrier film removal has a high selectivity and the process is stopped at the sacrificial layer. The main processing time on this second polishing platform 15 may, for the example given, be between 45 and 60 seconds. The end time may be triggered by an endpoint detector or the main processing time may have a fixed duration.

Subsequently, the first wafer is moved to the third polishing platform 17, the second wafer is moved to the second polishing platform 15, the third wafer is moved to the first polishing platform 13 and a fourth wafer is introduced into the load/unload station 11. On this third polishing platform 17, for the example given, the sacrificial layer may be removed. In alternative semiconductor processing stages, buffing may be performed on this third polishing platform. An example of a slurry that can be used for buffing may for example be Klebosol 1501-50 obtainable from Rohm and Haas Electronic Materials. The buffing step, which is a mechanical cleaning step, functions as a final planarization and defect reduction step. The main processing time on this third polishing platform 17 may, for the example given, be between 10 and 20 seconds and usually has a fixed duration.

Next, the first wafer is moved to the load/unload station 11 to be removed from the CMP tool 10, the second wafer is moved to the third polishing platform 17, the third wafer is moved to the second polishing platform 15, the fourth wafer is moved to the first polishing platform 13 and a fifth wafer is introduced into the CMP tool 10 through the load/unload station 11.

The above-described sequence may be repeated until all wafers to be treated have left the CMP tool 10.

A wafer-rinsing step is performed after each polishing phase. During this rinsing step, wafers are polished gently, i.e. at very low pressure and low speed, using DI water or, more in general, any suitable cleaning solution such as e.g. a solution of Benzotriazole with a concentration of e.g. between 0.0001 and 0.1 M, which is sprayed with high pressure onto the polishing pad. Conventionally, the rinsing step is performed during a fixed time period of a few seconds, typically between 10 and 15 seconds. The purpose of the rinsing step is to remove chemical residues and debris of the previous polishing step from the wafer surface. After the rinsing step, the wafer is lifted up from the polishing pad and moved on to the next polishing platform for a subsequent polishing phase. In a perfectly tuned polishing sequence, the wafer would be directly brought into the next polishing phase without any waiting time . However, in reality, and as described above, the wafer always has to wait for the longest polishing step among all polishing platforms 13, 15, 17 on the CMP tool 10 to finish, because all wafers are mounted on the same wafer transfer mechanism. For the

example given, the wafers on the second polishing platform 15 and on the third polishing platform 17 must wait for further processing on the first polishing platform 13 to end for about between 10 and 45 seconds and between 60 and 80 seconds, respectively, before being moved to the next step. This waiting in air is undesirable and is preferably avoided because, after rinsing, the surface of the wafer is wet and comprises traces of chemical residues coming from the slurry that has been used during the previous polishing step. Waiting in the atmosphere of a highly chemically active environment of a CMP tool 10 is not a desirable option, because this causes damage (corrosion) to, in the example given, the metal features on the wafer. Evidence of metal corrosion as a result of waiting in air during processing has been reported. In Fig. 4A a wafer 19a is illustrated that was continuously processed and hence did not have to wait in the CMP tool 10 during processing. Fig. 4B illustrates a wafer 19b which had to wait in the CMP tool 10 during processing and thus was not continuously processed. It can be seen that the wafer 19a in Fig. 4A comprises brown spots 20 on the wafer edges 21. For the wafer 19b illustrated in Fig. 4B, the waiting time in the CMP tool 10 was more than 1 minute. In that case, the brown spots 20 are visible with the naked eye. For shorter waiting periods, the damage or brown spots 20 can be made visible with a microscope.

The present invention proposes a change to the CMP tool configuration and controlling software, e.g. for eliminating the corrosion issue related to wet wafer waiting for processing in a CMP tool 10. The software contains a code for controlling the process. The software may be executed on any suitable processing engine such as a computer, an embedded microprocessor such as in a microcontroller, or on a digital logic device such as a programmable gate array, e.g. an FPGA. The software may be stored on any suitable storage medium, e.g. diskettes, a hard drive, tape storage, an optical disk, such as a CD-ROM or a DVD-ROM, a solid state memory, etc. According to the present invention, the time period of rinsing between two subsequent polishing steps on each polishing platform 13, 15, 17 no longer has a fixed duration. Instead, the end time of a rinsing step on all polishing platforms 13, 15, 17 must be triggered by the last endpoint signal of all the polishing platforms 13, 15, 17, i.e. by the endpoint signal of the polishing platform 13, 15, 17 on which the polishing step takes the longest time. This endpoint signal may be given after a fixed time period for a polishing platform 13, 15, 17 has elapsed, or after an endpoint detector has detected that an endpoint is reached. The endpoint may be detected by several methods. A preferred method is an optical method which relies on a change of an optical property of the polished surface. Optical measurement can be done in many ways, all of which are included within the scope

of the present invention. For example, a change in a reflective property of the polished surface may be used. In one embodiment of the present invention, the light from a laser source reflected on the wafer surface during polishing through a window embedded in the polishing pad is measured. When a layer of material is removed from the wafer surface, thereby exposing another, different layer/material underneath, the amount of light, that is reflected by the wafer, changes. As a consequence, the endpoint is reached. A second method may be based on a mechanical property of the polished surface. For example, in a further embodiment of the present invention the frictional force between the wafer and the polishing pad is measured or monitored during polishing. When changing from one material to another, the friction force changes. Hence, when a change in friction force is measured, the endpoint is reached. This friction measurement can be done in many ways, all of which are included within the scope of the present invention. In a further embodiment an acoustical method may be used to determine the endpoint. Polishing can generate acoustic energy, which can be monitored. When a layer of material is removed from the wafer surface, thereby exposing another, different layer/material underneath, the acoustic signal will change. This may be used as the endpoint. In a further embodiment an electrical method is used. For example an electrical property of the wafer may be measured. When a layer of material is removed from the wafer surface, thereby exposing another, different layer/material underneath, a change of the electrical property can be used as the endpoint.

However, with such a setting, it could happen that no or very little, i.e. too little, rinsing is performed on one or more of the polishing platforms 13, 15, 17, depending on the difference between the main process time of the different polishing platforms 13, 15, 17. Therefore, it is important that, after the endpoint signal of the slowest polishing platform 13, 15, 17, rinsing on all polishing platforms 13, 15, 17 continues for a limited period of time, which is required to provide decent and sufficient wafer surface cleaning. The extra time period for the rinsing step according to the invention is called minimum rinsing time. The minimum rinsing time may be between 1 and 60 seconds, and typically between 8 and 10 seconds. This minimum rinsing time is required to ensure a proper removal of chemical residues and debris.

In that way, the rinsing step may start at a different first moment in time at each of the different polishing platforms 13, 15, 17 but ends at the same or substantially the same second moment in time, the second moment in time being determined by the polishing platform 13, 15, 17 on which the polishing step takes the longest time. By substantially the same second moment in time is meant that the difference between the ending of the cleaning

or rinsing step at each polishing platform 13, 15, 17 does not exceed 2 seconds. Hence, the rinsing step takes a different time period on at least two, but possibly on each of the plurality of different polishing platforms 13, 15, 17, and, contrary to the prior art CMP tools, no longer has a fixed duration.

To implement the present invention on a CMP tool, a software option may be provided which allows users to set a certain minimum rinsing time in a process recipe. That minimum rinsing time is then added to the time period of the rinsing step when the last endpoint signal of all polishing platforms 13, 15, 17 is triggered, i.e. the actual rinsing time period is defined by the slowest polishing process in any of the polishing platforms 13, 15, 17 of the CMP tool 10. In that way wafers on all polishing platforms 13, 15, 17 may be lifted off at the same time or substantially the same time and may immediately be transferred to the next polishing step without waiting in the atmosphere.

The CMP tool 10 may be connected to a computer system 25. Through the computer system 25 parameters for the CMP process such as e.g. rotation speed of the platforms 13, 15, 17, pressure on the platforms 13, 15, 17, time duration for each processing step, etc., may be set. Optionally, in between the CMP tool 10 and the computer system 25, an amplifying element may be positioned to amplify the signal that is sent from the computer system 25 to the CMP tool 10.

Fig. 5 is a simplified block diagram of a computer system 25, in which the method of the present invention may be embodied. A computer system such as system 25, suitably programmed to embody the method of the present invention, is part of the invention.

A computer system 25 includes a processor 26 that may communicate with a number of peripheral devices via a bus subsystem 27. The processor 26 may for example be a microprocessor. The processor 26 may also be a programmable gate array such as a programmable logic array (PLA) or a programmable array logic (PAL) or a field programmable gate array (FPGA) or the like . The peripheral devices may include a memory subsystem 28, a user input facility 29 (for inputting parameters for example) and a file storage system 30. Depending on the implementation (the computer system 25 may be a desktop system, a portable system or an embedded controller), the computer system 25 may also comprise a display subsystem 31, and output devices such as e.g. a printer 32.

The term "bus system" is used generically so as to include any mechanism for allowing the various components of the system to digitally communicate with each other as intended. The different components of the computer system 25 need not be at the same

physical location. Portions of the computer system 25 could be connected via various network media, including wireless transmission media.

Memory subsystem 28 includes at least one memory, for example a number of memories including a main random access memory ("RAM") 33 and a read only memory ("ROM") 34 in which executable computer program instructions are stored. In some embodiments, a DMA controller 35 may be included, which enables transfer from or to memory without going through processor 26.

User input facility 29 typically includes a user interface adapter 36 for connecting a keyboard 37 and/or a pointing device 38 to bus subsystem 27. The pointing device 38 may be an indirect pointing device such as a mouse, trackball, touchpad or graphics tablet, or a direct pointing device such as a touch screen device incorporated into a display device 39.

Display subsystem 31 typically includes a display controller 40 for connecting a display device 39 to the bus subsystem 27. The display device 39 may be a cathode ray tube ("CRT"), a flat-panel device such as a liquid crystal display ("LCD") or a gas plasma-based flat-panel display, or a projection device, or the like . The display controller 40 provides control signals to the display device 39 and normally includes a display memory 41 for storing the pixels that appear on the display device 39.

The file storage system 30 provides persistent (non-volatile) storage for program and data files, and includes an I/O adapter 42 for connecting peripheral devices, such as disk and tape drives, to the bus subsystem 27. The peripheral devices typically include at least one hard disk drive 43 and at least one floppy disk drive ("diskette") 44. The hard disk drive 43 may include a cache memory subsystem 45, which includes a fast memory to speed up transfers to and from the disk drive. There may also be other devices such as a CD-ROM drive 46 and optical drives. Additionally, the system 25 may include hard disk drives of the type comprising removable media cartridges. The computer system 25 may be connectable to a wide area network such as the Internet by a suitable communications adapter and modem.

Those skilled in the art will appreciate that the hardware depicted in Fig. 5 may vary, depending on the implementation.

Software stored e.g. in the memory subsystem of the computer system 25, or on a diskette, a hard drive, a tape storage, an optical disk, such as a CD-ROM or a DVD-ROM, may be executed on the processor 26 of the computer system 25. Either a user has to set certain process parameters such as timing and speed parameters, e.g. by inputting these

parameters via a keyboard 37, or those parameters have to be fetched from a memory. These parameters are then used by the controller to control the driving of the CMP tool when carrying out the CMP process according to the present invention, i.e. these parameters are used for controlling how long and at what rotational speed and pressure each of the CMP platforms 13, 15, 17 is driven. The parameters are such that each platform has the same processing time, with processing time comprising polishing time and, optionally for each platform, rinsing time.

The present invention thus proposes a flexible rinsing time period in between two subsequent polishing steps during CMP processes. The invention has been described for a CMP process used during the formation of copper interconnects when manufacturing e.g. electronic devices, but it has to be understood that the CMP process and tool according to the invention can also be applied to other CMP processes used in other manufacturing processes. Furthermore, the CMP tool 10 that has been described comprises three polishing platforms 13, 15, 17. However, for other applications, the CMP tool 10 may alternatively comprise a different number of polishing platforms.

In the above-described embodiment, each processing step on each polishing platform 13, 15, 17 comprises a polishing step and a rinsing step. It is to be understood, however, that the above-described embodiment is not limiting to the invention. The CMP process may, according to other embodiments of the invention, for example, comprise at least two processing steps, simultaneously performed at different polishing platforms 13, 15, 17. Each processing step comprises a polishing step and at least one of the processing steps may furthermore comprise a rinsing step. For example, in a CMP process, a first processing step may comprise a polishing step having a first time duration and a rinsing step. A second processing step may only comprise a polishing step having a second time duration. According to the invention, the second time duration may be longer than the first time duration. The total processing time duration of the first processing step may then be adapted such that both the first and the second processing step end at substantially the same time. By ending at substantially the same time is meant that the difference between the end time of the first processing step and the end time of the second processing step is not longer than 2 seconds. Adaptation of the total processing time duration of the first processing step is performed by adjusting the time duration of the rinsing step, as the polishing time for a particular CMP process has a fixed time duration. In that way, a first wafer undergoing the first processing step will not have to wait for a second wafer that is undergoing the second processing step. Similarly, in CMP processes comprising more than two simultaneous

process steps, the time duration period of the different processing steps may be set such that all processing steps at different polishing platforms 13, 15, 17 end at substantially the same time and hence none of the wafers has to wait in air before being transferred to a next polishing platform 13, 15, 17.

The method and apparatus according to the present invention show two important advantages. First, there is no or substantially no wet wafer waiting in air in between two polishing steps and thus the risk of damage, such as e.g. corrosion, can be minimized. A second advantage is that no negative effect on tool throughput occurs, as after the latest, finished CMP stage the treated wafer just goes through a rinsing step during the minimum rinsing time. No extra time is added there, which would be the case if for example fixed end times for the rinsing steps would be set, as in that case a security margin would have to be built in. Another advantage of the invention is that polishing and rinsing is performed on the same wafer carrier. In most prior art CMP tools, rinsing may be performed on a different wafer carrier than the wafer carrier on which the polishing step is performed. This leads to large tools, which is a disadvantage because it takes up too much place in e.g. a clean room.

It is to be understood that although preferred embodiments, specific constructions and configurations, as well as materials, have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope and spirit of this invention.

CLAIMS:

1. A chemical mechanical planarization apparatus (10) with at least two polishing platforms (13, 15, 17), each having means for carrying out processing steps simultaneously, each processing step comprising a polishing step and at least one of said processing steps furthermore comprising a rinsing step after said polishing step, each processing step having a total processing step time, and the apparatus (10) furthermore comprises a control means adapted for setting the total processing step time such that the processing step at each polishing platform (13, 15, 17) ends substantially at the same time.

2. An apparatus (10) according to claim 1, further comprising means for determining the end time of each processing step by the end time of the slowest polishing step, and wherein the control means has means for setting the total processing step time by adjusting the time duration of each of the at least one rinsing steps.

3. An apparatus (10) according to claim 2, furthermore comprising an endpoint detector for determining the end time of the processing steps.

4. An apparatus (10) according to claim 1, each processing step comprising a polishing step followed by a rinsing step, and wherein the control means is adapted for controlling the duration of each rinsing step so that rinsing is performed during a time period determined by the difference between the end time of the preceding polishing step and the end time of the slowest polishing step, increased with a minimum rinsing time.

5. An apparatus according to claim 4, wherein the control means is adapted for controlling said minimum rinsing time to between 1 and 60 seconds.

6. An apparatus according to claim 5, wherein the control means is adapted for controlling said minimum rinsing time to between 8 and 10 seconds.

7. An apparatus (10) according to claim 1, wherein the apparatus (10) comprises a first, a second and a third polishing platform (13, 15, 17).

8. An apparatus (10) according to claim 7, wherein said first, second and third polishing platforms (13, 15, 17) are adapted to perform, respectively, copper CMP, barrier CMP and buffing.

9. A method for chemical mechanical planarization of substrates, the method comprising at least two simultaneous processing steps, each processing step comprising a polishing step and at least one of said processing steps furthermore comprising a rinsing step after said polishing step,
and wherein all processing steps are controlled so that they end substantially at the same time.

10. A method according to claim 9, wherein the end time of all processing steps is determined by the end time of the slowest polishing step and wherein the total processing step time is set by adjusting the time duration of each of the at least one rinsing steps.

11. A method according to claim 9, wherein each processing step comprises a rinsing step after said polishing step and wherein each rinsing step is performed during a time period determined by the difference between the end time of the preceding polishing step and the end time of the slowest polishing step, increased with a minimum rinsing time.

12. The method of any of the claims 9 to 11, wherein the substrate is a semiconductor wafer or a partially processed semiconductor substrate.

13. A computer program product for setting a time period for a processing step in a CMP process of a substrate when the computer program product is executed on a processing engine, the computer program containing a code for controlling a process comprising at least two simultaneous processing steps, each processing step comprising a polishing step and at least one of said processing steps furthermore comprising a rinsing step after said polishing step, wherein all processing steps end substantially at the same time.

14. A machine-readable data storage device storing the computer program product according to claim 13.

15. A method of manufacturing an electric or electronic device, the method comprising chemical mechanical planarization of a substrate, the chemical mechanical planarization comprising at least two simultaneous processing steps, each processing step comprising a polishing step and at least one of said processing steps furthermore comprising a rinsing step after said polishing step, wherein all processing steps are controlled such that they end substantially at the same time.

16. The method of claim 15, wherein the substrate is a semiconductor wafer or a partially processed semiconductor substrate.

17. A computer system (25) comprising an input means for receiving parameters and sending said parameters to a CMP tool for performing the method according to any of claims 9 to 12.

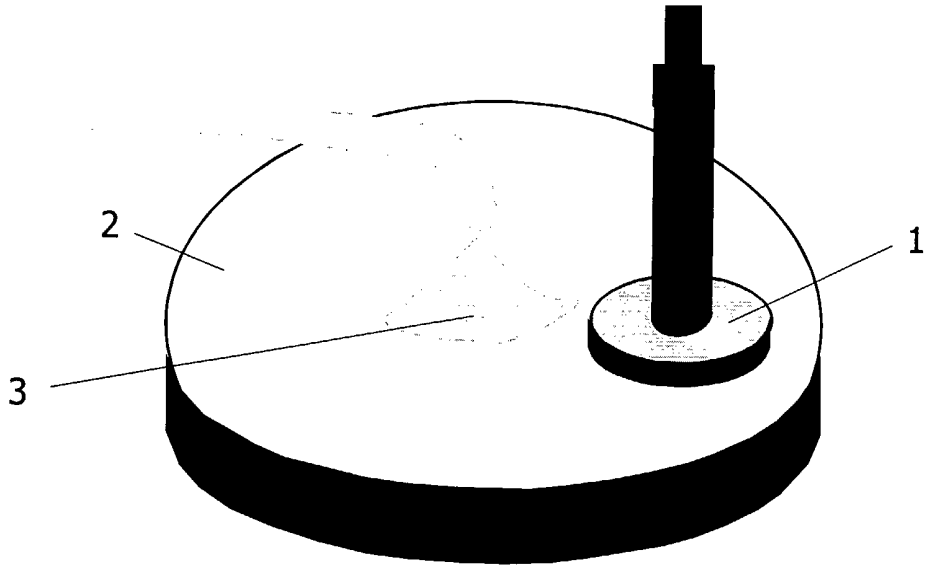

FIG.1

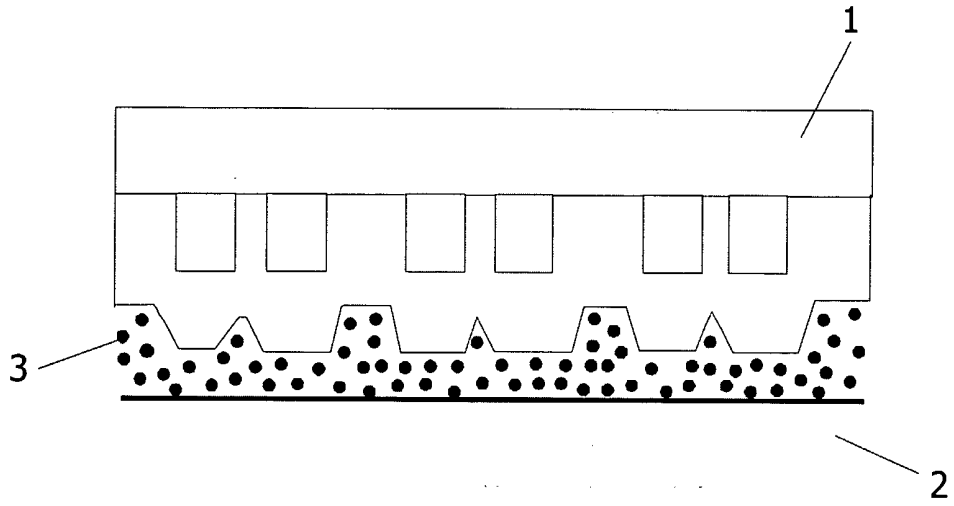

FIG.2

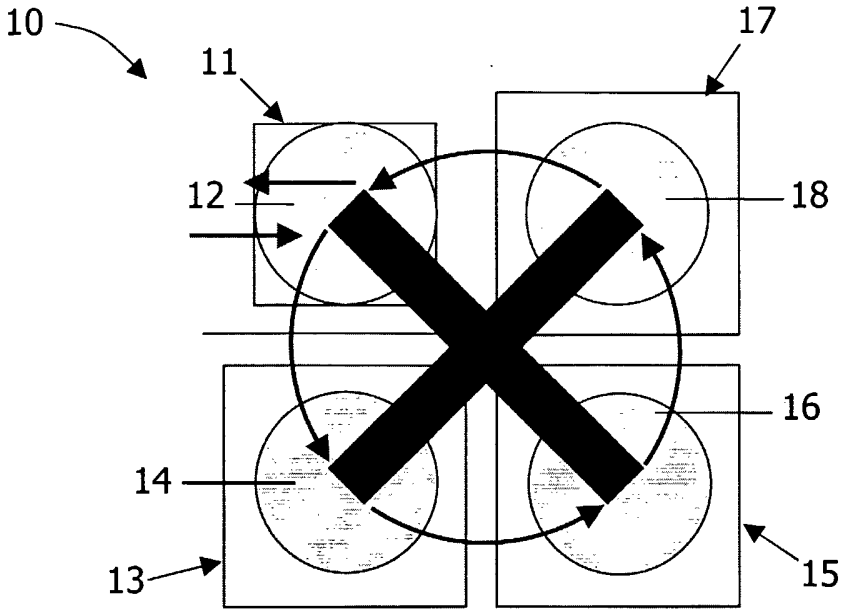

FIG.3

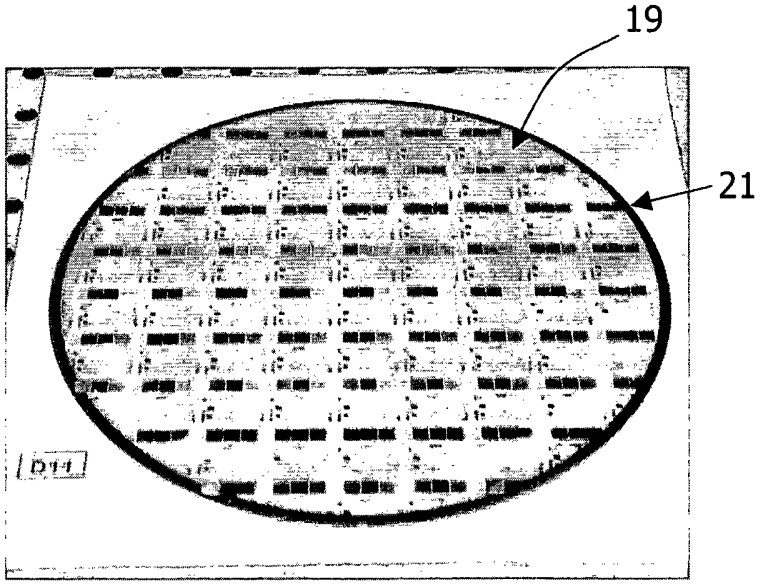

FIG.4A

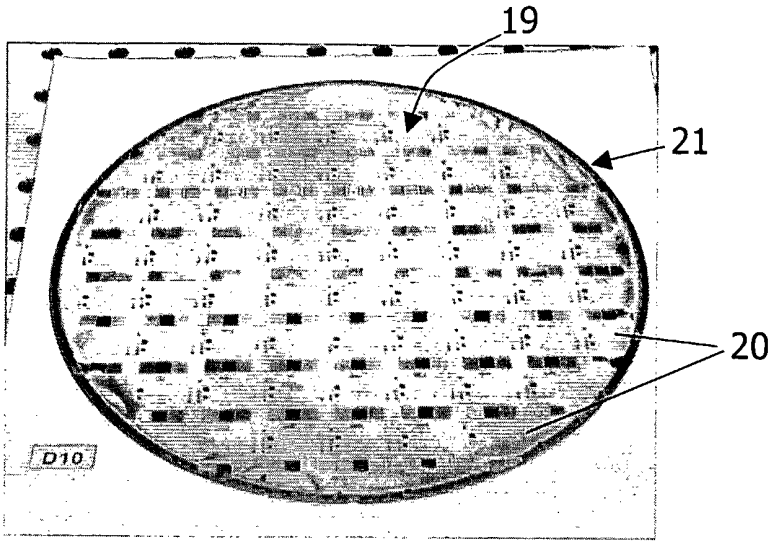
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FIG.4B

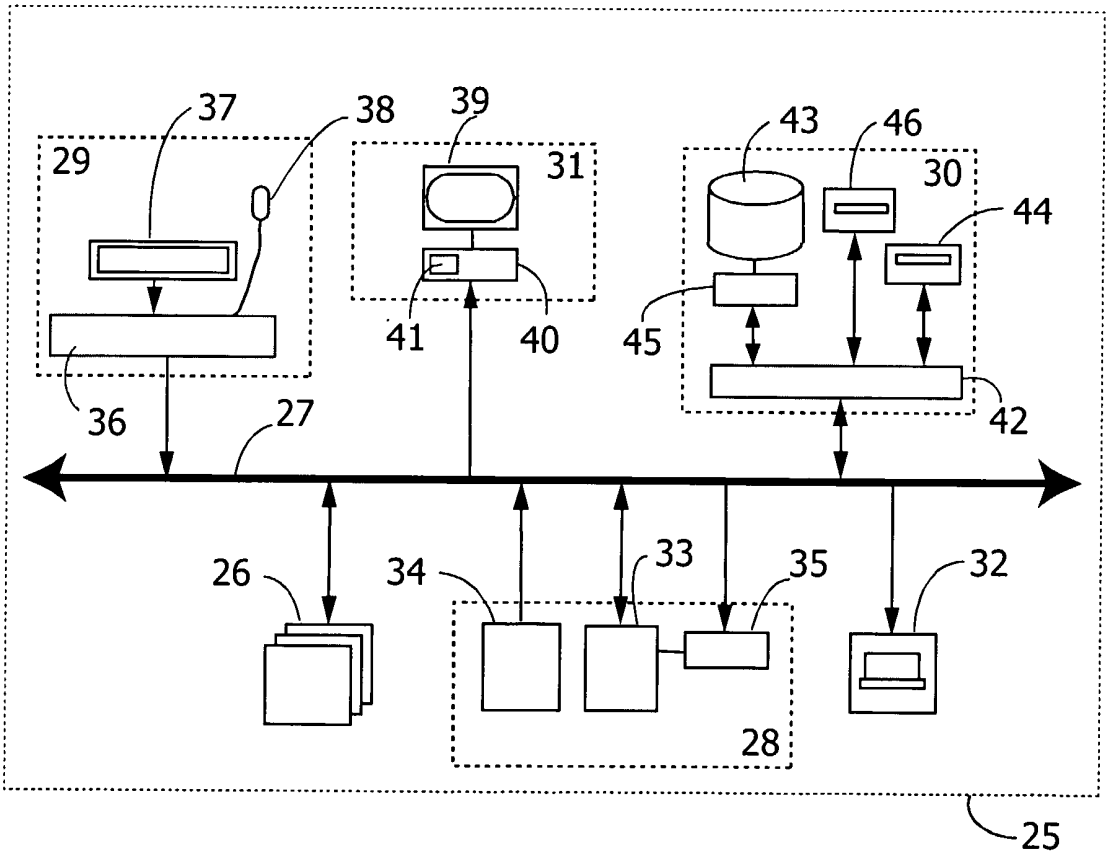
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FIG.5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/053043

A. CLASSIFICATION OF SUBJECT MATTER
B24B37/04 B24B49/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B24B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 126 517 A (TOLLES ET AL) 3 October 2000 (2000-10-03) the whole document	1-12, 14-17
X	WO 01/64395 A (SPEEDFAM-IPEC CORPORATION) 7 September 2001 (2001-09-07) page 5, line 30 - page 11, line 19; claim 18; figures 1-4	14,17
A	US 6 293 845 B1 (CLARK-PHELPS ROBERT B) 25 September 2001 (2001-09-25)	
A	US 2002/055192 A1 (REDEKER FRED C ET AL) 9 May 2002 (2002-05-09)	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 January 2006	17/01/2006

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Koller, S

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2005/053043

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [X] Claims Nos.: 13
because they relate to subject matter not required to be searched by this Authority, namely:

Art.52(2)c) and Guidelines C-IV,2.3.6

2. [ ] Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. [ ] As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB2005/053043

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