

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
9 December 2004 (09.12.2004)

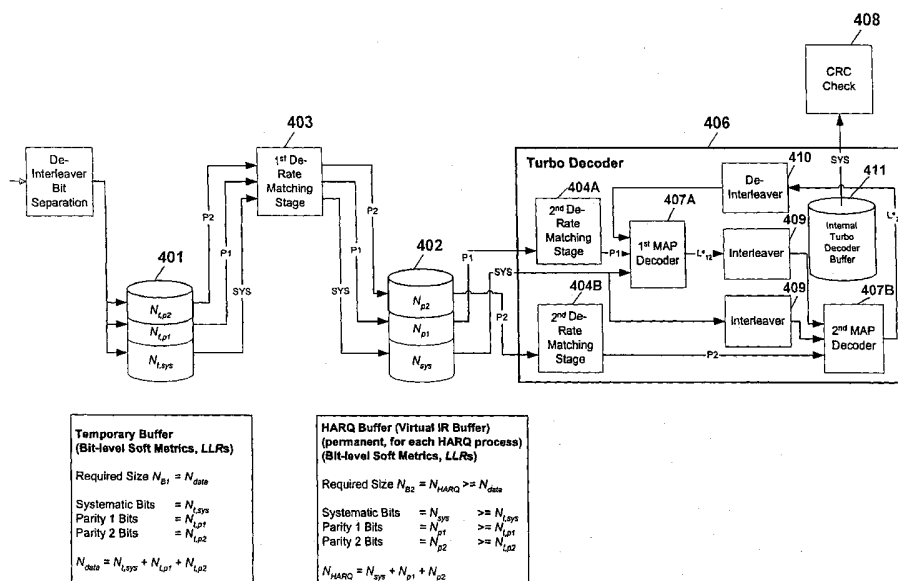
PCT

(10) International Publication Number
WO 2004/107641 A1

- (51) International Patent Classification⁷: **H04L 1/18**, 1/00
- (21) International Application Number:
PCT/EP2004/002463
- (22) International Filing Date: 10 March 2004 (10.03.2004)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
03012445.7 30 May 2003 (30.05.2003) EP
- (71) Applicant (for all designated States except US): **MAT-SUSHITA ELECTRIC INDUSTRIAL CO., LTD.** [JP/JP]; 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 (JP).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **WENGERTER, Christian** [DE/DE]; Bahnhofstr. 10d, 63924 Kleinheubach (DE). **SUZUKI, Hidetoshi** [JP/JP]; 6-2-803, Hikarinooka, Yokosuka-shi, Kanagawa 239-0847 (JP).
- (74) Agent: **KUHL, Dietmar**; Grünecker, Kinkeldey, Stockmair & Schwanhäusser, Maximilianstrasse 58, 80538 München (DE).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: A METHOD AND RECEIVER FOR BUFFERING DATA EMPLOYING HARQ AND TWO-STAGE RATE MATCHING ALGORITHM WITH ITERATIVE DECODING



(57) Abstract: A method and receiver for buffering data at the receiver of a packet transmission communication system employing hybrid ARQ types II/III and adaptive coding and modulation schemes, wherein the adaptive coding is performed by a two-stage rate matching algorithm. The idea underlying the invention is to jointly perform the second de-rate matching and the iterative decoding operation. As a result, the buffer conventionally needed upon completion of the second de-rate matching operation can be completely omitted, since the de-rate matching operation is included in the iterative decoding process.



Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A METHOD AND RECEIVER FOR BUFFERING DATA EMPLOYING HARQ AND TWO-STAGE RATE MATCHING ALGORITHM WITH ITERATIVE DECODING

This invention relates to packet transmission communication systems employing link adaptation by hybrid Automatic Repeat reQuest (ARQ) and Adaptive Modulation and Coding (AMC) techniques. A particular application is High Speed Downlink Packet Access (HSDPA) within the 3GPP standard.

A common technique for error detection and correction in packet transmission systems over unreliable channels is called hybrid ARQ, which is a combination of Forward Error Correction (FEC) and ARQ as described for example in S. Lin, D.J. Costello, M.J. Miller, "Automatic-repeat-request error-control schemes," *IEEE Commun. Mag.*, vol. 22, no. 12, pp. 5-17, December 1984.

If an FEC encoded packet is transmitted and the receiver fails to decode the packet correctly (errors are usually checked by a CRC (Cyclic Redundancy Check)), the receiver requests a retransmission of the packet. Generally (and throughout this document), the transmission of additional information is called "retransmission (of a packet)", although this retransmission does not necessarily mean a transmission of the same encoded information, but could also mean the transmission of any information belonging to the packet (e.g. additional redundancy information).

Depending on the information (generally code-bits/symbols), of which the transmission is composed of, and depending on how the receiver processes the information, the following hybrid ARQ schemes are defined:

Type I: If the receiver fails to decode a packet correctly, the information of the encoded packet is discarded and a retransmission is requested. This implies that all transmissions are decoded separately. Generally, retransmissions contain identical information (code-bits/symbols) to the initial transmission.

Type II: If the receiver fails to decode a packet correctly, a retransmission is requested, where the receiver stores the information of the (erroneous received)

encoded packet as soft information (soft-bits/symbols). This implies that a soft-buffer is required at the receiver. Retransmissions can be composed out of identical, partly identical or non-identical information (code-bits/symbols) according to the same packet as earlier transmissions. When receiving a retransmission the receiver combines the stored information from the soft-buffer and the currently received information and tries to decode the packet based on the combined information. The receiver can also try to decode the transmission individually, however generally performance increases when combining transmissions.

The combining of transmissions refers to so-called soft-combining, where multiple received code-bits/symbols are likelihood combined and solely received code-bits/symbols are code combined (see e.g. D. Chase, "Code combining: A maximum-likelihood decoding approach for combining an arbitrary number of noisy packets," *IEEE Trans. Commun.*, vol. 33, no. 4, pp. 385-393, May 1985 or B.A. Harvey and S. Wicker, "Packet Combining Systems based on the Viterbi Decoder," *IEEE Trans. Commun.*, vol. 42, no. 2/3/4, pp. 1544-1557, April 1994. Common methods for soft-combining are Maximum Ratio Combining (MRC) of received modulation symbols and log-likelihood-ratio (LLR) combining (LLR combining only works for code-bits).

Type II schemes are more sophisticated than Type I schemes, since the probability for correct reception of a packet increases with the number of received retransmissions. This increase comes at the cost of a required hybrid ARQ soft-buffer at the receiver. This scheme can be used to perform dynamic link adaptation by controlling the amount of information to be retransmitted. E.g. if the receiver detects that decoding has been "almost" successful, it can request only a small piece of information for the next retransmission (smaller number of code-bits/symbols than in previous transmission) to be transmitted. In this case it might happen that it is even theoretically not possible to decode the packet correctly by only considering this retransmission by itself (non-self-decodable retransmissions).

Type III: This is a subset of Type II with the restriction that each transmission must be self-decodable.

This invention is related to Type II and Type III schemes, where the received transmissions are soft-combined.

Adaptive Modulation and Coding (AMC) is a link adaptation technique as known for example from R. Love et al, *High speed downlink packet access performance*, Proc. IEEE VTC 2001-Spring, vol. 3, pp. 2234–2238, May 2001. The principle of AMC is to change the modulation and/or coding format in accordance with variations in the channel conditions. The channel conditions can be estimated e.g. based on feedback from the receiver. In a system with AMC, users in favorable positions e.g. users close to the cell site are typically assigned higher order modulation with higher code rates (e.g. 16-QAM with code rate $\frac{3}{4}$), while users in unfavorable positions e.g. users close to the cell boundary, are assigned lower order modulation with lower code rates (e.g. 16-QAM with code rate $\frac{1}{2}$). In the following the different combinations of coding rates and modulation schemes will be referred to as Modulation Coding Scheme (MCS) levels. A transmission will be split into Transmission Time Intervals (TTI), where the MCS level could change each TTI. In HSDPA the TTI interval is equal to 2 ms. The main benefits of AMC include that firstly higher data rates are available for users in favorable positions which in turn increases the average throughput of the cell and secondly a reduced interference variation due to link adaptation based on MCS selection instead of controlling the transmit power.

High Speed Downlink Packet Access (HSDPA) is a new technique that is standardized from Release 5 within the 3GPP standardization body. It shall provide higher data rates in the downlink by introducing enhancements to earlier releases. Among other enhancements HSDPA employs the link adaptation techniques Adaptive Modulation and Coding (AMC) and hybrid ARQ Type II/III. This functionality is implemented by a two-stage rate matching requiring a hybrid ARQ (co-called "virtual IR buffer") soft buffer in the receiver. The two-stage rate matching comprises two consecutive puncturing (rate matching) entities at the transmitter and accordingly two consecutive de-puncturing (de-rate matching) entities at the receiver.

A detailed description of the respective AMC and hybrid ARQ functionality in HSDPA is given in the 3GPP specifications TS 25.212 v. 5.3.0, December 2002 for the Frequency

Division Duplex (FDD) mode and in TS 25.222 v. 5.3.0, December 2002 for Time Division Duplex (TDD) mode.

The following description focuses on the HSDPA FDD mode. However, without loss of generality the same principle applies to the HSDPA TDD mode or any other system including uplink transmission employing a two-stage rate matching (puncturing approach).

The transmitter implementation is described in the following with reference to figure 1 (see also 3GPP, *Technical specification 25.212; Multiplexing and channel coding (FDD)*, v. 5.3.0, December 2002, chapter 4.5.4)

The N_{TTI} code bits from the Turbo encoder (see for more details, C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo-codes," *Proc. ICC '93*, Geneva, Switzerland, pp. 1064-1070, May 1993) are separated in a bit separation unit 101 into three streams containing the systematic bit stream (SYS) and two parity bit streams (P1, P2) generated by the Turbo encoder before input to the 1st stage 102 of the rate matching. The 1st rate matching stage 102 then matches the number of input bits to the size of the virtual IR buffer 103 (N_{HARQ} bits), which is defined by higher layers and is related to the buffer size available for the respective hybrid ARQ process in the receiver (mobile station). The number of bits the virtual IR buffer at the transmitter can store matches the number of bits the virtual IR buffer at the receiver can store. Note, that the absolute buffer sizes at transmitter and receiver are different. The transmitter stores hard-valued bits [0,1], which require one memory bit per code bit. The receiver stores soft-bits, for which usually 6-8 memory bits per code bit are used (implementation dependent). A soft-bit is a metric representing the probability of a received/demodulated bit being a one or a zero. Typically, log-likelihood-ratios (LLRs) are used for the soft-bit representation, however other metrics are also possible. Note that only the parity bits P1 and P2 are rate matched and the 1st rate matching is transparent for the systematic bits.

The 2nd rate matching stage 104 matches the number of bits after 1st rate matching stage 102 i.e. the number of bits of the virtual IR buffer 103 to the number of physical channel bits N_{data} available in the TTI and output from bit collection unit 105. This is necessary

since AMC is employed and N_{data} can vary from transmission to transmission depending on the current channel quality for the respective link.

A conventional HSDPA receiver implementation is described in the following in greater detail with reference to Figure 2 including several details regarding the SYS, P1 and P2 bit streams. In the receiver chain several buffers are required to perform appropriate processing of the received data, which is typically processed bit-wise using soft-bits.

The output of the de-interleaver is stored in a temporary buffer 201 using a bit separation unit in order to identify the systematic SYS, parity P1 and parity P2 bit streams. Buffer 201 needs to be capable of storing at least N_{data} soft-bits. Then the 1st de-rate matching is performed and the soft bits output from the de-rate matching stage 201 are combined with the content of buffer 202, which is the virtual IR buffer (HARQ buffer). Note that combining is only necessary if a retransmission is received. As shown in the figure, a depuncturing (and combining) of a currently received block of size N_{data} to HARQ process block of size N_{HARQ} is performed. Each stream (SYS, P1, P2) is depunctured ("de-rate matched") individually.

The virtual IR buffer 202 holds N_{HARQ} soft-bits from earlier failed transmissions for hybrid ARQ combining. It will be flushed when the receiver decoded a packet correctly or the transmission of the previous packet has been aborted by any reason. In case of soft-bits, flushing is usually done setting the soft-bit values representing equal probability of zero and one. If dealing with LLRs this means setting the soft-bit values to zero. Thereafter, the 2nd de-rate matching is carried out in the 2nd de-rate matching stage to generate N_{TTI} soft-bits for appropriate feeding of the Turbo decoder. These N_{TTI} soft-bits are stored in a temporary buffer 203.

In the second de-rate matching an HARQ block of size N_{HARQ} is depunctured to a full code block (rate 1/3) for straight Turbo decoding. Only bit streams P1 and P2 are depunctured whereas the de-rate matching stage is transparent to the SYS bits.

In contrast to buffer 201 and buffer 203, buffer 202 is not temporary and will be present as long as the hybrid ARQ process runs, since it needs to keep the soft-bits for combining with further retransmissions of a packet. Note, that several hybrid ARQ

processes can run in parallel and the virtual IR buffer for each process can be configured differently.

Moreover, there might be a higher layer procedure which resets the hybrid ARQ processes.

Note that the drawings of the buffers 201-203 in the figure show logical buffer units and do not necessarily refer to the physical assignment/segmentation of the buffers in the receiver structure. A supervising buffer management unit in the receiver could be present to make efficient use of the overall available receiver buffer, bearing in mind that the buffer could be shared among a number of parallel hybrid ARQ processes.

Figure 3 reveals some details of the turbo decoder shown in figure 2. The third buffer is indicated with 303 and corresponds to the buffer 203 in figure 2. The turbo decoder 306 comprises a first and second MAP decoder 307A, 307B, two interleaver units 309 and a de-interleaver unit 310. Further, an internal turbo decoder buffer 311 is provided, which outputs the soft bits to the CRC check unit 308.

The operation of the decoder is as follows. The decoder initially receives the stored soft bits of the data stream P1 at the first MAP decoder 307A. In addition, the systematic bits SYS are also fed into this decoder and through interleaver 309 in the second MAP decoder 307B. The two decoders could physically be the same processing block. The output Le_{12} of the first MAP decoder is applied through interleaver 309 to the second MAP decoder 307B. As its third input, this decoder receives the parity bits of data stream P2 from buffer 303. The output Le_{21} of the second MAP decoder 307B is applied to the de-interleaver 310 and fed back to the input of the first MAP decoder 307A.

The decoder works with a plurality of iterations, thereby improving the performance of the decoder until reliable data bits are obtained, which are stored in the internal turbo decoder buffer 311. The result is then checked by the CRC check unit 308 for correctness.

It is noted that during each iteration the turbo decoder 306 accesses the momentarily stored data bits from the buffer 303 which stores the result of the output from the second de-rate matching stage.

As an implementation variant the turbo decoder accesses the systematic bits from buffer 303 only at the first iteration step (during iterations the information of the systematic bits is stored jointly with L^e_{12}/L^e_{21}).

The complexity of network units of a communication system has a major impact on the cost of the units. This is especially true for the mobile station, because of its compact size and limited battery lifetime. The complexity is, aside from the processing capability, predominantly defined by the required buffer sizes, especially on the downlink, where the mobile station acts as a receiver as in HSDPA and buffers soft-bits for hybrid ARQ.

Therefore, a reduction of the required buffer size is desirable.

The object is solved by a method of buffering data at the receiver of a packet transmission communication system as set forth in claims 1 and 8.

The idea underlying the invention is to jointly perform the second de-rate matching and the iterative decoding operation. As a result, the buffer conventionally needed upon completion of the second de-rate matching operation can be completely omitted, since the de-rate matching operation is included in the iterative decoding process.

Note, that the invention can be applied to various implementation variants of the iterative (turbo) decoder.

Preferred embodiments of the method and receiver are subject to various dependent claims. According to a preferred embodiment, only the parity bit streams need to be de-rate matched at this stage and the systematic bits can be directly fed from the HARQ buffer into the decoder.

The invention will be described in the following with reference to the accompanying drawings, which show:

- Figure 1** a conventional transmitter implementation of AMC and hybrid ARQ functionality in HSDPA;
- Figure 2** a conventional receiver implementation of AMC and hybrid ARQ functionality in HSDPA;
- Figure 3** details of the turbo decoder shown in Figure 2; and
- Figure 4** a receiver implementation of AMC and hybrid ARQ functionality in HSDPA for illustrating the buffer saving compared to the implementation shown in Figure 2.

Figure 4 shows a receiver implementation for obtaining a reduction of the required buffer size.

An incoming data bit stream is first de-interleaved and separated into a systematic bit substream SYS and two parity bit substreams P1, P2. In buffer 401, the output of the de-interleaver/bit-separation unit is temporarily stored before being applied to the first de-rate matching stage 403. Subsequently, the data bit substreams are applied to HARQ (virtual IR) buffer 402.

The turbo decoder essentially comprises all components, which are shown in figure 3. Moreover, turbo decoder comprises two de-rate matching stages 404A, 404B shown as logically separated units. The de-rate matching operation could also be performed in one processing block. To each de-rate matching stage, the respective parity bit stream P1, P2 is applied as output from the HARQ buffer 402. As shown, the systematic bit stream SYS is directly applied to the first MAP decoder 407A.

Further, the turbo decoder 406 comprises a second MAP decoder 407B interleaver units 409, a de-interleaver unit 410 and an internal turbo decoder buffer 411.

The operation of the turbo decoder including the de-rate matching operation is as follows.

The decoder works with a plurality of iterations, where the probability for correct decoding increases with the number of iterations. Generally, one full-iteration is referred to as

performing a 1st and a 2nd MAP decoding step. A half-iteration is referred to as performing one of the MAP decoding steps. In typical implementation variants after each half-iteration either the changed soft-values of the systematic bits, L^e_{12}/L^e_{21} or a soft metric representing a combination of both are stored in the internal turbo decoder buffer. However, this is turbo decoder implementation dependent.

After a usually predefined number of full-iterations (typically 6-8) the changed soft-values of the systematic bits - caused by the turbo decoding process – are stored in the internal turbo decoder buffer and forwarded to the CRC check unit.

In more sophisticated implementation variants the changed soft-values of the systematic bits are stored in the internal turbo decoder buffer after each half- or full-iteration. This provides the possibility to perform a CRC check after each half- or full-iteration and, hence, to terminate the decoding process at an early state in case the CRC check does not fail.

Note, that generally the decoding process can also start with the 2nd MAP decoder, i.e. in a full-iteration first the 2nd MAP decoding and afterwards the 1st MAP decoding is performed.

During each iteration, the first map decoder 407A receives the parity bit stream P1, the systematic bit stream SYS from buffer 402 (depending on implementation variant, possibly only in the 1st iteration) and the output from de-interleaver 410 (except in the 1st iteration). For each iteration step, the parity bit stream P1 is output from the second buffer 402 and a de-rate matching operation is performed by the respective stage 404A. The second MAP decoder 407 B receives at each iteration step, the output L^e_{12} from the first MAP decoder through interleaver 409 as well as the SYS bit stream and the parity bit stream P2 as output from the second de-rate matching stage 404B, which accesses the data bits stored in buffer 402.

The output L^e_{21} of the second MAP decoder 407B is applied to the de-interleaver 410 and fed to the first MAP decoder 407A as described above with reference to figure 3. Note that the essential difference in the operation of the turbo decoder shown in figure 4 is the fact that the de-rate matching operation is repeatedly (during decoder iterations)

performed under access to the parity data bits stored in buffer 402. Although this comes at the expense of an increased processing complexity, a significant reduction in required buffer size can be obtained as the third buffer conventionally included after the second de-rate matching operation can be completely omitted. Hence, the second stage de-rate matching operation needs to be executed for each decoder iteration, whereas in a conventional implementation, the second stage de-rate matching operation needs to be executed only once and the result is stored in a buffer.

Since the second de-rate matching operation is not applied on the systematic bit stream SYS the turbo decoder 406 may access the SYS bits directly from the virtual IR buffer 402. Note that in this case, the access speed requirement for the buffer 402 is stricter since the turbo decoder needs to have fast access during iterations.

The required size for the buffers is shown in the figures. More specifically, it is apparent that temporary buffer 401 should be capable for storing N_{data} soft bits. Finally, the turbo decoder 306 comprises an internal turbo decoder buffer from which the systematic bits are applied to a CRC check unit 408.

The disclosed approach helps to reduce the required buffer size at the receiver by including the 2nd de-rate matching step into the iterative decoder. Since for the considered ARQ Type II/III schemes soft-bits need to be stored in the receiver, the disclosed implementation is particularly advantageous. This approach is especially of interest for the 3GPP High Speed Downlink Packet Access (HSDPA) technique, where the mobile station acts as a receiver and its complexity is significantly influenced by the required buffer sizes.

Note that in the description above only significant buffers are mentioned. It is common understanding that processing units generally include small buffer units for storing temporary needed information. Moreover, it is clear that the above described turbo decoder serves to exemplarily illustrate the subject matter of the invention. Variations of the iterative decoder are readily apparent to those skilled in the art, for example, it does not necessarily have to be a turbo decoder. In this case, it could be sufficient to process one parity bit stream.

CLAIMS

1. A method of buffering data at the receiver of a packet transmission communication system employing hybrid ARQ type II/III and adaptive coding and modulation schemes, wherein the adaptive coding is performed by a two-stage rate matching algorithm comprising the steps of:

receiving a data bit stream;

storing the data bit stream in a first buffer;

performing a first de-rate matching operation on the data bits stored in the first buffer;

combining the data bits stored in the first buffer with the data bits from an earlier transmission and storing the combined data bits in a second buffer;

performing a second de-rate matching operation on the combined data bits stored in the second buffer; and

performing a plurality of iterative decoding steps on the data bits obtained from the second de-rate matching operation.

whereby during each iteration the data bits stored in the second buffer are accessed and undergo the second de-rate matching operation.
2. The method according to claim 1, further comprising the steps of separating the data stream into a plurality of data bit streams prior to the steps of storing and de-rate matching.
3. The method according to claim 2, wherein the data bit stream is separated in at least one parity bit stream and at least one systematic bit stream.

4. The method according to claim 3, wherein the parity bit stream undergo the second de-rate matching operation whereas the systematic bit stream does not undergo the second de-rate matching operation prior to performing the plurality of iterative decoding steps.
5. The method according to one of claims 1 to 4, further comprising the step of de-interleaving the received data bit stream prior to the steps of storing and de-rate matching.
6. The method according to one of claims 1 to 5, wherein the de-rate matching operation is a de-puncturing operation.
7. The method according to one of claims 1 to 6, wherein the data is transmitted in the communication system employing a high speed downlink packet access frequency division duplex mode or time division duplex mode.
8. A receiver of a packet transmission communication system employing hybrid ARQ type II/III and adaptive coding and modulation schemes, wherein the adaptive coding is performed by a two-stage rate matching algorithm, comprising:

a first buffer (401) for storing a received data bit stream;

a first de-rate matching entity (403) for performing a de-rate matching operation on the data bits stored in the first buffer (401);

a second buffer for (402) combining the bits output from the first de-rate matching entity (403) with from earlier transmissions and storing the combined bits;

a second de-rate matching entity (404A, 404B) for performing a de-rate matching operation on the combined data bits stored in the second buffer (402); and

a decoder adapted to perform a plurality of iterative decoding steps on the bits of output from the second de-rate matching entity, such that during each iteration the

data bits stored in the second buffer are accessed and undergo a second de-rate matching operation.

9. The receiver according to claim 8, further comprising a decoder (406) comprising an internal decoder buffer.
10. The receiver according to claim 8 or 9 wherein the first buffer (401) is a temporary buffer and the second buffer (402) is a permanent HARQ buffer.
11. The receiver according to one of claims 8 to 10, wherein the iterative decoder is a turbo decoder.

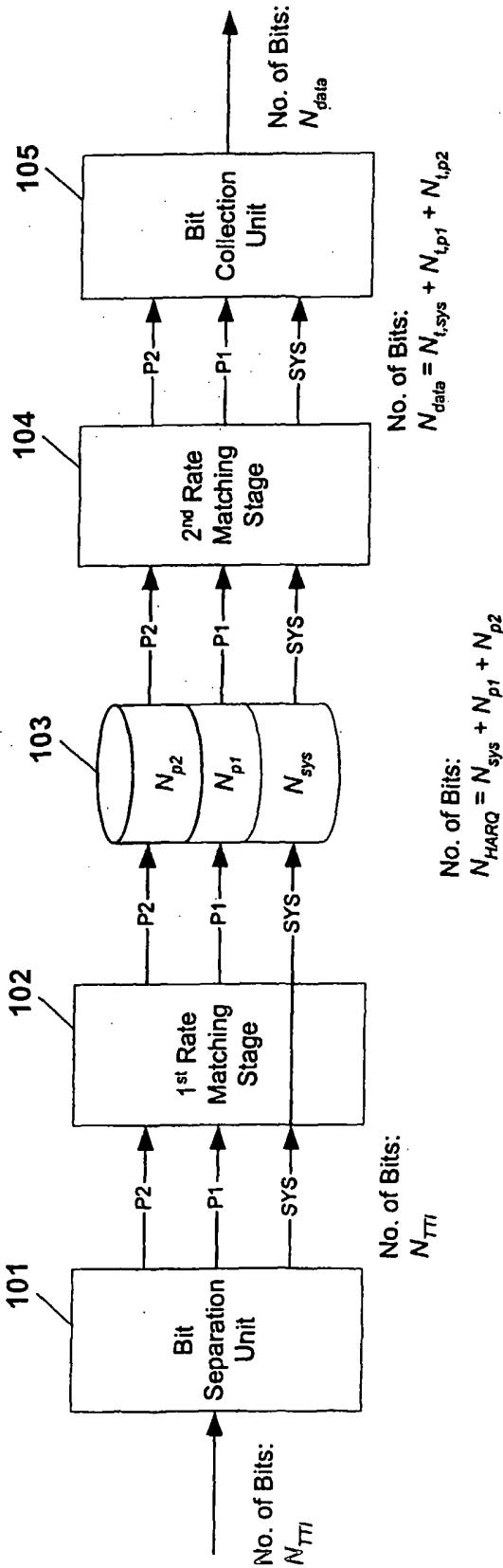
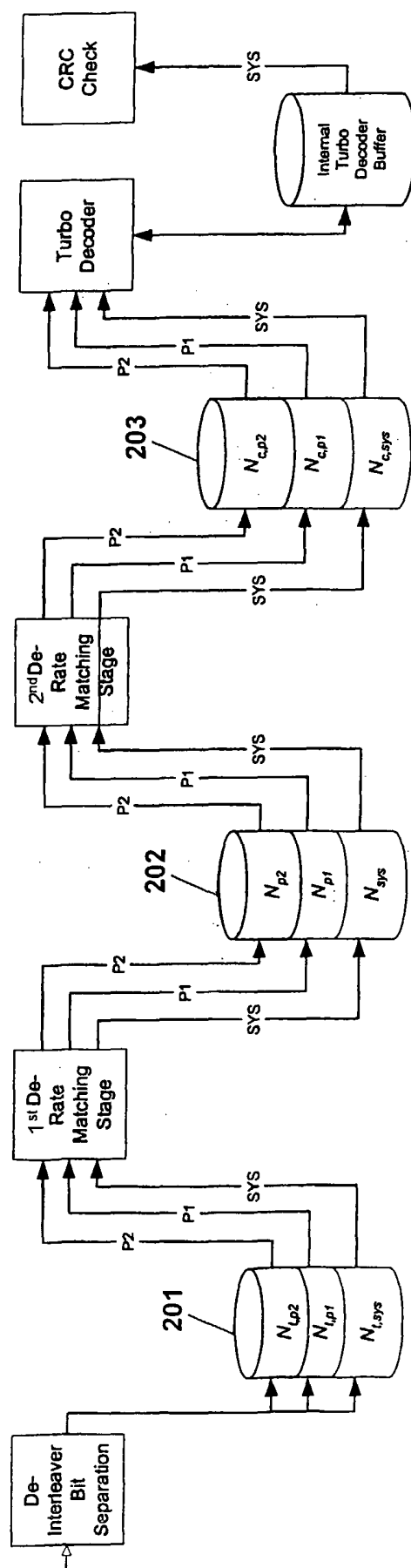


Fig. 1



Temporary Turbo Input Buffer (Bit-level Soft Metrics, LLRs)

Required Size	$N_{B3} = N_{\Pi} \geq N_{HARQ}$
Systematic Bits	$= N_{c,sys}$
Parity 1 Bits	$= N_{c,p1}$
Parity 2 Bits	$= N_{c,p2}$
	$N_{\Pi} = N_{c,sys} + N_{c,p1} + N_{c,p2}$ $= N_{sys}$ $> N_{p1}$ $> N_{p2}$

**HARQ Buffer (Virtual IR Buffer)
(permanent, for each HARQ process)
(Bit-level Soft Metrics, LLRs)**

Required Size	$N_{B2} = N_{HARQ}$	$\geq N_{data}$
Systematic Bits	$= N_{sys}$	$\geq N_{L1}$
Parity 1 Bits	$= N_{p1}$	$\geq N_{L1}$
Parity 2 Bits	$= N_{p2}$	$\geq N_{L1}$
N_{HARQ}	$= N_{sys} + N_{p1} + N_{p2}$	

Temporary Buffer (Bit-level Soft Metrics, LLRs)

$$\begin{aligned} \text{Required Size } N_{g1} &= N_{data} \\ \text{Systematic Bits} &= N_{l,sys} \\ \text{Parity 1 Bits} &= N_{l,p1} \\ \text{Parity 2 Bits} &= N_{l,p2} \\ N_{data} &= N_{l,sys} + N_{l,p1} + N_{l,p2} \end{aligned}$$

Fig. 2

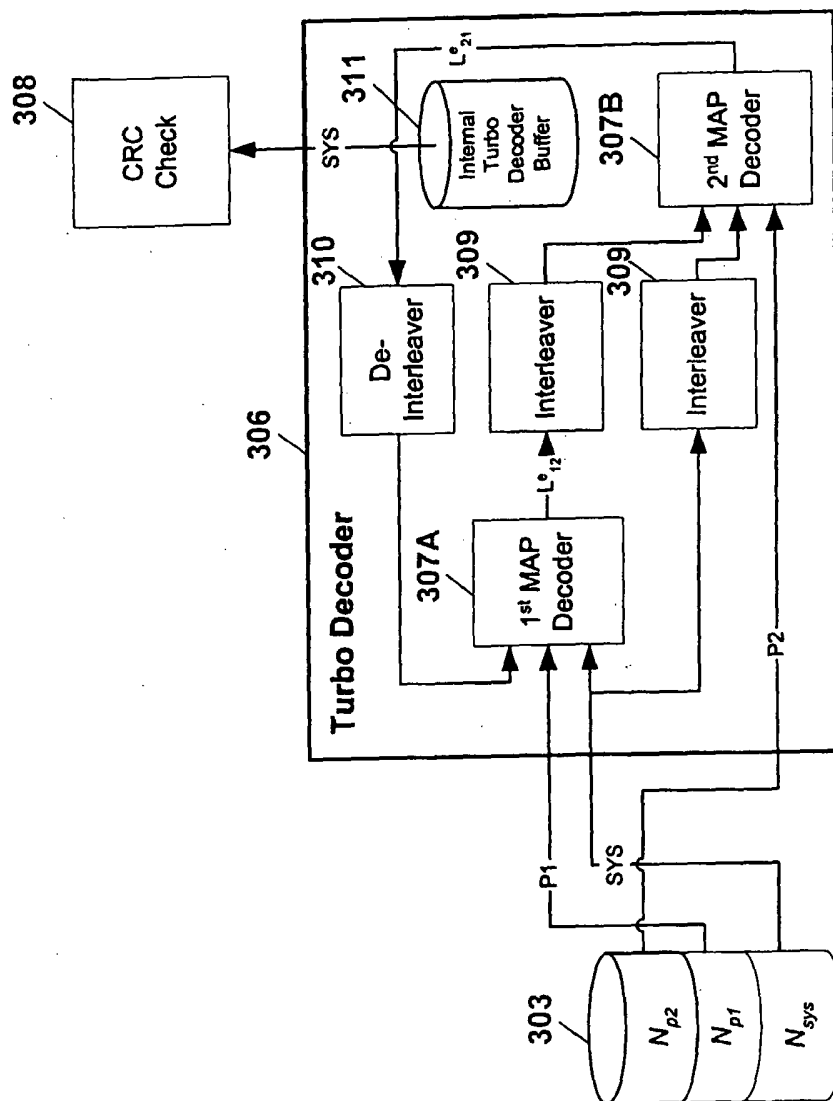
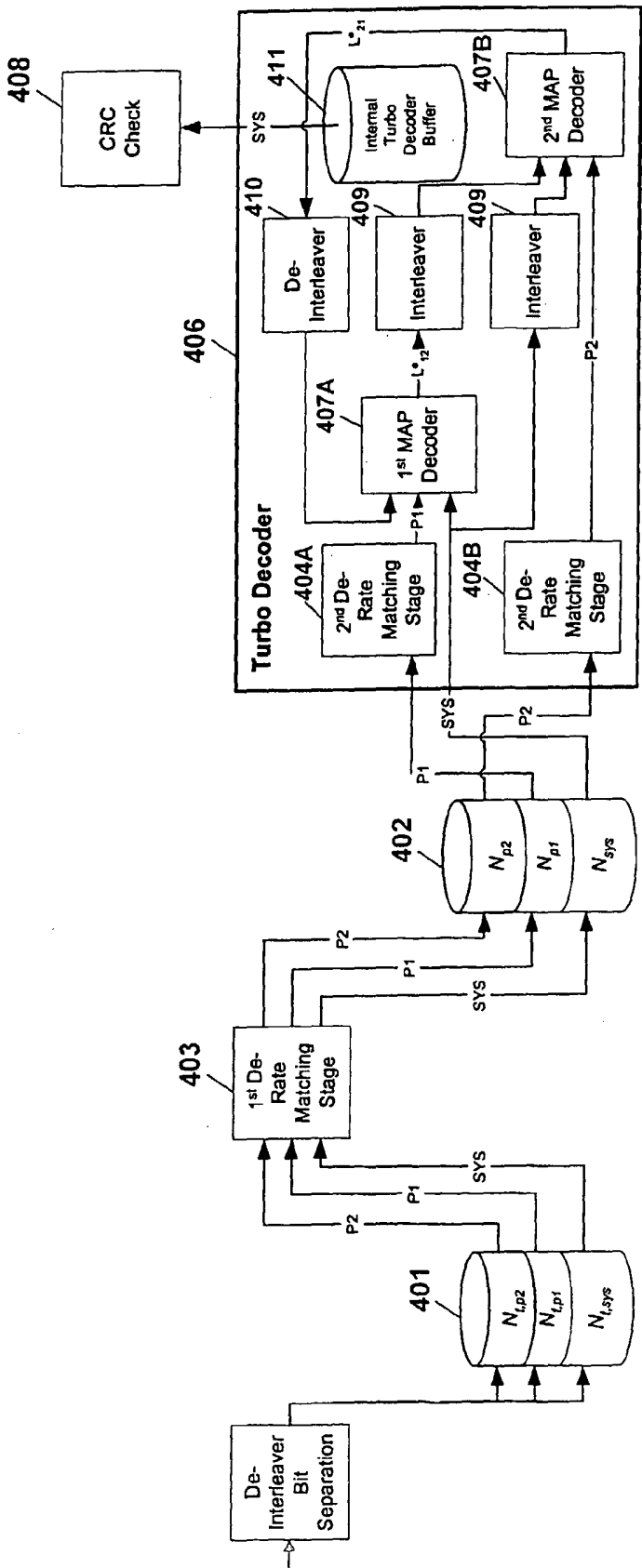


Fig. 3

4/4



HARQ Buffer (Virtual IR Buffer)
(permanent, for each HARQ process)
(Bit-level Soft Metrics, LLRs)

Required Size $N_{B2} = N_{HARQ} \geq N_{data}$

Systematic Bits $= N_{sys}$ $\geq N_{L,sys}$
Parity 1 Bits $= N_{p1}$ $\geq N_{L,p1}$
Parity 2 Bits $= N_{p2}$ $\geq N_{L,p2}$

$N_{HARQ} = N_{sys} + N_{p1} + N_{p2}$

Temporary Buffer
(Bit-level Soft Metrics, LLRs)

Required Size $N_{B1} = N_{data}$

Systematic Bits $= N_{L,sys}$
Parity 1 Bits $= N_{L,p1}$
Parity 2 Bits $= N_{L,p2}$

$N_{data} = N_{L,sys} + N_{L,p1} + N_{L,p2}$

Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/002463

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04L1/18 H04L1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"3rd Generation Partnership Project; Technical Specification Group Radio Access Network; High Speed Downlink Packet Access; Physical Layer Aspects (Release 5)" 3GPP TR 25.858 V1.0.0, XX, XX, December 2001 (2001-12), pages 1,3-23, XP002192345 page 9, line 1 -page 10, line 8 figure 2 ---	1-11
A	US 5 841 951 A (LI CHIA-HSIN ET AL) 24 November 1998 (1998-11-24) column 8, line 66 -column 9, line 5 ---	1-11
A	EP 0 696 129 A (XEROX CORP) 7 February 1996 (1996-02-07) column 9, line 48 - line 55 ---	1-11
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

10 May 2004

Date of mailing of the international search report

27/05/2004

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Agudo Cortada, E

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/002463

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TECHNICAL SPECIFICATION GROUP RADIO ACCESS NETWORK: "3GPP TR25.848 V4.0.0 Physical layer aspects of UTRA High Speed Downlink Packet Access (Release 4)" 3GPP TR 25.848 V4.0.0, XX, XX, 4 May 2001 (2001-05-04), pages 1-82, XP002189517 page 37, line 1 - line 3 -----	1-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP2004/002463

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5841951	A	24-11-1998	JP 9314864 A	09-12-1997
			US 5802212 A	01-09-1998
EP 0696129	A	07-02-1996	US 6427030 B1	30-07-2002
			BR 9503501 A	21-05-1996
			DE 69526469 D1	29-05-2002
			DE 69526469 T2	24-10-2002
			EP 0696129 A2	07-02-1996
			JP 8065515 A	08-03-1996
			US 6144775 A	07-11-2000