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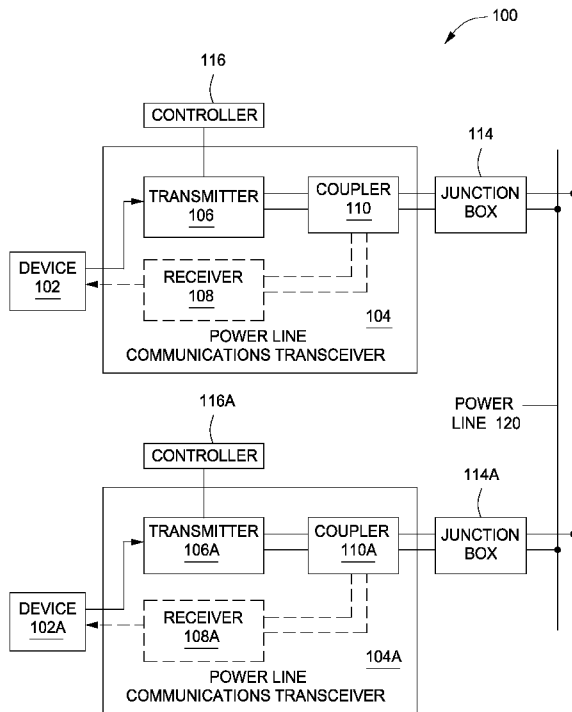


FIG. 1

(57) Abstract: Apparatus and system for communicating data via a power line. The apparatus comprises a transmitter comprising a modulator for generating a second digital signal based on input data; a digital buffer for amplifying the second digital signal to generate a third digital signal; a filter for filtering the third digital signal to generate an analog output waveform; and a coupler for coupling the analog output waveform to the power line.



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POWER LINE COMMUNICATIONS APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the present disclosure relate generally to power line communications and, more particularly, to an apparatus for providing communication over power lines.

Description of the Related Art

[0002] Power Line Communications (PLC) is a technology for utilizing power lines, such as the existing commercial AC power grid infrastructure, to communicate data between devices coupled to the power lines. PLC typically operates in a point-to-multipoint fashion where one transmitter at a time transmits over the power line while other devices coupled to the power line receive the transmitted signal.

[0003] For PLC transmission, a transmitter is generally coupled to the power line through an isolation transformer and sends a voltage stimulus on the power line (i.e., a voltage-based signal) in accordance with relevant standards for PLC, such as BS EN 50065-1:2001 "Specification for Signaling on Low-Voltage Electrical Installations in the Frequency Range 3 kHz to 148.5 kHz". These relevant standards set forth specifications for PLC operation, such as a maximum voltage level. As a result of power lines having undefined and variable impedances within the frequency band of interest for PLC, a transmitter module may be required to generate a large amount of current, for example on the order of hundreds of milliamperes, in order to meet the PLC voltage requirements.

[0004] Generally, PLC transmitters use linear amplifiers to achieve the required amplification and signal processing for PLC transmission. However, such devices dissipate high levels of power when operating to drive large currents on the power line and thus decrease the efficiency of the PLC transmitters. Additionally, the PLC transmitters generally perform filtering prior to the power amplification in order to

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satisfy spectral purity requirements set forth in the relevant standards, requiring a large number of costly components.

[0005] For receiving data transmitted over the power line, a PLC receiver is typically also coupled to the power line through an isolation transformer. The PLC receiver is required to provide a large input impedance to limit noise from the power line into the receiver prior to amplification, thereby requiring a costly number of components to perform such functions.

[0006] Therefore, there is a need in the art for an apparatus for efficient power line communications.

SUMMARY OF THE INVENTION

[0007] Embodiments of the present invention generally relate to an apparatus and system for communicating data via a power line. The apparatus comprises a transmitter comprising a modulator for generating a second digital signal based on input data; a digital buffer for amplifying the second digital signal to generate a third digital signal; a filter for filtering the third digital signal to generate an analog output waveform; and a coupler for coupling the analog output waveform to the power line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0009] Figure 1 is a block diagram of a system for communicating data over an AC power line in accordance with one or more embodiments of the present invention;

[0010] Figure 2 is a block diagram of a transmitter in accordance with one or more embodiments of the present invention;

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[0011] Figure 3 is a block diagram of a receiver in accordance with one or more embodiments of the present invention;

[0012] Figure 4 is a block diagram of a coupler in accordance with one or more embodiments of the present invention; and

[0013] Figure 5 is a block diagram of a system for inverting solar generated DC power to AC power using one or more embodiments of the present invention.

DETAILED DESCRIPTION

[0014] Figure 1 is a block diagram of a system 100 for communicating data over an AC power line in accordance with one or more embodiments of the present invention. The system 100 comprises a device 102 coupled to a power line communications transceiver (PLCT) 104, which is further coupled to an AC power line 120 ("power line 120") via a junction box 114. Additionally, the system 100 comprises a device 102A coupled to a PLCT 104A, which is further coupled to the power line 120 via a junction box 114A. The devices 102 and 102A are devices requiring communications bandwidth for transmitting and/or receiving data, such as a home computer, peripheral device, and the like, and are capable of communicating with one another over the power line 120 via the PLCTs 104 and 104A, respectively. In some embodiments, the PLCT 104 and/or the PLCT 104A may be coupled directly to the power line 120 without the use of junction boxes 114/114A. One particular embodiment that uses the inventive system is described below with respect to Figure 5.

[0015] The PLCT 104 comprises a transmitter 106 and a receiver 108, each coupled to the device 102, and a coupler 110 that couples both the transmitter 106 and the receiver 108 to the junction box 114. When the PLCT 104 is operating in a "transmit mode", the transmitter 106 is capable of transmitting data to the device 102A via the power line 120. The receiver 108 is capable of receiving data from the device 102A via the power line 120. The PLCT 104 may be able to simultaneously receive and transmit data; however, the transmitter 106 may generally blind the receiver 108 while active. In some embodiments, a controller 116 is coupled to the transmitter

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106 and provides a control signal for enabling and disabling the transmit mode. The controller 116 may be separate from the PLCT 104 as depicted in Figure 1, or, alternatively, the controller 116 may be a component of the PLCT 104.

[0016] Analogous to the PLCT 104, the PLCT 104A comprises a transmitter 106A, a receiver 108A, and a coupler 110A. The transmitter 106A and receiver 108A are coupled to the device 102A as well as the coupler 110A, and the coupler 110A is further coupled to the junction box 114A. When the PLCT 104A is operating in a transmit mode, the transmitter 106A is capable of transmitting data to the device 102 via the power line 120. The receiver 108A is capable of receiving data from the device 102 via the power line 120. The PLCT 104A may be able to simultaneously receive and transmit data; however, the transmitter 106A may generally blind the receiver 108A while active. In some embodiments, a controller 116A is coupled to the transmitter 106A and provides a control signal for enabling and disabling the transmit mode. The controller 116A may be separate from the PLCT 104A as depicted in Figure 1, or, alternatively, the controller 116A may be a component of the PLCT 104A.

[0017] In accordance with one or more embodiments of the present invention, when operating in the transmit mode the transmitter 106 receives digital input data from the device 102 and digitally processes the received data through a voltage amplification stage to generate digitally processed data. Following the voltage amplification stage, the transmitter 106 generates an analog voltage waveform for transmitting the digitally processed data over the power line 120 such that the analog voltage waveform characteristics (e.g., frequency, magnitude, spectral purity, and the like) meet relevant standards for PLC. In some embodiments, the analog voltage waveform may be generated to have a frequency within the band 50-500 KHz (for example, in the 95-148KHz band) and a maximum voltage on the order of 1 volt root mean square (RMS), i.e., 120 decibel/microvolt (dB μ V). The coupler 110 couples the generated analog voltage waveform to the power line 120.

[0018] During the transmit mode, the transmitter 106 presents a minimal impedance (e.g., within a range of 1-5 ohms) to the power line 120. In order to meet required

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output voltage levels given the variability of impedance on the power line 120, the transmitter 106 is capable of driving large currents, for example on the order of hundreds of milliamperes, on the power line 120. In order to drive such large currents, the transmitter 106 may employ a high-current rated complementary metal-oxide-semiconductor (CMOS) buffer, as described further below, for performing the voltage amplification in the digital domain and driving the necessary current levels.

[0019] When the PLCT 104 is receiving, the coupler 110 couples an analog signal from the power line 120 to the receiver 108. The receiver 108 converts the received analog voltage waveform to digital output data and provides the digital output data to the device 102. In some embodiments, the digital output data may be a digital representation of a modulated signal; for example, the digital output data may be a digital representation of an FSK signal (a digital FSK signal), and an FSK demodulator is contained within the device 102 or coupled between the receiver 108 and the device 102. The receiver 108, as further described below, may comprise a band-pass filter for filtering the received waveform to remove noise inherent to the power line 120. When the transmit mode is disabled, the PLCT 104 presents a large input impedance to the power line 120 (e.g., on the order of kilo-ohms). Such a large input impedance prevents the transmitter 106 from being “swamped out” when a large number of nodes are present on the power line 120.

[0020] In some alternative embodiments, the PLCT 104 comprises only the transmitter 106 and the coupler 110 for transmitting information via the power line 120; additionally or alternatively, the PLCT 104A may comprise only the transmitter 106A and the coupler 110A for transmitting information via the power line 120. In such embodiments, the receivers 108 and/or 108A are not used. The optional nature of including a receiver is represented by the dashed boxes of receivers 108 and 108A.

[0021] Figure 2 is a block diagram of a transmitter 106 in accordance with one or more embodiments of the present invention. The transmitter 106 comprises a frequency control generator 202 coupled to a direct digital synthesizer (DDS) 204,

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which is further coupled to a delta-sigma ($\Delta\Sigma$) modulator 206. The $\Delta\Sigma$ modulator 206 is coupled to a CMOS buffer 208, and an output from the CMOS buffer 208 is coupled to a low-pass filter 210. The CMOS buffer 208 is additionally coupled to the controller 116 for receiving an input to enable/disable the transmit mode. When the transmit mode is enabled, the CMOS buffer 208 presents a low transmit impedance (e.g., on the order of 1-5 ohms); when the transmit mode is disabled, the CMOS buffer 208 present a large input impedance (e.g., on the order of kilo-ohms).

[0022] The frequency control generator 202 is coupled to the device 102 for receiving a digital input data signal for transmission over the power line 120. The frequency control generator 202 generates a digital frequency control signal (for example, a 16 to 24 bit signal) based on the received data signal and couples the digital frequency control signal to the DDS 204. The DDS 204 operates at a high frequency and, in accordance with the frequency control signal, generates a digital frequency-shift keying (FSK) signal (i.e., a digital representation of an FSK signal). In some embodiments, the digital FSK signal may be on the order of 8-10 bits wide at a frequency of 25 MHz; alternatively, the digital FSK signal may comprise fewer or more bits and/or may be at a different frequency. In some alternative embodiments, minimum FSK modulation may be utilized; in some other alternative embodiments, modulation techniques other than FSK modulation may be utilized, such as M-ary quadrature amplitude modulation (QAM), quadrature phase-shift keying (QPSK), phase-shift keying (PSK), orthogonal frequency-division multiplexing (OFDM), pulse-amplitude modulation (PAM), or the like.

[0023] The DDS 204 output signal is coupled to the $\Delta\Sigma$ modulator 206, which may be a single-stage $\Delta\Sigma$ modulator or a multi-stage $\Delta\Sigma$ modulator. The $\Delta\Sigma$ modulator 206 encodes the received digital FSK signal utilizing pulse-density modulation (PDM) and provides a digital 1-bit output signal representing the received digital FSK signal. In some embodiments, the $\Delta\Sigma$ modulator 206 may operate at a frequency of 25 MHz; in alternative embodiments, the $\Delta\Sigma$ modulator 206 may operate at a different frequency.

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[0024] The frequency control generator 202, DD2 204, and $\Delta\Sigma$ modulator 206 form a modulator 212 that generates a digital signal based on the digital input data signal from the device 102. The digital signal from the modulator 212 (i.e., the output of the $\Delta\Sigma$ modulator 206) is coupled to the CMOS buffer 208 for amplifying the voltage. The CMOS buffer 208 may be a high-current rated CMOS buffer capable of providing sufficient current (e.g., hundreds of milliamperes) to maintain a required output voltage level when the power line impedance is very low; in some embodiments, the CMOS buffer 208 may be on the order of 0.15 to 0.25 micron technology. In some embodiments, the CMOS buffer 208 may comprise a plurality of buffers (e.g., sixteen buffers) coupled in parallel, each buffer capable of producing current on the order of 50 mA. The number of buffers coupled in parallel determines the amount of current that can be driven and is considered a design choice for the system.

[0025] Following the voltage amplification, the CMOS buffer 208 produces a digital output signal which is coupled to the low-pass filter 210 and filtered to generate an analog output. As a result of the $\Delta\Sigma$ modulator 206 running at a high frequency, for example 25 MHz, the low-pass filtering can be performed in the MHz frequency band to remove sufficient artifacts resulting from the $\Delta\Sigma$ modulation. The output of the low-pass filter 210 is coupled to the power line 120 through the coupler 110, as explained further below with respect to figure 4.

[0026] Figure 3 is a block diagram of a receiver 108 in accordance with one or more embodiments of the present invention. The receiver 108 receives an analog voltage waveform from the power line 120 through the coupler 110, as further described below, and generates a digital output data signal that is coupled to the device 102.

[0027] The receiver 108 comprises capacitors 302, 304, 306, and 314; an inductor 308; resistors 312 and 310; and an analog-to-digital (A/D) converter 316. In some embodiments, one or more the capacitors/inductor/resistors may be a parasitic component. The capacitors 302, 304, and 306 are coupled in series such that the capacitor 302 is coupled to the capacitor 304 which is in turn coupled to the capacitor 306, and the received analog waveform is coupled from the coupler 110

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across the series combination of capacitors 302, 304, and 306. The inductor 308 is coupled across the series combination of the capacitors 304 and 306. The capacitors 302, 304, and 306 and the inductor 308 perform band-pass filtering of the received analog voltage waveform to reduce noise that is inherently present on the power line 120 (i.e., to pass the signal of interest with minimal phase/amplitude distortion).

[0028] The resistor 310 is coupled across the capacitor 306. The resistor 312 is coupled between a first terminal of the resistor 310 and a first terminal of the capacitor 314; a second terminal of the resistor 310 is coupled to a second terminal of the capacitor 314. The A/D converter 316 is coupled across the capacitor 314 and is further coupled to the device 102. The resistors 310 and 312 form a high impedance resistive load, and the A/D converter 316 samples the voltage across this load to produce an FSK-modulated digital output signal for the device 102 (i.e., a digital representation of an FSK signal). In some embodiments, the device 102 comprises an FSK demodulator for demodulating the digital output signal; alternatively, an FSK demodulator may be coupled between the receiver 108 and the device 102. In some alternative embodiments, the digital output data signal may be a digital representation of a minimum FSK modulated signal, a QAM modulated signal, a QPSK modulated signal, a PSK modulated signal, an OFDM modulated signal, a PAM modulated signal, or the like.

[0029] In some embodiments, the resistors 310 and 312 may each be on the order of a few hundred ohms; the capacitors 304, 306, and 314 may each be on the order of a few nanofarads; the capacitor 302 may be on the order of several hundred picofarads; and the inductor 308 may be on the order of a few hundred microhenries.

[0030] Figure 4 is a block diagram of a coupler 110 in accordance with one or more embodiments of the present invention. The coupler 110 comprises a transformer 402, an inductor 404 to represent a leakage inductance of the transformer 402, a resistor 406, and capacitors 408 and 410. In some embodiments, the coupler 110 may be simplified. Generally, the transmit signal must be low pass filtered without

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increasing the output impedance and loading the receiver while inactive; the receive signal must be band pass filtered to pass the signal of interest and attenuate out of band noise, while maintaining high impedance in the band of interest.

[0031] The transformer 402 is an isolation transformer having a high coupling factor; for example, the coupling factor may be 0.95 or greater. Generally, the transformer 402 has a 1:1 turns ratio, although other turns ratios may also be utilized. A primary winding of the transformer 402 is coupled across each of the transmitter 106 and the receiver 108. A first terminal of a secondary winding of the transformer 402 is depicted as coupled to a first terminal of the inductor 404. The resistor 406 is coupled between a second terminal of the inductor 404 and a first terminal of the capacitor 408, which provides a safety function for coupling to the power line 120. The resistor 406 acts to damp an RLC tank formed by the resistor 406, the inductor 404, and the capacitor 408.

[0032] The capacitor 410 is coupled between a second terminal of the capacitor 408 and a second terminal of the secondary winding of the transformer 402, and is further coupled across two output terminals of the coupler 110 for coupling to the power line 120 through the junction box 114. The capacitor 410 provides an optional low-pass filtering function; in some alternative embodiments, the capacitor 410 may be removed from the coupler 110.

[0033] The coupler 110 couples the outbound analog voltage waveform from the transmitter 106 to the power line 120 and couples the inbound analog voltage waveform from the power line 120 to the receiver 108.

[0034] In some embodiments, the primary and secondary windings of the transformer 402 each have an inductance on the order of a few hundred microhenries; the inductor 404 (i.e., the leakage inductance of the transformer 402) is on the order of a few microhenries; the resistor 406 is on the order of a few ohms; the capacitor 408 is on the order of a few hundred nanofarads; and the capacitor 410 is on the order of a few nanofarads.

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[0035] Figure 5 is a block diagram of a system 500 for inverting solar generated DC power to AC power using one or more embodiments of the present invention. This diagram only portrays one variation of the myriad of possible system configurations and devices that may utilize the present invention. The present invention can be utilized by any device for power line communication, and can function in a variety of distributed environments and systems requiring communications over power lines.

[0036] The system 500 comprises a plurality of inverters $502_1, 502_2 \dots 502_n$, collectively referred to as inverters 502, a plurality of PV modules $504_1, 504_2 \dots 504_n$, collectively referred to as PV modules 504, a plurality of PLCTs $512_1, 512_2 \dots 512_n, 512_{n+1}$, collectively referred to as PLCTs 512, AC power line 506, an inverter controller 510, and a load center 508.

[0037] Each inverter $502_1, 502_2 \dots 502_n$ is coupled to a PLCT $512_1, 512_2 \dots 512_n$, respectively; in some alternative embodiments, each of the PLCTs $512_1, 512_2 \dots 512_n$ may be contained within the corresponding inverter $502_1, 502_2 \dots 502_n$. Each inverter $502_1, 502_2 \dots 502_n$ is additionally coupled to a PV module $504_1, 504_2 \dots 504_n$, respectively. The inverter controller 510 is coupled to the PLCT 512_{n+1} .

[0038] The PLCTs 512 are coupled to the AC power line 506 and operate analogously to the PLCTs 104 and 104A described above. In some embodiments, each of the PLCTs 512 may be coupled to a controller (i.e., one controller per PLCT 512), such as controller 116, for enabling/disabling a transmit mode of the PLCT 512. The AC power line 506 is further coupled to the load center 508 which houses connections between incoming commercial AC power lines from a commercial AC power grid distribution system and the AC power line 506. The inverters 502 convert DC power generated by the PV modules 504 into AC power, and meter out AC current that is in-phase with the commercial AC power grid voltage. The system 500 couples the generated AC power to the commercial AC power grid via the load center 508.

[0039] The inverter controller 510 is capable of receiving data from the inverters 502 and issuing command and control signals to the inverters 502 for controlling the

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functionality of the inverters 502. In accordance with one or more embodiments of the present invention, the PLCTs 512 enable such communication between the inverters 502 and the inverter controller 510 over the AC power lines 506. As previously described, the PLCTs 512 digitally process digital input data from the inverters 502 and/or the inverter controller 510 through a voltage amplification stage and generate a corresponding analog voltage waveform that is coupled to the AC power lines 506 for transmitting the received digital input data. Also, as previously described, the PLCTs 512 receive an analog voltage waveform from the AC power line 506 and process the received waveform to produce digital output data that is coupled to the inverters 502 and/or the inverter controller 510, thereby allowing the inverters 501 and the inverter controller 510 to communicate over the AC power lines 506.

[0040] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

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CLAIMS:

1. Apparatus for communicating via a power line, comprising:
 - a transmitter comprising a modulator for generating a second digital signal based on input data;
 - a digital buffer for amplifying the second digital signal to generate a third digital signal;
 - a filter for filtering the third digital signal to generate an analog output waveform; and
 - a coupler for coupling the analog output waveform to the power line.
2. The apparatus of claim 1, wherein the modulator comprises a direct digital synthesizer for generating a first digital signal based on the input data and a delta-sigma modulator for generating the second digital signal based on the first digital signal.
3. The apparatus of claim 2, wherein the first digital signal is a digital frequency shift keying (FSK) signal and the second digital signal is a pulse density modulated (PDM) signal.
4. The apparatus of claim 1, wherein the digital buffer receives a control signal for enabling a transmit mode.
5. The apparatus of claim 4, wherein the digital buffer presents a minimal impedance during the transmit mode.
6. The apparatus of claim 1, further comprising a receiver for receiving an analog input waveform from the power line via the coupler and generating a digital output signal based on the analog input waveform.
7. The apparatus of claim 6, wherein the receiver is capable of receiving the analog waveform when a transmit mode is disabled.

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8. The apparatus of claim 7, wherein the digital buffer presents a higher impedance when the transmit mode is disabled than when the transmit mode is enabled.

9. The apparatus of claim 1, wherein the coupler comprises a transformer, a resistor, a first capacitor and a second capacitor, wherein a primary winding of the transformer is coupled across an output of the transmitter; a secondary winding of the transformer is coupled across a series combination of the resistor, the first and the second capacitors, and an output of the coupler is coupled across the second capacitor.

10. The apparatus of claim 6, wherein the receiver comprises an analog to digital (A/D) converter, a first capacitor, a second capacitor, a third capacitor, a fourth capacitor, a first resistor, a second resistor, and an inductor; wherein the a/d converter is coupled across the first capacitor; a first terminal of the first resistor is coupled to a first terminal of the first capacitor and a second terminal of the first resistor is coupled to a first terminal of the second resistor, a first terminal of the second capacitor, and a first terminal of the third capacitor; a second terminal of the third capacitor is coupled to a first terminal of the fourth capacitor and a first terminal of the inductor; a second terminal of the inductor is coupled to a second terminal of the second capacitor, a second terminal of the second resistor, and a second terminal of the first capacitor; and an input to the receiver is coupled across a second terminal of the fourth capacitor and a second terminal of the inductor.

11. A system for communicating via a power line, comprising:

- an inverter; and

- an apparatus capable of being coupled to the power line, comprising:

- a transmitter comprising a modulator for generating a second digital signal based on input data from the inverter;

- a digital buffer for amplifying the second digital signal to generate a third digital signal;

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a filter for filtering the third digital signal to generate an analog output waveform; and

a coupler for coupling the analog output waveform to the power line.

12. The system of claim 11, wherein the modulator comprises a direct digital synthesizer for generating a first digital signal based on the input data and a delta-sigma modulator for generating the second digital signal based on the first digital signal.

13. The system of claim 12, wherein the first digital signal is a digital frequency shift keying (FSK) signal and the second digital signal is a pulse density modulated (PDM) signal.

14. The system of claim 11, wherein the digital buffer receives a control signal for enabling a transmit mode.

15. The system of claim 14, wherein the digital buffer presents a minimal impedance during the transmit mode.

16. The system of claim 11, further comprising a receiver for receiving an analog input waveform from the power line via the coupler, generating a digital output signal based on the analog input waveform, and coupling the digital output signal to the inverter.

17. The system of claim 16, wherein the receiver is capable of receiving the analog waveform when a transmit mode is disabled.

18. The system of claim 17, wherein the digital buffer presents a higher impedance when the transmit mode is disabled than when the transmit mode is enabled.

19. The system of claim 11, wherein the coupler comprises a transformer, a resistor, a first capacitor and a second capacitor, wherein a primary winding of the

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transformer is coupled across an output of the transmitter; a secondary winding of the transformer is coupled across a series combination of the resistor, the first and the second capacitors, and an output of the coupler is coupled across the second capacitor.

20. The system of claim 16, wherein the receiver comprises an analog to digital (A/D) converter, a first capacitor, a second capacitor, a third capacitor, a fourth capacitor, a first resistor, a second resistor, and an inductor; wherein the a/d converter is coupled across the first capacitor; a first terminal of the first resistor is coupled to a first terminal of the first capacitor and a second terminal of the first resistor is coupled to a first terminal of the second resistor, a first terminal of the second capacitor, and a first terminal of the third capacitor; a second terminal of the third capacitor is coupled to a first terminal of the fourth capacitor and a first terminal of the inductor; a second terminal of the inductor is coupled to a second terminal of the second capacitor, a second terminal of the second resistor, and a second terminal of the first capacitor; and an input to the receiver is coupled across a second terminal of the fourth capacitor and a second terminal of the inductor.

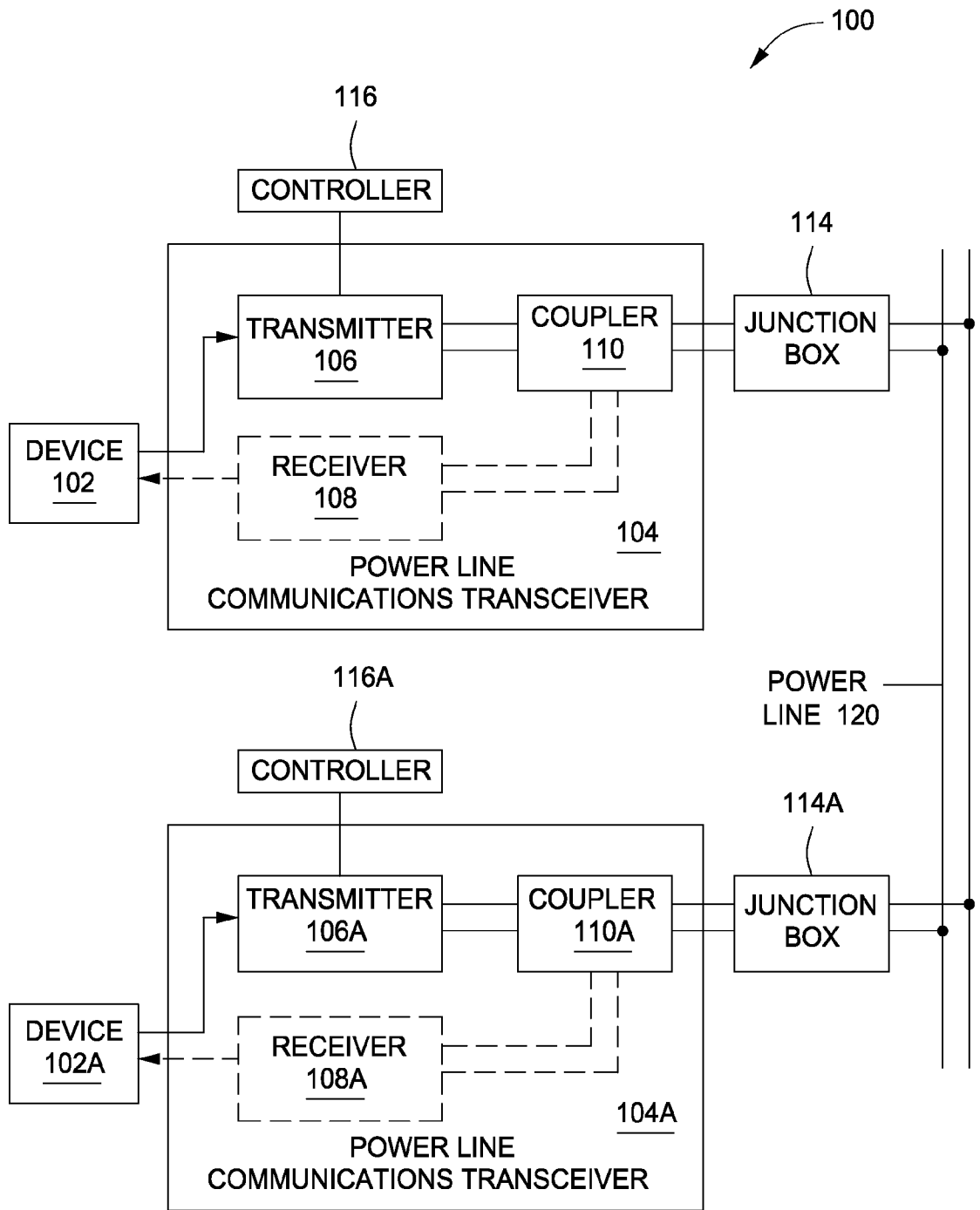


FIG. 1

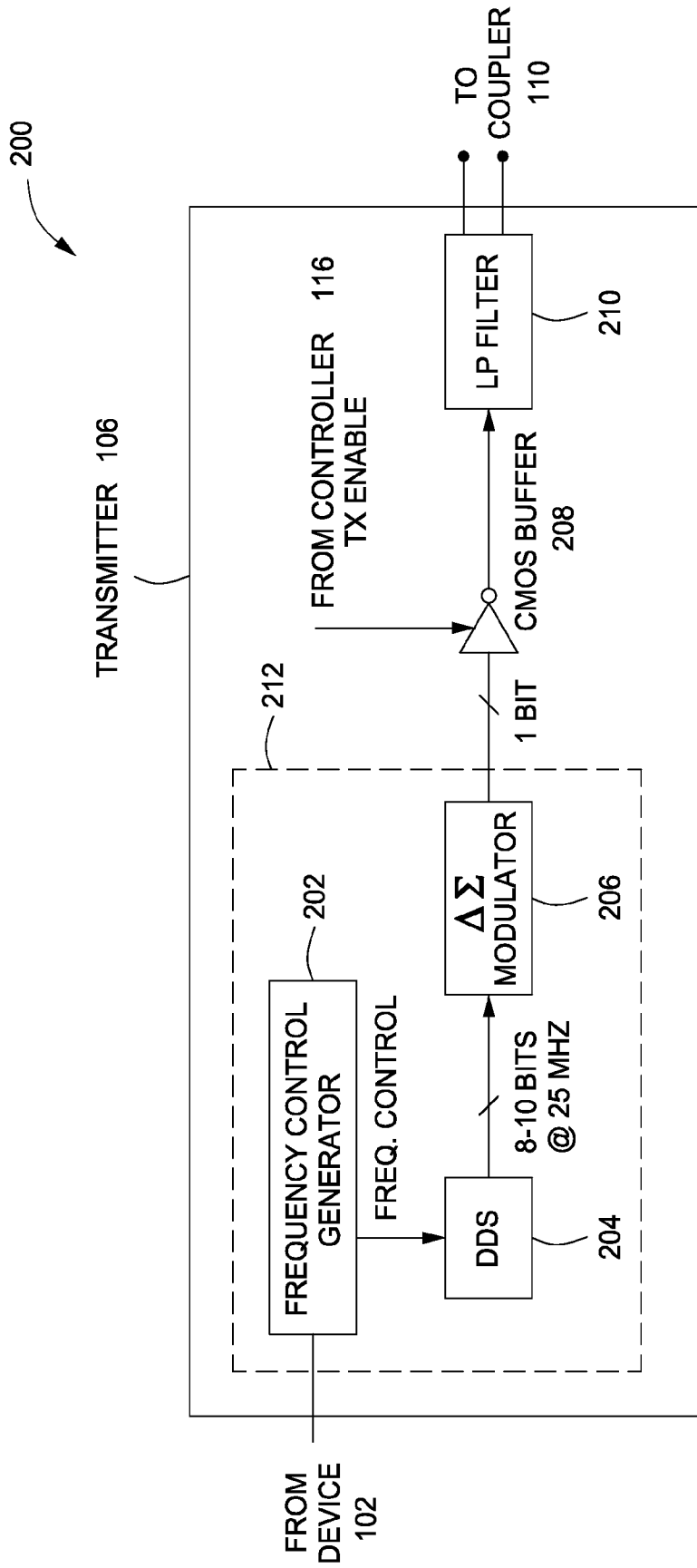


FIG. 2

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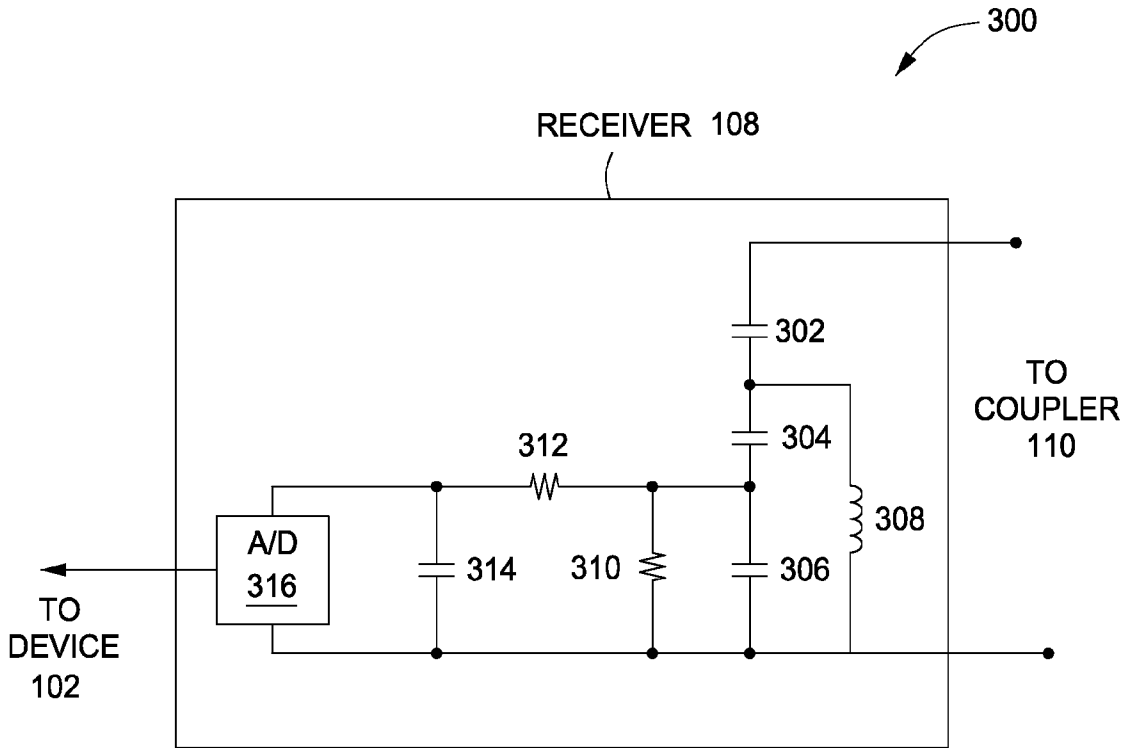


FIG. 3

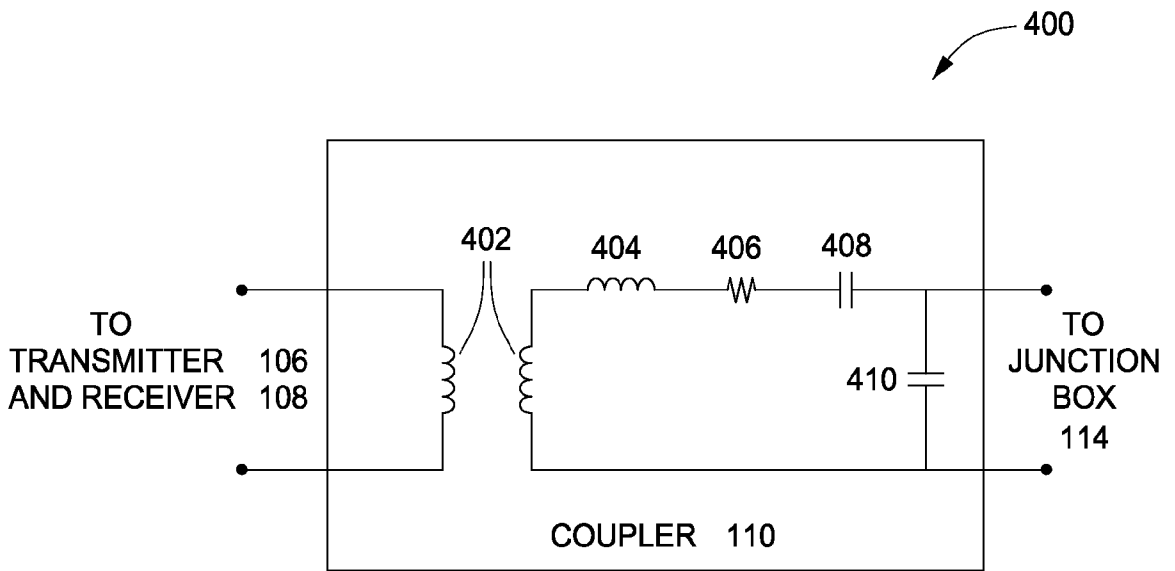


FIG. 4

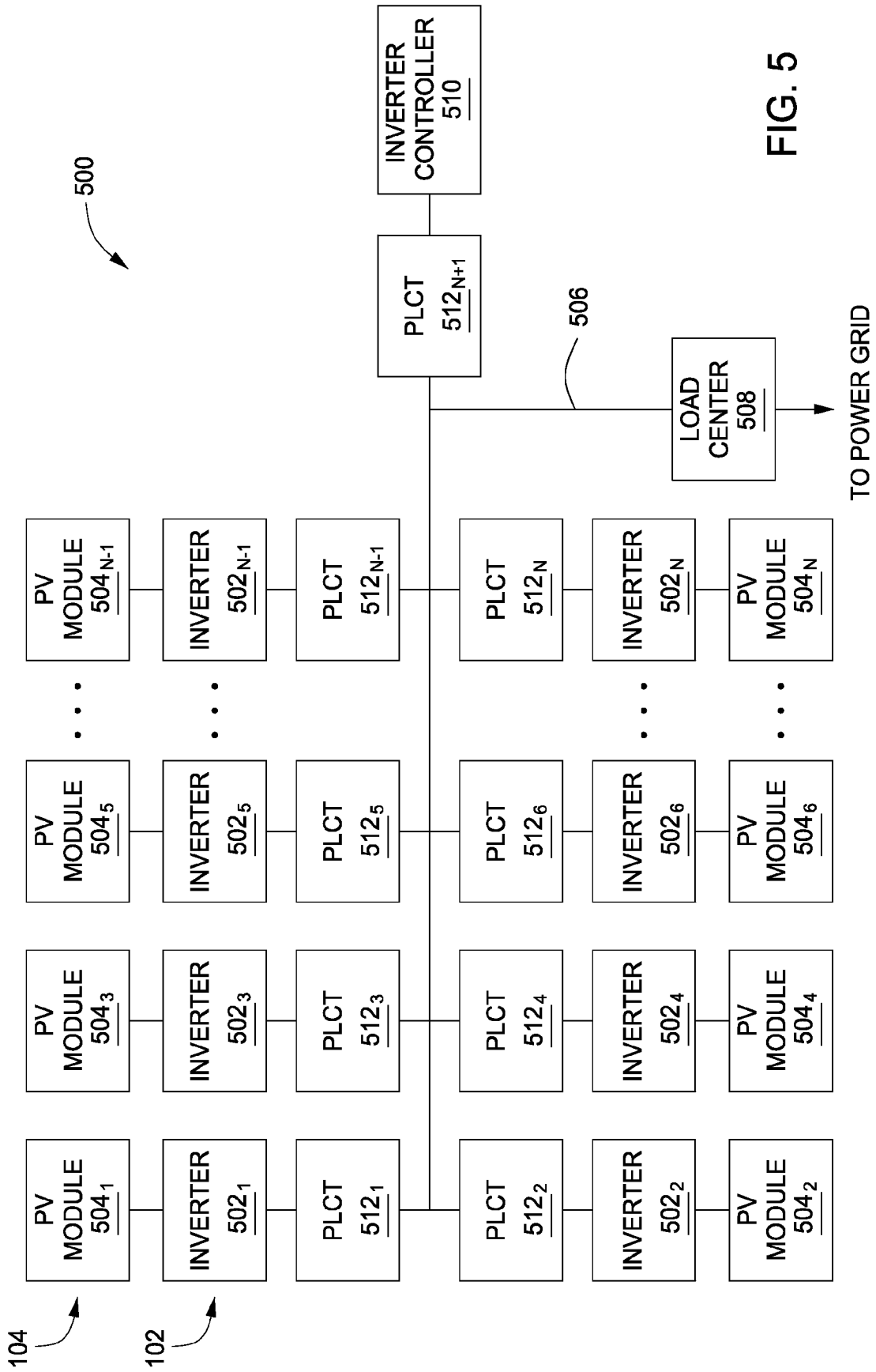


FIG. 5