United States Patent [19]

Anderson, Jr.

[11] **3,835,819**

[45] **Sept. 17, 1974**

[54] **DIGITAL ENGINE CONTROL APPARATUS AND METHOD**

[75] Inventor: **Robert L. Anderson, Jr.**, Pittsburgh, Pa.

[73] Assignee: **Essex International, Inc.**, Fort Wayne, Ind.

[22] Filed: **Dec. 29, 1972**

[21] Appl. No.: **319,345**

[52] **U.S. Cl.. 123/32 EA,** 123/139 AW, 123/119 R, 123/117 R, 235/150.21, 340/172.5

[51] **Int. Cl.** **F02m 52/00**

[58] **Field of Search**..... 123/32 EA, 119 R, 139 AL, 123/139 R, 139 AW, 140 MC, 140 CC; 235/150, 150.2, 150.21; 340/172.5

[56] **References Cited**

UNITED STATES PATENTS

2,868,183	1/1959	Reggio	123/140 CC
3,054,393	9/1962	Schmidt	123/139 AL
3,606,869	9/1971	Huntzinger et al	123/139 AW
3,659,563	5/1972	Monpetit	123/32 EA
3,689,753	9/1972	Williams et al.	235/150.21

FOREIGN PATENTS OR APPLICATIONS

2,004,269	8/1970	Germany	123/32 EA

Primary Examiner—Laurence M. Goodridge

Attorney, Agent, or Firm—Molinare, Allegretti, Newitt & Witcoff

[57] **ABSTRACT**

The disclosure describes digital apparatus and a digital method for operating a multicylinder internal combustion engine having spark plugs that are fired in response to an electrical fire signal and having fuel injectors that are opened to admit a quantity of fuel in response to an electrical fuel signal having a duration determined by the speed of the engine and the position of a throttle controlled by an operator of the engine.

51 Claims, 63 Drawing Figures

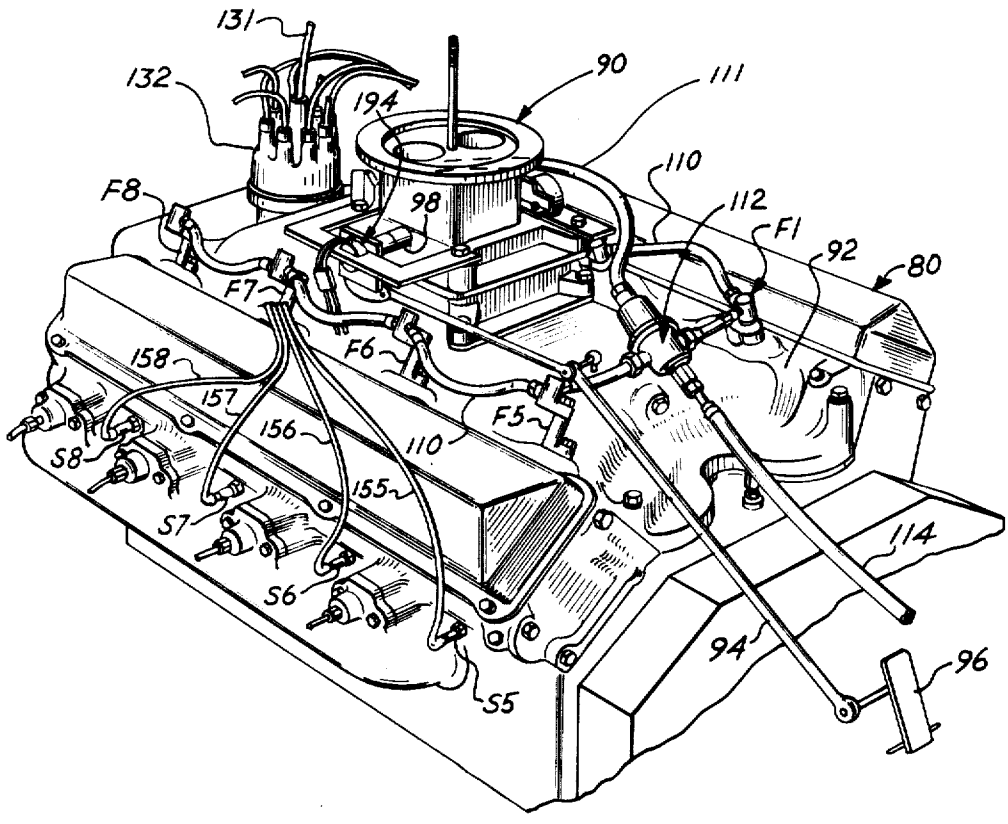


Fig. 1

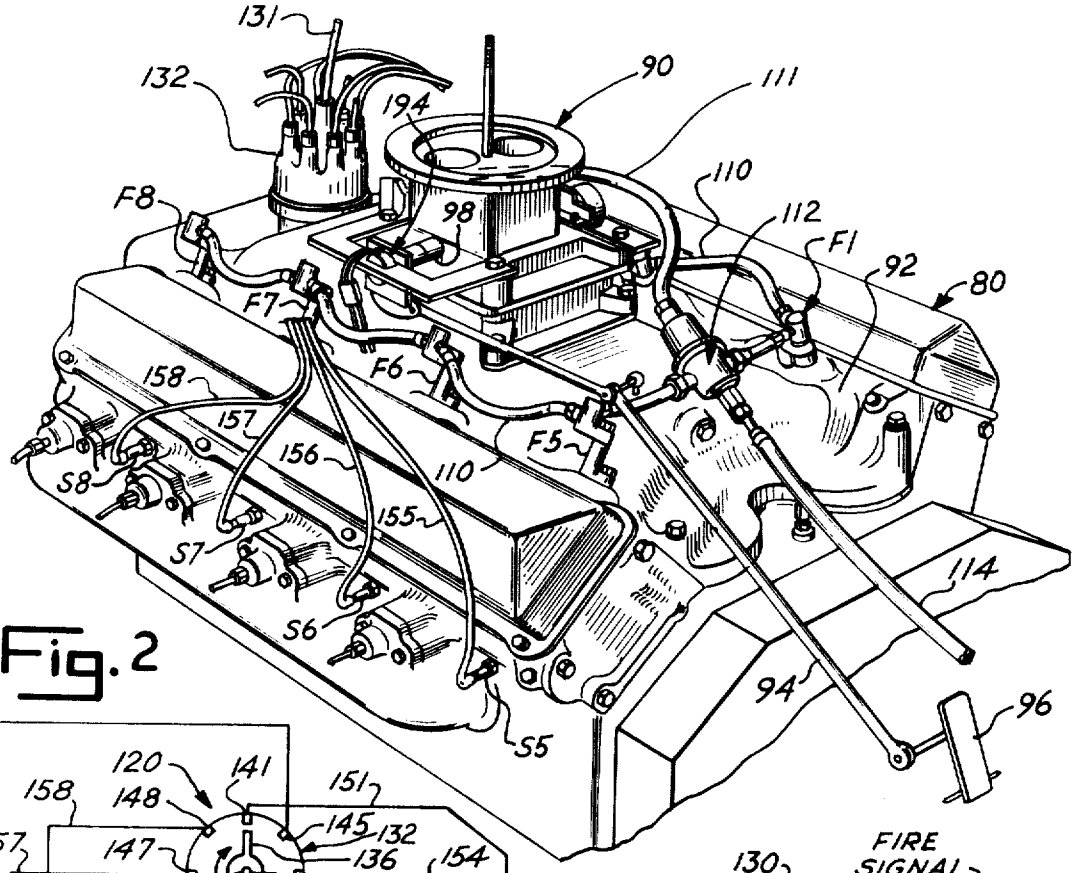
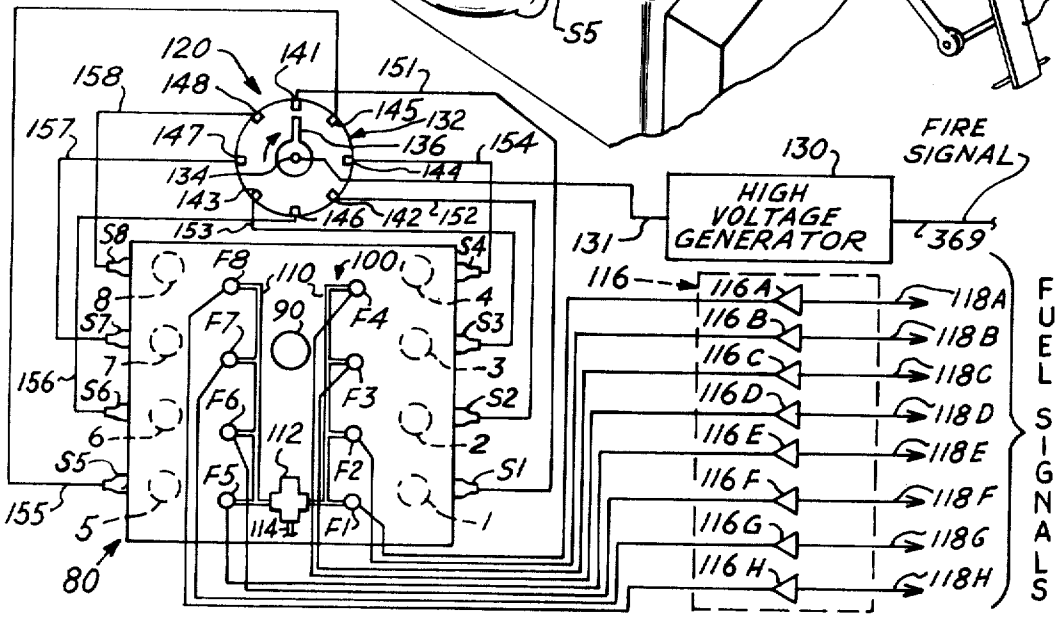

131
132
194
90
111
110
112
F1
92
80
F8
98
F7
F6
158
157
156
F5
110
S8
155
S7
S6
114
94
96
S5

Fig. 2


120
141
151
158
148
145
132
157
147
136
154
134
144
143
146
142
152
153
S8
S4
F8
110
100
8
4
S7
90
F4
S3
7
3
156
S6
F6
F3
S2
6
112
2
S5
F5
F2
S1
155
5
114
F1
1
80
130
FIRE SIGNAL
HIGH VOLTAGE GENERATOR
131
369
116
116A
116B
116C
116D
116E
116F
116G
116H
118A
118B
118C
118D
118E
118F
118G
118H
FUEL SIGNALS

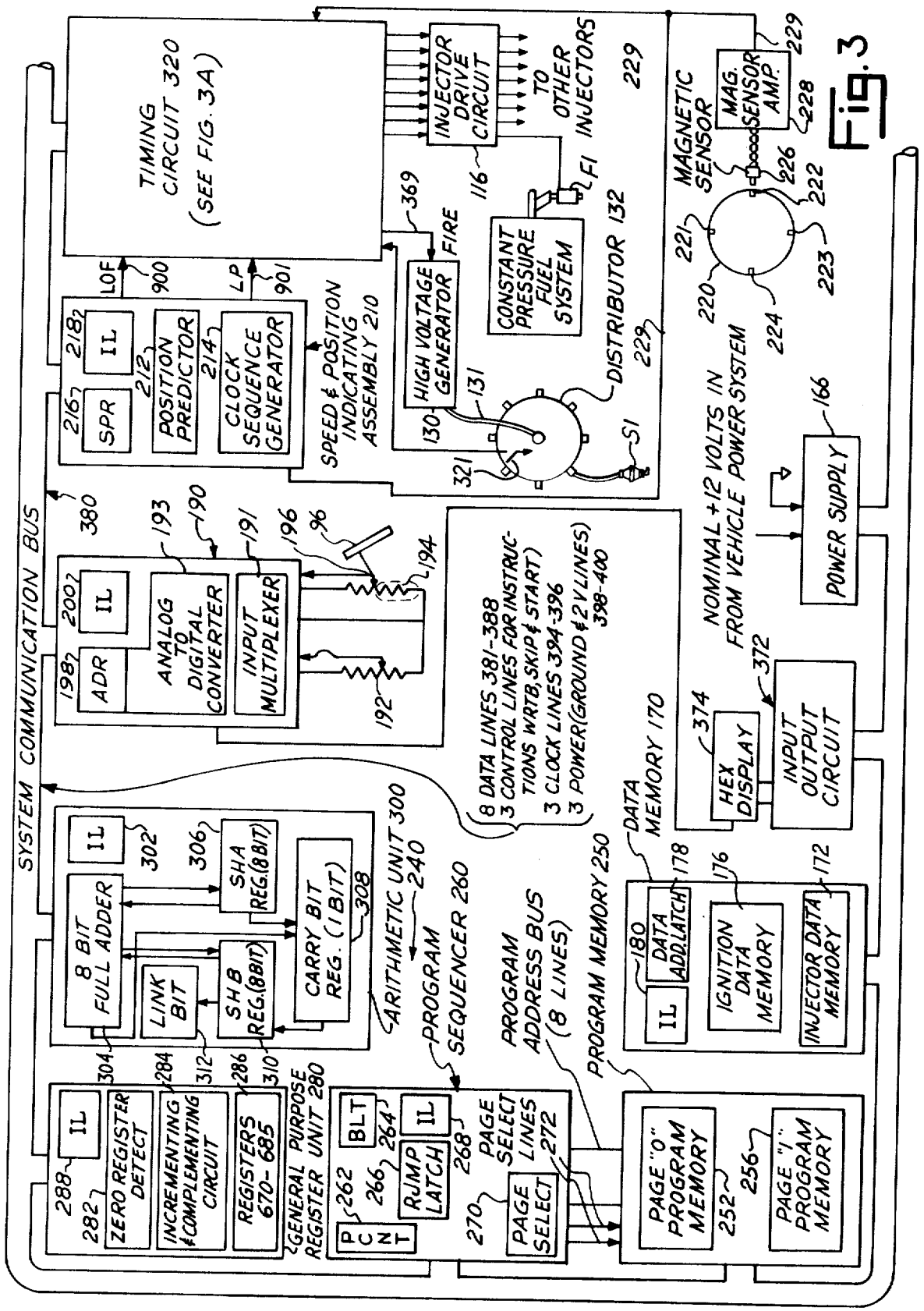

SYSTEM COMMUNICATION BUS
TIMING CIRCUIT 320 (SEE FIG. 3A)
INJECTOR DRIVE CIRCUIT
TO OTHER INJECTORS
MAGNETIC SENSOR
MAG. SENSOR AMP.
SPEED & POSITION INDICATING ASSEMBLY 210
HIGH VOLTAGE GENERATOR
CONSTANT PRESSURE FUEL SYSTEM
DISTRIBUTOR 132
NOMINAL +12 VOLTS IN FROM VEHICLE POWER SYSTEM
POWER SUPPLY
ANALOG TO DIGITAL CONVERTER
INPUT MULTIPLEXER
8 DATA LINES 381-388
3 CONTROL LINES FOR INSTRUCTIONS WRTB, SKIP & START)
3 CLOCK LINES 394-396
3 POWER(GROUND & 2 V LINES) 398-400
8 BIT FULL ADDER
LINK BIT
SHB REG.(8 BIT)
SHA REG.(8 BIT)
CARRY BIT REG. (1 BIT)
ARITHMETIC UNIT 300
PROGRAM SEQUENCER 260
PROGRAM ADDRESS BUS (8 LINES)
PROGRAM MEMORY 250
DATA MEMORY 170
DATA ADD. LATCH
IGNITION DATA MEMORY
INJECTOR DATA MEMORY
HEX DISPLAY
INPUT OUTPUT CIRCUIT
GENERAL PURPOSE REGISTER UNIT 280
ZERO REGISTER DETECT
INCREMENTING & COMPLEMENTING CIRCUIT
REGISTERS 670-685
PCNT
RJMP LATCH
PAGE SELECT
PAGE SELECT LINES 272
PAGE "0" PROGRAM MEMORY
PAGE "1" PROGRAM MEMORY
SPR
POSITION PREDICTOR 214
CLOCK SEQUENCE GENERATOR
ADR
IL
BLT

Fig. 3

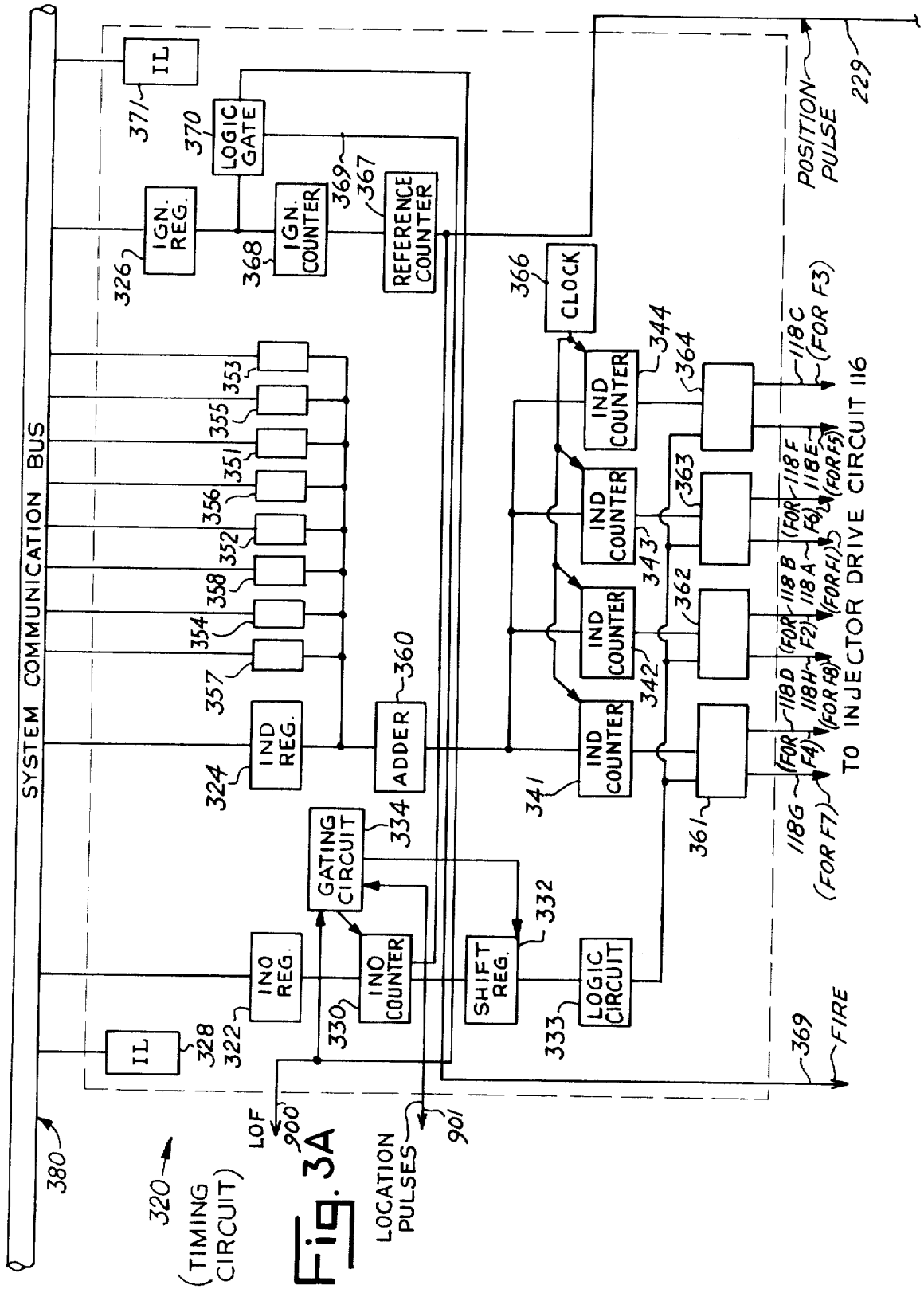

SYSTEM COMMUNICATION BUS
380
320
(TIMING CIRCUIT)
IL
328
322
INO REG.
330
INO COUNTER
LOF
900
LOCATION PULSES
901
GATING CIRCUIT
334
IND REG.
324
ADDER
360
357
354
358
352
356
351
355
353
SHIFT REG.
332
LOGIC CIRCUIT
333
IL
371
LOGIC GATE
370
IGN. REG.
326
IGN. COUNTER
368
369
REFERENCE COUNTER
367
CLOCK
366
POSITION PULSE
229
IND COUNTER
341
342
343
344
361
362
363
364
118G (FOR F7)
118D (FOR F4)
118H (FOR F8)
118B (FOR F2)
118A (FOR F1)
118F (FOR F6)
118E (FOR F5)
118C (FOR F3)
TO INJECTOR DRIVE CIRCUIT 116
369
FIRE

Fig. 3A

Fig. 4 INJECTION MAP

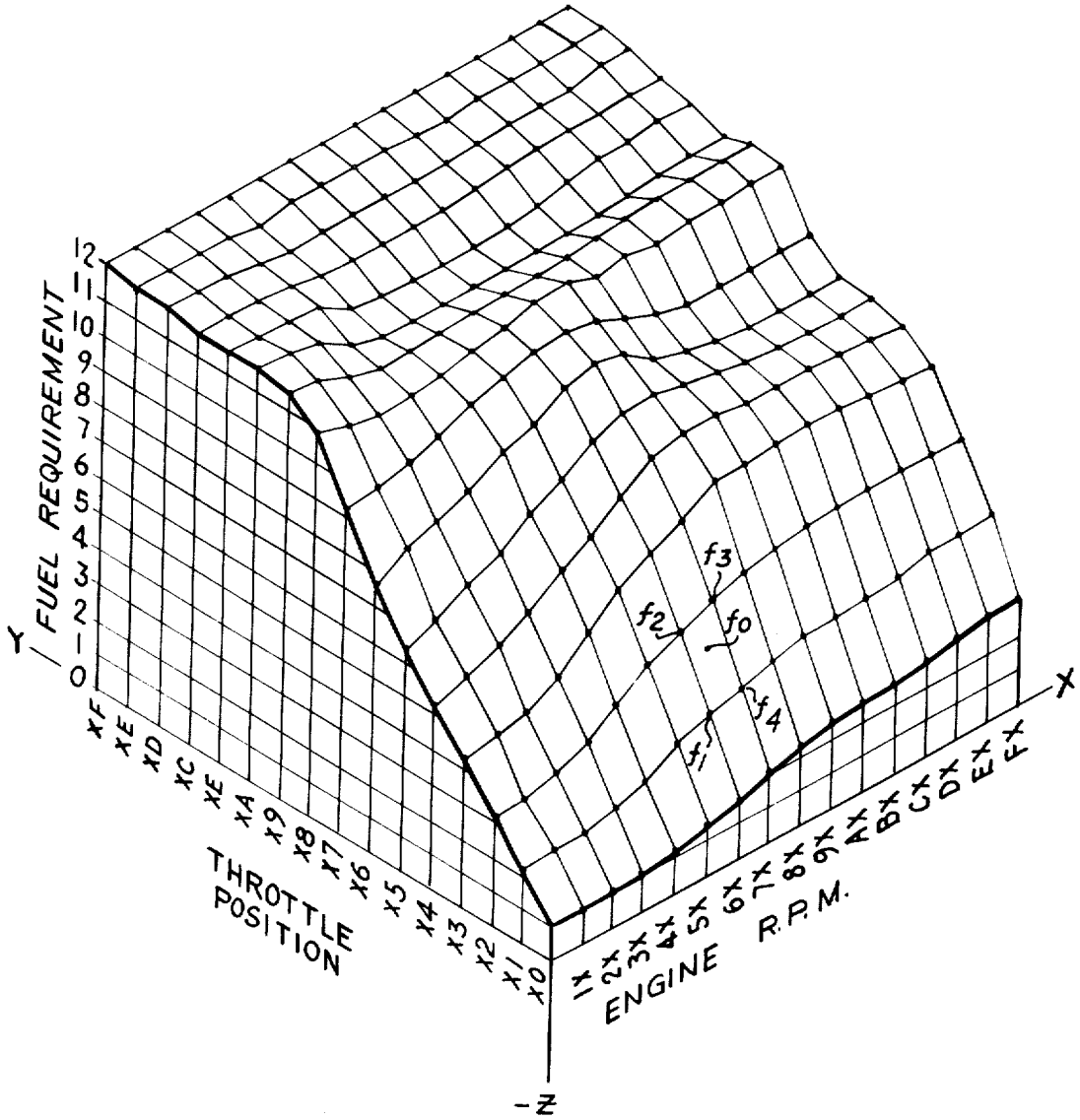


Fig. 5

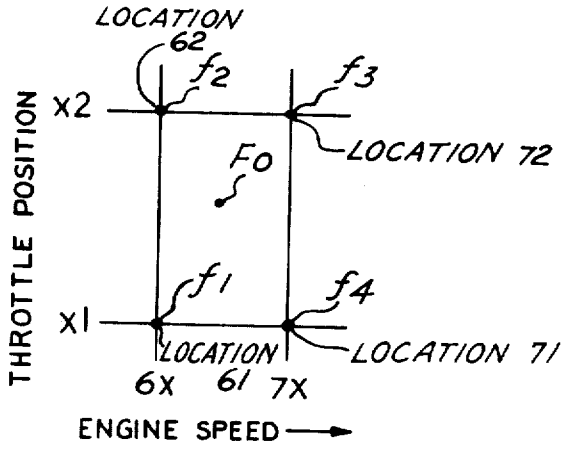

LOCATION
62
f2
f3
X2
LOCATION 72
Fo
f1
f4
X1
LOCATION
LOCATION 71
6X 61 7X
THROTTLE POSITION
ENGINE SPEED

Fig. 6

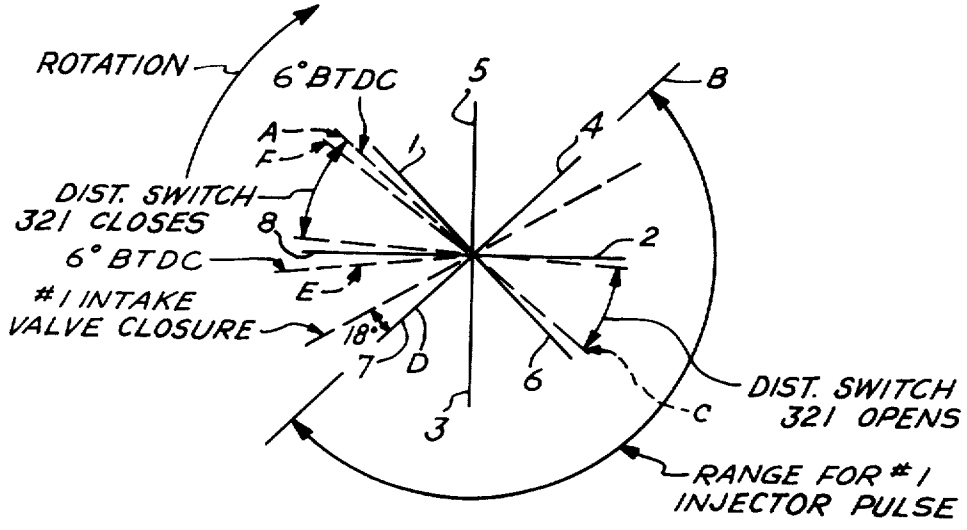

ROTATION
6°BTDC
5
B
A
F
1
4
DIST. SWITCH
321 CLOSES
8
2
6°BTDC
E
#1 INTAKE
VALVE CLOSURE
18°
7
D
6
DIST. SWITCH
321 OPENS
C
3
RANGE FOR #1
INJECTOR PULSE

Fig. 11

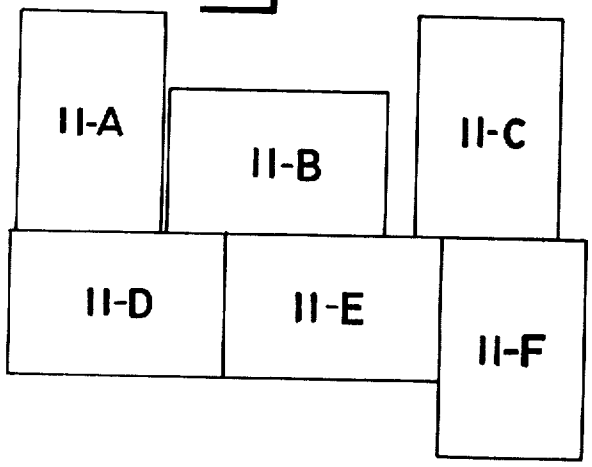


Fig. 8

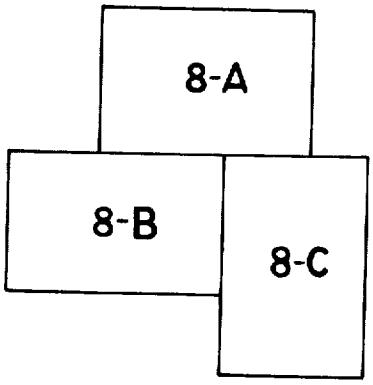


Fig. 12

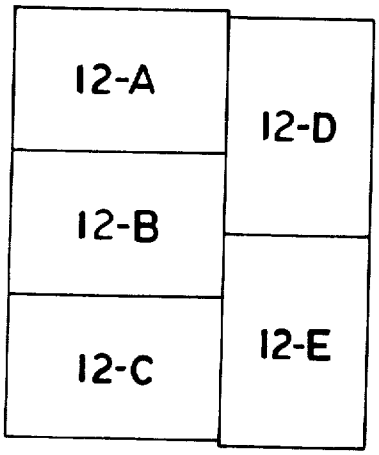


Fig. 7

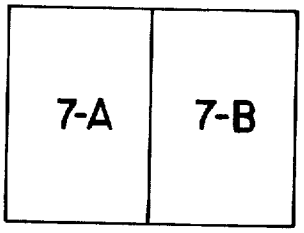


Fig. 10

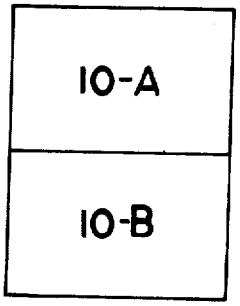
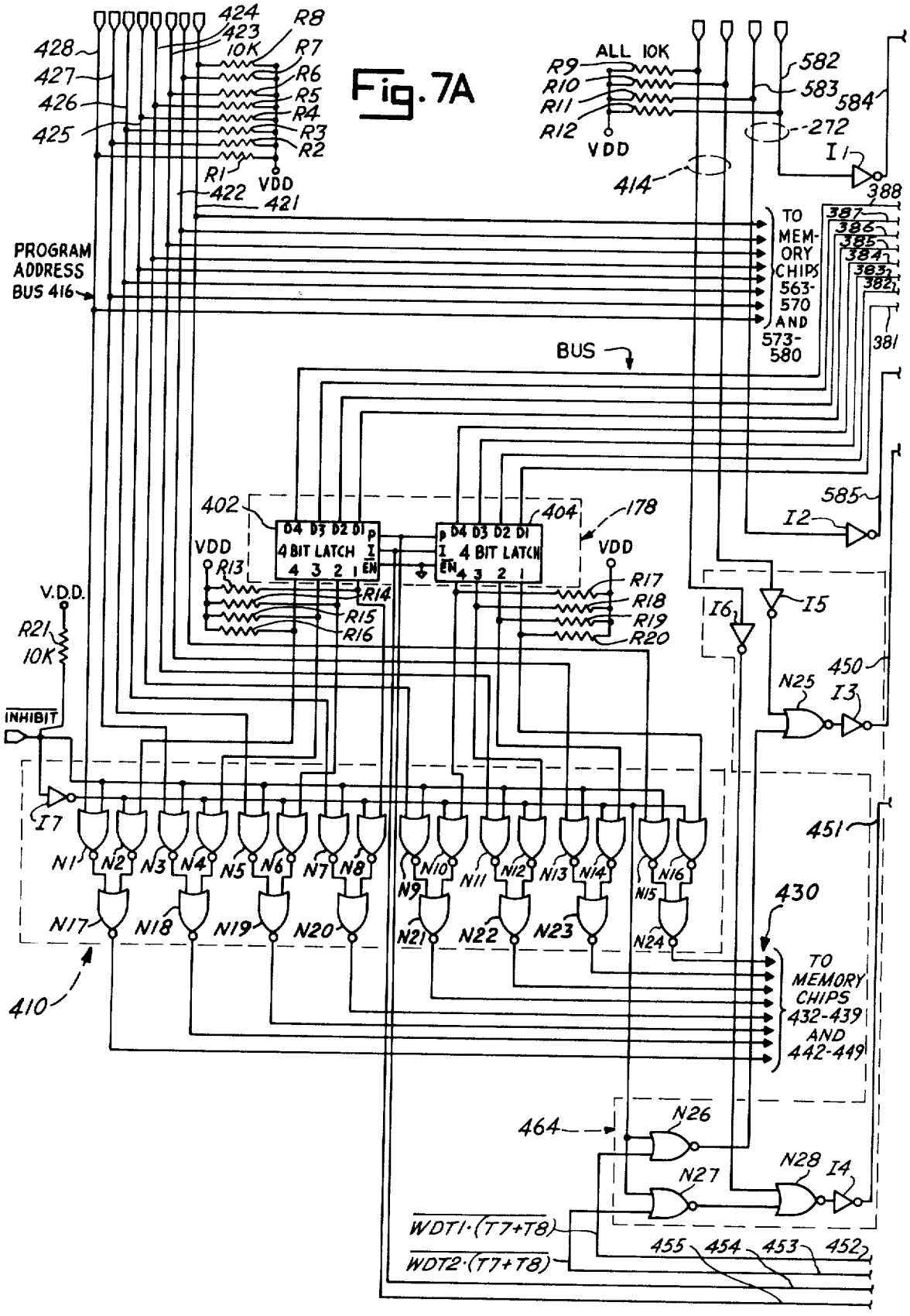


Fig. 7A


424
423
428
427
426
425
10K
R8
R7
R6
R5
R4
R3
R2
R1
VDD
422
421
PROGRAM ADDRESS BUS 416
ALL 10K
R9
R10
R11
R12
VDD
582
583
584
272
I1
414
388
387
386
385
384
383
382
381
TO MEMORY CHIPS 563-570 AND 573-580
BUS
585
I2
402
404
178
D4 D3 D2 D1
4 BIT LATCH
VDD
R13
R14
R15
R16
R17
R18
R19
R20
I6
I5
V.D.D.
R21
10K
450
N25
I3
INHIBIT
I7
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N13
N14
N15
N16
N17
N18
N19
N20
N21
N22
N23
N24
451
430
410
TO MEMORY CHIPS 432-439 AND 442-449
464
N26
N27
N28
I4
WDT1·(T7+T8)
WDT2·(T7+T8)
455
454
453
452

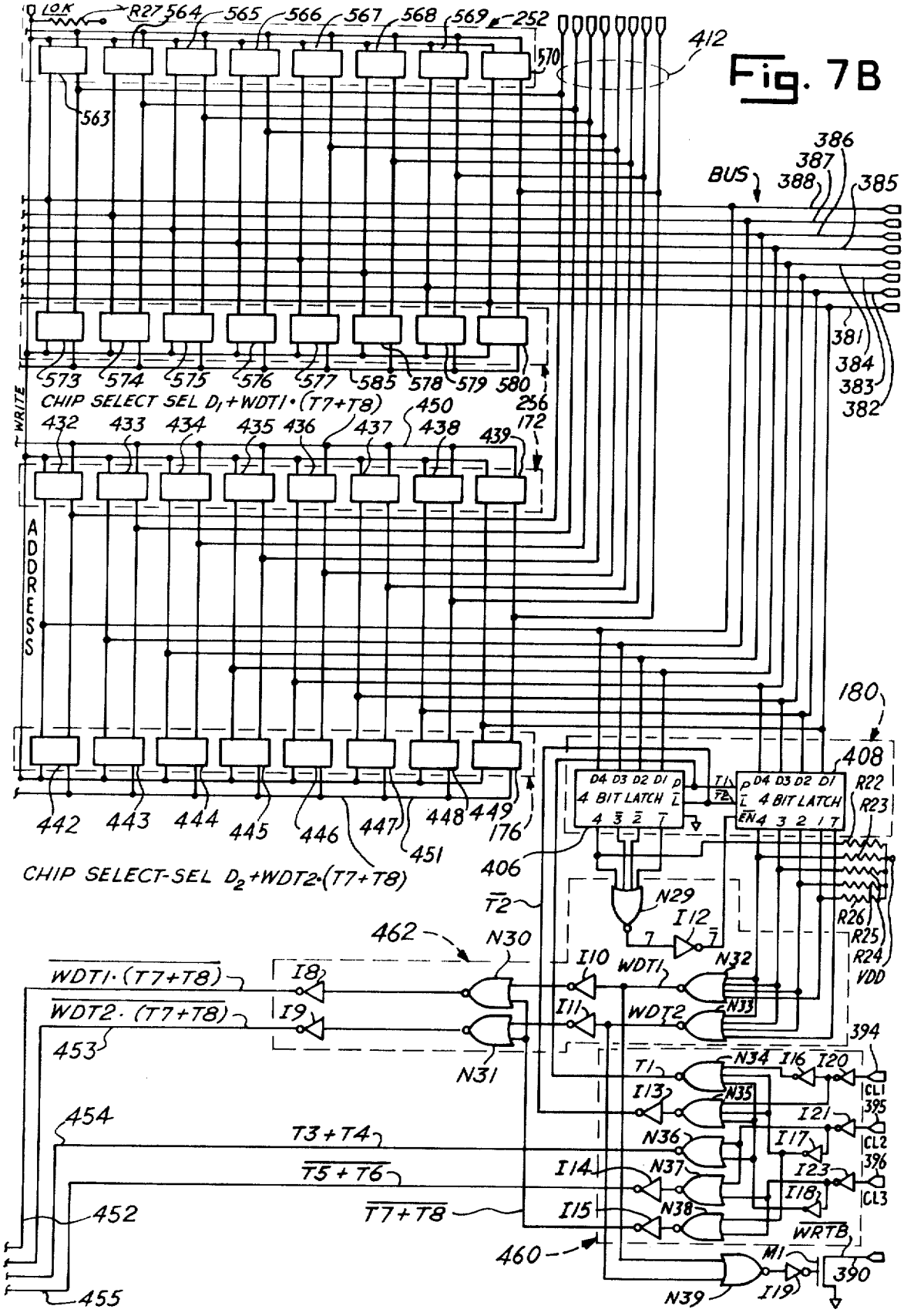

LOK
R27
564
565
566
567
568
569
252
412
570
563
386
387
388
385
BUS
381
384
383
382
573
574
575
576
577
585
578
579
580
256
172
CHIP SELECT SEL D_1+WDT1·(T7+T8)
450
439
T WRITE
ADDRESS
432
433
434
435
436
437
438
442
443
444
445
446
447
448
449
176
451
CHIP SELECT-SEL D_2+WDT2·(T7+T8)
180
408
D4 D3 D2 D1
4 BIT LATCH
R22
R23
R26
R25
R24
VDD
406
$\overline{T2}$
N29
I12
462
N30
WDT1·(T7+T8)
I8
$\overline{WDT2\cdot(T7+T8)}$
I9
453
N31
I10
WDT1
N32
I11
WDT2
N33
394
T1
N34
I16
I20
CL1
395
I13
N35
I21
CL2
396
454
T3+T4
N36
I17
$\overline{T5+T6}$
I14
N37
I23
CL3
I18
452
$\overline{T7+T8}$
I15
N38
WRTB
460
M1
390
455
N39
I19

Fig. 7B

Fig. 7C

INST	CODE	BUS 87654321
WDT1	70	01110000
WDT2	71	01110001

Fig. 8D

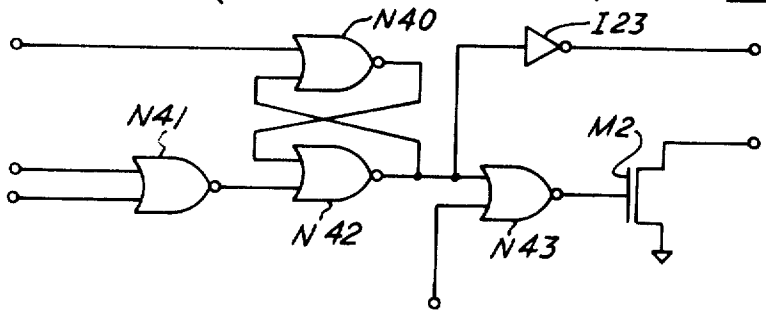
INST	CODE	BUS 87654321
CONV	80	10000000
WRAD	81	10000001
SEN0	82	10000010
SEN1	83	10000011
SEN2	84	10000100
SEN3	85	10000101
SBT0	86	10000110
SBT1	87	10000111
SBT2	88	10001000
RST0	89	10001001
RST1	8A	10001010
RST2	8B	10001011
SEL3	8C	10001100
SEL2	8D	10001101
SEL1	8E	10001110
SEL0	8F	10001111

Fig. 7D

	CL1	CL2	CL3
T1	0	0	0
T2	1	0	0
T3	1	1	0
T4	1	1	0
T5	0	1	1
T6	1	1	1
T7	1	0	1
T8	0	0	1

BIT LATCHES 402, 404, 406, 408
482, 490, 491, 604-607, 689, 690, 764,
765, 866, 867, 892 & 894
(4 TIMES PER PACKAGE)

Fig. 7E



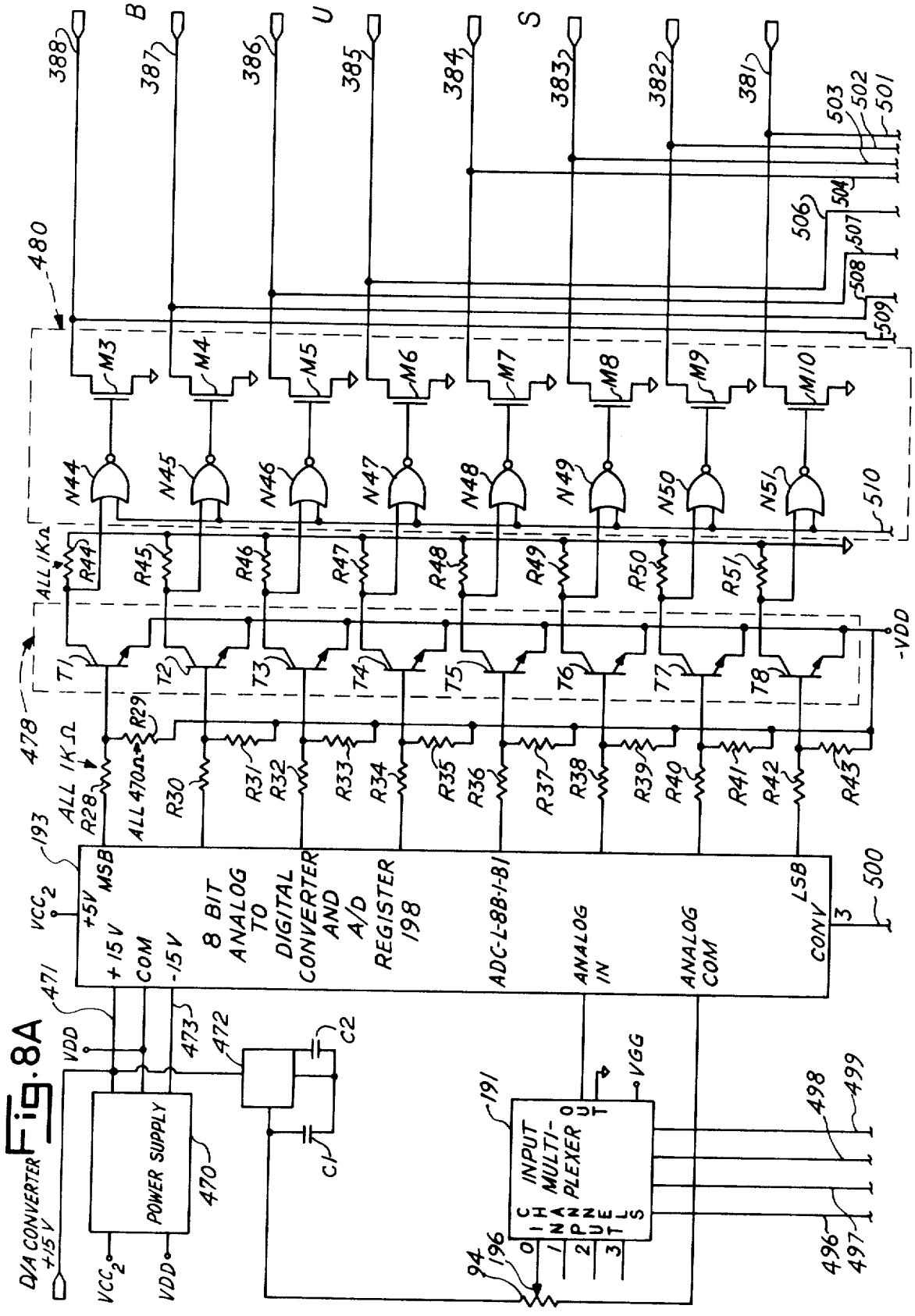

D/A CONVERTER
+15 V
VCC2
VDD
POWER SUPPLY
470
471
VDD
473
472
C2
C1
+5V
+15 V
COM
-15 V
MSB
LSB
8 BIT ANALOG TO DIGITAL CONVERTER AND A/D REGISTER 198
ADC-L-8B-I-BI
ANALOG IN
ANALOG COM
CONV
193
500
478
ALL 1KΩ
ALL 470Ω
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
T1
T2
T3
T4
T5
T6
T7
T8
-VDD
480
ALL 1KΩ
R44
R45
R46
R47
R48
R49
R50
R51
N44
N45
N46
N47
N48
N49
N50
N51
M3
M4
M5
M6
M7
M8
M9
M10
510
388
387
386
385
384
383
382
381
B
U
S
503
502
501
504
506
507
508
509
191
INPUT MULTI-PLEXER
VGG
94
196
498
499
496
497

Fig. 8A

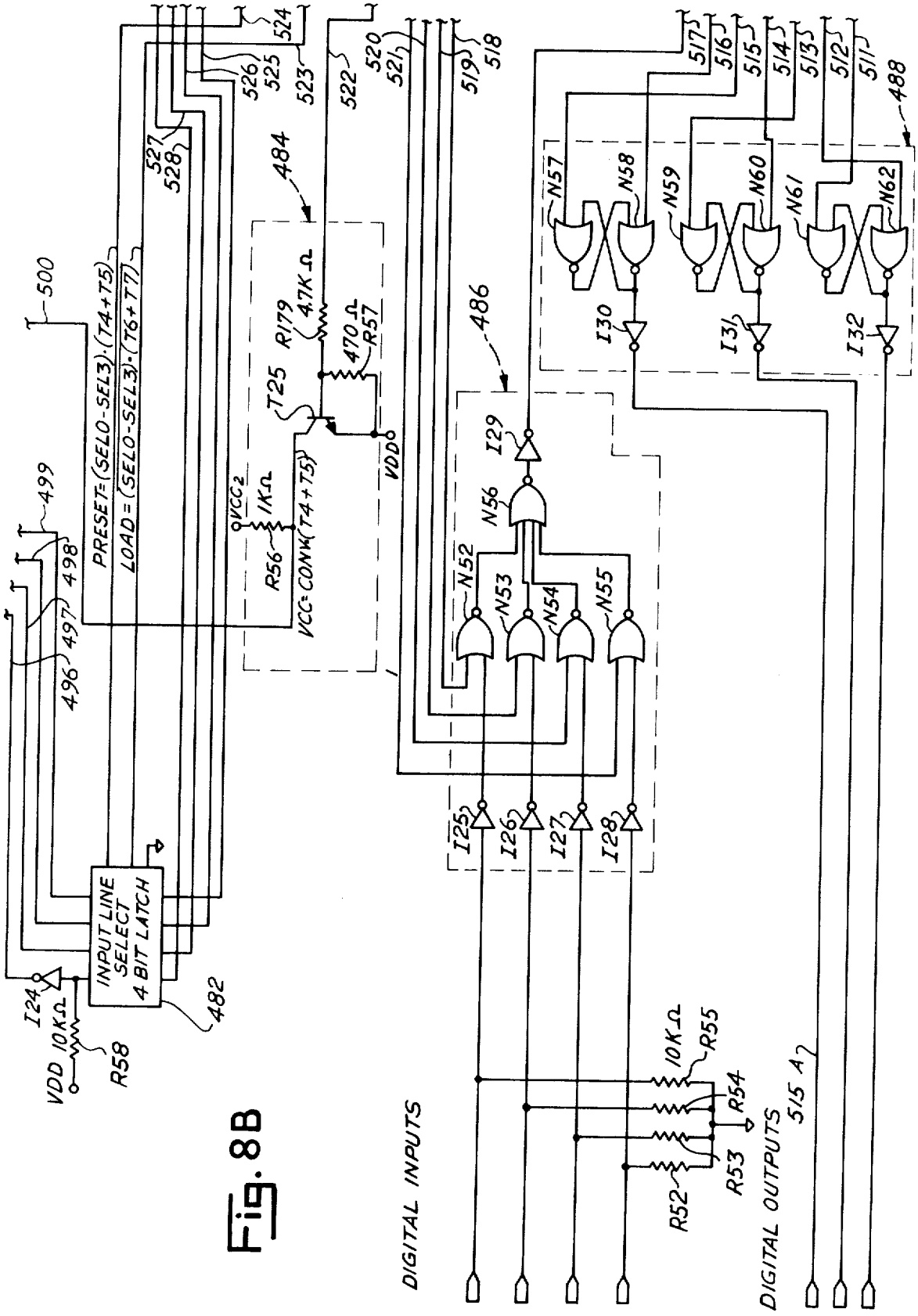

INPUT LINE SELECT 4 BIT LATCH
PRESET=(SEL0-SEL3)·(T4+T5)
LOAD=(SEL0-SEL3)·(T6+T7)
VCC=CONN(T4+T5)
VCC2
VDD
DIGITAL INPUTS
DIGITAL OUTPUTS
R58
R56
R179
R57
R52
R53
R54
R55
T25
I24
I25
I26
I27
I28
I29
I30
I31
I32
N52
N53
N54
N55
N56
N57
N58
N59
N60
N61
N62
482
484
486
488
496
497
498
499
500
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
1K Ω
4.7K Ω
470 Ω
10K Ω
515 A

Fig. 8B

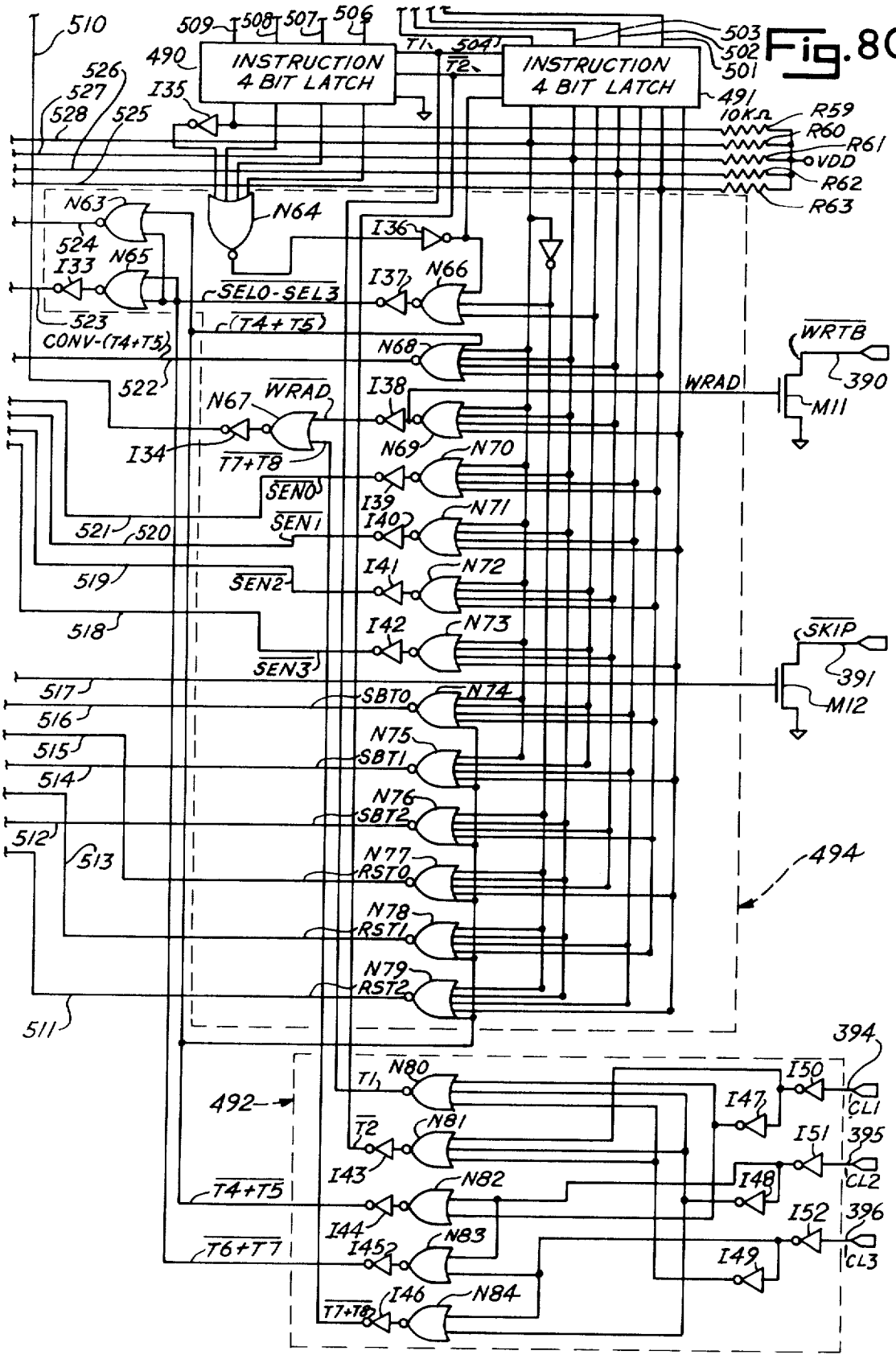

INSTRUCTION 4 BIT LATCH
INSTRUCTION 4 BIT LATCH
490
491
492
494
10KΩ
R59
R60
R61
R62
R63
VDD
WRTB
WRAD
SKIP
M11
M12
390
391
394
395
396
CL1
CL2
CL3
SELO-SEL3
CONV-(T4+T5)
SEN0
SEN1
SEN2
SEN3
SBT0
SBT1
SBT2
RST0
RST1
RST2
N63
N64
N65
N66
N67
N68
N69
N70
N71
N72
N73
N74
N75
N76
N77
N78
N79
N80
N81
N82
N83
N84
I33
I34
I35
I36
I37
I38
I39
I40
I41
I42
I43
I44
I45
I46
I47
I48
I49
I50
I51
I52
T1
T2
T4+T5
T6+T7
T7+T8
501
502
503
504
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528

Fig. 8C

Fig. 9

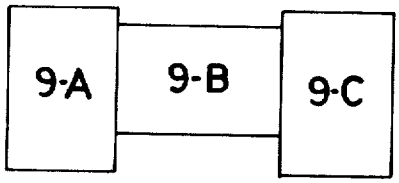

9-A
9-B
9-C

Fig. 9A

CL1
CL2
CL3
394
395
396
I53
M13
I54
VDD
M15
M17
M14
M16
M18
I55
214
N85
N86
I56
I59
I62
I58
I61
I63
I57
I60
D1
D2
D3
VDD VGG
M19
START
I64
553
VGG
VDD
PRECISION CRYSTAL
M22
M20
M21
M23
531
D4
D5
D6
DIVIDE BY FOUR
N87
N88
VGG
VDD
M24
INHIBIT

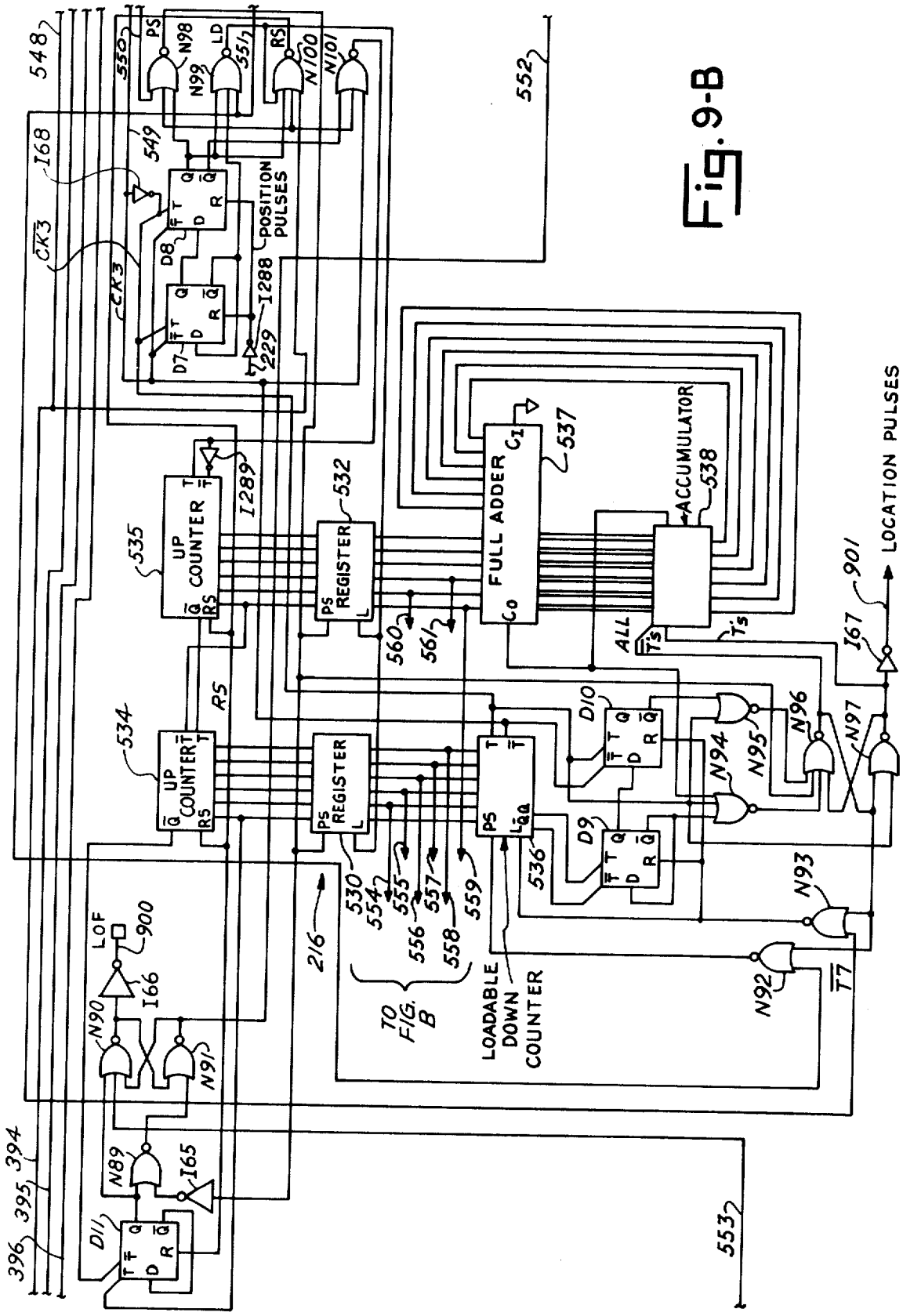

548
530
PS
N98
LD
551
RS
N100
N101
552
549
I68
CK3
CK3
D8
D7
POSITION PULSES
I288
I229
I289
535
UP COUNTER
532
PS REGISTER
537
FULL ADDER
538
ACCUMULATOR
560
561
ALL
Ts
Ts
I67
901
LOCATION PULSES
534
UP COUNTER
RS
PS REGISTER
D10
D9
536
N94
N95
N96
N97
N93
N92
T7
530
542
555
557
559
556
558
216
TO FIG. B
LOADABLE DOWN COUNTER
LOF
900
I66
N90
N91
N89
I65
D11
394
395
396
553

Fig. 9-B

Fig. 9C

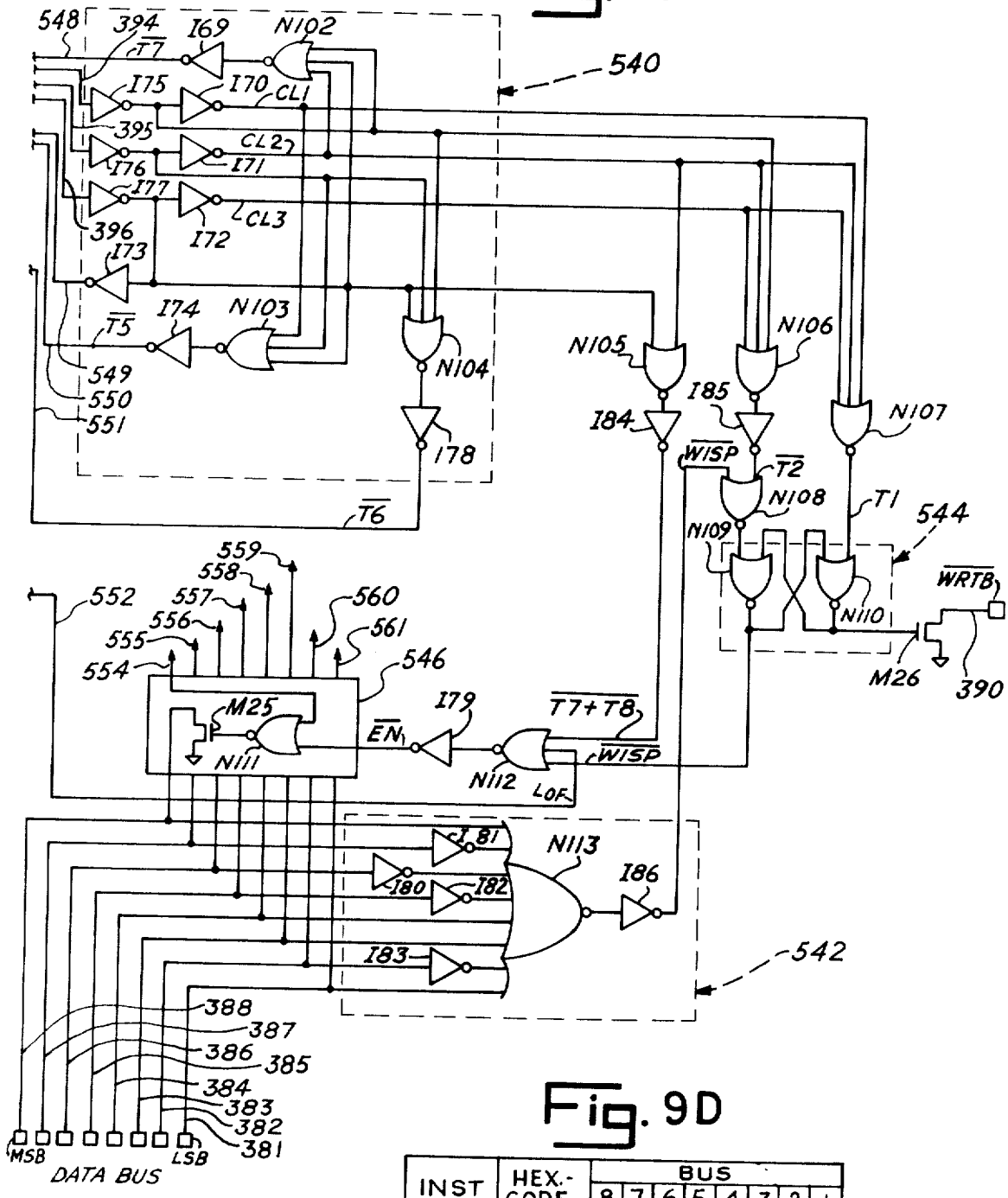


Fig. 9D

INST	HEX.-CODE	BUS 8	7	6	5	4	3	2	1
WISP	72	0	1	1	1	0	0	1	0

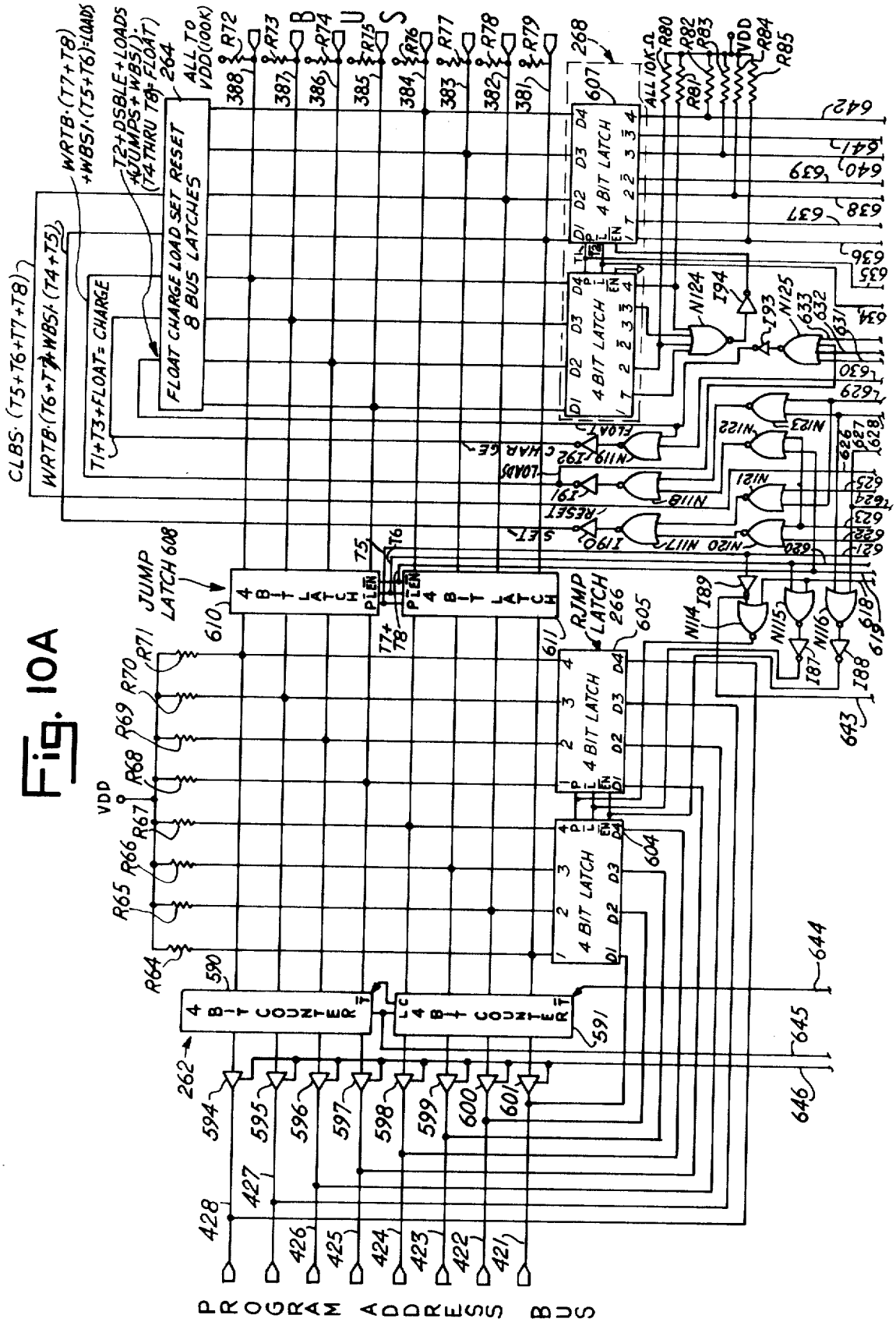

PROGRAM ADDRESS BUS
JUMP LATCH 608
RJMP LATCH 266
4 BIT LATCH
FLOAT CHARGE LOAD SET RESET 8 BUS LATCHES
ALL TO VDD(100K)
VDD
CLBS·(T5+T6+T7+T8)
WRTB·(T6+T7+WBS1·(T4+T5)
WRTB·(T7+T8)+WBS1·(T5+T6)=LOADS
T2+DSBLE+LOADS+JUMPS+WBS1·(T4 THRU T8)=FLOAT
T1+T3+FLOAT=CHARGE

Fig. 10A

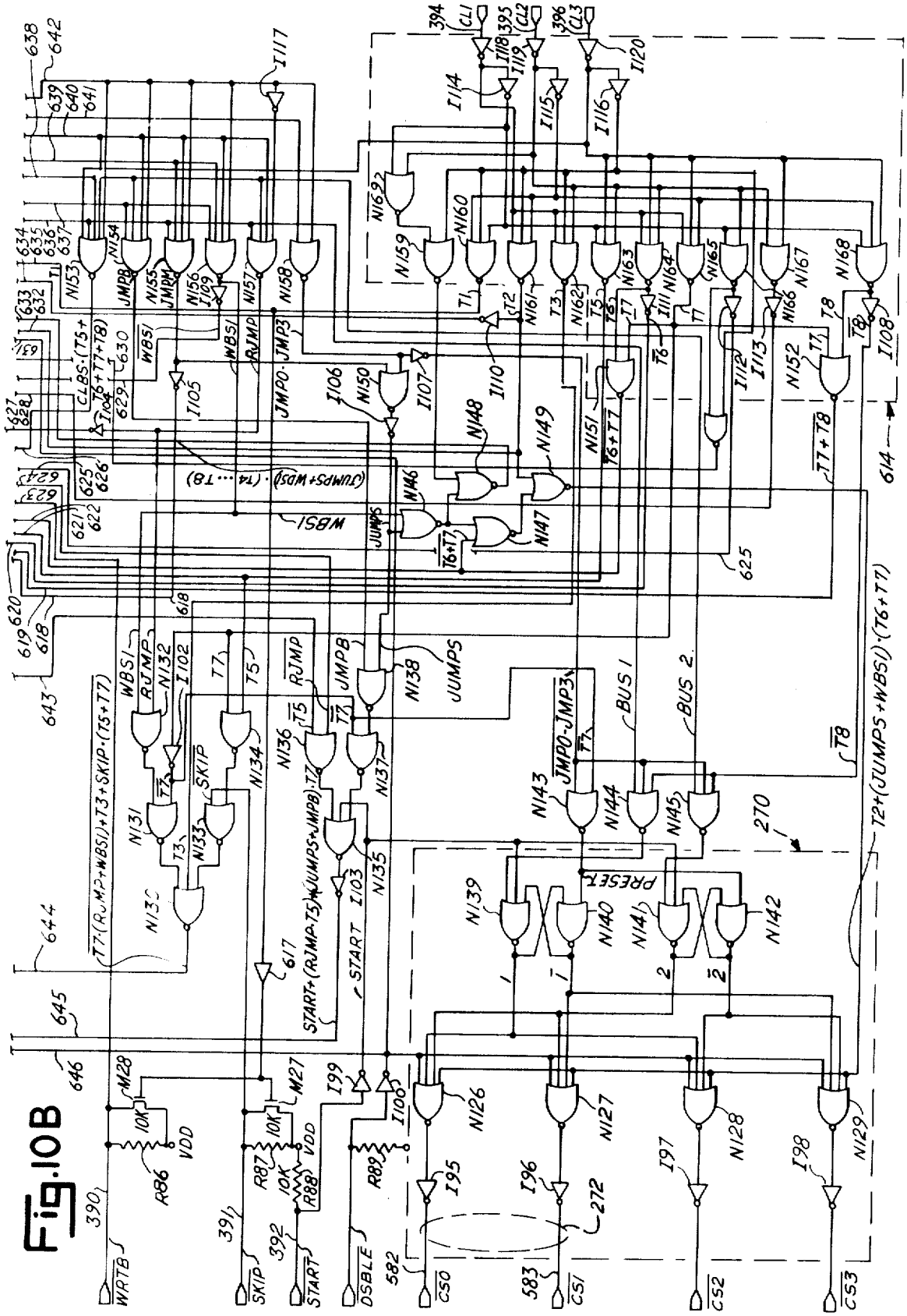


Fig. 10B

Fig. 10C

INST	CODE	BUS 87654321
CLBS	50	01010000
JMPB	51	01010001
JMPM	52	01010010
WBS 1	53	01010011
JMP 0	54	01010100
JMP 1	55	01010101
JMP 2	56	01010110
JMP 3	57	01010111
RJMP	58	01011000

00	CHIP SELECT LATCH
01	
10	
11	

Fig. 10D

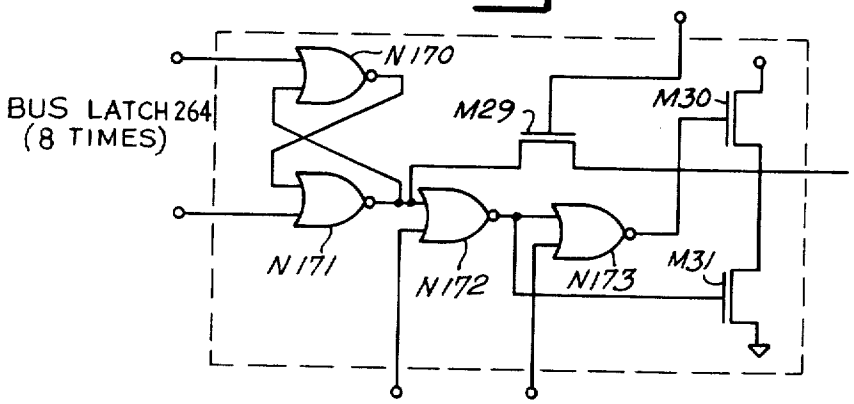
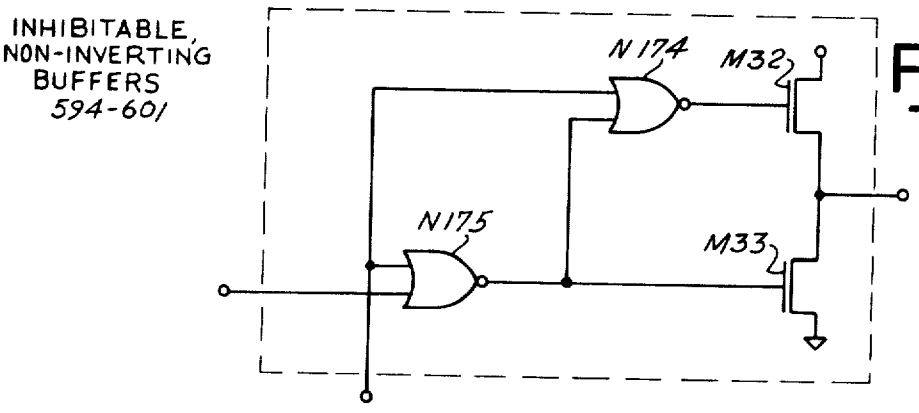


Fig. 10E



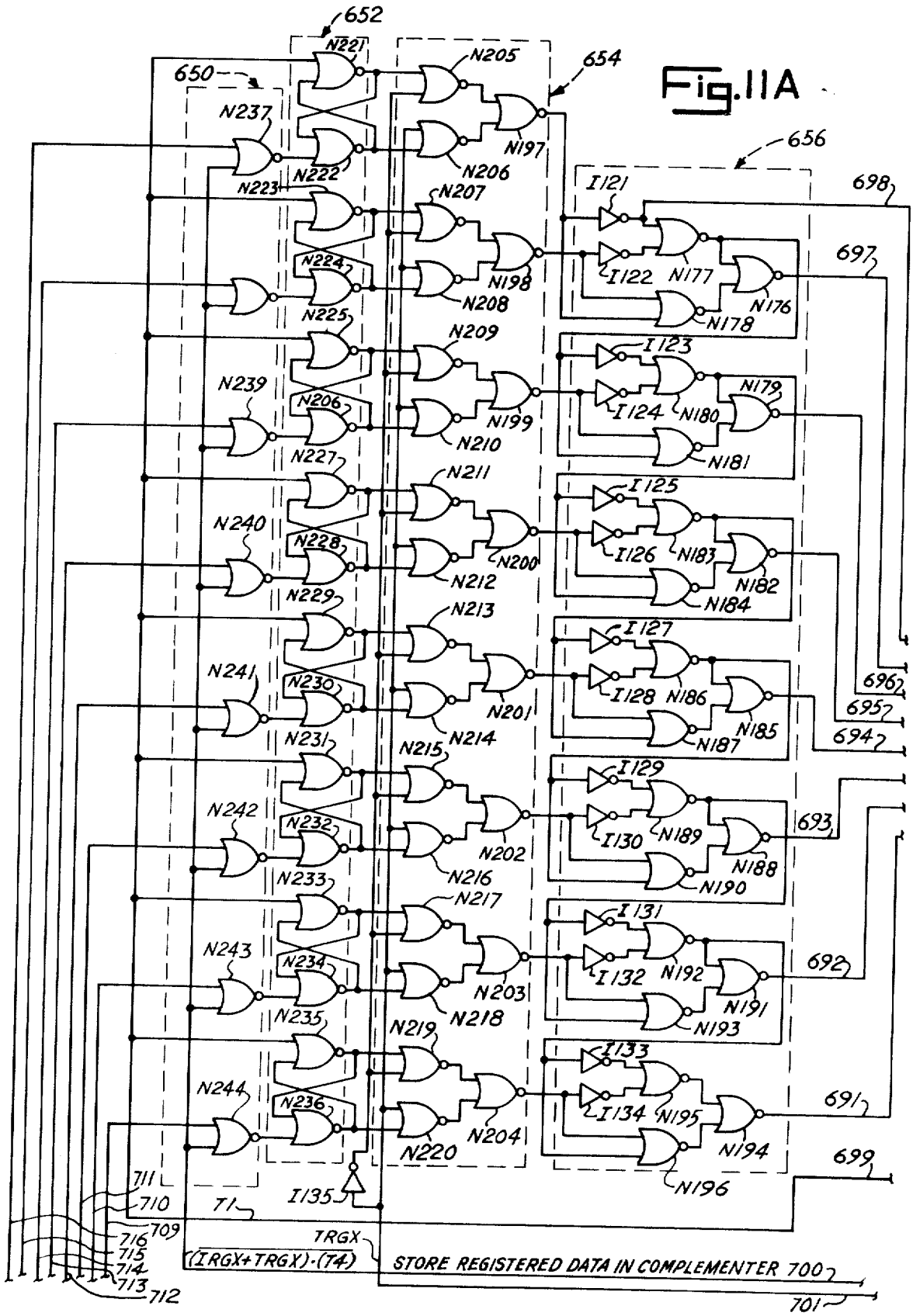

652
650
654
656
N221
N205
N237
N222
N197
N206
N223
N207
N224
N198
N208
N225
N209
N239
N206
N199
N210
N227
N211
N240
N228
N200
N212
N229
N213
N241
N230
N201
N214
N231
N215
N242
N232
N202
N216
N233
N217
N243
N234
N203
N218
N235
N219
N244
N236
N204
N220
I121
I122
N177
N176
N178
698
697
I123
I124
N180
N179
N181
I125
I126
N183
N182
N184
I127
I128
N186
N185
N187
696
695
694
I129
I130
N189
N188
N190
693
I131
I132
N192
N191
N193
692
I133
I134
N195
N194
N196
691
699
711
710
709
716
715
714
713
712
I135
71
TRGX
(IRGX+TRGX)·(74)
STORE REGISTERED DATA IN COMPLEMENTER 700
701

Fig. 11A

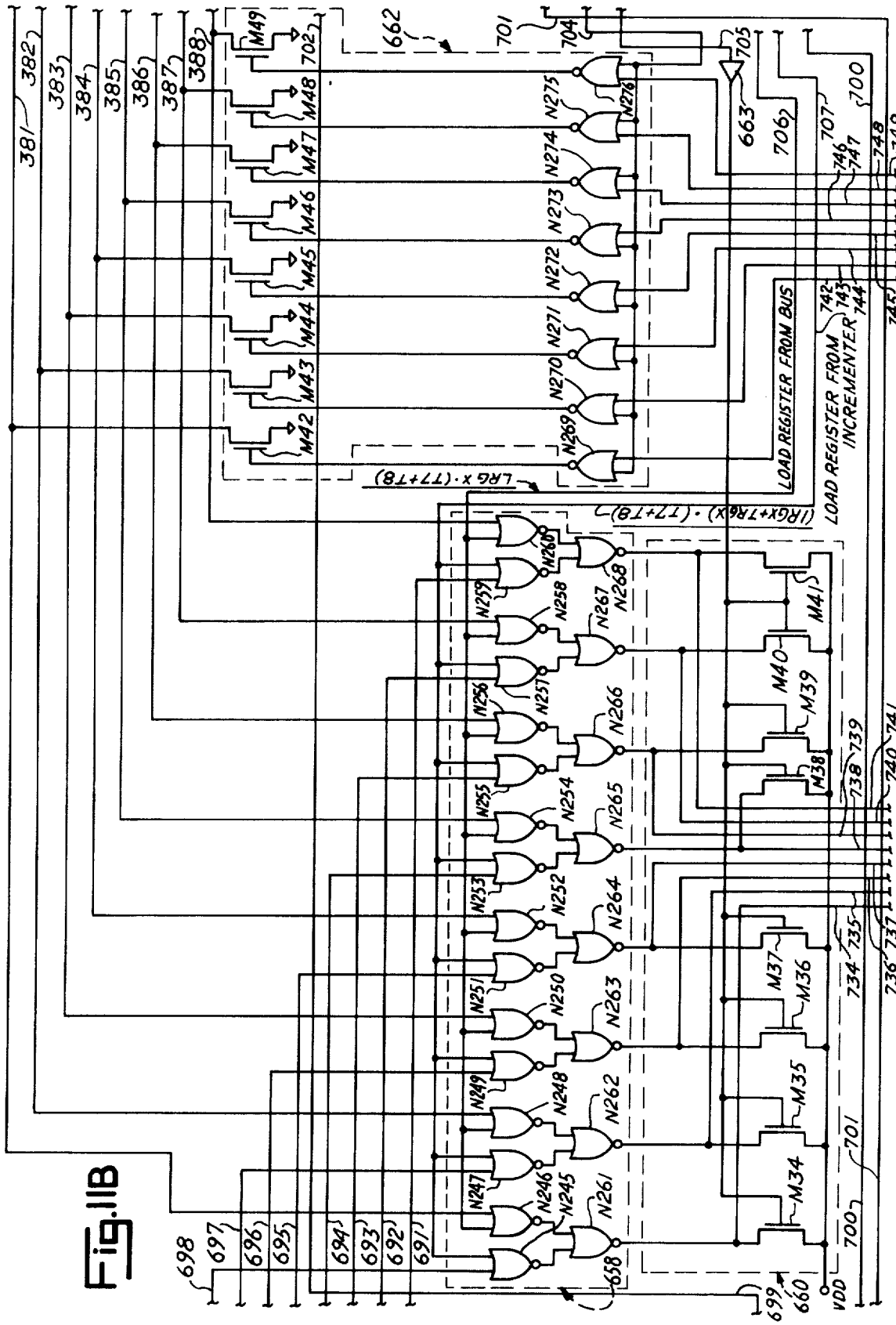

LOAD REGISTER FROM BUS
LOAD REGISTER FROM INCREMENTER
LRG x·(77+78)
(IRGX+TR6X)·(77+78)
VDD

Fig. 11B

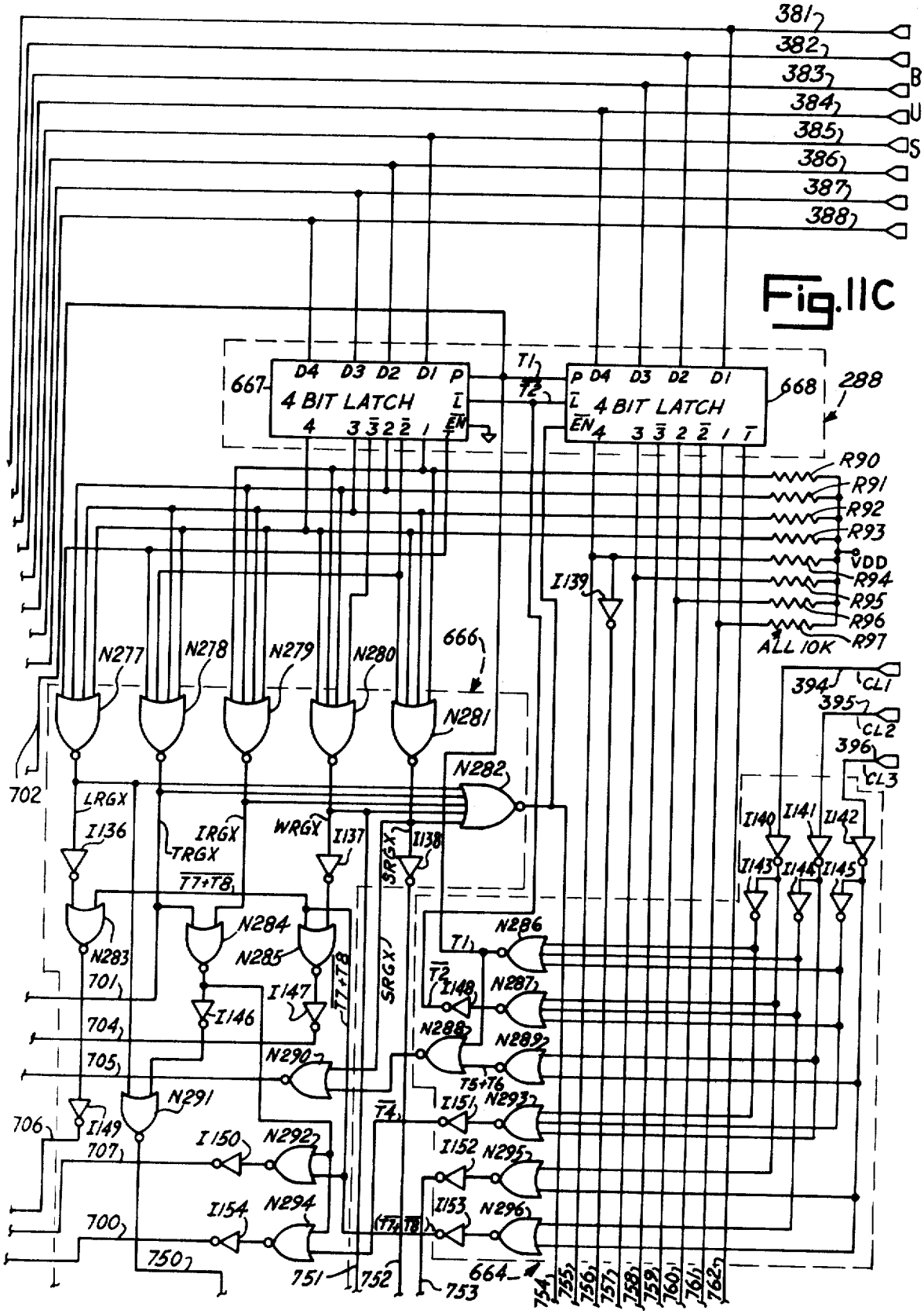

381
382
383
384
385
386
387
388
BUS
667
4 BIT LATCH
D4 D3 D2 D1 P
668
288
R90
R91
R92
R93
VDD
R94
R95
R96
ALL 10K R97
I139
666
N277
N278
N279
N280
N281
N282
702
LRGX
I136
IRGX
TRGX
WRGX
I137
SRGX
I138
N283
N284
N285
701
I146
I147
704
705
N290
N291
706
I149
I150
707
N292
I154
N294
700
750
751
752
753
664
N286
N287
I148
N288
N289
T5+T6
I151
N293
I152
N295
I153
N296
754
755
756
757
758
759
760
761
762
394
395
396
CL1
CL2
CL3
I140
I141
I142
I143
I144
I145

Fig. 11C

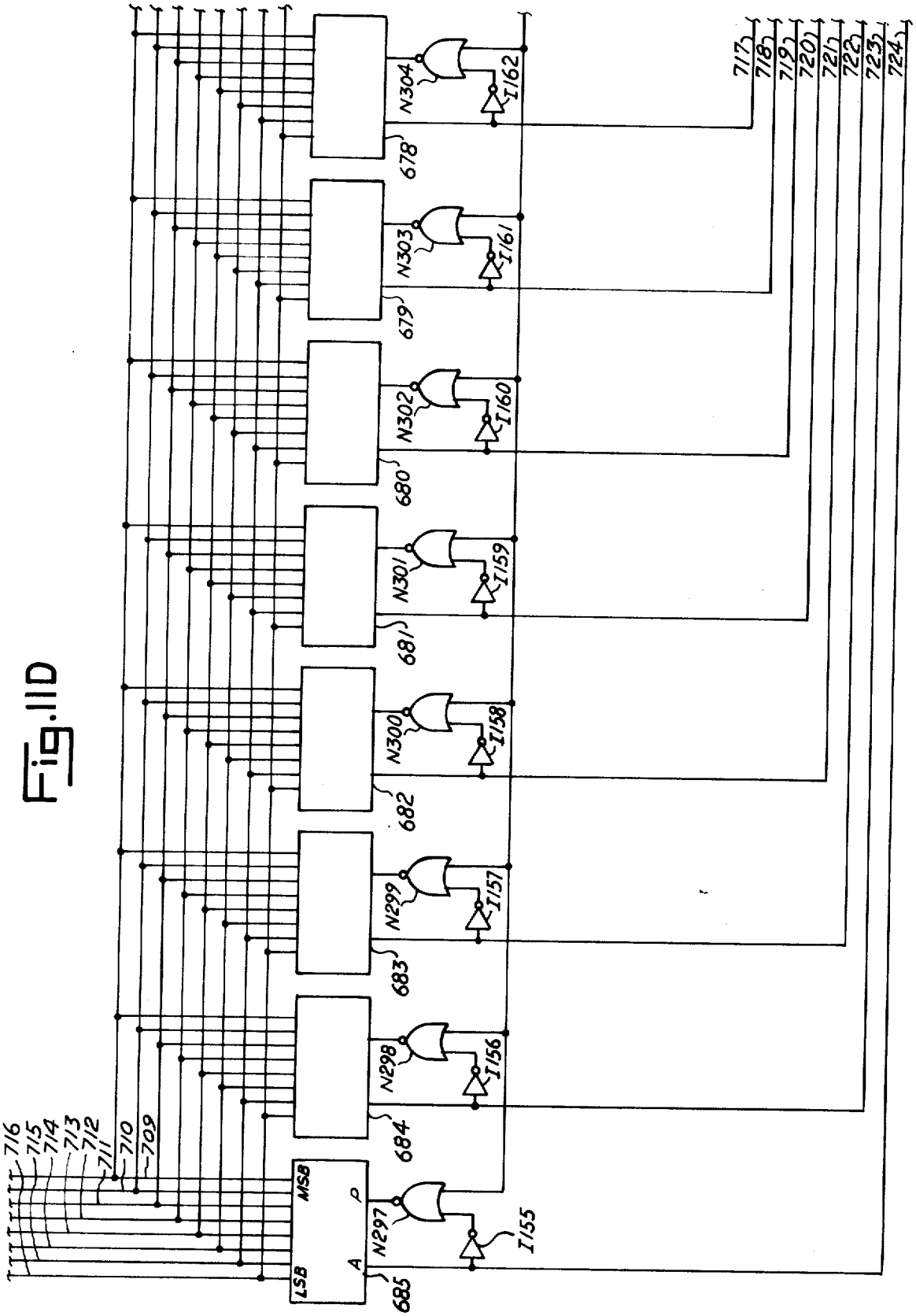

716
715
714
713
712
711
710
709
MSB
LSB
D
A
N297
N298
N299
N300
N301
N302
N303
N304
I155
I156
I157
I158
I159
I160
I161
I162
685
684
683
682
681
680
679
678
717
718
719
720
721
722
723
724

Fig. 11D

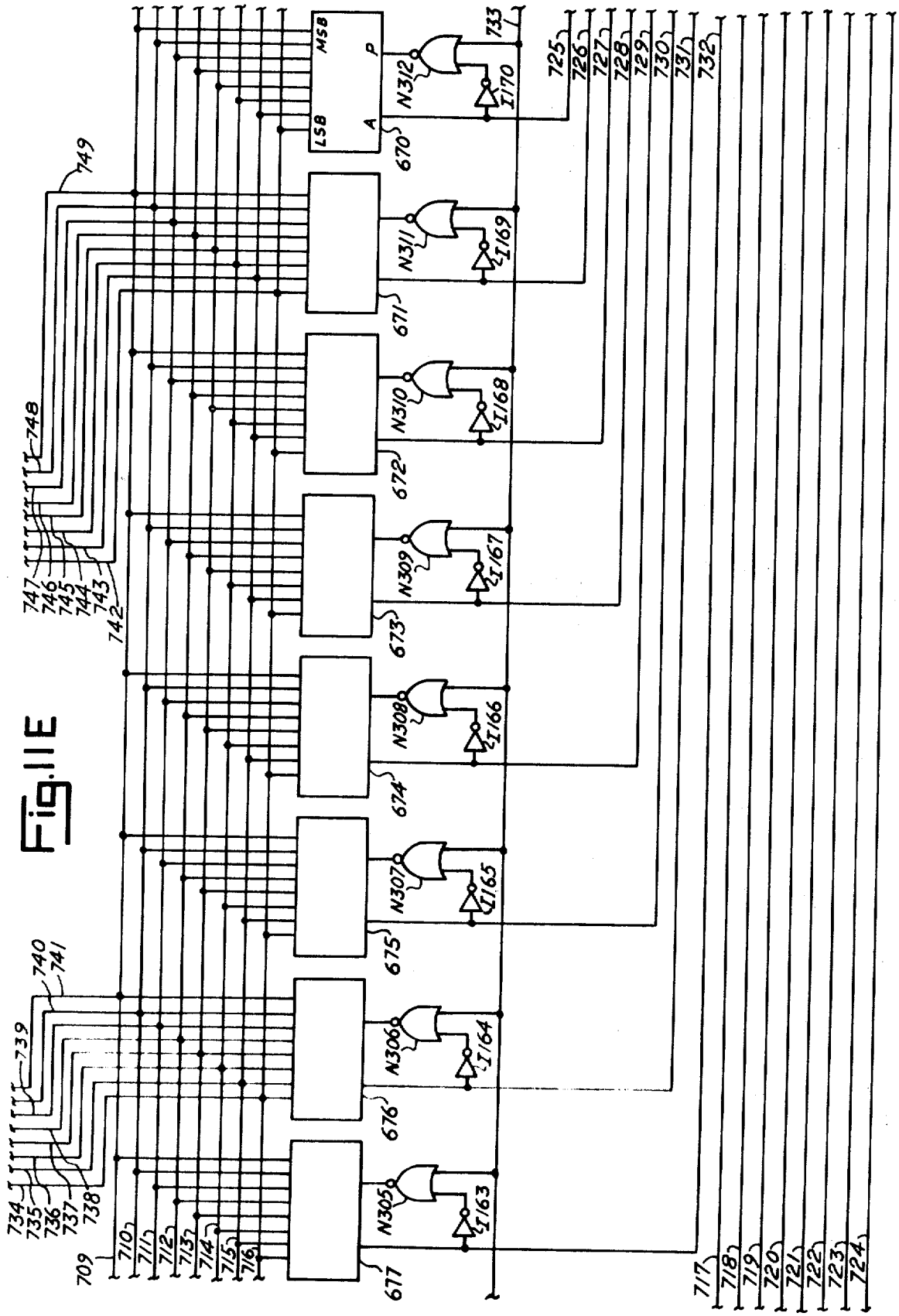

MSB
LSB
P
A
N312
I170
N311
I169
N310
I168
N309
I167
N308
I166
N307
I165
N306
I164
N305
I163
670
671
672
673
674
675
676
677
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749

Fig. 11E

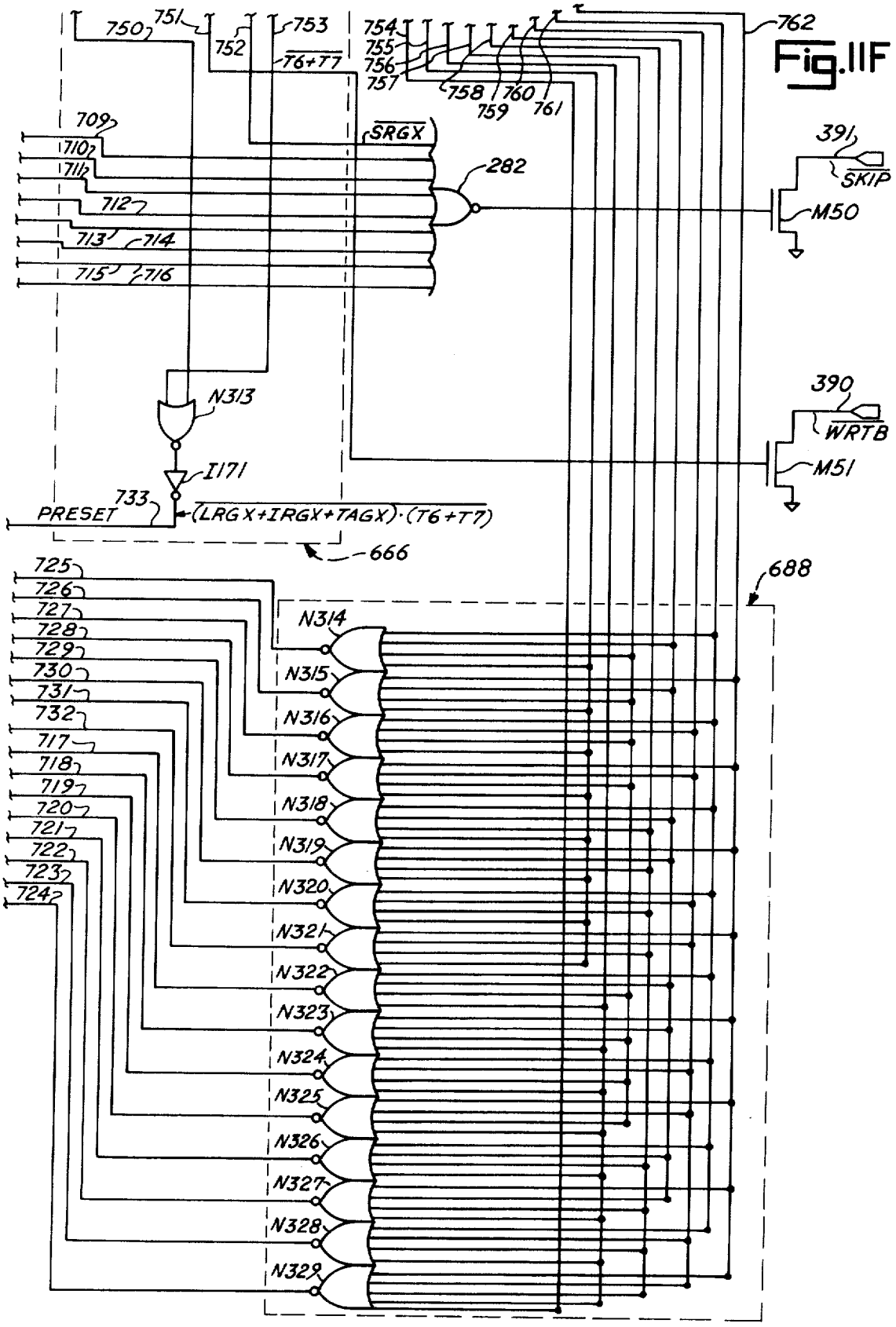
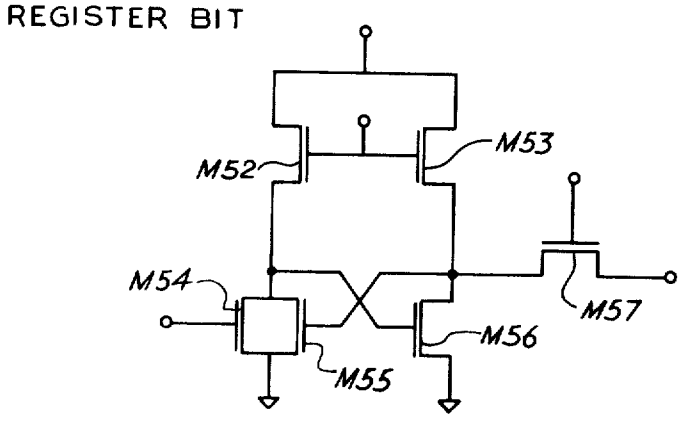

750
751
752
753
T6+T7
754
755
756
757
758
759
760
761
762
709
710
711
712
713
714
715
716
SRGX
282
391
SKIP
M50
390
WRTB
M51
N313
I171
733
PRESET
(LRGX+IRGX+TAGX)·(T6+T7)
666
688
725
726
727
728
729
730
731
732
717
718
719
720
721
722
723
724
N314
N315
N316
N317
N318
N319
N320
N321
N322
N323
N324
N325
N326
N327
N328
N329

Fig. 11F

Fig. 11G

INST	CODE	BUS 87654321
IRGX	0X	0000XXXX
LRGX	1X	0001XXXX
SRGX	2X	0010XXXX
TRGX	3X	0011XXXX
WRGX	4X	0100XXXX

Fig. 11H



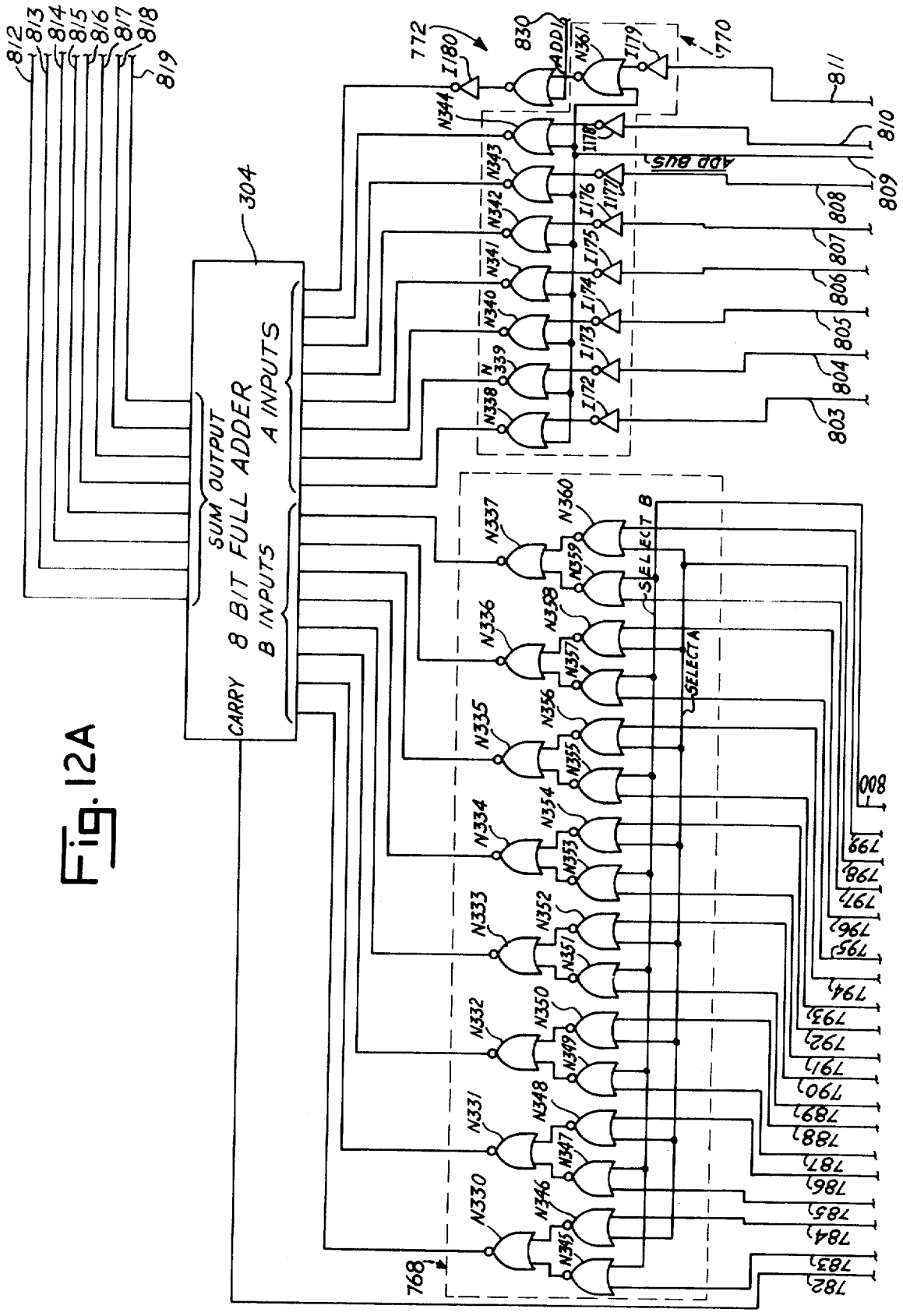

812
813
814
815
816
817
818
819
304
8 BIT FULL ADDER
A INPUTS
B INPUTS
SUM OUTPUT
CARRY
772
I180
830
ADD/4
N361
I179
770
811
810
ADD BUS
809
808
807
806
805
804
803
N344
N343
N342
N341
N340
N339
N338
I178
I177
I176
I175
I174
I173
I172
N337
N360
N359
N336
N358
N357
N335
N356
N355
N334
N354
N353
N333
N352
N351
N332
N350
N349
N331
N348
N347
N330
N346
N345
SELECT B
SELECT A
768
800
799
798
797
796
795
794
793
792
791
790
789
788
787
786
785
784
783
782

Fig. 12A

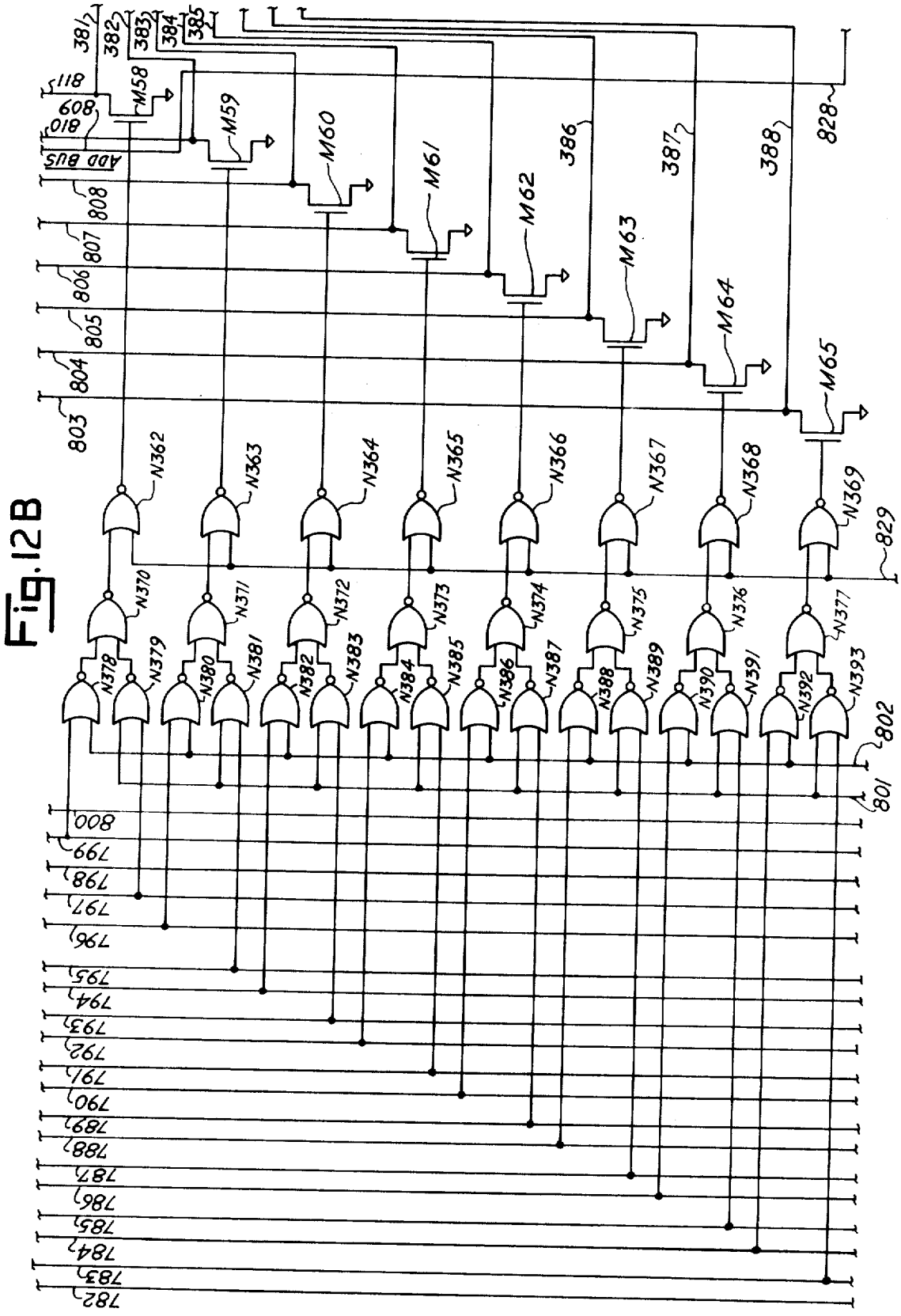

381
382
383
384
385
386
387
388
828
118
809
810
ADD BUS
808
807
806
805
804
803
M58
M59
M60
M61
M62
M63
M64
M65
N362
N363
N364
N365
N366
N367
N368
N369
829
N370
N371
N372
N373
N374
N375
N376
N377
N378
N379
N380
N381
N382
N383
N384
N385
N386
N387
N388
N389
N390
N391
N392
N393
802
801
800
799
798
797
796
795
794
793
792
791
790
789
788
787
786
785
784
783
782

Fig. 12B

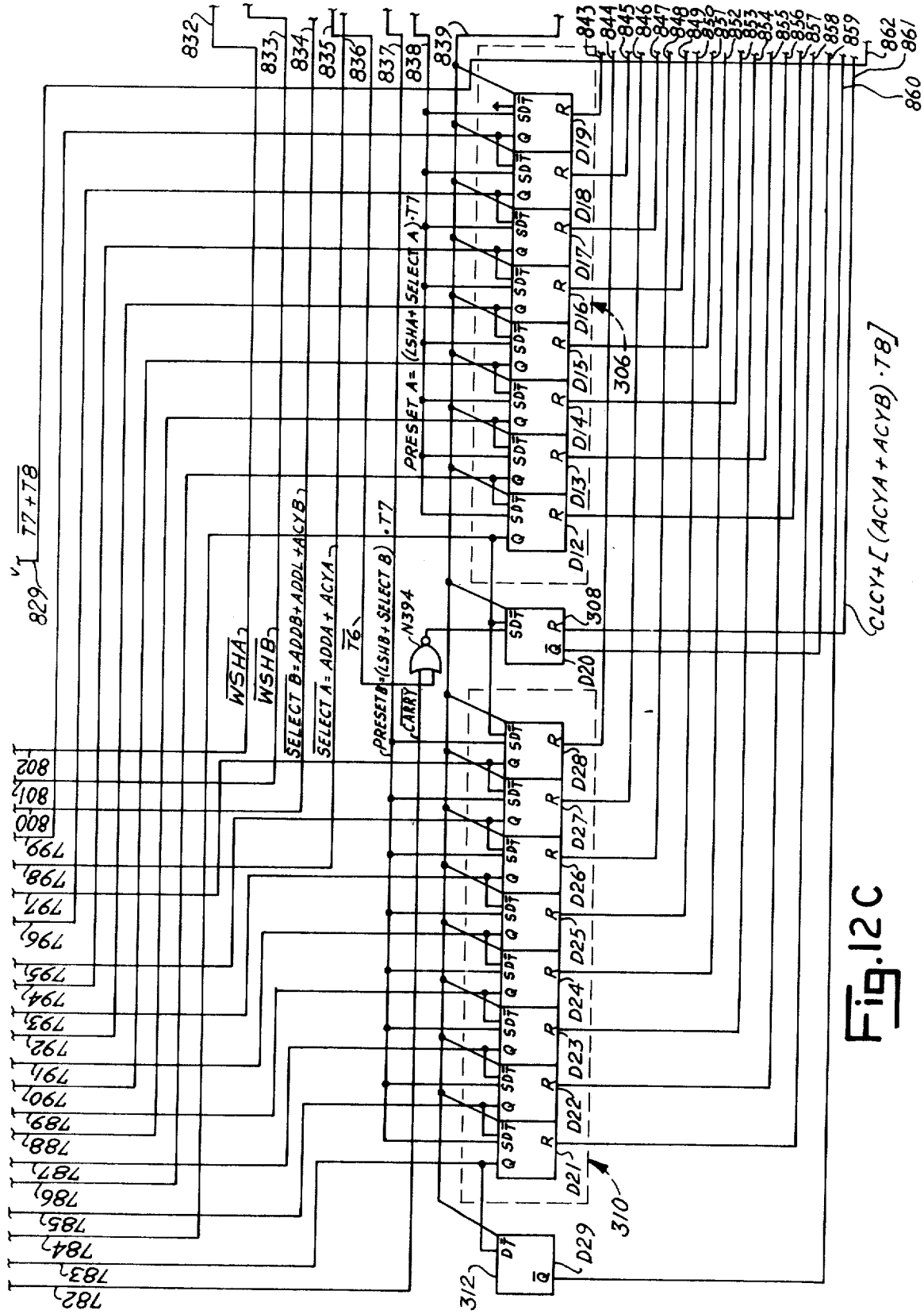

832
833
834
835
836
837
838
839
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
862
861
860
829
T7+T8
WSHA
WSHB
SELECT B=ADDB+ADDL+ACYB
SELECT A=ADDA+ACYA
T6
PRESET B=(LSHB+SELECT B)·T7
CARRY
N394
PRESET A=((LSHA+SELECT A)·T7
CLCY+[(ACYA+ACYB)·T8]
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
306
308
310
312
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802

Fig. 12C

Fig. 12D

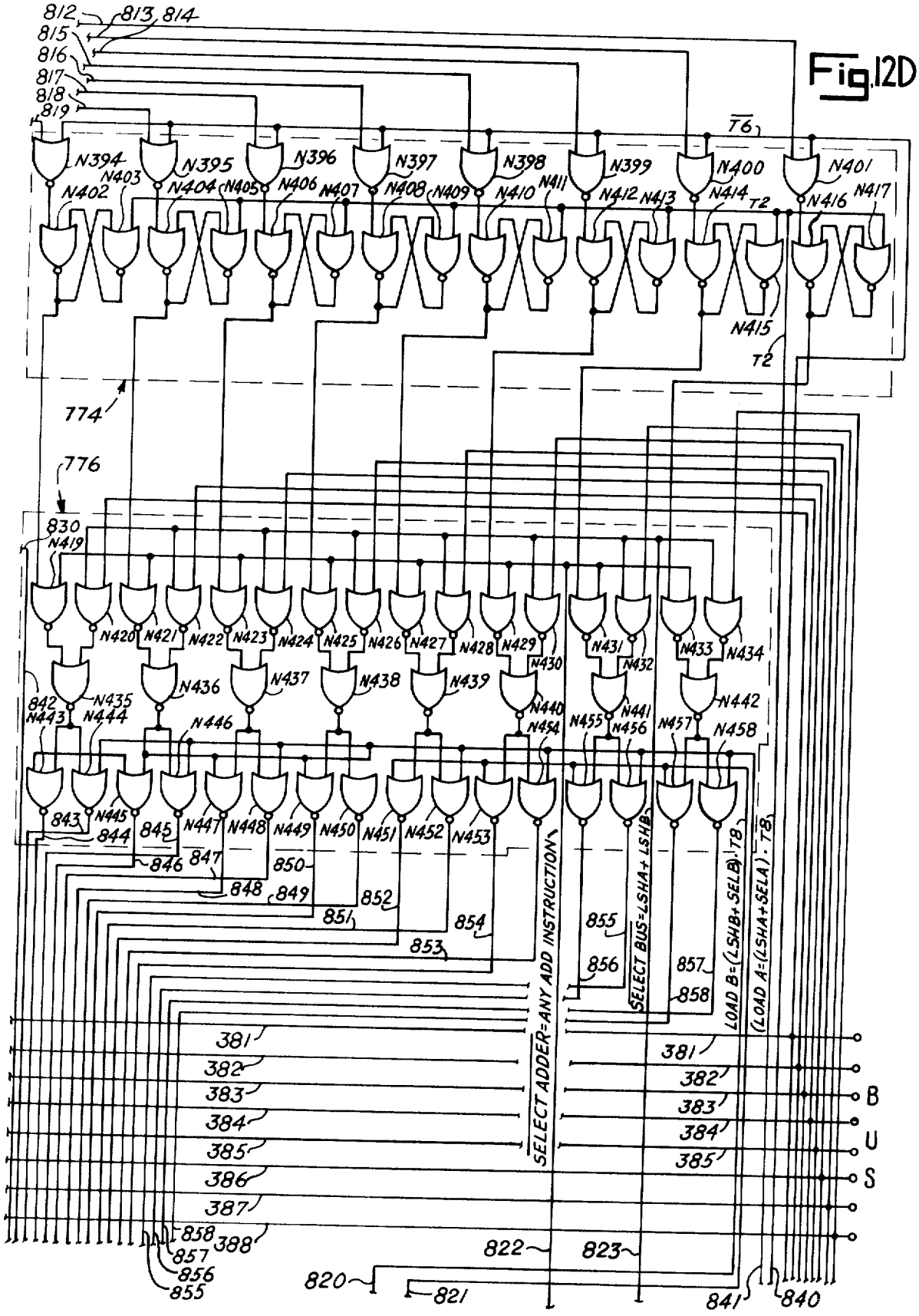
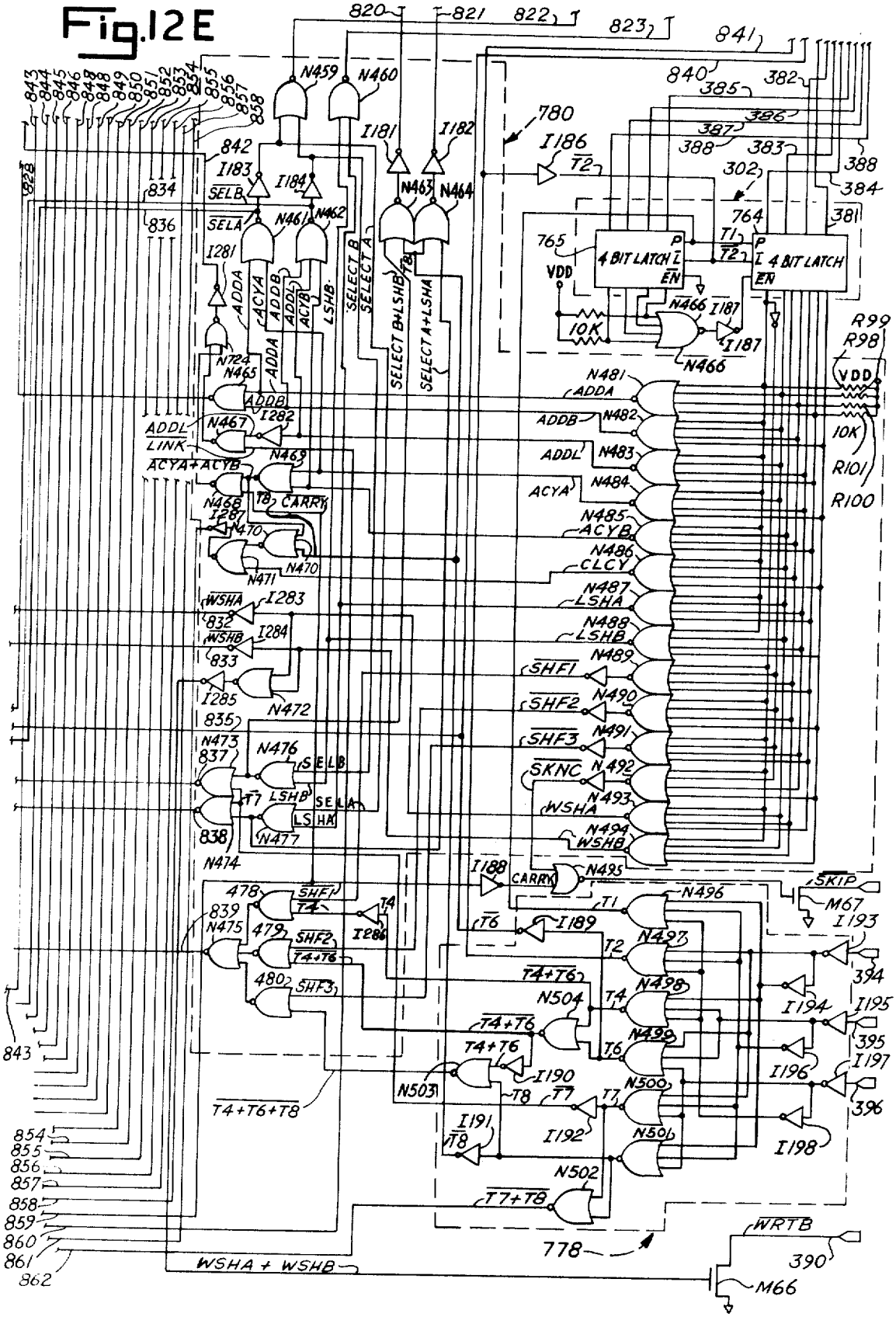

812
813
814
815
816
817
818
819
N394
N395
N396
N397
N398
N399
N400
N401
N402
N403
N404
N405
N406
N407
N408
N409
N410
N411
N412
N413
N414
N416
N417
N415
T6
T2
774
776
830
N419
N420
N421
N422
N423
N424
N425
N426
N427
N428
N429
N430
N431
N432
N433
N434
N435
N436
N437
N438
N439
N440
N441
N442
842
N443
N444
N446
N454
N455
N456
N457
N458
843
N445
844
845
N447
N448
N449
N450
N451
N452
N453
846
847
848
849
850
851
852
853
854
855
856
857
858
SELECT ADDER=ANY ADD INSTRUCTION
SELECT BUS=(LSHA+LSHB)
LOAD B=(LSHB+SELB)·T8
(LOAD A=(LSHA+SELA)·T8
381
382
383
384
385
386
387
388
B
U
S
820
821
822
823
840
841

Fig. 12E


820
821
822
823
841
840
385
382
386
387
388
383
384
381
302
764
765
780
I186
T2
T1
P
I 4 BIT LATCH
EN
VDD
10K
N466
I187
R99
R98
R101
R100
N459
N460
I181
I182
842
I183
I184
SELB
SELA
N461
N462
N463
N464
834
836
828
I281
ADDA
ACYA
ADDB
ACYB
ADDL
LSHB
SELECT B
SELECT A
SELECT B+LSHB
SELECT A+LSHA
N465
N467
I282
LINK
ACYA+ACYB
N468
N469
CARRY
I287
N470
N471
WSHA
WSHB
I283
I284
I285
832
833
N472
835
N473
N476
837
838
N474
N477
478
479
480
SHF1
SHF2
SHF3
839
N475
I286
843
T4+T6+T8
T4+T6
N503
I190
I191
I192
N504
N502
T7+T8
778
854
855
856
857
858
859
860
861
862
WSHA + WSHB
N481
N482
N483
N484
N485
N486
N487
N488
N489
N490
N491
N492
N493
N494
N495
SHF1
SHF2
SHF3
SKNC
CLCY
LSHA
LSHB
I188
I189
N496
N497
N498
N499
N500
N501
I193
I194
I195
I196
I197
I198
394
395
396
SKIP
M67
WRTB
390
M66

INST	CODE	BUS 87654321
ADDA	60	01100000
ADDB	61	01100001
ADDL	62	01100010
ACYA	63	01100011
ACYB	64	01100100
CLCY	65	01100101
LSHA	66	01100110
LSHB	67	01100111
SHF1	68	01101000
SHF2	69	01101001
SHF3	6A	01101010
SKNC	6B	01101011
WSHA	6C	01101100
WSHB	6D	01101101

Fig. 12F

Fig. 12G

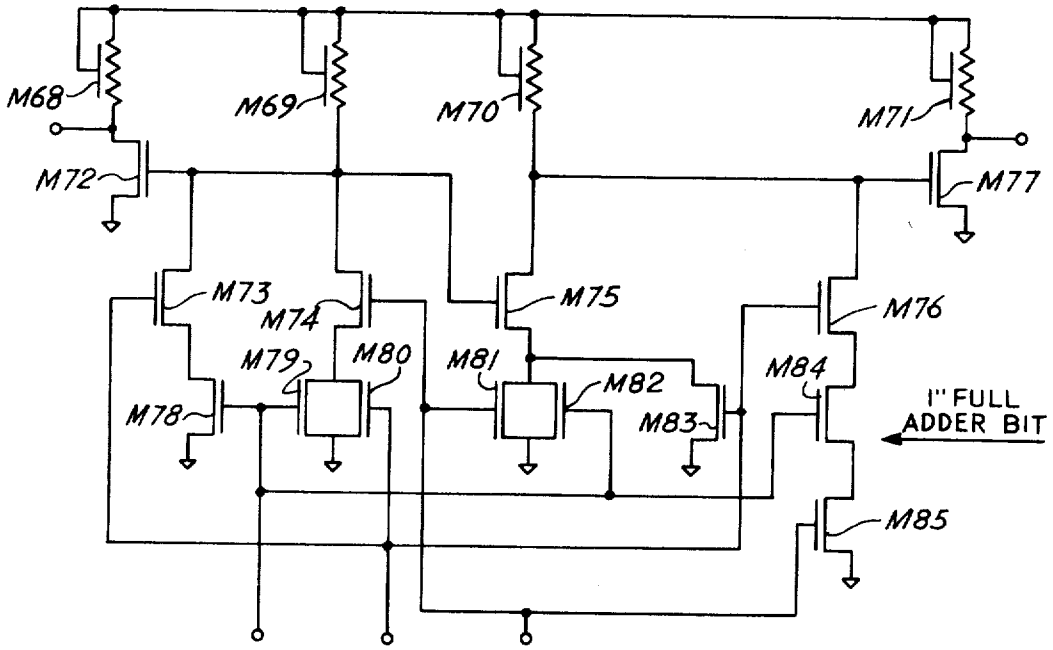
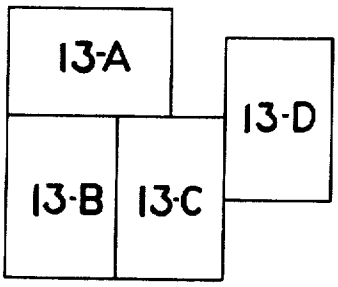


Fig. 13



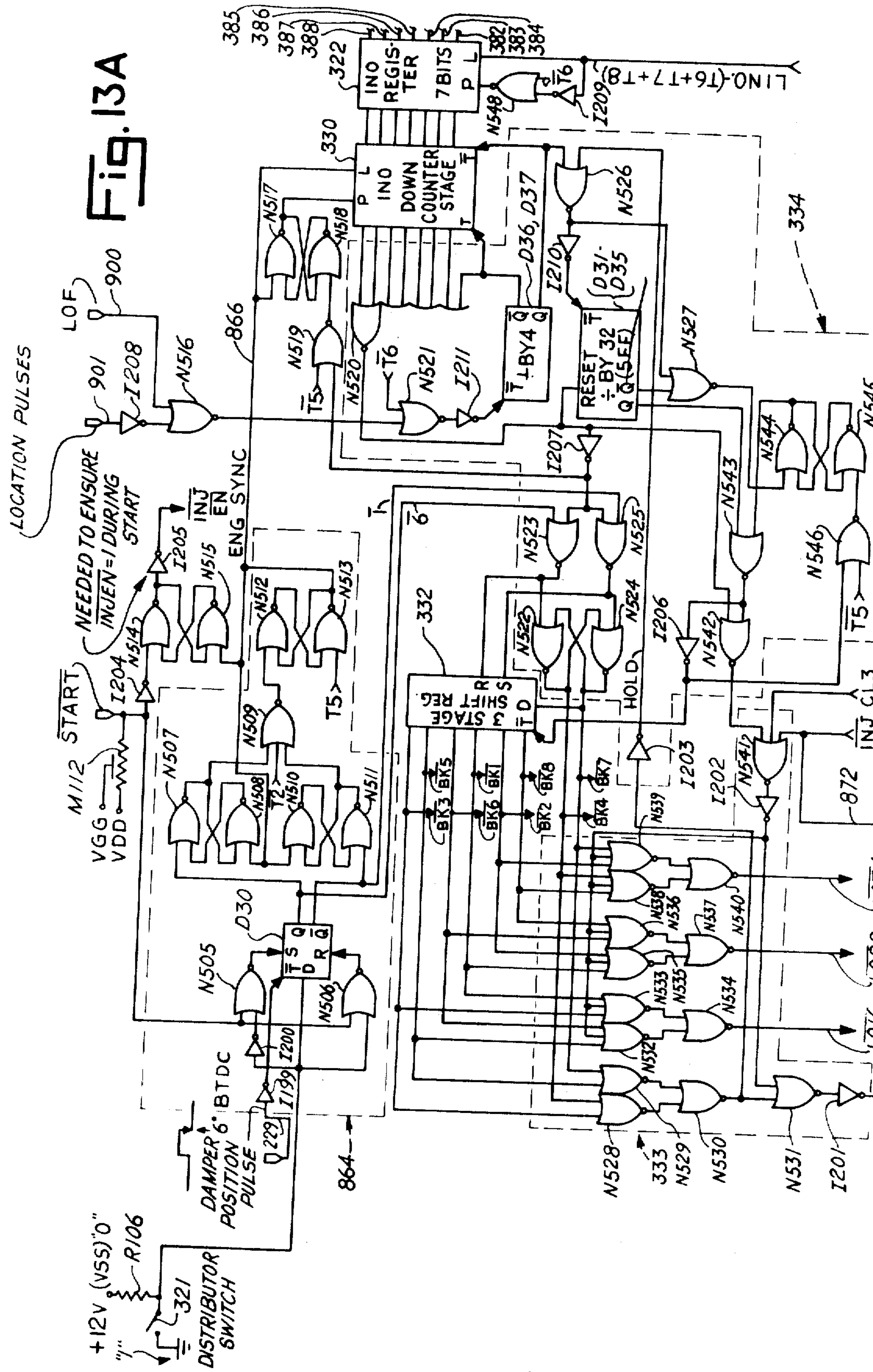

LOCATION PULSES
LOF
START
VGG
VDD
NEEDED TO ENSURE INJEN=1 DURING START
INJ EN
ENG SYNC
INO REGISTER 7 BITS
INO DOWN COUNTER STAGE
LINO·(T6+T7+T8)
÷BY4
RESET ÷ BY 32 (5FF)
3 STAGE SHIFT REG.
HOLD
CL3
T1...T4
LO74
LO82
LO76
LO53
+12V
(VSS) "0"
DISTRIBUTOR SWITCH
DAMPER POSITION PULSE
6° BTDC

Fig. 13A

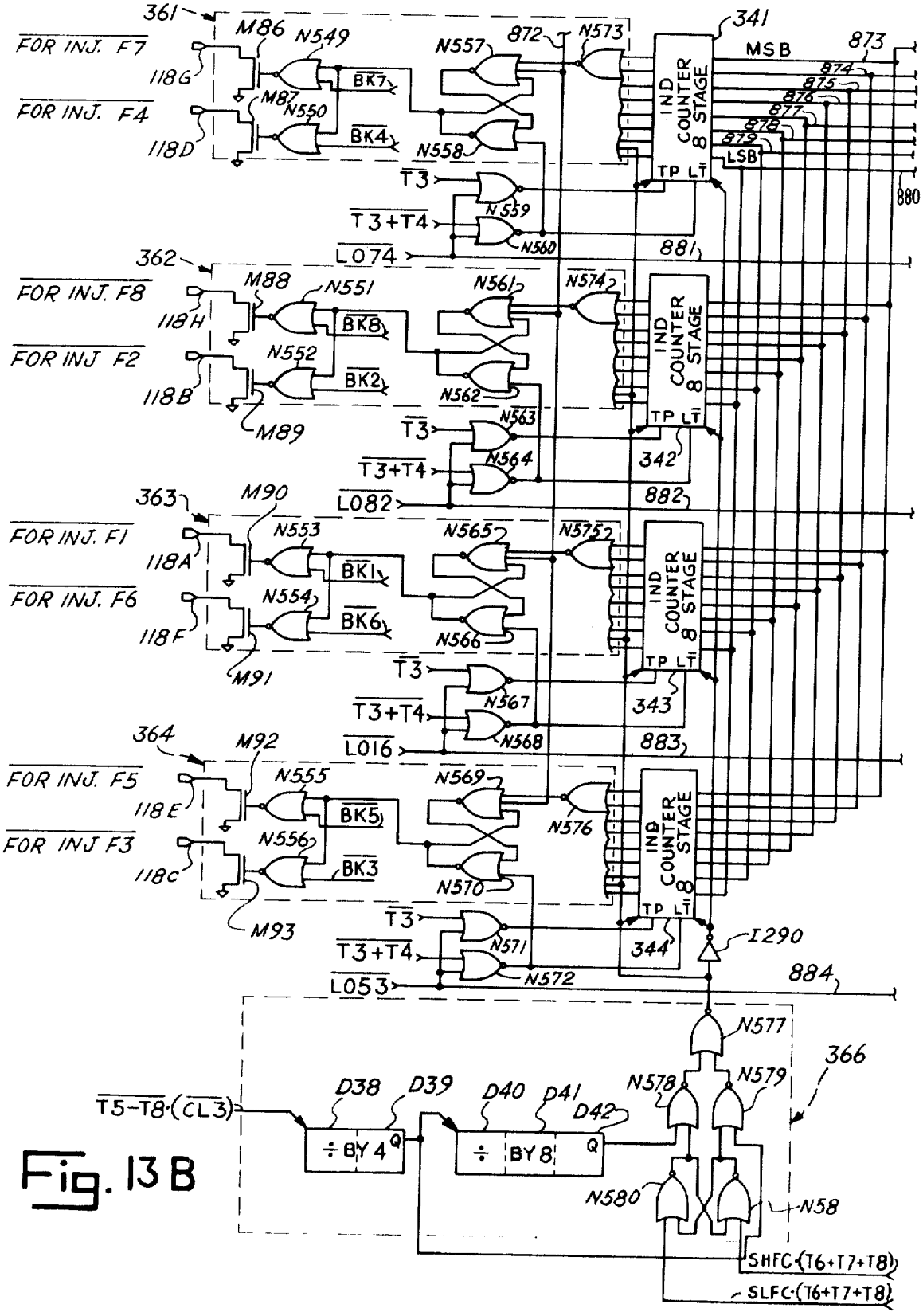

361
FOR INJ. F7
118G
FOR INJ. F4
118D
M86
M87
N549
N550
BK7
BK4
N557
N558
872
N573
341
MSB
873
874
875
876
877
878
879
LSB
880
IND COUNTER 8 STAGE
TP LT
T3
T3+T4
LO74
N559
N560
881
362
FOR INJ. F8
118H
FOR INJ F2
118B
M88
M89
N551
N552
BK8
BK2
N561
N562
N574
T3
T3+T4
N563
N564
342
LO82
882
363
FOR INJ. F1
118A
FOR INJ. F6
118F
M90
M91
N553
N554
BK1
BK6
N565
N566
N575
T3
T3+T4
N567
N568
343
LO16
883
364
FOR INJ. F5
118E
FOR INJ F3
118C
M92
M93
N555
N556
BK5
BK3
N569
N570
N576
T3
T3+T4
N571
N572
344
I290
LO53
884
N577
366
N578
N579
T5-T8·(CL3)
D38
D39
D40
D41
D42
÷ BY 4
÷ BY 8
Q
N580
N58
SHFC·(T6+T7+T8)
SLFC·(T6+T7+T8)

Fig. 13B

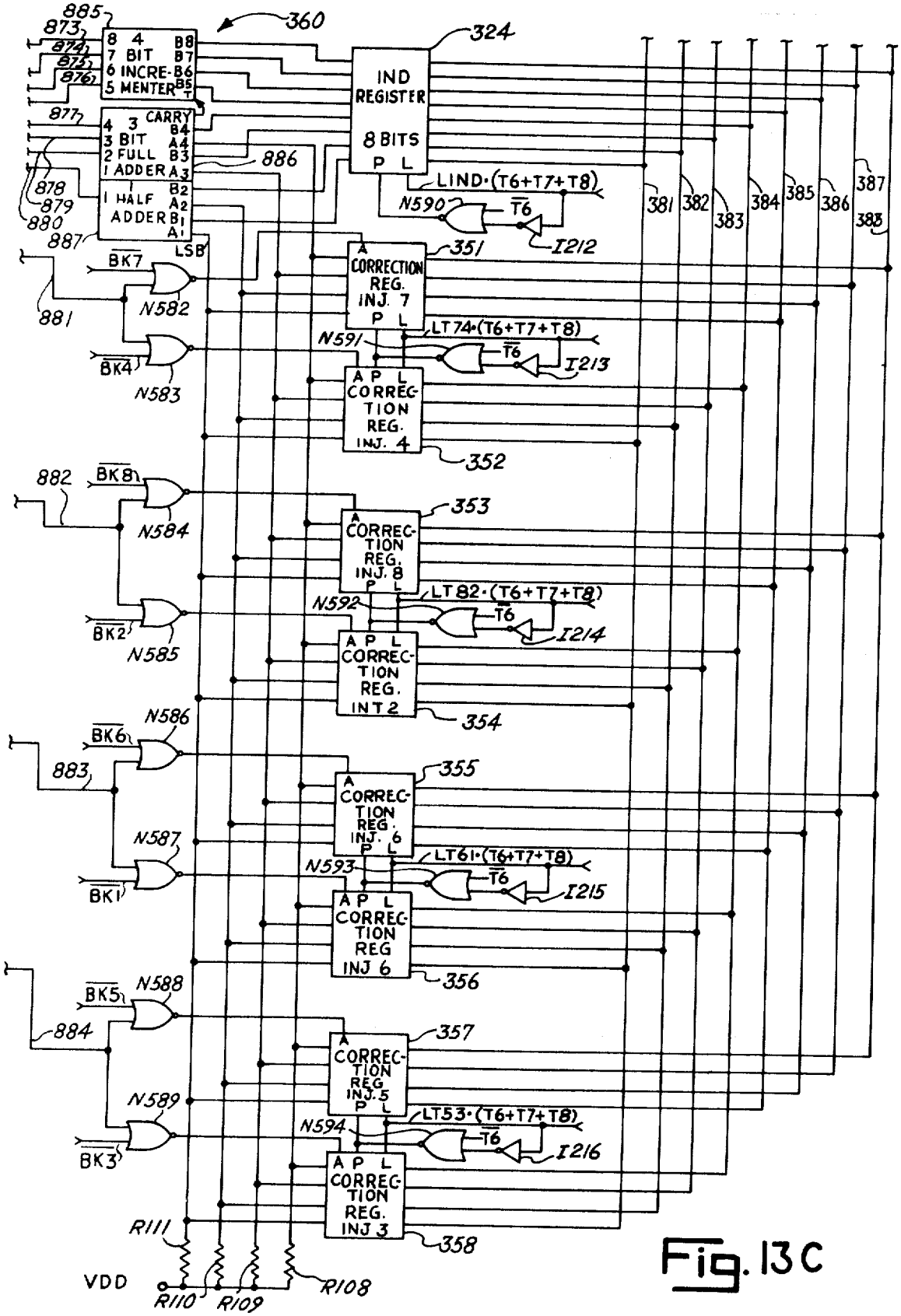

360
324
IND REGISTER 8 BITS P L
8 4 B8
7 BIT B7
6 INCRE- B6
5 MENTER B5
CARRY B4
4 3 BIT A4
2 FULL B3
1 ADDER A3
1 HALF ADDER B2 A2 B1 A1
LSB
LIND·(T6+T7+T8)
N590
T6
I212
381 382 383 384 385 386 387 388
A CORRECTION REG. INJ. 7 P L
351
LT74·(T6+T7+T8)
N591
I213
A P L CORRECTION REG. INJ. 4
352
A CORREC-TION REG. INJ. 8 P L
353
LT82·(T6+T7+T8)
N592
I214
A P L CORREC-TION REG. INT 2
354
A CORREC-TION REG. INJ. 6 P L
355
LT61·(T6+T7+T8)
N593
I215
A P L CORREC-TION REG INJ 6
356
A CORREC-TION REG INJ. 5 P L
357
LT53·(T6+T7+T8)
N594
I216
A P L CORREC-TION REG. INJ 3
358
BK7 N582 881
BK4 N583
BK8 N584 882
BK2 N585
BK6 N586 883
BK1 N587
BK5 N588 884
BK3 N589
873 874 875 876 877 878 879 880 885 886 887
R111 R110 R109 R108
VDD

Fig. 13C

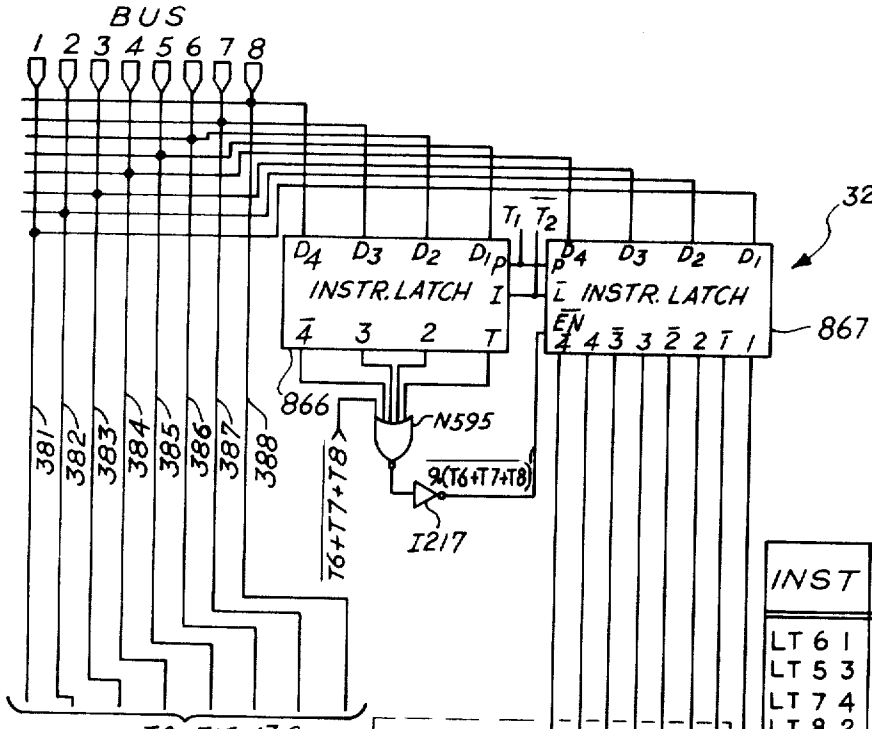
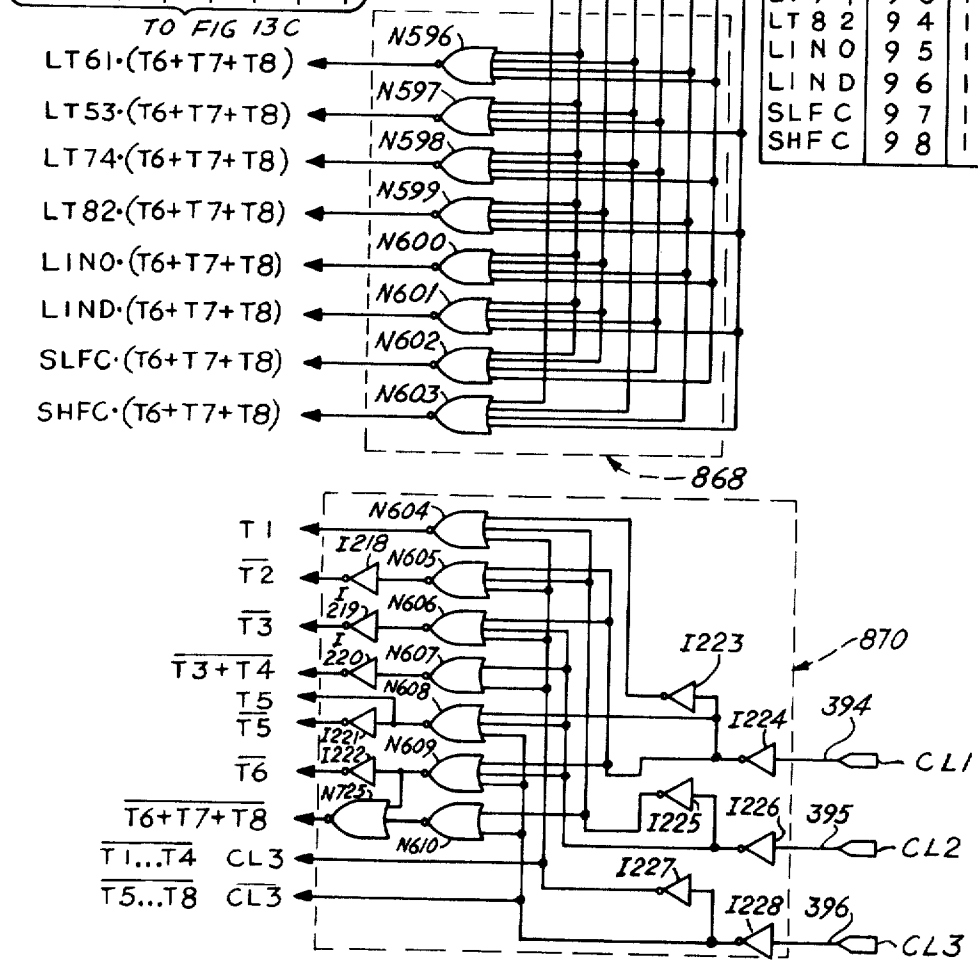


Fig. 13D

Fig. 13E

INST	CODE	BUS 8 7 6 5 4 3 2 1
LT 6 1	9 1	1 0 0 1 0 0 0 1
LT 5 3	9 2	1 0 0 1 0 0 1 0
LT 7 4	9 3	1 0 0 1 0 0 1 1
LT 8 2	9 4	1 0 0 1 0 1 0 0
LI N 0	9 5	1 0 0 1 0 1 0 1
LI N D	9 6	1 0 0 1 0 1 1 0
SLF C	9 7	1 0 0 1 0 1 1 1
SHF C	9 8	1 0 0 1 1 0 0 0



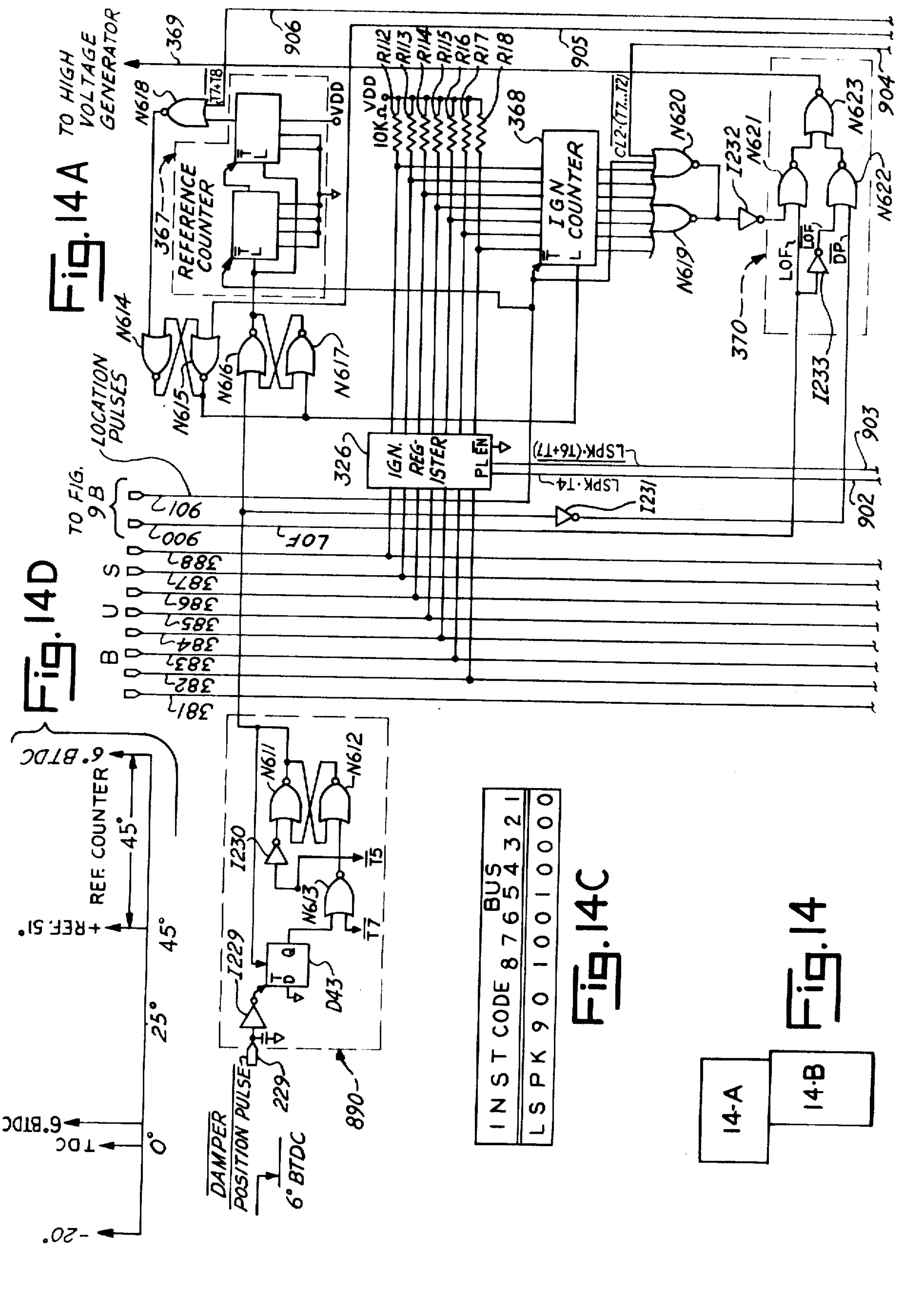


Fig. 14A
TO HIGH VOLTAGE GENERATOR
REFERENCE COUNTER
IGN COUNTER
IGN. REGISTER
LOCATION PULSES
TO FIG. 9B
BUS
Fig. 14D
REF. COUNTER
DAMPER POSITION PULSE
6° BTDC
Fig. 14C
INST CODE 8 7 6 5 4 3 2 1
LSPK 9 0 1 0 0 1 0 0 0 0
Fig. 14
14-A
14-B

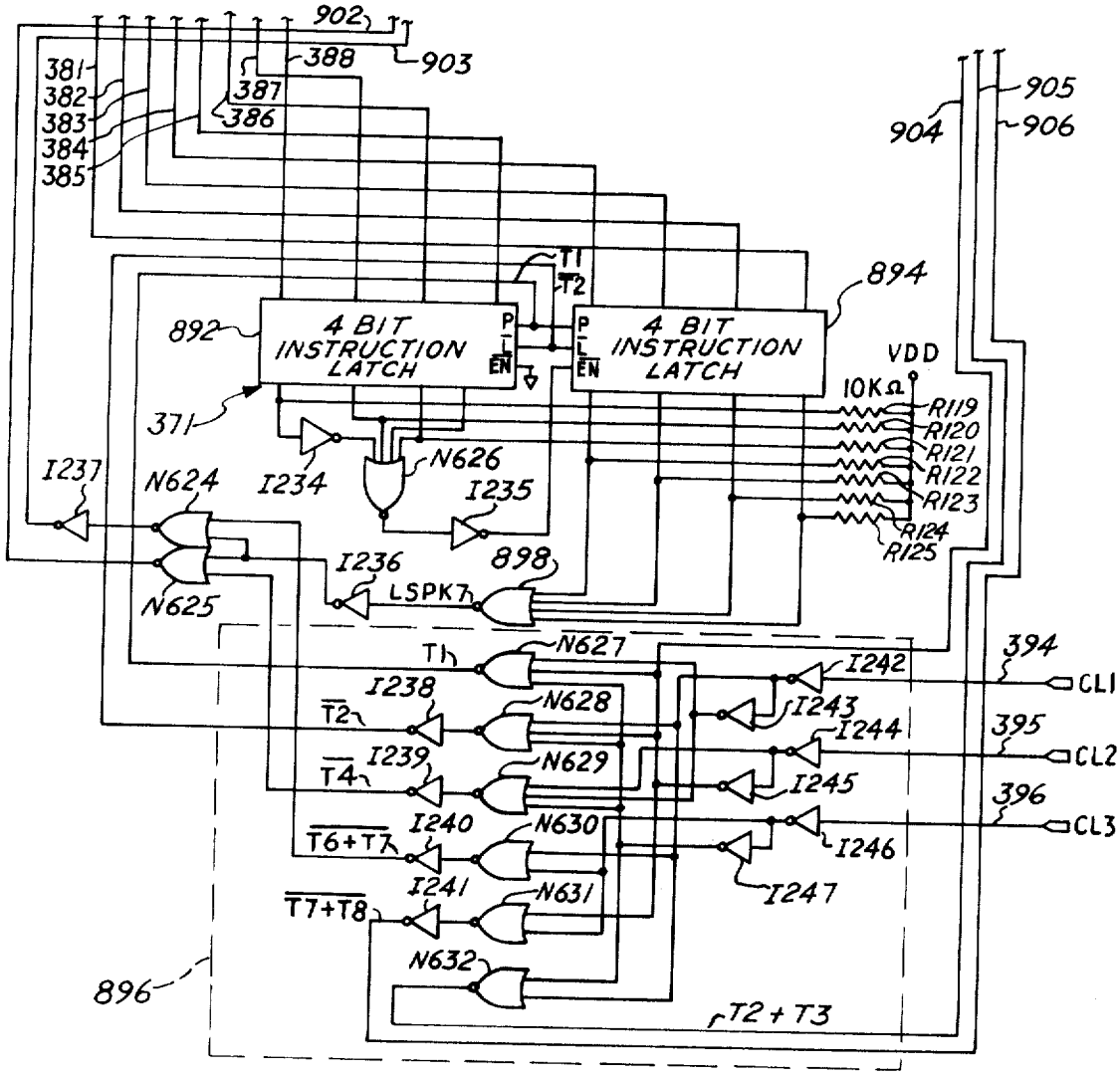

902
903
388
387
386
381
382
383
384
385
904
905
906
894
892
4 BIT INSTRUCTION LATCH
4 BIT INSTRUCTION LATCH
T1
T2
P
L
EN
VDD
10KΩ
R119
R120
R121
R122
R123
R124
R125
371
I237
N624
I234
N626
I235
N625
I236
LSPK7
898
T1
N627
I242
394
CL1
I238
T2
N628
I243
I244
395
CL2
I239
T4
N629
I245
396
CL3
I240
T6+T7
N630
I246
I241
T7+T8
N631
I247
N632
896
T2 + T3

Fig. 14 B

Fig 15

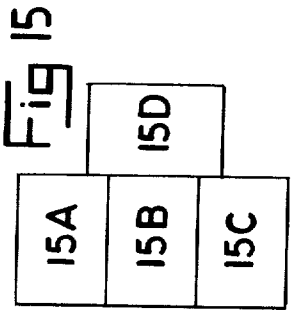


Fig 15A

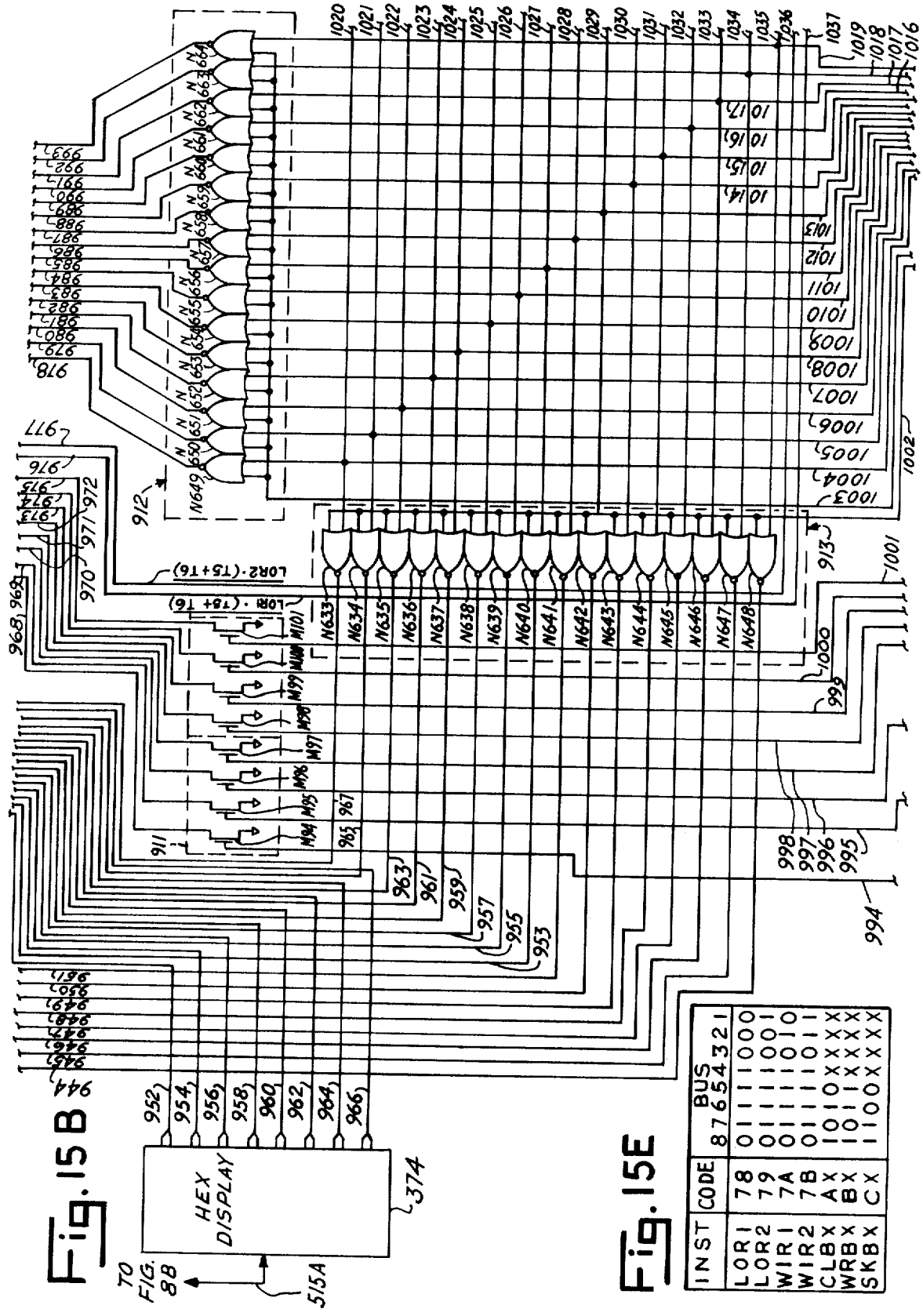


Fig. 15B

INST	CODE	BUS 87654321
LOR1	78	01111000
LOR2	79	01111001
WIR1	7A	01111010
WIR2	7B	01111011
CLBX	AX	1010XXXX
WRBX	BX	1011XXXX
SKBX	CX	1100XXXX

Fig. 15E

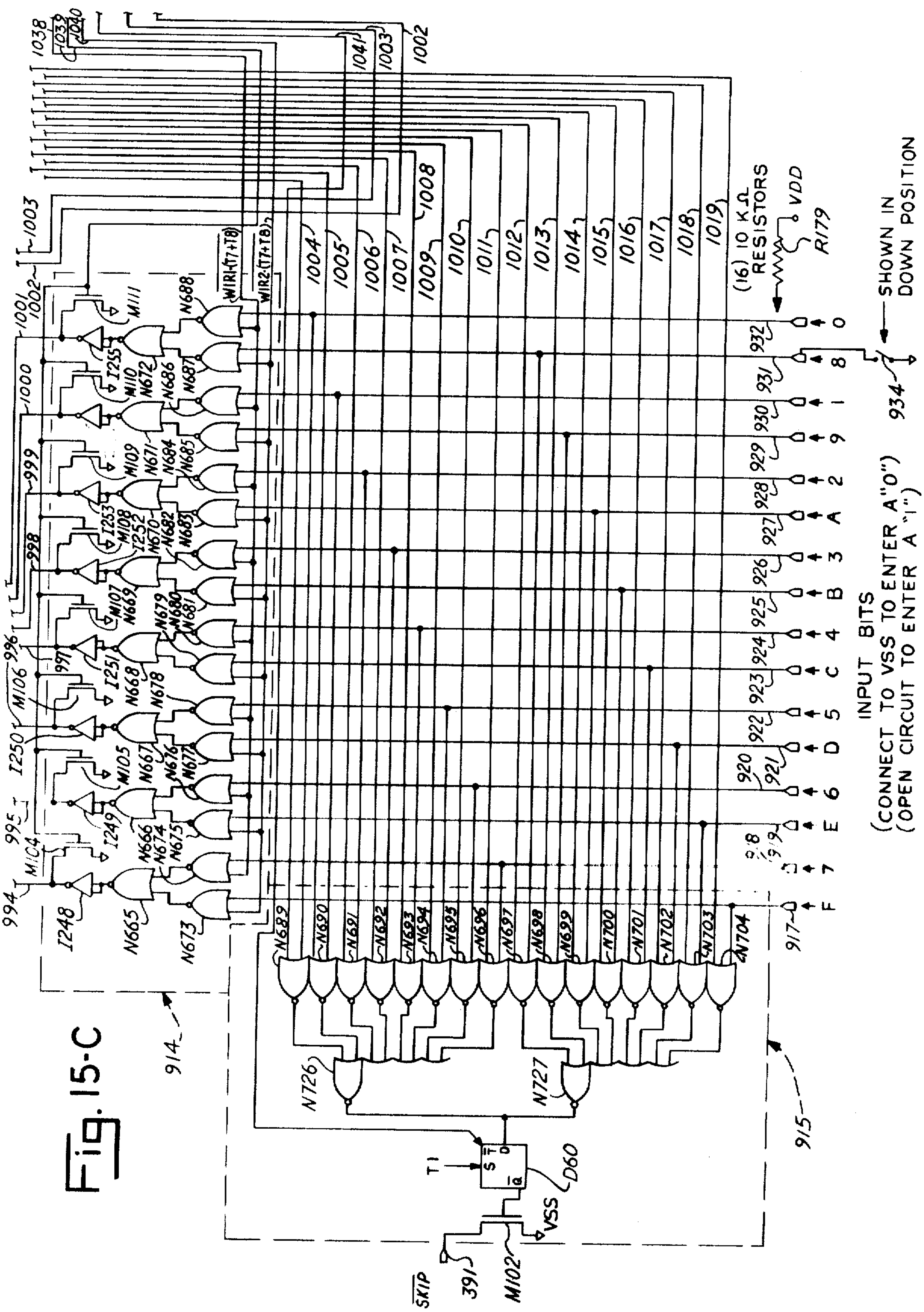
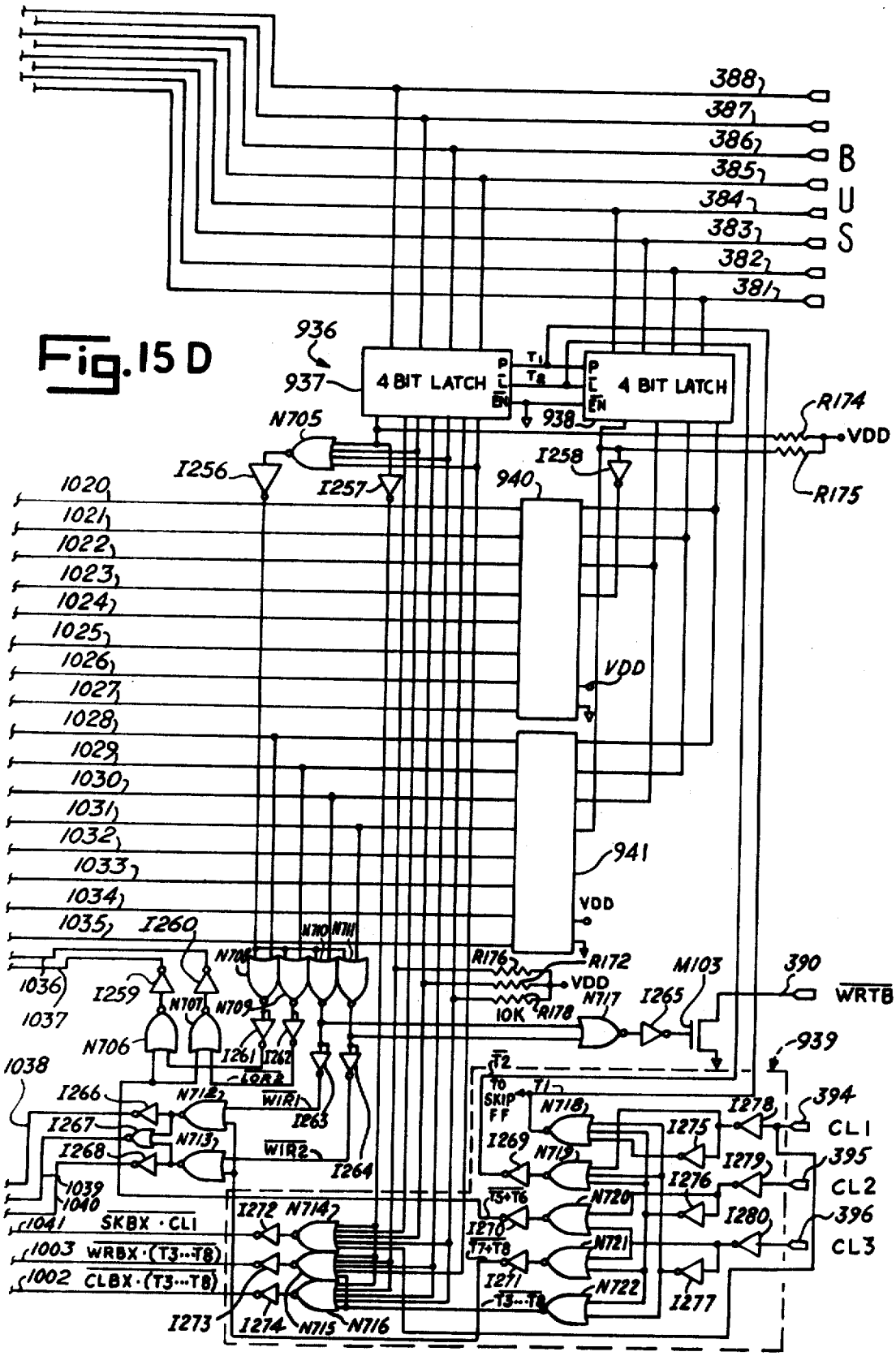

(16) 10 KΩ RESISTORS
VDD
R179
SHOWN IN DOWN POSITION
934
INPUT BITS
(CONNECT TO VSS TO ENTER A "0")
(OPEN CIRCUIT TO ENTER A "1")
0 8 1 9 2 A 3 B 4 C 5 D 6 E 7 F
N726
N727
D60
T1
VSS
SKIP
391
M102
914
915

Fig. 15-C

Fig. 15 D


388
387
386
385
384
383
382
381
B
U
S
936
937
4 BIT LATCH
4 BIT LATCH
938
R174
VDD
R175
N705
I256
I257
I258
940
941
VDD
VDD
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
I260
1036
1037
1038
I259
N706
N707
N708
N709
I261
I262
I263
I264
I266
I267
I268
N712
N713
WIR1
WIR2
LOAD
1039
1040
1041
SKBX · CLI
1003 WRBX · (T3···T8)
1002 CLBX · (T3···T8)
I272
N714
I273
I274
N715
N716
R176
R172
VDD
10K
R178
N717
I265
M103
390
WRTB
939
T2
T1
TO SKIP FF
N718
I269
N719
T5+T6
N720
I270
T7+T8
N721
I271
T3···T8
N722
I275
I276
I277
I278
I279
I280
394
395
396
CL1
CL2
CL3

DIGITAL ENGINE CONTROL APPARATUS AND METHOD

The apparatus includes a digital data memory that stores 256 fuel digital words each representing a discrete engine fuel requirement at a particular engine speed and throttle position, and 256 ignition digital words each representing a discrete engine spark timing requirement at a particular engine speed and throttle position. These digital words are empirically determined for each different type of engine to be operated and are stored in the data memory before the apparatus begins to control the engine. Each digital word is stored in the memory at an address represented by two digital numbers. The first address number is proportional to a throttle position and the second address number is proportional to the reciprocal of engine speed.

The apparatus also includes a digital program memory for storing operating instructions.

As the engine operates, electronic circuitry converts the engine speed and throttle position into digital electrical signals representing engine condition digital numbers.

Selection circuitry, including an arithmetic unit controlled by the operating instructions, compares the address numbers with the engine condition digital numbers in order to select the data memory addresses most nearly approximating the actual throttle position and speed of the engine.

The circuitry then interpolates between the digital words stored at the selected addresses in order to produce a resultant fuel digital word that corresponds to the engine fuel requirement and a resultant ignition digital word that corresponds to the engine spark timing requirement.

The resultant fuel and ignition digital words are stored in separate registers. An open-time digital word is also stored in order to determine the time at which each injector opens and begins supplying fuel to a cylinder.

A device attached to the engine crankshaft damper generates a position signal when the engine is in a predetermined position. In order to operate the number one cylinder of the engine, the position signal initiates additional signals by which the open-time digital word is loaded into an open-time electronic counter, and the counter is stepped until a predetermined counter value is reached. When the open-time counter reaches its predetermined value, the electrical fuel signal is produced and the number one injector is opened to admit fuel into the number one cylinder. In response to the production of the fuel signal, the resultant fuel digital word is loaded into a fuel electronic counter, and the counter is stepped until a predetermined value is reached. At this time, the fuel signal is terminated so that the number one injector closes. The ignition resultant digital word then is loaded into an ignition electronic counter in response to another position pulse. After the ignition electronic counter is stepped and reaches it predetermined value, the fire signal is produced and the number one spark plug is fired. These techniques are used to individually fire all spark plugs and to individually operate all injectors of the engine.

BACKGROUND OF THE INVENTION

This invention relates to internal combustion engine control and more specifically relates to an apparatus and a method for controlling an internal combustion engine by means of electronic techniques.

During the past several years, the Federal Government, as well as various states, have placed strict controls on the combustion products that can be emitted from automotive engines. In order to meet such controls, designers and engineers have used a variety of techniques for reducing engine emissions. While these techniques have reduced emissions to some extent, they have also adversely affected performance characteristics of the engine. For example, emission control devices have been known to reduce the starting, warm-up, and driveability characteristics of engines and have generally increased fuel consumption.

Some prior engine control techniques employ fuel injectors that are opened in response to an electrical signal in order to admit fuel into an engine cylinder. In order to control the electrical signal, analog electrical circuits have been employed. Experience has shown that these analog circuits are not precise enough to provide long-term accurate control over a fuel injector. Moreover, analog circuits are not well suited to the mass production techniques generally employed by automobile manufactures because small changes in component values can alter the operating characteristics of the circuits sufficiently to impair the accuracy of the fuel quantities injected into the engine cylinders. In addition, changes in component values due to the age and the adverse environmental conditions found in automotive engine compartments also decrease the accuracy with which analog circuits can control the injection of fuel. These same factors also render analog circuits deficient in their ability to control the ignition timing of an internal combustion engine. Moreover, the manner in which analog circuits control an engine generally can not be altered without physically substituting components of the circuit. This is an expensive process requiring the services of skilled technicians.

SUMMARY OF THE INVENTION

In order to overcome the deficiencies of the prior art engine control devices, the applicant has invented an entirely new control concept in which engine control requirements over a wide range of operating conditions are experimentally determined and are prestored in a data memory in the form of digital control data. As the engine is operated, the memory is instantaneously analyzed to select the precise control data needed to insure optimum engine operation. For example, data stored in the memory can be obtained in about 0.0000125 second, whereas an engine operating at 3,000 RPM requires about 0.020 second to complete one revolution. This technique provides engine control with a degree of speed, flexibility and accuracy previously unattainable. By merely changing the data stored in the memory, the engine may be automatically tuned for maximum performance, emission control, fuel economy, or other operating modes, without physically replacing any components.

According to an important feature of the invention, the engine operating characteristics of engine speed and throttle position are used to select data stored in the digital memory. Although engine speed and throttle position have been used in the past in mechanical engine control systems, the applicant is believed to be the first to recognize that these operating characteristics

significantly reduce engine response time when used in connection with an electronic digital control system. By reducing engine response time, the applicant's invention enables the engine to instantaneously follow the varying commands of the operator thereby increasing the driveability of a vehicle employing the engine.

According to another feature of the invention, the digital control data is stored in the data memory in the form of many discrete control digital words. Each digital word represents an engine control requirement (such as fuel quantity) at a particular combination of engine operation characteristics, such as a specific engine speed and a specific throttle position. As the engine is operated, the engine operating characteristics are continuously converted into engine condition digital numbers so that any change in the operating characteristics (e.g., the movement of the throttle) is immediately detected. These engine control digital numbers are used to select from the data memory one or more of the control digital words that at least approximately correspond to the control requirement of the engine at the instantaneous operating characteristics represented by the engine condition digital numbers. In the normal case, the instantaneous operating condition of the engine will not correspond precisely to any of the particular combinations of engine operating characteristics at which a control digital word is stored. In order to increase accuracy, the system derives a composite resultant control digital word, which is proportional to the exact engine control requirement, from the stored control digital words that approximate the exact engine control requirement. This derivation may be achieved by a process of arithmetic interpolation. If such accuracy is not desired, this interpolation can be eliminated, and the resultant control digital word can be derived by merely selecting a single control digital word from the data memory and by transmitting the single word to a storage unit. The resultant control digital word is stored for a fraction of a second until another sample of the engine operating characteristics is taken. At that time, a new resultant control digital word is generated which reflects any change in engine operating conditions.

While the resultant control digital word is being derived and stored, a position signal is generated when the engine is in a predetermined position. This position signal is used to initiate the operation of a control means that can produce a control signal proportional to the value of the resultant control digital word in order to control the engine. For example, if the system is used to control ignition timing, means responsive to the position signal produces a control signal that enables the firing of a spark plug at the end of an operating interval proportional to the value of the resultant control digital word. By operating interval is meant either an interval of time or an interval of mechanical movement, such as degrees of crankshaft rotation. In this manner, the value of the resultant control digital word can control spark advance with a degree of accuracy heretofore unattainable. A similar technique is employed to control the operating interval during which fuel is injected into the engine. By employing these techniques, fuel can be injected in the precise quantities needed for instantaneous response to an operator's commands in a way which will optimize engine operation.

According to another feature of the invention, one of the engine condition digital numbers is proportional to the reciprocal of engine speed. It has been found that this feature enables the engine to be accurately controlled at slow engine speeds near idle speed.

According to another feature of the invention, operating instructions are stored in a program memory in the form of instruction digital words. The instruction digital words control the overall operation of the system, including the selection of control digital words from the data memory. By using this technique, the entire operating method of the system can be revised to accommodate a variety of requirements without replacing any components.

According to another feature of the invention, each control device, such as a fuel injector, associated with an individual cylinder of the engine is separately controlled.

According to another feature of the invention, the operating requirements of each cylinder are taken into account so that each cylinder is individually controlled according to its own operating requirements. As a resultant, the exact control requirements of the engine can be satisfied with a degree of accuracy previously unattainable.

According to still another feature of the present invention, a separate correction digital number is stored for each cylinder of the engine, and the value of each control signal for controlling fuel to each individual cylinder is altered by the composite value of the resultant control digital word and the correction digital number so that each cylinder is separately operated according to its own requirements.

According to still another feature of the invention, the engine is operated at a predetermined value of an operating characteristic, such as a particular speed, by sequentially converting the operating characteristic to digital numbers in a time-spaced manner and by using these numbers to make small changes in a control function, such as fuel quantity, until the desired value (e.g., speed) is achieved. This technique offers a method of maintaining an engine at a particular idle speed, even during the warm-up cycle, with a degree of accuracy unavailable through conventional techniques.

DESCRIPTION OF THE DRAWINGS

These and other advantages and features of the present invention will hereafter appear in connection with the accompanying drawings in which the numbers refer to the parts throughout and in which:

FIG. **1** is a fragmentary, perspective view of an exemplary internal combustion engine having a fuel injection and spark distribution system appropriate for use in connection with the present invention;

FIG. **2** is a top plan, schematic view of the engine and associated apparatus shown in FIG. **1** together with additional exemplary apparatus required to operate the engine;

FIG. **3** is a block diagram, schematic drawing of a preferred system embodying the present invention;

FIG. **3A** is a block diagram of the timing circuit **320** shown in FIG. **3**;

FIG. **4** is an injection map which graphically illustrates the manner in which the fuel requirements of the exemplary engine are stored in the data memory of the system;

FIG. 5 is an enlarged view of a portion of the injection map shown in FIG. 3;

FIG. 6 is a timing diagram showing the relative movement between various parts of the system and exemplary engine;

FIG. 7 illustrates the manner in which FIGS. 7A and 7B should be arranged;

FIGS. 7A and 7B are electronic logic schematic diagrams showing a preferred form of a program memory and a data memory used in the system;

FIG. 7C is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 7A and 7B;

FIG. 7D is a timing diagram showing the condition of the three system clock lines during 8 separate timing periods or slots T1 - T8;

FIG. 7E is an electronic logic schematic diagram showing a preferred form a bit latch used in the system;

FIG. 8 illustrates the manner in which FIGS. 8A - 8C should be arranged;

FIGS. 8A - 8C are electronic logic schematic diagrams showing a preferred form of analog to digital converter used in the system;

FIG. 8D is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 8A - 8C;

FIG. 9 illustrates the manner in which FIGS. 9A - 9C should be arranged;

FIG. 9A - 9C are electronic logic schematic drawings showing a preferred form of a speed and position indicating assembly for use in the system;

FIG. 9D is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 9A - 9C;

FIG. 10 illustrates the manner in which FIGS. 10A and 10B should be arranged;

FIGS. 10A and 10B are electronic logic schematic diagrams showing a preferred form of a program sequencer for use in the system;

FIG. 10C is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 10A and 10B;

FIG. 10D is an electronic logic schematic diagram illustrating a preferred form of one bit of a bus latch for use in the system;

FIG. 10E is an electronic logic schematic diagram illustrating a preferred form of an inhibitable noninverting buffer amplifier for use in the system;

FIG. 11 illustrates the manner in which FIGS. 11A - 11F should be arranged;

FIG. 11A - 11F are electronic logic schematic diagrams showing the preferred form of general registers for use in the system;

FIG. 11G is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 11A - 11F;

FIG. 11H is an electronic schematic drawing showing one bit of a preferred form of register for use in the system;

FIG. 12 illustrates the manner in which FIGS. 12A - 12E should be arranged;

FIGS. 12A - 12E are electronic logic schematic diagrams showing a preferred form of an arithmetic unit for use in the system;

FIG. 12F is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 12A - 12E;

FIG. 12G is an electric schematic drawing showing one bit of a preferred form of full adder for use in the arithmetic unit;

FIG. 13 illustrates the manner in which FIGS. 13A - 13E should be arranged;

FIGS. 13A - 13D are electronic logic schematic diagrams showing a preferred form of an injector timing circuit for use in the system;

FIG. 13E is a decoding table showing the condition of the communication bus during the performance of instructions used by the apparatus shown in FIGS. 13A - 13D;

FIG. 14 illustrates the manner in which FIGS. 14A and 14B should be arranged;

FIGS. 14A and 14B are electronic logic schematic diagrams showing a preferred form of ignition timing circuit for use in the system;

FIG. 14C is a decoding table showing the condition of the communication bus during the performance of the LSPK instruction by the apparatus shown in FIGS. 14A and 14B;

FIG. 14D is a timing diagram showing the time interval of the engine cycle during which the reference counter operates;

FIG. 15 illustrates the manner in which FIGS. 15A - 15D should be arranged;

FIGS. 15A - 15D are electronic logic schematic diagrams showing a preferred form of input-output circuitry for use in the system; and

FIG. 15E is a timing decoding table showing the condition of the communication bus during the performance of instructions by the apparatus shown in FIGS. 15A - 15D.

DESCRIPTION OF THE PREFERRED EMBODIMENT

GENERAL DESCRIPTION

Referring to FIGS. 1 and 2, an exemplary form of apparatus for use in connection with the present invention would comprise a conventional V-8 internal combustion engine 80 having cylinders 1-8 in which pistons (not shown) reciprocate. An air horn 90, which can comprise the throttle body of a carburetor, is mounted on top of an intake manifold 92 in order to control the amount of air flowing into the engine. The air horn opening is controlled by a throttle plate (not shown) like the throttle plate in a conventional carburetor. The throttle plate is rotated by a shaft 98 that is connected by conventional linkage 94 to an accelerator pedal 96 which is controlled by the operator of the engine.

A fuel injector assembly 100 is mounted on top of the engine. The assembly comprises fuel injector F1 - F8 that inject fuel into the intake manifold adjacent the intake valves for cylinders 1-8, respectively, The fuel injectors are a well-known electro-mechanical type which open in response to an electrical fuel control signal to allow fuel into the intake manifold adjacent a particular cylinder. The injectors are connected by a common fuel line 110. The pressure in the fuel line is controlled by a pressure regulator 112 that provides a

substantially constant pressure drop relative to manifold pressure at all injectors during all phases of operation. As a result of this constant pressure drop fuel system, the amount of fuel injected into a cylinder by each injector depends on the duration of time during which the injector is open. Fuel is supplied to regulator **112** through a supply line **114** from a source of fuel (not shown). Line **111** provides the manifold pressure reference signal to the regulator.

Electrical fuel control signals are supplied to injectors F1 – F8 by means of an injector drive circuit **116** comprising drive amplifiers **116A–116H**. The amplifiers are a well-known type capable of driving the coils of injectors F1–F8 in response to fuel signals received over conductors **118–118H**.

A spark distributor assembly **120** controls the firing of spark plugs S1–S8 that are mounted in cylinders **1–8**, respectively. A conventional high voltage generator **130**, such as a capacitive discharge unit, produces a high voltage pulse in response to an electrical fire control signal. The high voltage pulse is transmitted over a conductor **131** to a top terminal **134** of a conventional rotary distributor **132**. A rotor **136** located inside distributor **132** distributes the high voltage pulses at top terminal **134** to each of electrodes **141–148** and through ignition wires **151–158** to spark plugs S1–S8, respectively.

Referring to FIG. **3**, a preferred form of apparatus used to produce and time the fuel signals and fire signals which control the fuel injectors and spark plugs basically comprises a power supply **166**; a data memory **170**; an analog to digital unit **190**; a speed and position indicating assembly **120**; a selecting assembly **240** comprising a program memory **250**, a program sequencer **260**, a general purpose register unit **280**, and an arithmetic unit **300**; a timing circuit **320**; an input/output circuit **372**; and a communication bus **380**.

Referring to FIG. **3**, power supply **166** is a conventional device which supplies a −14 volt and a −28 volt potential to each unit of the system from a nominal +12 volt input which can be supplied from the engine battery.

Referring to FIG. **3**, data memory **170** comprises an injector data memory **172** capable of storing 256, **8**-bit fuel control digital words. Each fuel digital word numerically represents a fuel requirement of the engine at a particular engine speed and throttle position. Each fuel digital word is stored in the memory at an address defined by a **4**-bit speed digital number proportional to the reciprocal of engine speed and a **4**-bit throttle digital number proportional to a throttle position.

Data memory **170** also comprises an ignition data memory **176** capable of storing 256, **8**-bit ignition control digital words. Each ignition digital word numerically represents an ignition timing requirement of the engine at a particular engine speed and throttle position. Each ignition digital word is stored at an address defined by a **4**-bit speed digital number proportional to reciprocal engine speed and a **4**-bit throttle digital number proportional to a throttle position. The fuel and ignition digital words are determined empirically by operating the engine at a variety of engine speeds and throttle positions that are expected to be encountered during actual operating conditions. The fuel and ignition timing requirements are recorded, are converted into **8**-bit digital numbers, and are loaded into the data memories. Of course, the values of the numbers change depending on the type of tuning and engine performance desired.

Data memory **170** also comprises a data address latch **178** that temporarily stores the address at which a desired digital word is stored and an instruction latch (IL) **180** that tells the data memory when to read out or read in data.

Analog to digital unit **190** comprises a wiper arm **196** of a potentiometer **194** that is controlled by accelerator pedal **96** through linkage **94**. An additional potentiometer **192** controlled by another engine operating characteristic, such as temperature, can also be provided. An input multiplexer **191** selects the potentiometer voltage to be converted and transmits it to an analog to digital converter **193**. Converter **193** converts the analog voltage on wiper arm **196** into a corresponding throttle digital number that is stored in an analog to digital register (ADR register) **198**. The operation of the converter is controlled by an instruction latch (IL) **200**.

Still referring to FIG. **3**, speed and position indicating assembly **210** comprises an engine member position predictor **212** of the type more fully described in the co-pending application of the present applicant and Bay E. Estes, III, entitles "Engine Member Position Predictor," filed, Dec. 12, 1972, U.S. Pat. Ser. No. 314,398, now U.S. Pat. No. 3,767,902, issued Oct. 23, 1973.

The assembly also comprises a clock sequence generator **214** that controls the time multiplex sequencing of the information flow within the system. Position predictor **212** receives input data from an engine crankshaft damper **220** that is fabricated with slots **221–224** displaced from each other by 90° of arc. The slots are rotated adjacent a conventional magnetic sensor **226** that detects changes in magnetic flux density. Each time a slot is rotated adjacent the sensor, an electronic circuit **228** produces a position or damper pulse having a standardized amplitude and duration. The slots and sensor are arranged so that the trailing edge of a position pulse occurs as each piston reaches its 6° before top dead center position. The repetition rate of the position pulses, of course, depends on the engine speed. Piston predictor **212** acts as an analog to digital converter by converting the repetition rate of the position pulses into a corresponding **8**-bit speed digital number that is stored in a speed register (SPR) **216**. The utilization of the number stored in the speed register is controlled by an instruction latch (IL) **218**. Position predictor **212** also produces **128** location pulses per 90° of engine rotation (crank-shaft rotation) on a conductor **901** in order to predict the exact location of the engine during its entire operating cycle.

Program memory **250** comprises a page zero digital program memory **252** and a page one digital program memory **256**. Each of these program memories contains operating instructions which enable other units of the system to control the production and timing of the fuel and fire signals. This is an important feature of the invention, since it enables the capability of the system to be expanded without necessitating changes in the physical structure of the system. For example, the system could be expanded to take into account engine operating characteristics other than engine speed and throttle position, such as intake manifold pressure, ambient air pressure, ambient temperature, and engine

temperature, in order to control the fuel and fire signals. These additional characteristics could be read into converter **193** by additional sensors, and could be used for control purposes by merely revising the operating instructions stored in the program memory.

Program sequencer **260** comprises a program counter (PCNT) **262** that causes the operating instructions from the program memory to be sequentially performed in a proper order. The sequencer also comprises a bus latch (BLT) **264** which enables every unit of the system to transmit data. Instructions are also sequenced by an RJMP latch **266** and an instruction latch (IL) **268.** Page select gates **270** and page select lines **272** determine whether an instruction will be read out of the page zero or page one program memories.

General purpose register unit **280** comprises a zero detect register **282,** an incrementing and complementing circuit **284,** and **16** separate general purpose registers **670–685** collectively identified by the number **286.** An instruction latch (IL) **288** controls the overall operation of the general purpose registers.

Arithmetic unit **300** comprises an instruction latch (IL) **302,** an **8**-bit full adder **304,** an **8**-bit SHA register **306,** a **1**-bit carry register **308,** an **8**-bit SHB register **310,** and a **1**-bit link bit register **312.** Arithmetic unit **300** provides a means for interpolating between the discrete fuel and ignition digital words stored in the data memory so that the precise fuel and ignition timing requirements of the engine can be determined.

The component units of selecting assembly **240,** i.e., program memory **250,** program sequencer **260,** general purpose register unit **280,** and arithmetic unit **300,** are programmed to select one or more fuel and ignition digital words stored in data memory **170** that at least approximately correspond to the fuel and ignition timing requirements of the engine at the speed and throttle position represented by the speed and throttle digital numbers stored in registers **216** and **198,** respectively. The selecting assembly also derives from the one or more selected digital words a resultant fuel control digital word and a resultant ignition control digital word that precisely define the fuel and ignition timing control requirements of the engine.

The resultant fuel and ignition digital words are used by timing circuitry **320** (FIG. 3A in order to control the fuel injectors and spark plugs of the engine. Timing circuitry **320** receives position pulses over conductor **229,** location pulses from assembly **210** over a conductor **901,** and a distributor reference signal from a distributor switch **321** that indicates the period of time during which cylinder one is in the ignition portion of its operating cycle.

Referring to FIG. 3A, timing circuitry **320** comprises an injection open-time (INO) register **322** that stores an **8**-bit open-time digital word representing the time at which each of the fuel injectors should open. Likewise, an injection duration (IND) register **324** stores the resultant fuel digital word derived by selecting assembly **240,** and an ignition timing (IGN) register **326** stores the resultant ignition digital word derived by the selecting assembly. The opening of injectors F1–F8 is controlled through an instruction latch (IL) **328** by an INO counter **330,** a shift register **332** and a clock gating circuit **334.** The duration of the fuel injection, i.e., the time during which each of injectors F1–F8 remains open, is controlled by IND counters **341–344,** correction registers **352–358** (corresponding to fuel injectors F1–F8, respectively), adder circuit **360** and output logic circuits **361–364.** Correction registers **351–358** hold correction digital numbers that adjust the amount of fuel injected into cylinders according to the individual fuel requirement variations of the cylinders. IND counters **341–344** are controlled by a two speed clock **366** that produces clock pulses which step or count the counters.

The firing of spark plugs S1–S8 is controlled through an instruction latch (IL) **371** by an ignition reference counter **376,** an ignition (IGN) counter **368,** and an output logic gate **370** that sets the ignition timing to a particular degree of advancement during starting.

Input/output circuit **372** provides a means of reading data into and out of the system. The circuit includes a conventional HEX display unit **374** that is capable of simultaneously displaying two digits in hexadecimal notation.

All units of the system are connected through a common communication bus **380** comprising **8** data lines **381–388, 3** instruction control lines **390–391, 3** clock lines **394–396** which are sequenced by clock sequence generator **214,** and **3** power lines **398–400** which supply DC voltage from power supply **166.** This communication bus is an important feature which allows each unit of the system to be placed at any location along the bus. New circuitry can be added at any point on the bus in order to increase the memory capacity, or for any other purpose, without rewiring any existing unit. Data is transmitted between various units of the system on the **8** data lines in a timemultiplexed manner determined by the states of the three clock lines.

The basic operation of the system, together with a preferred form of the method aspect of the invention will now be described:

Before the system can control an engine, the engine must be tested at the speed and throttle positions encountered during operation in order to determine its fuel and ignition timing requirements. These requirements vary depending on the type of engine operation desired. After the requirements have been determined numerically, they can be plotted in the form of a graph or map. Such a map showing the fuel requirements of an exemplary engine tuned for maximum performance is plotted in FIG. **4** wherein the X axis represents engine speed or RPM, the Y axis represents the position of the throttle or accelerator pedal **96,** and the Z axis represents a quantity of fuel in terms of milliseconds of injector open-time duration per engine revolution. Each point on the map corresponds to a fuel digital word stored at an address defined by a specific engine speed and a specific throttle position. Each fuel digital word represents the average fuel requirement of all eight cylinders of the engine. An analogous map could be plotted for ignition timing requirements.

Experience has shown that all cylinders of a typical internal combustion engine do not have the same fuel requirements. As a result, a single fuel digital word does not represent the precise fuel requirements of all engine cylinders. In order to provide precise fuel control for all cylinders of the engine, the individual fuel requirements of each cylinder are determined empirically and are converted into corresponding correction digital numbers. These numbers are loaded into correction registers **351–358** through input/output circuit **372** or from data stored in program memory **250.** Alternatively, read only registers can be used which perma-

nently retain the correction digital numbers. After the fuel and ignition maps have been plotted, the data from the map is read into data memory **170** through input/output circuit **372.** If a read only memory is used, this step is not necessary since the data is stored in the memory during the manufacturing process.

After the fuel and ignition digital words and the correction digital numbers are stored, operating instructions must be stored in program memory **250** through input/output circuit **372.** In the present system, approximately 250 operating instructions are stored in the form of discrete digital words. These operating instructions are sequentially initiated one-at-a-time by program sequencer **260.**

When the system is turned on, power supply **166** provides a start pulse which initializes the various registers and output lines of the system. For example, the open-time digital word stored in INO register **322** is initialized to regulate the time at which each injector opens to admit fuel to a cylinder.

After the initialization and input/output routines are completed, the reciprocal engine speed stored in speed register **216** is transmitted over the communication bus to register **685** in general purpose registers **286.** Register **685** is then incremented and checked for a zero condition in order to determine whether the engine is in an underspeed condition (e.g., being cranked by the starter) or whether the engine is at operating speed (i.e., idle speed or above). If a normal speed condition is detected, clock **366** is switched to its high speed state.

Selecting assembly **240** now selects four fuel digital words that are stored at addresses closely corresponding to the speed and throttle position at which the engine is being operated. The selection process is graphically illustrated in FIGS. **4** and **5.** (The actual speed digital number stored in register **216** and used in the selection process is inversely proportional to engine speed. However, for ease of explanation, FIG. **4** has been drawn as if the speed digital number were directly proportional to engine speed). As previously described, FIG. **4** represents a "map" of the **256** fuel digital words stored in digital memory **170.** If the engine is operating at a speed corresponding to an engine RPM of 65 along the X axis of FIG. **4** and a throttle position corresponding to 16 throttle position units along the Y axis of FIG. **4,** a resultant fuel digital word corresponding to the engine fuel requirement at these operating conditions would be located at word position *f***0.** By observing FIG. **4,** it will be noted that the fuel digital words most closely surrounding word position *f***0** are words *f***1**–*f***4.** In order to operate the engine, the selecting assembly first selects words *f***1**–*f***4** and then interpolates between the words in order to determine the value of the fuel quantity which would be represented if a fuel digital word were stored at location *f***0.** This fuel quantity is then stored as a resultant fuel digital word which indicates the precise engine fuel requirement at that engine speed and throttle position represented by the speed and throttle digital numbers stored in registers **216** and **198.** In the present example in which the engine speed is proportional to **65,** the number held in speed register **216** also corresponds to **65** in hexadecimal notation. This number is stored in register **216** as an **8**-bit binary number as follows: **01100101.** In this number, the first (left hand) **4** bits represent the number **6,** and the last (right hand) **4** bits represent the number **5.** The first **4** bits also represent a speed index or address line number corresponding to the address line **6***x* along the X axis of the FIG. **4** map, and the last **4** bits represent a speed residual number **5** corresponding to a fractional portion of the 16 unit increment between the index or address lines **6***x* and **7***x*. As a result of this arrangement, if the first **4** bits are separated from the second **4** bits, the speed index number can be separated from the speed residual number. In the present system, separation is carried out by shifting the **8**-bit speed number into SHA register **306** and by then shifting the speed number **4** bits to the left into SHB register **310.** At the end of this operation, the speed index number is held in the SHB register and the speed residual number is held in the SHA register.

After the speed index and speed residual numbers are calculated and stored, the instructions initiate an analog to digital conversion in converter **193** and store the results in the form of an **8**-bit digital throttle number in A/D register **198,** the throttle pot **196** having been selected through the multiplexer by previous instructions. The throttle number is transmitted through the communication bus to the SHA register where the throttle index number and throttle residual number are calculated in the same manner described with respect to the speed index and residual numbers. In the present example in which the throttle position is proportional to **16,** the throttle number held in register **198** also corresponds to **16** in hexadecimal notation. The number is stored in register **198** as an **8**-bit binary number as follows: **00010110.** In this number, the first (left hand) **4** bits represent the number **1** and the last (right hand) **4** bits represent the number **6.** As can be seen from FIG. **4,** throttle number **16** represents a throttle index number **1** corresponding to the address line *x***1** along the Y axis of the FIG. **4** map, and a throttle residual number **6** which corresponds to a fractional portion of the **16** unit increment between throttle index or address lines *x***1** and *x***2** of the FIG. **4** map. In FIG. **4,** the bit positions are reversed from the normal convention so that the most significant bit is positioned to the right of the least significant bit.

The speed index number and throttle index number are combined to designate the address of fuel digital word f**1** (FIG. **4**) by writing the **4**-bit speed index number to the left of the **4**-bit throttle index number. In hexadecimal notation, this number reads **61,** and its binary equivalent stored in the system registers is **01100001.** This number corresponds to the address of "corner" word f**1** from which the addresses of words *f***2**–*f***4,** which surround word location *f***0,** can be calculated. In order to calculate the value of the word location f**0** from the values of words *f***1**–*f***4,** the system solves the following interpolation equation:

$$f0\,(r_x, r_y) = w_1 f_1 + w_2 f_2 + w_3 f_3 + w_4 f_4/\Delta$$

where:

$$w_1 = \Delta - r_x - r_y + r_x r_y/\Delta$$

$$w_2 = r_y - r_x r_y/\Delta$$

$$w_3 = r_x r_y/\Delta$$

$$w_4 = r_x - r_x r_y/\Delta$$

rx = speed residual number,

$\Sigma wi = \Delta = 16$, ry = throttle residual number

The address of *f***2** is calculated by adding **1** to the ad-

dress of *f*1 (61). This is possible because *f*2 is located at the same speed index number as *f*1, namely 6, and is located at the next ascending throttle index number from *f*1, namely 2. As a result, the address of digital word *f*2 is 62. The address of digital word *f*4 is calculated by adding 15 to the address of word *f*2. This process can be visually represented in connected with FIG. 4 by assuming that the *f*2 address is incremented 15 times. As the integers are added to the *f*2 address, the resulting addresses would appear to move toward the left parallel to the Y axis until the throttle address line *x*F is reached. At this point, the addition of one more integer moves the address to throttle address line *x*0 and increases the speed index number by one digit to 7. After 15 integers have been added to the word *f*2 address, the address of word *f*4 is reached. As in the case of the word *f*1 address, the word *f*3 address may be calculated by adding the integer one to the word *f*4 address.

As soon as the addresses of words *f*1–*f*4 are known, the values of these words can be obtained from data memory **170**, and the rest of the terms of the interpolation equation may be calculated by conventional arithmetic techniques in order to determine the value of word location *f*0. This value is stored as a resultant fuel digital word in IND register **324**. A similar routine is used in order to analyze the data stored in ignition data memory **176** in order to obtain a resultant ignition digital word that is stored in the IGN register **326**.

Of course, if the engine speed and throttle position precisely correspond to an existing address in data memory **170**, the interpolation routine is not required. In addition, if enough fuel digital words are stored in data memory **170**, the different increments of speed and throttle position represented by the addresses will be sufficiently close to the actual engine operating conditions to obviate the need for interpolation.

Engine speed and throttle position are sampled every few milliseconds, and new resultant fuel and ignition digital words are stored in registers **324** and **326** at the same rate. As a result, any change in the values of the engine operating characteristics instantaneously results in resultant fuel and ignition digital words which represent the fuel and ignition timing requirements needed to meet the changed conditions. The resultant fuel and ignition digital words are used by timing circuitry **320** in order to individually operate each spark plug and fuel injector in the system at the appropriate time during the engine operating cycle.

Referring to FIG. 3A, timing circuitry **320** basically operates as follows:

Each time a position pulse related to cylinder **1** is received by INO counter **330**, the counter is loaded with the open-time digital number held in INO register **322**. Thereafter, the counter is stepped by divided location pulses until it overflows or reaches a predetermined value, thereby resetting shift register **332**. As soon as shift register **332** is reset, logic circuit **333** switches output logic circuit **363** that produces a fuel pulse which opens injector F1. Additional location pulses from the speed and position indicating assembly **210** trigger shift register **332** every 90° of engine rotation so that injectors F5, F4 and F2 associated with cylinders **5**, **4** and **2**, respectively, are sequentially opened. When a position pulse associated with cylinder **6** is received by the circuitry, the INO counter again is loaded and is stepped to produce a fuel signal that opens injector F6. Injector F6, instead of F1, is opened due to the condition of switch **321**. Thereafter, the location pulses from the speed and position indicating assembly **210** trigger shift register **332** every 90° of engine rotation in order to open injectors F3, F7 and F8 associated with cylinders **3**, **7** and **8**, respectively.

The duration of time during which the injectors remain open is determined by the value of the resultant fuel digital word stored in IND register **324** and the value of the correction digital numbers stored in correction registers **351–358**. As previously explained, the resultant fuel digital word stored in IND register **324** represents the average fuel requirement of all cylinders of the engine. However, the cylinders of the engine normally require a quantity of fuel which deviates from the average amount to a greater-or-lesser extent. Correction digital numbers which take into account the individual fuel requirement variation of each cylinder are loaded into correction registers **351–358**. As the injector associated with a cylinder is opened, the correction digital number held in the correction register associated with that cylinder is added to the number held in IND register **324** by adder circuit **360**, and the sum is loaded into one of IND counters **341–344**.

In response to a signal from logic circuit **333**, the loaded IND counter is stepped until it overflows or reaches a predetermined value. At that time, one of the output logic circuits **361–364** closes the correct injector, thereby terminating the injection of fuel in the cylinder.

The manner in which the resultant fuel and ignition digital words are used to control the fuel injectors and spark plugs can be more completely understood with reference to FIG. **6** and the following discussion of the operation of cylinder **1**.

FIG. **6** is a timing diagram representing a complete engine cycle or 720° of crankshaft rotation. If the timing diagram is circumscribed in a clockwise direction, radial lines **1–8** represent the top dead center positions of the pistons in the like-numbered cylinders in their proper firing order. Assuming the piston in cylinder **1** is approaching its 6° before top dead position A (i.e., its BTDC position) on the ignition phase of its operating cycle, a position pulse is produced by magnetic sensor **228**, and switch **321** is closed. As previously explained, since damper **220** consists of **4** slots arranged 90° apart, a position pulse is produced as each piston approaches its 6° BTDC position. As the piston in cylinder **1** passes its 6° BTDC position, switch **321** is open and the position pulse is terminated. A position pulse is terminated as each piston passes its 6° BTDC position.

The termination of the position pulse causes the **8**-bit open-time number in INO register **322** to be loaded into INO counter **330**. (FIG. 3A) As the crankshaft continues to rotate, counter **330** is stepped by clock pulses from clock gating circuit **334** which, in turn, receives location pulses transmitted over conductor **901** from speed and position indicating assembly **210**. Since assembly **210** produces 1.42 pulses per degree of crankshaft rotation, 128 pulses per 90° of crankshaft rotation are received over conductor **901**. This is an important feature because it enables the fire and fuel signals to be position dependent rather than time dependent. Of course, since the engine is rotating, the production of the signals can also be expressed in terms of time intervals. The location pulses are divided by

four in circuit **334** before they are used to step counter **330.** Counter **330** continues to be stepped until it overflows to its **0** count state. Output logic detects this condition and then switches shift register **332** to its **0** state. In response to the **0** state of shift register **332,** logic circuit **333** and output logic circuit **363** produce a fuel signal that is amplified by drive amplifier **116A** (FIG. **2**) so that injector **F1** opens at position B in FIG. **6.** The amount of rotational arc (and the time interval) between positions A and B of FIG. **6** is controlled by the value of the open-time digital word. Thus, by merely changing the value of this word, the opening time of the fuel injectors can be adjusted to suit changing engine conditions. For example, an open-time digital word resulting in relatively early opening of the injectors can be used during starting to facilitate the production of a rich fuel mixture.

As soon as shift register **332** has been switched to its **0** state, the **4**-bit correction digital number stored in correction register **351** (corresponding to cylinder **1**) is added by adder **360** to the **4** least significant bits of the resultant fuel digital word stored in IND register **324.** If an overflow bit is produced by this operation, it is added to the most significant **4** bits of the resultant fuel digital word. The corrected resultant fuel digital word is loaded into IND counter **343** which is stepped by clock pulses having a period of 50 microseconds produced by clock **366.** As soon as counter **343** overflows to its **0** state, output logic circuit **363** terminates the fuel signal to injector **F1,** thereby closing the injector and preventing further fuel from being injected into cylinder **1.** As shown in FIG. **6,** the fuel signal terminates at position D. This position is 18° prior to the closure of the intake valve for cylinder **1.** Of course, the precise location of position D will vary depending on the value of the corrected resultant fuel digital word loaded into counter **343.**

As fuel is injected into the intake manifold adjacent cylinder **1** by injector **F1,** it is mixed with air from air horn **90.** The resulting fuel-air mixture is drawn into cyliner **1** as soon as the intake valve for cylinder **1** opens. After the fuel-air mixture has been drawn into cylinder **1** and the intake valve has closed, the piston in cylinder **1** moves toward its 90° BTDC position (position E in FIG. **6**). During this time, a position pulse used in connection with cylinder **8** is generated and is used to load reference counter **367.** The reference counter is stepped by location pulses from speed and position indicating assembly **210.** The number loaded into the reference counter is adjusted so that the crankshaft will rotate through about 45° of arc before the reference counter overflows. This technique establishes a new reference point for loading IGN counter **368** which is approximately 51° prior to the TDC position of the piston in cylinder **1.** As soon as the reference counter overflows to its **0** state, the **8**-bit resultant ignition digital word stored in IGN register **326** is loaded into IGN counter **368,** and this counter also is stepped with location pulses from speed and position indicating assembly **210.**

As soon as IGN counter **368** overflows to its **0** state, a fire signal is produced on conductor **369** which causes high voltage generator **130** to generate a high voltage that is transmitted to top terminal **134** of rotary distributor **132** (FIG. **2**). At this point in time, rotor **136** of distributor **132** passes adjacent electrode **141** so that spark plug **S1** is fired. In this example, the value of the resultant ignition digital word stored in IGN register **326** caused spark plug **S1** to fire when the piston in cylinder **1** is in its 12° BTDC position (position F in FIG. **6**). Of course, the exact position at which spark plug **S1** fires depends on the value of the resultant ignition digital word.

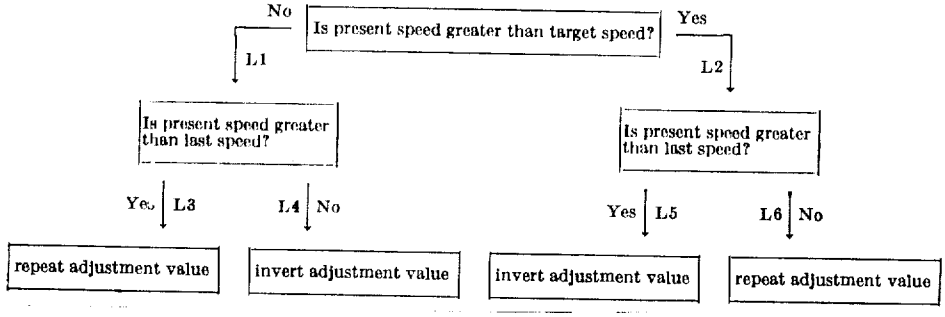
Timing circuitry **320** operates cylinder **6** in the same manner as cylinder **1.** As previously explained, the remaining cylinders are also operated in an analogous manner, except that shift register **332** is switched by gating circuit **334** rather than INO counter **330.**

When the engine is being started, the foregoing procedures are altered somewhat by the instructions loaded in program memory **250.** As previously noted, the **8**-bit speed digital number loaded into speed register **216** is inversely proportional to the speed of the engine. Speed and position indicating assembly **210** is designed so that the maximum possible number is loaded into the speed register if the engine speed falls below about 300 RPM. As a result, during starting, the speed register is loaded with the number FF in hexadecimal notation. In order to check for an underspeed or starting condition, the speed digital number stored in speed register **216** is transmitted to register **685** of general purpose register unit **280.** Register **685** is then incremented (i.e., the number one is added to the register contents), and the result is checked for a zero condition. If a zero condition is detected, the circuitry selects the low speed of clock **366** which produces pulses having a period of 400 microseconds. An open-time digital number is loaded into INO register **322** which opens the injectors at the earliest time practical. In addition, a long count number is loaded into IND counters **341–344** which, together with the slow speed of clock **366,** provides a fuel signal for each cylinder having a duration of about 20 milliseconds. This relatively long fuel signal duration provides a rich fuel mixture which is required in order to start the engine. During engine starting, reference counter **367,** IGN counter **368,** and IGN register **326** are not used. The fire signal is obtained directly from the position pulse which occurs at the 6° BTDC position of each piston. This mode of operation is achieved by logic gate **370** under control of an LOF signal which is automatically produced by position indicating assembly **210** whenever engine RPM is below about 300 RPM.

If the throttle is closed and the automatic idle routine has been switched on by the operator, the foregoing procedure is again altered by the instructions stored in program memory **250.** During the automatic idle routine, the system holds the engine speed at a specified target RPM by changing fuel signal duration. Fuel signal duration is repeatedly changed by a relative small adjustment or delta value which is added to or subtracted from the value of the resultant fuel digital word in order to achieve and maintain the target RPM. Basically, the system compares the present engine speed with the last-measured engine speed and the target speed in order to determine whether the adjustment value or its inverse should be applied to the resultant fuel digital word. The adjustment value or its inverse is combined with the resultant fuel digital word so that the engine speed keeps progressing toward the target speed. For example, if the engine speed is greater than the target speed, but the last application of the adjustment value moved it closer to the target speed, the adjustment value is repeated. Likewise, if the present

speed is less than the target speed, but the last application of the adjustment value increased the engine speed toward the target speed, the adjustment value is repeated. If the last application of the adjustment value moved the present speed away from the target speed, the adjustment value is inverted and again combined with the resultant fuel digital word in order to move the engine speed toward the target speed. The process is described by the following logic Diagram A.

Logic Diagram A



In order to achieve this mode of operation, the system stores in registers a target digital number representing the target speed, the last previous speed digital number held in speed register **216**, and a delta digital number representing a small change in the normal magnitude of the resultant fuel digital word. The present speed digital number held in register **216** is also utilized. Using these numbers, the system produces logic signals representing logical decisions L1–L6 shown on Diagram A.

If logic signals corresponding to decisions **L3** or **L6** are generated, the value of the delta digital number is added to the resultant fuel digital word before it is used in IND counters **341–344.** If logic signals corresponding to decisions L4 and **L5** are generated, the value of the delta digital number is inverted before it is added to the resultant fuel digital word.

DETAILED DESCRIPTION

The following description is given in terms of negative logic. That is, a voltage level corresponding to a logic state **1** is more negative than a voltage level corresponding to a logic state **0.**

COMMUNICATION BUS **380**, TIME MULTIPLEXING, AND INFORMATION TRANSFER

Each instruction in program memory **250** is executed during eight successive time slots designated T1 . . . T8. The state of clock lines **394–396** (designated CL1, CL2, and CL3 respectively) defines the time slot in which the system operates. These clock lines are available to every unit of the system through communication bus **380.**

The states of the clocklines which define the eight time slots T1–T8 are shown in FIG. 7D in the sequence in which they occur. This sequence is never modified. Clock lines CL1, CL2 and CL3 sequence through a reflected Gray code in which only one line changes state at a time.

Information transfer within the system is accomplished through time-multiplexed communication bus **380** and associated memory. In addition to data lines **381-388** that are available to every unit in the system, the bus includes control line **390** which carries a $\overline{\text{WRTB}}$ instruction permitting any unit in the system to place data in **8**-bit bus latch **264.** The data present on the bus data lines varies according to the time slot and instruction being executed as follows:

Time Slot T1: Bus lines are charged to **1** states by low impedance active devices.

Time Slot T2: Data from program memory **250** is placed on the bus. This data is the code for the instruction that is to be executed during the current T time slot sequence.

Time slot T3: Bus lines are charged to **1** states by low impedance active devices.

Time Slots T4–T8: If the instruction to be executed is a single word instruction, the data contained in the associated **8**-bit bus latch is placed on the bus. All instructions are single word instructions with the exceptions of JMPM, WBSI, JMPO, JMP1, JMP2 and JMP3.

Time Slots T4–T5: (Double word instructions.) The bus is left in an idling state. In this state, the bus lines are maintained at **1** states (where they were put at T3) by pull-up devices with sufficient drive to supply any leakage currents required by the system.

Time Slots T6–T7: (double word instructions.) Data from program memory **250** is place on the bus.

Time Slot T8: (Double word instructions.) The bus returns to the idle state described above.

Any unit in the system can communicate with any other unit by transmitting **8**-bit data words to bus latch **264** through the bus. The unit that needs to transmit data places it in the bus latch during the execution of some instruction, and the unit that requires the data reads it from the bus during the next or some future instruction execution.

Data is presented in the bus as follows: Some time prior to time slot T6, the $\overline{\text{WRTB}}$ line **390** is pulled to its **0** state. This line is held at its **0** state through time slot T8 and is released at time slot T1 of the next instruction. Bus latch **264** is set to all **1** states and the bus lines are charged to **1** states by active devices whenever line **390** is at its **0** state during time slot T6. The data that is to be stored in the bus latch is presented to the bus at time slot T7 and is held stable through time slot T8. The data is removed at the end of time slot T8.

COMMON ELECTRONIC ELEMENTS

The major units of this system connected together by the communication bus shown in FIG. **2** are described in more detail in connection with FIGS. 7A–15D. There are many electronic elements common to each of these FIGURES. For example, the FIGURES de-

scribe NOR gates N1–N727, inverters I1–I290, D-type flip-flops D1–D60, bipolar transistors T1–T25, MOS field effect transistors M1–M112, capacitors C1–C2, and resistors R1–R179.

DATA MEMORY 170

Data memory **170** is shown in more detail in FIGS. 7A and 7B. As shown on the drawings, address latch **178** comprises bit latches **402, 404** and instruction latch **180** comprises bit latches **406, 408.** These latches, together with all other 4-bit latches in the system, are shown in more detail in FIG. 7E.

Data memory **170** further comprises gating circuits **410** which enable external data entry into the memory chips in a convenient manner. A data-in cable **412** and a memory select cable **414** control the memory when data is read into the memory chips from an external source. Communication with the program sequencer is provided through a program address bus **416** comprising conductors **421–428.** A memory address bus **430** provides a means for locating digital words at a particular address within the injection memory chips **432–439** and the ignition memory chips **442–449** (FIG. 7B). Each of these chips comprises a conventional **256** bit memory such as memory part no. **1101** manufactured by Intel Corporation.

Chip selection gates **464** energize select line **450** or **451** to determine whether the injection memory chips or the ignition memory chips will transfer their data onto the communication bus. Conductors **452–455** provide additional paths for transmitting signals among certain elements of the data memory.

Referring to FIG. 7B, the data memory **170** further comprises a timing decoding circuit **460** and an instruction decoding circuit **462.**

ANALOG TO DIGITAL UNIT 190

Referring to FIGS. 8A–8C, analog to digital unit **190** comprises a power supply **470** which supplies a plus 15 volt voltage line **471** and a minus 15 volt voltage line **473.** In addition, conventional regulator **472** provides a supply voltage of about 10 volts which biases throttle potentiometer **194.** Input multiplexer **191** determines which of input channels **0–3** will be analyzed by the apparatus. The output of multiplexer **191** is connected to analog to digital converter **193** which may be of a standard type such as Model L–8B–1–B–1 manufactured by Datel Systems, Inc. Converter **193** also includes A/D register **198** shown in FIG. **3.**

Unit **190** further comprises a voltage level shifting circuit **478,** output enable gates **480,** an input line select latch **482,** a voltage level shifting circuit **484,** an input sensing gate **486,** and output latches **488.**

As shown in FIG. 8C, instruction latch **218** comprises 4-bit latches **490** and **491** of the type shown in FIG. 7E. Timing decoding gates **492** and instruction decoding gates **494** are used to operate unit **190** from the communication bus. Conductors **496–528** provide additional connections between various elements of the circuitry.

SPEED AND POSITION INDICATING ASSEMBLY 210

FIG. 9A illustrates clock sequence generator **214** in detail. The generator comprises a precision crystal **531** that operates at 2.56 megahertz and has its output divided by 8 in order to produce a control signal at 320 kilohertz. This control signal is used to produce time slots T1–T8, each having a 1562.5 nanosecond duration which corresponds to a 640 kilohertz timeslot rate or an instruction execution rate of 80,000 per second.

Referring to FIG. 9B, speed register **216** comprises registers **530, 532.** Assembly **210** also contains upcounters **534, 535,** a down counter **536,** a full adder **537,** and an accumulator **538,** all connected as shown.

Referring to FIG. 9C, assembly **210** further comprises timing decoding gates **540,** instruction decoding gates **542,** and an instruction latch **544** that controls the operation of the assembly from the communication bus.

An output driver circuit **546** enables the speed register **216** to transfer data to the communication bus. Conductors **548–561** connect various elements of the assembly.

PROGRAM MEMORY 250

Referring to FIG. 7B, page **0** memory **252** comprises memory chips **563–570,** and page **1** memory **256** comprising memory chips **573–580.** Each of these memory chips is identical to the chips of ignition data memory **176.**

Referring to FIG. 7A, page select lines **272** comprise conductors **582** and **583** that are connected to the program sequencer and which transmit selection signals to the page **0** and page **1** memories through conductors **584** and **585,** respectively.

PROGRAM SEQUENCER 260

Referring to FIGS. **10A** and **10B,** program counter **262** of program sequencer **260** comprises conventional **4** bit counters **590** and **591.** The sequencer also comprises inhibitable, non-inverting buffers **594–601** shown in more detail in FIG. **10E.**

As explained previously, bus latch **264** provides a means for every unit of the system to transmit data over the communication bus. The bus latch consists of **8** latches like the one shown in FIG. **10D.**

Referring to FIG. **10A,** RJMP latch **266** comprises **4**-bit latches **604** and **605;** instruction latch **268** comprises **4**-bit latches **606** and **607;** and a jump latch **608** comprises 4-bit latches **610** and **611,** all of the type shown in FIG. 7E.

Referring to FIG. **10B,** the program sequencer further comprises timing decoding gates **614** and a buffer amplifier **617.** Page selected gates **270** select either the page **0** or page **1** memory chips in the program memory. The remainder of gates shown on FIG. **10B** are for instruction decoding purposes. The program sequencer also includes conductors **618–646** which interconnect various units of the circuitry.

GENERAL PURPOSE REGISTER UNIT 280

Incrementing and complementing circuit **284** of general purpose register unit **280** is shown in more detail in FIG. **11A.** The circuit comprises storage enable gates **650** that enable a temporary storage latch **652** to hold information used in complementing select gates **654** in order to perform the function of complementing the data transmitted to their inputs. An incrementer **656** adds **1** to the least significant bit of the data complemented by select gates **654.**

Referring to FIG. **11B,** general purpose register unit **280** further comprises select gates **658,** bus precharge gates **660,** and data output gates **662.** Bus precharge gates **660** are controlled through a buffer amplifier **663.**

Referring to FIG. **11C,** general purpose register unit **280** also comprises timing decoding gates **664** and in-

struction decoding gates **666.** Instruction latch **288** consists of **4**-bit latches **667** and **668** of the type shown in FIG. **7E.**

Referring to FIGS. **11D** and **11E**, general purpose registers **286** comprises register chips **670–685.** Each of these register chips comprises eight circuits of the type shown in FIG. **11H.**

Referring to FIG. **11F**, general purpose register unit **280** also comprises register decode gates **688.** Zero register detect gate **282,** as shown in FIG. **11F**, comprises a multiple input NOR gate. In addition, conductors **691–762** are used to conduct signals between various elements of the general purpose registers.

ARITHMETIC UNIT **300**

Referring to FIG. **12A**, full adder **304** comprises eight circuits of the type shown in detail in FIG. **12G.** Arithmetic unit **300** also comprises select gates **768** which determine the origin of the data which is added in adder **304.** Enable gates **770** transmit data on the communication bus into adder **304.** An add **1** circuit **772** adds **1** to the total in counter **304** if the value stored in the carry bit or link bit registers equals **1.**

FIG. **12B** describes in detail an output circuit for transmitting data stored in the SHA or SHB registers to the bus. SHA register **306,** carry bit register **308,** SHB register **310** and a link bit register bit **312** are each shown in detail in FIG. **12C**, and each comprises one or more D-type flip-flops.

Referring to FIG. **12D**, arithmetic unit **300** also comprises a temporary storage register **774** and select gates **776** that route data from the temporary storage register or the bus to the SHA or SHB registers.

Referring to FIG. **12E**, instruction latch **302** of arithmetic unit **300** comprises latches **764** and **765** of the type shown in FIG. **7E.** Timing decoding gates **778** and instruction decoding gates **780** also are shown in FIG. **12E.** In addition, signals are transmitted between the various elements of the arithmetic unit by conductors **782–862.**

TIMING CIRCUITRY **320**

INO Register **322,** INO Counter **330,** shift register **332,** logic circuit **333** and gating circuit **334** are shown in more detail in FIG. **13A.**

Referring to FIGS. **13A–13D**, the injection portion of timing circuitry **320** further comprises an engine synchronizing circuit **864** that switches engine synchronizing conductor **866** to its **1** state when cylinder **1** or **6** is at its 6° before top dead center position.

IND counters **341–344,** output logic circuits **361–364** and clock **366** are shown in more detail in FIG. **13B.**

IND Register **324,** correction registers **351–358,** and adder **360** are shown in more detail in FIG. **13C.** Adder **360** comprises a **4**-bit incrementer **885** connected to the **4** most significant bits of IND register **324,** a **3**-bit full adder having its carry output connected to incrementer **885,** and a half adder **887,** all connected as shown.

As shown in FIG. **13D**, instruction latch **328** comprises instruction latches **866** and **867** of the type shown in FIG. **7E.** In addition, the injection portion of timing circuitry **320** comprises instruction decoding gates **868** and timing decoding gates **870.** Signals are transmitted between various portions of the timing circuitry by conductors **872–884.** Additional connections between the elements of FIGS. **13A–13D** are identicated by like timing and instruction mnemonics associated with like conductors.

The ignition control portion of timing circuitry **320** is shown in FIGS. **14A** and **14B.** Aside from the components shown in FIG. **3A**, the circuit also comprises pulse standardizing gates **890** that convert the damper position pulse into pulses of uniform duration commencing at time slot **T7.** As shown in FIG. **14B**, instruction latch **371** comprises **4**-bit instruction latches **892** and **894** of the type shown in FIG. **7E.** The circuit also comprises timing decoding gates **896** and an instruction decoding NOR gate **898.** Signals are transmitted between various elements of the circuitry over conductors **900–906.**

INPUT/OUTPUT CIRCUIT **372**

Referring to FIG. **15A**, input/output circuit **372** comprises an output register OR1 consisting of flip-flops D45–D51 and an output register OR2 consisting of flip-flops D52–D59. The output registers operate a lamp drive circuit **908** that drives one incandescent lamp for each output register flip-flop. Exemplary lamps **909, 910** are shown in the drawings.

Referring to FIG. **15B**, Circuit **372** also comprises a bus drive circuit **911** that writes data to the bus. A gating circuit **912** writes data in a predetermined one of **16** bit positions, and a gating circuit **913** clears data from a predetermined one of **16** bit positions. The data and the bit position are determined by an instruction from the program memory.

Referring to FIG. **15C**, circuit **372** comprises **16** input lines **917–932,** each input line being controlled by a manual switch, such as switch **934** and being biased by a resistor, such as resistor R**199.**

The input lines are also identified by hexadecimal notation as lines **0–F.** The input lines aree divided into two groups of eight lines each. A selection circuit **914** selects either one group or the other for reading data into the system. Another selection circuit **915** samples a predetermined one of the input lines, and, if the sampled line is at a logical **1** state, initiates a SKIP instruction. For example, in response to an SKB5 instruction, circuit **915** samples conductor **922,** and if the conductor is in its logical **1** state, initiates a SKIP instruction over conductor **391.**

Referring to FIG. **15D**, circuit **372** also comprises an instruction latch **936** consisting of **4**-bit latches **937** and **938** of the type shown in FIG. **7E.** A timing decoding circuit **939** decodes the time slots transmitted over clock lines **394–396.** The remaining circuitry shown in FIG. **15D** is for instruction decoding purposes. This circuitry includes **8**-bit latches **937** and **938** which serve a dual purpose. The latches set or reset individual bits in output registers OR1, OR2, and they sense individual bits in input lines **917–932.** Instructions from the program memory determine which bit is acted on by the latches.

As previously explained, the system described in the drawings operates in accordance with operating instructions stored in program memory **250** and sequenced by program sequencer **260.** The system is capable of executing each of the instructions defined as follows:

INSTRUCTION DEFINITIONS

Instruction Mnemonic	Actual Instruction Stored In Program Memory	Description of Instruction
ADDA	60	ADD BUS TO SHA REGISTER
ADDB	61	ADD BUS TO SHB REGISTER
ADDL	62	ADD 1 TO SHB REGISTER IF LINK BIT IS SET
ACYA	63	ADD 1 TO SHA IF CARRY BIT IS SET (CLEAR CARRY)
ACYB	64	ADD 1 TO SHB IF CARRY BIT IS SET (CLEAR CARRY)
CLBS	50	CLEAR BUS TO ZERO
CLBX	AX	CLEAR (RESET) BIT X OF 16 BIT I/O OUTPUT
CLCY	65	CLEAR CARRY BIT
CONV	80	INITIATE A/D CONVERSION
IRGX	0X	INCREMENT REGISTER X (ADD 1)
JMPB	51	JUMP TO PAGE ADDRESS TAKEN FROM BUS
JMPM	52	JUMP AND MARK ADDRESS FOLLOWING JUMP ADDRESS FOR RJMP COMMAND (SAVE RETURN)
JMP0	54	JUMP TO PAGE ADDRESS IN PAGE 0, CONTAINED IN NEXT WORD
JMP1	55	JUMP TO PAGE ADDRESS IN PAGE 1, CONTAINED IN NEXT WORD
JMP2	56	JUMP TO PAGE ADDRESS IN PAGE 2, CONTAINED IN NEXT WORD
JMP3	57	JUMP TO PAGE ADDRESS IN PAGE 3, CONTAINED IN NEXT WORD
LIND	96	LOAD INJECTOR DURATION (IND) REGISTER
LIN0	95	LOAD INJECTOR OPEN TIME (IN0) REGISTER
LRGX	1X	LOAD REGISTER X FROM BUS
LOR1	78	LOAD OUTPUT REGISTER OR1 FROM BUS
LOR2	79	LOAD OUTPUT REGISTER OR2 FROM BUS
LSHA	66	LOAD SHA REGISTER FROM BUS
LSHB	67	LOAD SHB REGISTER FROM BUS
LSPK	90	LOAD IGNITION TIMING REGISTER 326 FROM BUS
LT16	91	LOAD CORRECTION REGISTERS 351 AND 356 FROM BUS
LT53	92	LOAD CORRECTION REGISTERS 355 AND 353 FROM BUS
LT47	93	LOAD CORRECTION REGISTERS 354 and 357 FROM BUS
LT28	94	LOAD CORRECTION REGISTERS 352 AND 358 FROM BUS
RJMP	58	RETURN TO LAST MARKED ADDRESS (BY JMPM)
RST0	89	RESET A/D OUTPUT BIT 0
RST1	8A	RESET A/D OUTPUT BIT 1
RST2	8B	RESET A/D OUTPUT BIT 2
SBT0	86	SET A/D OUTPUT BIT 0
SBT1	87	SET A/D OUTPUT BIT 1
SBT2	88	SET A/D OUTPUT BIT 2
SEL0	8F	SELECT CHANNEL 0 FOR A/D
SEL1	8E	SELECT CHANNEL 1 FOR A/D
SEL2	8D	SELECT CHANNEL 2 FOR A/D
SEL3	8C	SELECT CHANNEL 3 FOR A/D
SEN0	82	SENSE A/D INPUT BIT 0. IF 1 SKIP 2.
SEN1	83	SENSE A/D INPUT BIT 1. IF 1 SKIP 2.
SEN2	84	SENSE A/D INPUT BIT 2. IF 1 SKIP 2.

INSTRUCTION DEFINITIONS-Continued

Instruction Mnemonic	Actual Instruction Stored In Program Memory	Description of Instruction
SEN3	85	SENSE A/D INPUT BIT 3. IF 1 SKIP 2.
SHFC	98	SELECT HIGH FREQUENCY CLOCK FOR INJECTOR TIMING
SHF1	68	SHIFT SHA AND SHB LEFT 1 (THRU LINK AND CARRY)
SHF2	69	SHIFT SHA AND SHB LEFT 2 (THRU LINK AND CARRY)
SHF3	6A	SHIFT SHA AND SHB LEFT 3 (THRU LINK AND CARRY)
NOOP	FF	PERFORMS NO OPERATION. THIS IS USED TO PROVIDE SPACES EITHER FOR SKIP TYPE INSTRUCTIONS OR IN ANTICIPATION OF NEED FOR FUTURE PROGRAM CHANGES IN SPECIFIC INSTRUCTION SEQUENCES
SKBX	CX	SKIP 2 IF BIT X OF 16 BIT I/O IS 1
SKNC	6B	SKIP 2 IF CARRY IS NOT SET
SLFC	97	SELECT LOW FREQUENCY CLOCK FOR INJECTOR TIMING
SRGX	2X	SKIP 2 IF REGISTER X IS ZERO
TRGX	3X	TWO'S COMPLEMENT REGISTER X (NEGATE)
WBSI	53	WRITE CONTENTS OF NEXT WORD TO BUS
WDT1	70	WRITE DATA FROM INJECTOR DATA MEMORY TO BUS
WDT2	71	WRITE DATA FROM IGNITION DATA MEMORY TO BUS
WIR1	7A	WRITE INPUT REGISTER 1 (16 BIT I/O) TO BUS
WIR2	7B	WRITE INPUT REGISTER 2 (16 BIT I/O) TO BUS
WISP	72	WRITE ENGINE SPEED TO BUS
WRAD	81	WRITE RESULTS OF A/D CONVERSION TO BUS
WRBX	BX	WRITE (SET) BIT X OF 16 BIT I/O
WRGX	4X	WRITE CONTENTS OF REGISTER X TO BUS
WSHA	6C	WRITE CONTENTS OF SHA REGISTER TO BUS
WSHB	6D	WRITE CONTENTS OF SHB REGISTER TO BUS

The foregoing instructions have been used to develop a program carried out by the program sequencer which operates the system in the manner described above.

PROGRAM

GENERAL PURPOSE REGISTER ASSIGNMENTS

REGISTER	670	(0)	RX : W4
REGISTER	671	(1)	RY : W1
REGISTER	672	(2)	USED TO INDICATE INJ (00)/IGN (01) TO INTERP
REGISTER	673	(3)	TEMP USED BY INTERP
REGISTER	674	(4)	UNUSED
REGISTER	675	(5)	LCNT FOR AUTO-IDLE ROUTINE
REGISTER	676	(6)	MULTIPLIER FOR BOTH MULT ROUTINES : TEMP
REGISTER	677	(7)	W3
REGISTER	678	(8)	W2
REGISTER	679	(9)	DELTA FOR AUTO-IDLE ROUTINE
REGISTER	680	(A)	LRPM (PREVIOUS RPM) FOR AUTO-IDLE
REGISTER	681	(B)	IGNITION FUDGE VALUE
REGISTER	682	(C)	INJECTOR FUDGE VALUE
REGISTER	683	(D)	CURRENT INJECTOR OPEN COUNT
REGISTER	684	(E)	YI : AFI
REGISTER	685	(F)	ENG SPEED : XI : RET FOR INTERP : TEMP

SWITCH ASSIGNMENTS

(0) SOURCE/DESTINATION (S/D) SWITCH (LSB)
(1) SOURCE/DESTINATION (S/D SWITCH
(2) SOURCE/DESTINATION (S/D SWITCH (MSB)
(3) DISPLAY DATA FROM SOURCE SPECIFIED BY S/D SWITCHES
(4) ENTER DATA TO DESTINATION SPECIFIED BY S/D SWITCHES
(5) OUTPUT CURRENT IGNITION TIMING
(6) OUTPUT CURRENT INJECTOR DURATION
(8) LSB DATA ENTRY SWITCH
.
.
(15) MSB DATA ENTRY SWITCH

Program Memory Address Page	Address Within Page	Instruction	STRT 000: Instruction Mnemonic	Operation Performed
0	00	53 START	WBSI 88	INITIALIZE ALL CORRECTION REG. TO MIDPOINT
0	01	88		
0	02	91	LT16	
0	03	92	LT53	
0	04	93	TL47	
0	05	94	LT28	
0	06	50	CLBS	CLEAR 16 BIT OUTPUT REGISTERS
0	07	78	LOR1	
0	08	79	LOR2	
0	09	1B	LRGB	ZERO FUDGE VALUES
0	0A	1C	LRGC	
0	0B	19	LRG9	INITIALIZE AUTO-IDLE
0	0C	1A	LRGA	
0	0D	89	RST0	CLEAR A/D OUTPUT BITS
0	0E	8A	RST1	
0	0F	8B	RST2	
0	10	53	WBSI F0	
0	11	F0		
0	12	1D	LRGD	INITIALIZE OPEN COUNT (INO) REGISTER 322
0	13	55 BEGIN	JMP1 DSPLY	GO CHECK FOR DISPLAY REQ. AND DATA IN
0	14	C3		
0	15	72 CONT	WISP	WRITE ENGINE SPEED FROM SPEED REGISTER 216 TO BUS
0	16	1F	LRGF	SAVE IT IN REGISTER 685 (F)
0	17	0F	IRGF	CHECK FOR UNDER-SPEED CONDITION BY INCREMENTING REGISTER 685
0	18	2F	SRGF	TEST FOR ZERO (UNDER-SPEED=CRANKING)
0	19	54	JMP0 ENT1	PATH FOR NON UNDER-SPEED
0	1A	27		
0	1B	97	SLFC	SELECT LOW FREQUENCY OF CLOCK 366
0	1C	53	WBSI CE	PICK 20 MS INJECTOR DURATION
0	1D	CE		
0	1E	96	LIND	GIVE IT TO MAIN INJECTOR DURATION (IND) REGISTER 324
0	1F	53	WBSI F0	PICK A QUICK OPEN COUNT
0	20	F0		
0	21	95	LIN0	GIVE IT TO INJECTOR OPEN (INO) REGISTER 322
0	22	53	WBSI 81	PICK UP 6° BTDC FOR IGNITION TIMING (FOR EXIT)
0	23	81		
0	24	90	LSPK	GIVE IT TO IGNITION TIMING (IGN) REGISTER 326
0	25	54	JMP0 BEGIN	GO KEEP WATCH ON ENGINE SPEED
0	26	13		
0	27	98 ENT1	SHFC	SELECT HIGH FREQUENCY OF CLOCK 366
0	28	66	LSHA	BEGIN CALCULATION OF SPEED INDEX (XI)

SCALE ENGINE SPEED VALUE FOR MAP CONTROL ROUTINE

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
0	29	50	CLBS	
0	2A	67	LSHB	
0	2B	6A	SHF3	FORM WISP/2 IN SHB
0	2C	6A	SHF3	
0	2D	68	SHF1	
0	2E	65	CLCY	
0	2F	4F	WRGF	PICK UP WISP + 1 FROM REG. 685
0	30	61	ADDB	SHB = WISP + (WISP/2) + 1
0	31	6D	WSHB	GET RESULTS TO BUS
0	32	6B	SKNC	CHECK FOR CARRY (SPEED ABOVE CRANKING BUT LOW)
0	33	53	WBSI FF	INDICATE LOWEST POSSIBLE MAP SPEED
0	34	FF		
0	35	1F	LRGF	

MAP CONTROL ROUTINE

0	36	8F	SEL0	SELECT CHANNEL 0 ON A/D CONVERTER (THROTTLE CHANNEL)
0	37	80	CONV	INITIATE A/D CONVERSION
0	38	50	CLBS	BEGIN CALCULATION OF RX, RY, XI AND YI
0	39	67	LSHB	CLEAR SHB REGISTER 310
0	3A	4F	WRGF	ENGINE SPEED TO BUS
0	3B	66	LSHA	ENGINE SPEED TO SHA REGISTER 306

MAP CONTROL ROUTINE—Continued

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
			STRT 000:	
0	3C	69	SHF2	SHIFT SHA REGISTER 306 AND SHB REGISTER 310 LEFT 2 BITS
0	3D	69	SHF2	SHIFT SHA REGISTER 306 AND SHB REGISTER 310 LEFT 2 BITS
0	3E	6D	WSHB	SHB REGISTER NOW HAS SPEED INDEX (XI)
0	3F	1F	LRGF	XI TO REGISTER 685 (F)
0	40	50	CLBS	
0	41	67	LSHB	CLEAR SHB REGISTER
0	42	69	SHF2	SHIFT LEFT 4 MORE BITS
0	43	69	SHF2	
0	44	6D	WSHB	SHB REGISTER NOW HAS SPEED RESIDUAL (RX)
0	45	10	LRG0	RX TO REGISTER 670 (O)
				NOW GET YI AND RY
0	46	50	CLBS	
0	47	67	LSHB	CLEAR SHB REGISTER
0	48	81	WRAD	BEGIN CHECK FOR THROTTLE OUT OF RANGE
0	49	66	LSHA	
0	4A	65	CLCY	
0	4B	53	WBSI 10	GET TEST CONSTANT TO BUS
0	4C	10		
0	4D	60	ADDA	THIS ADD WILL CARRY IF THROTTLE IS TOO LARGE
0	4E	6B	SKNC	TEST FOR CARRY
0	4F	54	JMP0 ENT4	GO FIX THINGS UP IF TOO LARGE
0	50	6F		
0	51	81	WRAD	A/D CONVERTER RESULT TO BUS
0	52	66 ENT5	LSHA	THROTTLE (VALUE) TO SHA REGISTER
0	53	69	SHF2	SHIFT TO LEFT 4 BITS
0	54	69	SHF2	
0	55	6D	WSHB	SHB REGISTER NOW HAS THROTTLE INDEX (YI)
0	56	1E	LRGE	YI TO REGISTER 684 (E)
0	57	50	CLBS	
0	58	67	LSHB	CLEAR SHB REGISTER
0	59	69	SHF2	SHIFT LEFT 4 MORE BITS
0	5A	69	SHF2	
0	5B	6D	WSHB	SHB REGISTER NOW HAS THROTTLE RESIDUAL (RY)
0	5C	11	LRG1	RY TO REGISTER 671 (1) NOW GO THROUGH AUTO-IDLE ROUTINE IF FUDGE DELTA IS NON-ZERO. GOAL HERE IS TO FUDGE INJECTOR DURATION, WHENEVER THROTTLE IS IN THE CLOSED POSITION, IN SUCH A MANNER AS TO ACHIEVE A SPECIFIC ENGINE RPM.
0	5D	29	SRG9	BYPASS AUTO-IDLE IF FUDGE DELTA IS ZERO
0	5E	54	JMP0 AUTO	JUMP TO AUTO-IDLE ROUTINE
0	5F	C6		
				CALCULATE AF1 (CORNER ADDRESS OF MAP BRACKETING VALUES). SAVE IT FOR USE BY INTERPOLATION ROUTINE.
0	60	4F ENT2	WRGF	XI (SPEED INDEX) TO BUS
0	61	66	LSHA	XI TO SHA
0	62	69	SHF2	CALCULATE 16*XI (SHIFT 4 BITS)
0	63	69	SHF2	
0	64	4E	WRGE	
0	65	60	ADDA	SHA = 16*XI + YI
0	66	6C	WSHA	
0	67	1E	LRGE	SAVE AF1 (AF1 MEANS ADDRESS OF F1) NOW GO DO MAP INTERPOLATION FOR INJECTOR DURATION
0	68	50	CLBS	TELL INTERPOLATION ROUTINE TO USE INJECTOR MAP
0	69	12	LRG2	
0	6A	53	WBSI RET1	GIVE RETURN ADDRESS TO INTERPOLATION ROUTINE
0	6B	73		
0	6C	1F	LRGF	
0	6D	55	JMP1 WGHTS	GO TO INTERPOLATION THRU WEIGHTS CALCULATING CODE
0	6E	00		
				FIX-UP ROUTINE FOR TOO LARGE Y VALUE (THROTTLE)
0	6F	53 ENT4	WBSI EF	OVERFLOW VALUE FOR THROTTLE
0	70	EF		
0	71	54	JMP0 ENT5	GO BACK TO NORMAL CODE SEQUENCE
0	72	52		
0	73	4C RET1	WRGC	GET FUDGE VALUE TO BUS
0	74	66	LSHA	PUT IT IN SHA REGISTER FOR FUDGE CHECK ROUTINE
0	75	52	JMPM FUDGE	JUMP TO FUDGE CHECK SUBROUTINE
0	76	A4		
0	77	13	LRG3	STORE INJECTOR DURATION VALUE TEMPORARILY

MAP CONTROL ROUTINE—Continued

Program Memory Address Page	Address Within Page	Instruction	STRT 000: Instruction Mnemonic	Operation Performed
0	78	FF	NOOP	PERFORM NO OPERATION (THIS IS TO LEAVE SPACE FOR AN ANTICIPATED COMMAND)
0	79	FF	NOOP	
0	7A	FF	NOOP	
0	7B	FF	NOOP	
0	7C	FF	NOOP	
0	7D	FF	NOOP	
0	7E	FF	NOOR	
0	7F	C6	SKB6	TEST FOR INJECTOR DURATION DISPLAY REQUEST
0	80	54	JMP0 ENT6	PATH FOR NO DISPLAY WANTED
0	81	85		
0	82	86	SBT0	GENERATE STROBE TO LOAD REGISTER 671 (1) INTO HEX DISPLAY
0	83	89	RST0	
0	84	FF	NOOP	PERFORM NO OP. (LEAVE SPACE)
0	85	33 ENT6	TRG3	COMPLIMENT FOR INJECTOR HARDWARE
0	86	43	WRG3	
0	87	96	LIND	GIVE DURATION TO INJECTOR UNIT
0	88	4D	WRGD	PICK UP OPEN COUNT
0	89	95	LIN0	GIVE IT TO INJECTOR HARDWARE
0	8A	02	IRG2	GO TO MAP AND FIGURE NEW IGNITION TIMING VALUE TELL INTERP ROUTINE TO USE IGNITION MAP
0	8B	53	WBSI RET2	GIVE RETURN ADDRESS TO INTERP
0	8C	90		
0	8D	1F	LRGF	
0	8E	55	JMP1 INTRP	JUMP TO INTERP (NO WEIGHT CALC ENTRY)
0	8F	21		
0	90	4B RET2	WRGB	GET IGNITION FUDGE VALUE TO BUS
0	91	66	LSHA	PUT IT IN SHA REGISTER FOR FUDGE CHECK ROUTINE
0	92	52	JMPM FUDGE	JUMP TO FUDGE CHECK SUBROUTINE
0	93	A4		
0	94	90	LSPK	GIVE RESULT TO IGNITION UNIT
0	95	FF	NOOP	
0	96	78	LOR1	OUTPUT IGNITION TIMING TO 16 BIT I/O
0	97	FF	NOOP	
0	98	FF	NOOP	
0	99	FF	NOOP	
0	9A	FF	NOOP	
0	9B	FF	NOOP	
0	9C	C5	SKB5	TEST FOR IGNITION TIMING DISPLAY REQUEST
0	9D	54	JMP0 BEGIN	GO BACK THROUGH UPDATE AGAIN
0	9E	13		
0	9F	86	SBT0	STROBE INTO HEX READOUT
0	A0	89	RST0	
0	A1	FF	NOOP	
0	A2	54	JMP0 BEGIN	GO BACK THROUGH UPDATE AGAIN
0	A3	13		
0	A4	65 FUDGE	CLCY	BEGIN CHECK FOR NEGATIVE FUDGE
0	A5	53	WBSI 80	
0	A6	80		
0	A7	60	ADDA	
0	A8	6B	SKNC	NO CARRY IMPLIES POSITIVE FUDGE
0	A9	54	JMP0 FUD1	GO PROCESS NEGATIVE FUDGE
0	AA	B4		
0	AB	60	ADDA	FIX UP FUDGE VALUE IN SHA
0	AC	65	CLCY	BEGIN CHECK FOR OVERFUDGE
0	AD	6D	WSHB	
0	AE	60	ADDA	
0	AF	6C	WSHA	GET NORMAL RESULT TO BUS
0	B0	6B	SKNC	SKIP IS NORMAL I.E., NO OVERFUDGE
0	B1	53	WBSI FF	IF CARRY, RETURN MAXIMUM VALUE
0	B2	FF		
0	B3	58	RJMP	EXIT THROUGH ENTRY
0	B4	60 FUD1	ADDA	FIX FUDGE VALUE BACK UP
0	B5	65	CLCY	BEGIN CHECK FOR UNDERFUDGE
0	B6	6D	WSHB	GET VALUE
0	B7	60	ADDA	ADD FUDGE
0	B8	53	WBSI 01	GET ABORT VALUE TO BUS
0	B9	01		

SCALE ENGINE SPEED VALUE FOR MAP CONTROL ROUTINE

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
0	BA	6B	SKNC	CHECK FOR CARRY (THERE SHOULD BE ONE NORMALLY)
0	BB	6C	WSHA	GET GOOD VALUE TO BUS
0	BC	FF	NOOP	
0	BD	16	LRG6	BEGIN CHECK FOR ZERO VALUE
0	BE	26	SRG6	
0	BF	58	RJMP	RETURN IF VALUE IS NONZERO
0	C0	FF	NOOP	
0	C1	53	WBSI 01	
0	C2	01		
0	C3	58	RJMP	EXIT THROUGH ENTRY
0	C4	4F INTEX	WRGF	EXIT ROUTINE FOR INTERPOLATION (MUST BE IN PAGE 0)
0	C5	51	JMPB	EXIT TO CALLING ROUTINE AUTO-IDLE
0	C6	81 AUTO	WRAD	GET THROTTLE POSITION TO BUS
0	C7	13	LRG3	STORE IT TEMPORARILY FOR ZERO CHECK
0	C8	23	SRG3	TEST FOR CLOSED THROTTLE
0	C9	54	JMP0 AUT1	PATH FOR THROTTLE NOT CLOSED
0	CA	F5		
0	CB	25	SRG5	CHECK FOR LOOP DELAY CONTROL REGISTER EXHAUSTED
0	CC	54	JMP0 AUT2	PATH FOR INCREMENT DELAY LOOP AND EXIT
0	CD	F2		
0	CE	53	WBSI DO	PICK UP −48 AS LOOP DELAY COUNT
0	CF	D0		
0	D0	15	LRG5	REINITIALIZE LOOP DELAY
0	D1	72	WISP	PICK UP PRESENT UNMODIFIED RPM
0	D2	13	LRG3	SAVE IT TEMPORARILY
0	D3	65	CLCY	BEGIN TEST FOR PRESENT SPEED ABOVE TARGET
0	D4	53	WBSI 93	(= MINUS 700RPM = TARGET SPEED)
0	D5	93		
0	D6	66	LSHA	
0	D7	43	WRG3	
0	D8	60	ADDA	
0	D9	6B	SKNC	NO CARRY IF SPEED IS GREATER THAN TARGET
0	DA	54	JMP0 AUT3	PATH FOR PRESENT RPM LESS THAN OR EQUAL TO TARGET RPM
0	DB	EF		
0	DC	33	TRG3	PATH FOR PRESENT RPM GREATER THAN TARGET RPM
0	DD	65 AUT4	CLCY	
0	DE	43	WRG3	
0	DF	66	LSHA	
0	E0	4A	WRGA	
0	E1	60	ADDA	
0	E2	6B	SKNC	
0	E3	39	TRG9	DELTA = −DELTA
0	E4	FF	NOOP	
0	E5	49	WRG9	PICK UP FUDGE DELTA
0	E6	66	LSHA	
0	E7	4C	WRGC	PICK UP INJECTOR DURATION FUDGE
0	E8	60	ADDA	MODIFY IT BY DELTA
0	E9	6C	WSHA	GET MODIFIED VALUE TO BUS
0	EA	1C	LRGC	UPDATE INJECTOR FUDGE
0	EB	72	WISP	GET UNMODIFIED ENGINE SPEED TO BUS
0	EC	1A	LRGA	STORE IT AS LRPM LAST RPM
0	ED	54	JMP0 ENT2	RETURN TO MAIN PROGRAM
0	EE	60		
0	EF	3A AUT3	TRGA	REVERSE LRPM:PRESENT RPM COMPARISON TEST
0	F0	54	JMP0 AUT4	
0	F1	DD		
0	F2	05 AUT2	IRG5	UPDATE LOOP DELAY CONTROL
0	F3	54	JMP0 ENT2	RETURN TO MAIN PROGRAM
0	F4	60		
0	F5	53 AUT1	WBSI 01	
0	F6	01		
0	F7	15	LRG5	PUT LONG INITIAL CLOSED THROTTLE DELAY
0	F8	54	JMP0 ENT2	RETURN TO MAIN PROGRAM
0	F9	60		
			STRT 256:	GET TO PAGE 1 TO WRITE INTERPOLATION ROUTINE
1	00	50 WGHTS	CLBS	BEGIN CALCULATION OF W1...W4
1	01	66	LSHA	INITIALIZE FOR MULTIPLY ROUTINE
1	02	67	LSHB	
1	03	40	WRG0	RX TO BUS
1	04	16	LRG6	RX TO MULTIPLIER REGISTER 676

SCALE ENGINE SPEED VALUE FOR MAP CONTROL ROUTINE—Continued

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
1	05	41	WRG1	RY TO BUS (MULTIPLICAND)
1	06	52	JMPM SMULT	GO FORM RX*RY
1	07	6C		
1	08	69	SHF2	DO DIVISION BY SHIFTING INTO SHB REGISTER
1	09	69	SHF2	
1	0A	6D	WSHB	SHB = RX*RY/16 = W3
1	0B	17	LRG7	SAVE W3
1	0C	30	TRG0	FORM −RX
1	0D	31	TRG1	FORM −RY
1	0E	41	WRG1	
1	0F	61	ADDB	SHB = −RY + RY*RY/16
1	10	6D	WSHB	
1	11	18	LRG8	
1	12	38	TRG8	[8] = RY−RX*RY/16 = W2
1	13	40	WRG0	−RX
1	14	61	ADDB	SHB = −RX−RY + RX*RY/16
1	15	53	WBSI 10	16 (CONSTANT)
1	16	10		
1	17	61	ADDB	SHB = 16−RX−RY + RX*RY/16 = W1
1	18	6D	WSHB	
1	19	11	LRG1	[1] = W1
1	1A	47	WRG7	[7] = RX*RY/16
1	1B	67	LSHB	
1	1C	40	WRG0	−RX
1	1D	61	ADDB	SHB = −RX + RX*RY/16 = −W4
1	1E	6D	WSHB	
1	1F	10	LRG0	
1	20	30	TRG0	[0] = RX−RX*RY/16 = W4
1	21	50 INTRP	CLBS	BEGIN INTERPOLATION CALCULATION
1	22	66	LSHA	INITIALIZE FOR MULTIPLY ROUTINE
1	23	67	LSHB	
1	24	41	WRG1	[1] = W1
1	25	16	LRG6	W1 TO MULTIPLIER REGISTER 676
1	26	4E	LRGE	FETCH AF1
1	27	22	SRG2	TEST FOR INJECTOR OR IGNITION ENTRY
1	28	55	JMP1 INT1	PATH FOR IGNITION ENTRY
1	29	60		
1	2A	70	WDT1	PICK UP F1 FROM INJECTOR MAP
1	2B	52 INT2	JMPM SMULT	GO DO REPEAT DOUBLE PRECISION ACCUMULATION ROUTINE TO FORM W1*F1
1	2C	6C		
1	2D	48	WRG8	[8] = W2
1	2E	16	LRG6	W2 TO MULTIPLIER REGISTER 676
1	2F	0E	IRGE	CALCULATE AF2 = AF1 + 1
1	30	4E	WRGE	FETCH AF2
1	31	22	SRG2	TEST FOR INJECTOR OR IGNITION ENTRY
1	32	55	JMP1 INT3	PATH FOR IGNITION ENTRY
1	33	63		
1	34	70	WDT1	PICK UP F2 FROM INJECTOR MAP
1	35	52 INT4	JMPM SMULT	FORM W1*F1 + W2*F2
1	36	6C		
1	37	40	WRG0	W4
1	38	16	LRG6	W4 TO MULTIPLIER REGISTER 676
1	39	6C	WSHA	SAVE CONTENTS OF SHA REGISTER
1	3A	13	LRG3	
1	3B	4E	WRGE	
1	3C	66	LSHA	
1	3D	53	WBSI 0F	0F = 15
1	3E	0F		
1	3F	60	ADDA	CALCULATE AF 4 = AF2 + 15
1	40	6C	WSHA	
1	41	1E	LRGE	
1	42	43	WRG3	
1	43	66	LSHA	RESTORE SHA REGISTER
1	44	4E	WRGE	FETCH AF4
1	45	22	SRG2	TEST FOR INJECTOR OR IGNITION ENTRY
1	46	55	JMP1 INT5	PATH FOR IGNITION ENTRY
1	47	66		
1	48	70	WDT1	PICK UP F4 FROM INJECTOR MAP
1	49	52 INT6	JMPM SMULT	FORM W1*F1 + W2*F2 + W4*F4
1	4A	6C		
1	4B	47	WRG7	[7] = W3
1	4C	16	LRG6	W3 TO MULTIPLIER REGISTER 676
1	4D	0E	LRGE	CALCULATE AF3 = AF4 + 1
1	4E	4E	WRGE	
1	4F	22	SRG2	TEST FOR INJECTOR OR IGNITION ENTRY
1	50	55	JMP1 INT7	PATH FOR IGNITION ENTRY
1	51	69		

SCALE ENGINE SPEED VALUE FOR MAP CONTROL ROUTINE—Continued

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
1	52	70	WDT1	PICK UP F3 FROM INJECTOR MAP
1	53	52 INT8	JMPM SMULT	FORM W1*F1+W2*F2+W4*F4+W3*F3
1	54	6C		
1	55	69	SHF2	SCALE RESULT
1	56	69	SHF2	SHB = (W1*F1+W2*F2+W3*F3+W4*F4)/16 = f0
1	57	4E	WRGE	BEGIN RESTORATION OF AF1
1	58	66	LSHA	
1	59	53	WBSI EF	GET −17 TO BUS TO SUBTRACT FROM AF1
1	5A	EF		
1	5B	60	ADDA	PERFORM SUBTRACTION
1	5C	6C	WSHA	
1	5D	1E	LRGE	
1	5E	54	JMP0 INTEX	EXIT TO CALLING ROUTINE
1	5F	C4		
1	60	71 INT1	WDT2	PICK UP F1 FROM IGNITION MAP
1	61	55	JMP1 INT2	
1	62	2B		
1	63	71 INT3	WDT2	PICK UP F2 FROM IGNITION MAP
1	64	55	JMP1 INT4	
1	65	35		
1	66	71 INT5	WDT2	PICK UP F4 FROM IGNITION MAP
1	67	55	JMP1 INT6	
1	68	49		
1	69	71 INT7	WDT2	PICK UP F3 FROM IGNITION MAP
1	6A	55	JMP1 INT8	
1	6B	53		
				MULTIPLICATION SUBROUTINE OR DOUBLE ACCUMULATION ROUTINE WHICH PERFORMS MULTIPLICATION DURING f0 CALCULATION
1	6C	26 SMULT	SRG6	CHECK FOR MULTIPLIER ZERO
1	6D	55	JMP1 SML 1	PATH TO CONTINUE
1	6E	70		
1	6F	58	RJMP	EXIT IMMEDIATELY IF MULTIPLIER IS ZERO
1	70	36 SML1	TRG6	INITIATE LOOP CONTROL
1	71	65 SML2	CLCY	
1	72	60	ADDA	PERFORM DOUBLE PRECISION ACCUMULATION
1	73	64	ACYB	
1	74	06	IRG6	UPDATE LOOP CONTROL
1	75	26	SRG6	CHECK FOR LOOP EXHAUSTED
1	76	55	JMP1 SML2	PATH TO CONTINUE IN LOOP
1	77	71		
1	78	58	RJMP	EXIT THROUGH ENTRY
				NOW BEGIN CHECK FOR DATA DISPLAY AND INPUT REQUESTS
1	89	C3 DSPLY	SKB3	CHECK FOR DATA DISPLAY REQUEST
1	8A	55	JMP1 DSP1	PATH FOR NO DATA DISPLAY REQUEST
1	8B	BC		
1	8C	52	JMPM SDADD	GO GET SOURCE ADDRESS
1	8D	93		
1	8E	53	WBSI DSPX	GET BASE ADDRESS OF DISPLAY ROUTINES
1	8F	9E		
1	90	61	ADDB	CALCULATE JUMP ADDRESS
1	91	6D	WSHB	GET IT TO BUS
1	92	51	JMPB	JUMP TO IT
1	93	7A SDADD	WIR1	BEGIN CALCULATION OF SOURCE/ DEST ADDRESS
1	94	66	LSHA	
1	95	6A	SHF3	GET RID OF MOST SIGNIFICANT 5 BITS
1	96	69	SHF2	
1	97	50	CLBS	CLEAR SHB
1	98	67	LSHB	
1	99	6A	SHF3	SHB NOW HAS S/D BITS
1	9A	6D	WSHB	COPY TO BUS
1	9B	68	SHF1	SHB= 2*SHB
1	9C	61	ADDB	SHB= 3* (S/D BITS)
1	9D	58	RJMP	SUBROUTINE RETURN
1	9E	45 DSPX	WRG5	PICK UP LCNT FOR DISPLAY
1	9F	55	JMP1 DOUT	
1	A0	B6		
1	A1	49	WRG9	PICK UP DELTA
1	A2	55	JMP1 DOUT	
1	A3	B6		
1	A4	4A	WRGA	PICK UP LRPM (PREVIOUS RPM)
1	A5	55	JMP1 DOUT	
1	A6	B6		
1	A7	4B	WRGB	PICK UP IGNITION FUDGE VALUE
1	A8	55	JMP1 DOUT	

SCALE ENGINE SPEED VALUE FOR MAP CONTROL ROUTINE—Continued

Program Memory Address Page	Address Within Page	Instruction	Instruction Mnemonic	Operation Performed
1	A9	B6		
1	AA	4C	WRGC	PICK UP INJECTOR FUDGE VALUE
1	AB	55	JMP1 DOUT	
1	AC	B6		
1	AD	4D	WRGD	PICK UP CURRENT OPEN COUNT
1	AE	55	JMP1 DOUT	
1	AF	B6		
1	B0	72	WISP	WRITE UNMODIFIED ENGINE SPEED FOR DISPLAY
1	B1	55	JMP1 DOUT	
1	B2	B6		
1	B3	8F	SEL0	SELECT CHANNEL 0 ON A/D (THROTTLE)
1	B4	80	CONV	INITIATE A/D CONVERSION
1	B5	81	WRAD	GET A/D RESULTS TO BUS
1	B6	78 DOUT	LOR1	LOAD OUTPUT REGISTER OR1
1	B7	86	SBT0	STROBE INTO HEX DISPLAY
1	B8	89	RST0	
1	B9	FF	NOOP	
1	BA	54	JMP0 CONT	RETURN TO MAIN PROGRAM
1	BB	15		
1	BC	C4 DSP1	SKB4	CHECK FOR DATA INPUT REQUEST
1	BD	54	JMP0 CONT	RETURN TO MAIN PROGRAM
1	BE	15		
1	BF	52	JMPM SDADD	GO GET DESTINATION ADDRESS
1	C0	93		
1	C1	53	WBSI INDX	GET BASE ADDRESS OF INPUT ROUTINES
1	C2	C7		
1	C3	61	ADDB	CALCULATE JUMP ADDRESS
1	C4	6D	WSHB	GET IT TO BUS
1	C5	65	CLCY	
1	C6	51	JMPB	
1	C7	7B INDX	WIR2	INPUT CORRECTION REGISTERS 351 AND 356
1	C8	91	LT16	
1	C9	6B	SKNC	
1	CA	7B	WIR2	INPUT CORRECTION REGISTERS 355 AND 353
1	CB	92	LT53	
1	CC	6B	SKNC	
1	CD	7B	WIR2	INPUT CORRECTION REGISTERS 354 AND 357
1	CE	93	LT47	
1	CF	6B	SKNC	
1	D0	7B	WIR2	INPUT CORRECTION REGISTERS 352 AND 358
1	D1	94	LT28	
1	D2	6B	SKNC	
1	D3	7B	WIR2	
1	D4	1B	LRGB	INPUT IGNITION FUDGE VALUE
1	D5	6B	SKNC	
1	D6	7B	WIR2	
1	D7	1C	LRGC	LOAD INJECTOR FUDGE VALUE
1	D8	6B	SKNC	
1	D9	7B	WIR2	
1	DA	1D	LRGD	LOAD INJECTOR OPEN COUNT
1	DB	6B	SKNC	
1	DC	7B	WIR2	
1	DD	19	LRG9	LOAD AUTO-IDLE DELTA
1	DE	54	JMP0 CONT	RETURN TO MAIN PROGRAM
1	DF	15		

Much of the information included in the instruction definitions and the program has been included in the drawings. The outputs of the various instruction decoding circuits have been labeled with the instructions decoded by the circuit. The timing decoding circuit outputs have also been labeled with the various time slots T1–T8 which are decoded at the output. Instruction decoding tables 7C, 8D, 9D, 10C, 11G, 12F, 13E, 14C and 15E are also included to aid interpretation of the drawings and to show the exact manner in which the detailed circuitry operates.

For example, FIG. 7C indicates that instruction WDT1 is carried out by data memory **170** shown in FIGS. 7A and 7B. As noted in the instruction definitions, data is written from the injector data memory to the bus during the WDT1 instruction. The exact manner in which this instruction is carried out is shown by the Boolean Algebra notations in FIGS. 7A and 7B.

Referring to FIG. 7B, timing decoding circuit **460** and instruction decoding circuit **462** operate so that conductor **452** is switched to its **1** state under the following condition written in Boolean Algebra notation and noted on conductor **452**: $\overline{WDT1 \cdot (T7 + T8)}$. According to this notation, conductor **452** is switched to its **0** state during time slots T7 and T8 when the WDT1 instructions is in instruction latch **180**. This condition holds both inputs of NOR gate N26 (FIG. 7A) in their **0** states. The input opposite conductor **452** is normally **0** due to the presence of inverter **17**. NOR gate N26 is switched to its **1** state, thereby switching NOR gate N25 to its **0** state and switching conductor **450** to its **1** state. When conductor **450** is in its **1** state, injector memory chips **432–439** are enabled to read data onto the bus. The exact manner in which the other instruc-

tions are executed by the circuitry can be similarly determined from the drawings.

Those skilled in the art will appreciate that the apparatus and method described above is merely exemplary of the preferred practice of the invention, and that modifications can be made without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. In a fuel system for an internal combustion engine including a source of fuel for a fuel injection means that is opened to admit a predetermined quantity of fuel to the engine in response to an electrical fuel signal, improved apparatus for controlling the fuel signal comprising:

first means for generating a first engine condition digital number having a value representing a first operating characteristic of the engine;

second means for generating a second engine condition digital number having a value representing a second operating characteristic of the engine;

data memory means for storing each of a plurality of fuel digital words representing a plurality of discrete engine fuel requirements;

program memory means for storing a plurality of instruction digital words representing a plurality of operating instructions;

a program sequencer for initiating the operating instructions in a predetermined order;

selecting means responsive to the operating instructions for producing a resultant fuel digital word representing the engine fuel requirement by selecting one or more of the fuel digital words depending on the values of the first and second engine condition digital numbers;

means for storing the resultant fuel digital word;

means for generating a position signal when the engine is in a predetermined position;

means responsive to the position signal for producing said fuel signal at the end of a predetermined operating interval; and

means for altering the value of the fuel signal as a function of the value of the resultant fuel digital word so that the proper quantity of fuel is admitted to the engine through the fuel injector means.

2. Apparatus, as claimed in claim **1**, wherein the first and second means each comprises an analog to digital converter.

3. Apparatus, as claimed in claim **1**, wherein the data memory means comprises means for storing each fuel digital word at a predetermined address that represents a predetermined value of the first engine operating characteristic and a predetermined value of the second engine operating characteristic, and wherein the selecting means comprises:

means responsive to the first and second engine condition digital numbers for selecting a plurality of the predetermined addresses, each selected address representing values of the first and second engine operating characteristics that at least approximately correspond to the values of the first and second engine operating characteristics represented by the first and second engine condition digital numbers; and

means for deriving from the fuel digital words stored at the selected addresses a single resultant fuel digital word.

4. Apparatus, as claimed in claim **3**, wherein the data memory means comprises means for uniquely identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the first operating characteristic and by a preselected digital second address number proportional to a preselected value of the second operating characteristic.

5. Apparatus, as claimed in claim **4**, wherein the selecting means comprises:

means for comparing the first address numbers with the first engine condition digital number and for comparing the second address numbers with the second engine condition digital number, and for selecting a plurality of selected addresses identified by first and second address numbers that approximate the values of the first and second engine condition digital numbers; and

means for interpolating between the fuel digital words stored at the selected addresses to produce the resultant fuel digital word.

6. Apparatus, as claimed in claim **1**, wherein the selecting means comprises:

an arithmetic unit for interpolating between the selected fuel digital words in accordance with the operating instructions.

7. Apparatus, as claimed in claim **1**, wherein the means for generating a position signal comprises:

a first member mounted to a fixed portion of the engine;

a second member mounted to a cyclically moving portion of the engine so that the second member periodically passes adjacent the first member; and

means for producing the position signal when the second member passes adjacent the first member.

8. Apparatus, as claimed in claim **1**, wherein the means responsive to the position signal comprises:

a clock generator for generating clock pulses at a predetermined rate;

a counter;

means for storing an open-time digital number having a value proportional to said predetermined operating interval;

means for loading the open-time digital number into the counter in response to the position signal;

means for transmitting clock pulses to the counter so that the counter counts to a predetermined value; and

means responsive to the counter for commencing the production of the fuel signal after the counter has counted to the predetermined value.

9. Apparatus, as claimed in claim **1**, wherein the means for altering comprises:

a clock generator for generating clock pulses at a predetermined rate;

a counter;

means for loading the resultant fuel digital word into the counter in response to the commencement of the fuel signal;

means for transmitting the clock pulses to the counter so that the counter counts to a predetermined value; and

means for terminating the fuel signal when the counter has counted to the predetermined value.

10. Apparatus, as claimed in claim **1**, wherein the internal combustion engine comprises a first cylinder and

a second cylinder, wherein the fuel injection means comprises a first fuel injector for admitting fuel to the first cylinder and a second fuel injector for admitting fuel to the second cylinder, wherein the fuel signal comprises a first current pulse for controlling the first fuel injector and a second current pulse for controlling the second fuel injector, wherein the means responsive to the position signal comprises means for commencing the production of the first current pulse at the end of a first predetermined operating interval and means for commencing the production of the second current pulse at the end of a second predetermined operating interval, and wherein the means for altering comprises means for separately altering the values of the first and second current pulses so that a quantity of fuel proportional to the value of the resultant fuel digital word is separately admitted to the first cylinder through the first fuel injector and to the second cylinder through the second fuel injector.

11. Apparatus, as claimed in claim **10,** wherein the means for storing comprises means for storing a first correction digital number and a second correction digital number and wherein the means for altering comprises means for altering the value of the first current pulse so that a quantity of fuel is admitted to the first cylinder proportional to the combined values of the resultant fuel digital word and the first correction digital number and means for altering the value of the second current pulse so that a quantity of fuel is admitted to the second cylinder proportional to the combined values of the resultant fuel digital word and the second correction digital number.

12. In a control system for an internal combustion engine including means for operating a controlled member in response to an electrical control signal, improved apparatus for controlling the control signal comprising:

first means for generating a first engine condition digital number having a value representing a first operating characteristic of the engine;

second means for generating a second engine condition digital number having a value representing a second operating characteristic of the engine;

data memory means for storing each of a plurality of control digital words representing a plurality of control requirements;

program memory means for storing a plurality of instruction digital words representing a plurality of operating instructions;

a program sequencer for initiating the operating instructions in a predetermined order;

selecting means responsive to the operating instructions for producing a resultant control digital word representing the engine control requirement by selecting one or more of the control digital words depending on the values of the first and second engine condition digital numbers;

means for storing the resultant control digital word; and

means for generating a position signal for controlling the control signal as a function of the value of the resultant control digital word.

13. Apparatus, as claimed in claim **12,** wherein the control system comprises an ignition system, wherein the means for operating comprises a means for producing a spark in order to explode a fuel mixture inside the engine, wherein the control signal comprises an electrical fire signal; and wherein the resultant control digital word represents a spark timing requirement of the engine.

14. Apparatus, as claimed in claim **12,** wherein the data memory means comprises means for storing each control digital word at a predetermined address that represents a predetermined value of the first engine operating characteristic and a predetermined value of the second engine operating characteristic, and wherein the selecting means comprises:

means responsive to the first and second engine condition digital numbers for selecting a plurality of the predetermined addresses, each selected address representing values of the first and second engine operating characteristics that at least approximately correspond to the values of the first and second engine operating characteristics represented by the first and second engine condition digital numbers; and

means for deriving from the control digital words stored at the selected addresses a single resultant control digital word.

15. Apparatus, as claimed in claim **14,** wherein the data memory means comprises means for uniquely identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the first operating characteristic and by a preselected digital second address number proportional to a preselected value of the second operating characteristic.

16. Apparatus, as claimed in claim **15,** wherein the selecting means comprises means for comparing the first address numbers with the first engine condition digital number and for comparing the second address numbers with the second engine condition digital number, and for selecting a plurality of the predetermined addresses identified by first and second address numbers that approximate the values of the first and second engine condition digital numbers; and

means for interpolating between the control digital words stored at the selected addresses to produce the resultant control digital word.

17. Apparatus, as claimed in claim **12,** wherein the selecting means comprises:

an arithmetic unit for interpolating between the selected control digital words in accordance with the operating instructions.

18. Apparatus, as claimed in claim **12,** wherein the means for generating a position signal comprises:

a first member mounted to a fixed portion of the engine;

a second member mounted to a cyclically moving portion of the engine so that the second member periodically passes adjacent the first member; and

means for producing the position signal when the second member passes adjacent the first member.

19. Apparatus, as claimed in claim **12,** wherein the means responsive to the position signal comprises:

a clock generator for generating clock pulses at a predetermined rate;

a counter;

means for loading the resultant control digital word into the counter in response to the position signal;

means for transmitting the clock pulses to the counter so that the counter counts to a predeter-

mined value; and

means responsive to the counter for producing the control signal after the counter has counted to the predetermined value.

20. In a system for controlling the operation of an internal combustion engine including a source of fuel for a fuel injection means that is opened to admit a predetermined quantity of fuel to the engine in response to an electrical fuel signal and a spark means for producing a spark cable of igniting the fuel inside the engine in response to a fire signal, improved apparatus for controlling the fuel signal and the timing of the fire signal comprising:

first means for generating a first engine condition digital number having a value representing a first operating characteristic of the engine;

second means for generating a second engine condition digital number having a value representing a second operating characteristic of the engine;

data memory means for storing each of a plurality of fuel digital words representing a plurality of discrete engine fuel requirements and for storing each of a plurality of ignition digital words representing a plurality of ignition timing requirements for the engine;

selecting means for producing a resultant fuel digital word for controlling the amount of fuel injected into the engine and a resultant ignition digital word for controlling the ignition timing of the engine by selecting one or more of the fuel digital words and one or more of the ignition digital words depending on the values of the first and second engine condition digital numbers;

means for storing the resultant fuel digital word and for storing the resultant ignition digital word;

means for generating one or more position signals when the engine is in one or more predetermined positions;

first means responsive to one of the one or more position signals for producing said fuel signal at the end of a first predetermined operating interval;

means for altering the value of the fuel signal as a function of the value of the resultant fuel digital word so that a proper amount of fuel is admitted to the engine through the fuel injection means; and

second means responsive to one of the one or more position signals for producing the fire signal at the end of a second operating interval that is a function of the value of the resultant ignition digital word.

21. Apparatus, as claimed in claim **20,** wherein the first operating characteristic comprises engine speed and the second operating characteristic comprises the position of a member controlled by the operator of the engine.

22. Apparatus, as claimed in claim **20,** wherein the first and second means each comprises an analog to digital converter.

23. Apparatus, as claimed in claim **20,** wherein the data memory means comprises means for storing each fuel digital word and each ignition digital word at a predetermined address that represents a predetermined value of the first engine operating characteristic and a predetermined value of the second engine operating characteristic, and wherein the selecting means comprises:

means responsive to the first and second engine condition digital numbers for selecting a plurality of the predetermined addresses, each selected address representing values of the first and second engine operating characteristics that at least approximately correspond to the values of the first and second engine operating characteristics represented by the first and second engine condition digital numbers; and

means for deriving from the fuel and ignition digital words stored at the selected addresses a single resultant fuel digital word and a single resultant ignition digital word.

24. Apparatus, as claimed in claim **23,** wherein the data memory means comprises means for uniquely identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the frst operating characteristic and a preselected digital second address number proportional to a preselected value of the second operating characteristic.

25. Apparatus, as claimed in claim **24,** wherein the selecting means comprises:

means for comparing the first address numbers with the first engine condition digital number and for comparing the second address numbers with the second engine condition digital number, and for selecting a plurality of selected addresses identified by first and second address numbers that approximate the values of the first and second engine condition digital numbers; and

means for interpolating between the digital words stored at the selected addresses to produce the resultant fuel digital word and the resultant ignition digital word.

26. Apparatus, as claimed in claim **20,** wherein the selecting means comprises:

an arithmetic unit for interpolating between the selected fuel and ignition digital words in accordance with the operating instructions.

27. Apparatus, as claimed in claim **20,** wherein the means for generating a position signal comprises:

a first member mounted to a fixed portion of the engine;

a second member mounted to a cylically moving portion of the engine so that the second member periodically passes adjacent the first member; and

means for producing the position signal when the second member passes adjacent the first member.

28. Apparatus, as claimed in claim **20,** wherein the first means comprises:

a clock generator for generating clock pulses at a predetermined rate;

a counter;

means for storing an open-time digital number having a value proportional to said first operating interval;

means for loading the open-time digital number into the counter in response to the position signal;

means for transmitting clock pulses to the counter so that the counter counts to a predetermined value; and

means responsive to the counter for commencing the production of the fuel signal after the counter has counted to the predetermined value.

29. Apparatus, as claimed in claim **20,** wherein the means for altering comprises:

a clock generator for generating clock pulses at a

predetermined rate;
a counter;
means for loading the resultant fuel digital word into the counter in response to the commencement of the fuel signal;
means for transmitting clock pulses to the counter so that the counter counts to a predetermined value; and
means for terminating the fuel signal when the counter has counted to the predetermined value.

30. Apparatus, as claimed in claim **20,** wherein the second means comprises:
a clock generator for generating clock pulses at a predetermined rate;
a counter;
means for loading the resultant ignition digital word into the counter in response to the position signal;
means for transmitting the clock pulses to the counter so that the counter counts to a predetermined value; and
means responsive to the counter for producing the fire signal after the counter has counted to the predetermined value.

31. A method of injecting fuel into an internal combustion engine including a source of fuel for a fuel injection means that is opened to admit a predetermined quantity of fuel to the engine in response to an electrical fuel signal, said method comprising the steps of:
storing a plurality of fuel digital words representing a plurality of discrete engine fuel requirements;
storing a plurality of instruction digital words representing a plurality of operating instructions;
initiating the operating instructions in a predetermined order;
generating a first engine condition digital number having a value representing a first operating characteristic of the engine;
selecting under control of the operating instructions one or more of the fuel digital words depending on the values of the first and second engine condition digital numbers so that each selected fuel digital word at least approximately represents the fuel requirement of the engine;
deriving from the one or more selected fuel digital words a resultant fuel digital word representing the engine fuel requirement;
storing the resultant fuel digital word;
generating a position signal when the engine is in a predetermined position;
producing said fuel signal at the end of a predetermined operating interval initiated by the generation of the position signal; and
altering the value of the fuel signal as a function of the resultant fuel digital word so that the proper quantity of fuel is admitted to the engine through the fuel injection means.

32. A method, as claimed in claim **31,** wherein the step of storing comprises the step of storing each fuel digital word at a predetermined address that represents a predetermined value of the first engine operating characteristic and a predetermined value of the second engine operating characteristic, and wherein the step of selecting comprises the steps of:
selecting a plurality of the predetermined addresses, each selected address representing values of the first and second engine operating characteristics that at least approximately correspond to the value of the first and second engine operating characteristics represented by the first and second engine condition digital numbers; and
deriving from the fuel digital words stored at the selected addresses a single resultant fuel digital word.

33. A method as claimed in claim **32,** wherein the step of storing comprises the step of identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the first operating characteristic and a preselected digital second address number proportional to a preselected value of the second operating characteristic.

34. A method as claimed in claim **33,** wherein the step of selecting comprises the steps of:
comparing the first address numbers with the first engine condition digital number;
comparing the second address numbers with the second engine condition digital number;
selecting a plurality of the predetermined addresses identified by first and second address numbers that approximate the values of the first and second engine condition digital numbers; and
interpolating between the fuel digital words stored at the selected addresses to produce the resultant fuel digital word.

35. A method, as claimed in claim **31,** wherein the internal combustion engine comprises a plurality of cylinders, wherein the fuel injection means comprises a separate fuel injector for each cylinder of the engine, wherein the fuel signal comprises a separate current pulse for independently operating each fuel injector, wherein the step of producing the fuel signal comprises the steps of producing separate current pulses for opening each fuel injector independently of the other fuel injectors, and wherein the step of altering comprises the step of individually altering the value of each current pulse so that a quantity of fuel proportional to the value of the resultant fuel digital word is separately admitted to the engine through each fuel injector.

36. A method, as claimed in claim **35,** wherein the step of storing comprises the step of storing a separate correction digital number for each cylinder of the engine, and wherein the step of altering comprises the steps of separately combining the value of the resultant fuel digital word with the value of each correction digital number so that a quantity of fuel is admitted to each cylinder in proportion to the combined values of the resultant fuel digital word and the correction digital number stored for use with that cylinder.

37. A method of controlling a member of an internal combustion engine that is controllable in response to an electrical control signal, said method comprising the steps of:
storing a plurality of control digital words representing a plurality of engine control requirements;
storing a plurality of instruction digital words representing a plurality of operating instructions;
initiating the operating instructions in a predetermined order;
generating a first engine condition digital number having a value representing a first operating characteristic of the engine;
generating a second engine condition digital number having a value representing a second operating characteristic of the engine;

selecting one or more of the control digital words depending on the values of the first and second engine condition digital numbers so that each selected control digital word at least approximately represents the control requirement of the engine;

deriving from the one or more selected control digital words a resultant control digital word representing the engine control requirement;

storing the resultant control digital word;

generating a position signal when the engine is in a predetermined position; and

controlling the control signal in response to the position signal as a function of the value of the resultant control digital word.

38. A method, as claimed in claim **37,** wherein the step of storing comprises the step of storing each control digital word at a predetermined address that represents a predetermined value of the first engine operating characteristic and a predetermined value of the second engine operating characteristic, and wherein the step of selecting comprises the steps of:

selecting a plurality of the predetermined addresses, each selected address representing values of the first and second engine operating characteristics that at least approximately correspond to the values of the first and second engine operating characteristics represented by the first and second engine condition digital numbers; and

deriving from the control digital words stored at the selected addresses a single resultant control digital word.

39. A method, as claimed in claim **38,** wherein the step of storing comprises the step of identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the first operating characteristic and a preselected digital second address number proportional to a preselected value of the second operating characteristic.

40. A method, as claimed in claim **39,** wherein the step of selecting comprises the steps of:

comparing the first address numbers with the first engine condition digital number;

comparing the second address numbers with the second engine condition digital number;

selecting a plurality of the predetermined addresses identified by first and second address numbers that approximate the values of the first and second engine condition digital numbers; and

interpolating between the control digital words stored at the selected addresses to produce the resultant digital word.

41. A method, as claimed in claim **37,** wherein the controllable member is a means for producing a spark capable of exploding a fuel mixture inside the engine, wherein each control digital word represents an ignition time at which a spark must be provided, and wherein the resultant control digital word represents a spark timing requirement of the engine.

42. In a control system for an internal combustion engine comprising first control means for controlling the operation of a first cylinder of the engine in response to a first control signal and second control means for controlling the operation of a second cylinder of the engine in response to a second control signal, improved apparatus for individually controlling the first and second control means comprising:

means for generating a control digital word having a value representing a control requirement of the engine at the predetermined operating condition;

means for storing the control digital word;

means for storing a first correction digital number having a value representing a control requirement characteristic of the first cylinder;

means for storing a second correction digital number having a value representing a control requirement characteristic of the second cylinder;

means for initiating the production of the first control signal and the second control signal;

means for altering the duration of the first control signal so that the operation of the first control means is controlled in proportion to the combined values of the control digital word and the first correction digital number and for altering the duration of the second control signal so that the operation of the second control means is controlled in proportion to the combined values of the control digital word and the second correction digital number.

43. Apparatus, as claimed in claim **42,** wherein the means for storing the control digital word comprises a first register, wherein the means for storing the first correction digital number comprises a second register and wherein the means for storing the second correction digital number comprises a third register.

44. Apparatus, as claimed in claim **42,** wherein the means for altering comprises:

means for adding the value of the first correction digital number to the value of the control digital word to produce a first corrected control digital word and for adding the value of the second correction digital number to the value of the control digital word to produce a second corrected control digital word;

a clock generator for generating clock pulses at a predetermined rate;

counting means;

means for loading the first corrected control digital word into the counting means and for producing a first output signal when the counting means has been stepped by the clock pulses to a predetermined value;

means responsive to the first output signal for terminating the first control signal;

means for loading the second corrected control digital word into the counting means and for producing a second output signal when the counting means has been stepped by the clock pulses to a predetermined value; and

means for terminating the second control signal in response to the second output signal.

45. Apparatus, as claimed in claim **42,** wherein the control system comprises a fuel system, wherein the first control means comprises a first fuel injection means for admitting fuel into the first cylinder, wherein the second control means comprises a second fuel injection means for admitting fuel into the second cylinder and wherein the control requirements each comprise a fuel requirement of a cylinder.

46. A method of regulating a control function of an internal combustion engine so that the engine operates at a predetermined value of an engine operating characteristic, the method comprising the steps of:

storing a target digital number representing the predetermined value of the engine operating characteristic;

converting the value of the engine operating characteristic at a first point in time into a first test digital number;

converting the value of the engine operating characteristic at a second point in time later than the first point in time into a second test digital number;

producing a first logic signal if the second test digital number is greater in value than the target digital number;

producing a second logic signal if the second test digital number is less in value than the target digital number;

producing a third logic signal if the second test digital number is greater in value than the first test digital number;

producing a fourth logic signal if the second test digital number is less in value than the first test digital number;

storing a delta digital number representing a small change in the value of the control function;

changing the control function in an amount proportional to the value of the delta digital number in response to the first and fourth logic signals;

changing the control function in an amount proportional to the value of the delta digital number in response to the second and third logic signals;

changing the control function in an amount proportional to the inverse of the value of the delta digital number in response to the first and third logic signals; and

changing the control function in an amount proportional to the inverse of the value of the delta digital number in response to the second and fourth logic signals.

47. A method, as claimed in claim **41,** wherein the control function is the quantity of fuel supplied to the engine, wherein the engine operating characteristic is engine speed, and wherein the delta digital number represents a small change in the quantity of fuel normally provided to the engine.

48. A method for controlling the operation of an internal combustion engine including a source of fuel for a fuel injection means to admit a predetermined quantity of fuel to the engine in response to an electricl fuel signal and spark means for producing a spark capable of igniting the fuel inside the engine in response to a fire signal, said method comprising the steps of:

generating a first engine condition digital number having a value representing a first operating characteristic of the engine;

generating a second engine condition digital number having a value representing a second operating characteristic of the engine;

storing a plurality of fuel digital words and a plurality of ignition digital words in pairs, each pair comprising a fuel digital word and an ignition digital word stored at a single predetermined address that represents a predetermined value of the first engine condition digital number and a predetermined value of the second engine digital number, said fuel digital words representing a plurality of engine fuel requirements and said ignition digital words representing a plurality of discrete spark requirements timing requirements of the engine;

selecting one or more of the predetermined addresses depending on the values of the first and second condition digital numbers;

deriving from the one or more fuel digital words and ignition digital words stored at the one or more selected addresses, a resultant fuel digital word and a resultant ignition digital word;

storing the resultant fuel digital word;

storing the resultant ignition digital word;

generating a position signal when the engine is in a predetermined position;

producing said fuel signal at the end of a predetermined operating interval initiated by the generation of the position signal;

altering the value of the fuel signal as a function of the resultant fuel digital word so that the proper quantity of fuel is admitted to the engine through the fuel injection means; and

generating the fire signal at the end of a variable operating interval initiated by the generation of the position signal, the operating interval being varied as a function of the value of the resultant ignition digital word.

49. A method, as claimed in claim **48,** wherein the first operating characteristic comprises engine speed and the second operating characteristic comprises the position of a member controlled by an operator of the engine.

50. A method, as claimed in claim **48,** wherein the step of storing comprises the step of identifying each predetermined address by a preselected digital first address number proportional to a preselected value of the first operating characteristic and a preselected digital second address number proportional to a preselected value of the second operating characteristic.

51. A method, as claimed in claim **50,** wherein the step of selecting comprises and steps of:

comparing the first address numbers with the first engine condition digital number;

comparing the second address numbers with the second engine condition digital number;

selecting a plurality of a predetermined addresses identified by first and second address numbers that approximate the value of the first and second engine condition digital numbers; and

interpolating between the fuel and ignition digital words stored at the selected addresses to produce the resultant fuel digital word and the resultant ignition digital word.

* * * * *