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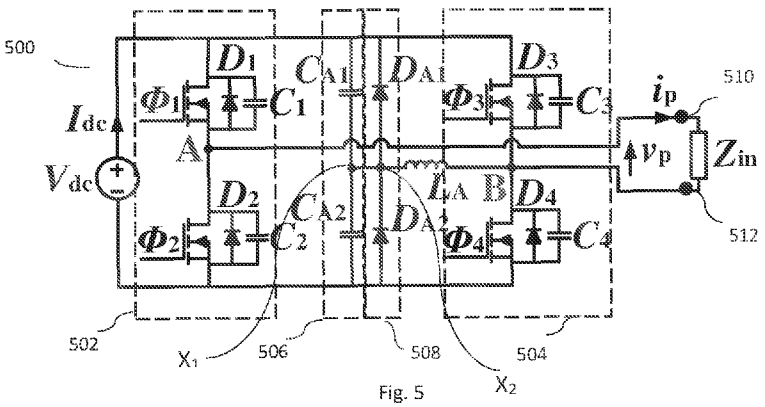

Fig. 5

(57) Abstract: A phase-shift modulated full-bridge power inverter comprises: a leading bridge leg comprising: a first power switch having a first power switch parasitic capacitance; and a second power switch having a second power switch parasitic capacitance. A lagging bridge leg comprises a third power switch having third power switch parasitic capacitance; and a fourth power switch having a fourth power switch parasitic capacitance. Each of the power 10 switches is switched on and off in a switching cycle. An augmented passive circuit comprises an inductor which combines with the third power switch parasitic capacitance and the fourth power switch capacitance to form a resonator when a first one of the third and fourth power switches is switched off and a second one of the third and fourth power switches is in a switched off state. Energy stored in the parasitic capacitance of the second one of the third 15 and fourth power switches is discharged before the second one of the third and fourth power switches is switched on.

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PHASE-SHIFT MODULATED FULL-BRIDGE POWER INVERTERS AND METHODS OF OPERATION THEREOF

Technical Field

The invention relates generally to the field of power electronics, more particularly to transfer power wirelessly. Aspects of the invention relate to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system. Another aspect of the invention relates to a method of operating a phase-shift modulated full-bridge power inverter in a wireless power transfer system. Another aspect of the invention relates to a method of fitting an augmented passive circuit to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system. Another aspect of the invention relates to a kit of augmented passive circuit parts for fitting to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system.

In this respect, it is worth noting the term "augmented passive circuit" is used in the sense that no active switches are required in the augmented passive circuit.

One aspect of the invention has particular, but not exclusive, application in reducing power loss in the power inverter. For instance, use of the techniques disclosed herein may allow for the power inverter to enable all power switches in a wireless power transfer power inverter to be soft-switched for all operating regions. Use of the techniques disclosed herein may allow for zero-voltage switching (ZVS) to be achieved in all of the power switches of the power inverter for all load conditions, without the need for coordinated control and communication with the receiver circuit.

Background

With improvements of switching speeds and power capabilities, power electronic devices such as power metal-oxide-semiconductor field-effect-transistors (MOSFETs) and insulated gate bipolar transistors (IGBT) have been widely used in electrical energy conversion. Recent advances in wide-band-gap (WBG) semiconductor technology further enhance the switching frequency range and power ratings of these power devices. Power converters based on power electronics technology can switch at hundreds of kilo-Hertz in commercial switched

mode power supplies (SMPS) and are being considered for switching up to tens of Mega-Hertz for some emerging applications such as wireless power transfer (WPT).

A major limitation on the switching frequency is the switching power loss in the power switches of a power converter. During the turn-on and turn-off processes, the instantaneous voltage across and the current in the power switch change with time. The instantaneous product of this transient voltage and current contribute to the switching power loss of such power switch. The switching power loss results in heat loss and thermal stress on the structure of the power switch. The large rate of change of voltage (dv/dt) and rate of change of current (di/dt) also contribute to electromagnetic interference (EMI). Traditional switching methods without reducing the switching power loss is called "hard-switching" techniques. In the previous two decades, "soft-switching" methods have been developed and used for many power converters and power inverters. Soft-switching methods create zero voltage and/or zero current for the power switch during the turn-on and turn-off transient process so that the switching loss can ideally be eliminated. Soft-switching techniques can be classified as zero-voltage switching (ZVS) and zero-current switching (ZCS).

Soft-switching techniques for half-bridge and full-bridge power inverters, under 50% duty-cycle pulse-width-modulation (PWM) control, were reported in the 1980s and 1990s in several seminal papers [1]-[3]. Switching the inverter at an operating frequency that falls into the inductive region of the load impedance can ensure ZVS on the condition that the load current is continuous. Under light load condition, the load current becomes discontinuous and ZVS condition is lost. This problem can be solved by adding an augmented inductive-capacitor (LC) circuit branch across the load to maintain a minimum continuous current to ensure ZVS [4].

For full-bridge power inverters under phase-shift modulation (PSM) control, discontinuous current occurs when the phase-shift angle is large (e.g., above 150°). Adding an additional LC circuit branch cannot achieve ZVS. This well-known problem has been a major technical challenge that has not yielded a good solution despite several proposals being made in the past. A recent review paper [5] provides a comprehensive coverage of various forms of symmetric PWM phase-shift converters [6] and asymmetric PWM phase-shift converters [7]

with high-frequency isolation transformers for dc/dc power conversion. That said, the phase-shift converters in [6] and [7] were proposed as dc-dc power supplies for telecommunication applications which are different from WPT considerations, as herein, because the coupling coefficients in WPT applications are not always constant as in high-frequency isolation transformer. The uncertain and yet large leakage inductance in the loosely coupled transmitter and receiver coils in a WPT system could affect the soft-switching conditions in a phase-shift converter.

A partial solution to achieve soft-switching in phase-shift modulated power inverter is to use a quasi-resonant circuit as reported in [8]. Another suggestion of achieving soft switching in phase-shift modulated inverter is to use the modified inverter as reported in [9]. This is a rather complicated circuit when compared with a standard full-bridge inverter (with four switches with anti-parallel diodes). The extra components include 8 diodes and eight inductors. The authors of this reference claim that their circuit can achieve ZCS for a wide operating region (i.e., not full operating region). It is understood that this reference shows the quasi-resonant circuit cannot achieve soft switching for the full phase-shift angular range and hard switching occurs when the phase-shift angle exceeds 120 degrees. Industrial control integrated circuits for full ZVS of phase-shift inverter are available [10], but it requires coordinated control of the transmitter and receiver circuits.

Phase-shift control is commonly used in WPT systems as reflected in recent publications [11]-[18]. In [11], the effects of the dead time on the harmonics were examined. Phase-shift control was used for power and signal transfer in [12] and balancing currents in three-phase WPT systems in [13]. Phase-shift control is also used on the active rectifier on the receiver side of the WPT systems [14]. Phase shift control for soft switching for a wide operating range [15] and improving efficiency at light load [16] has been reported. Other WPT control schemes for parameter estimation and maximum efficiency tracking based on phase-shift inverters can be found in [17] and [18]. However, soft switching of phase-shift inverter for full operating range of phase-shift angle from 0^{o} and 180^{o} is difficult to achieve without communication and coordinated control between the transmitter (Tx) and receiver (Rx) circuits.

Hard-Switching of Known WPT Systems with Phase Shift Control

A. Known SS-Compensated WPT Systems

The schematic diagram of a known SS-compensated WPT system is depicted in Fig. 1. The dc voltage V_{dc} is converted to a high-frequency ac voltage v_p by a full-bridge inverter. The power is transmitted via the SS-compensated resonators. L_p and L_s are the self-inductance of the transmitting and receiving coils, respectively. M is the mutual inductance between the two coils. R_p and R_s are the equivalent series resistances (ESRs) of the resonators. The compensated capacitors C_p and C_s are designed in resonance with the self-inductances of the coils, such that the switching frequency and the resonant frequencies of the resonators are equal as

$$\omega = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}} \quad (1)$$

where ω is the switching angular frequency of the inverter. For the resonators, according to the Kirchoff's circuit laws,

$$v_{p1} = \left(j\omega L_p + \frac{1}{j\omega C_p} + R_p\right) i_{p1} - j\omega M i_{s1} \quad (2.1)$$

$$j\omega M i_{p1} = \left(j\omega L_s + \frac{1}{j\omega C_s} + R_s\right) i_{s1} + v_{s1} \quad (2.2)$$

where i_{p1} and i_{s1} are the fundamental components of transmitter and receiver currents, and v_{s1} is the fundamental component of the output voltage of the receiving resonator. By substituting (1) into (2.1) and (2.2) to eliminate L_p, C_p, L_s, and C_s,

$$v_p = R_p i_p - j\omega M i_s \quad (3.1)$$

$$j\omega M i_p = R_s i_s + v_s \quad (3.2)$$

According to (3.1), the receiver current i_{s1} can be regulated by the fundamental component of the input voltage of the transmitting resonator (i.e., v_{p1}). The diode-bridge rectifier converts the receiver current to i_{rec}, the harmonics of which is filtered by the shunt capacitor C_f, such that a dc current I_b can charge the battery load. The charging current has a linear relationship with the amplitude of v_{p1} (i.e., V_{p1}). A larger V_{p1} results in a larger I_b. According to (3.2), v_{s1} can be regulated by the transmitter current i_{p1}. The diode-bridge rectifier converts v_{s1} to the charging voltage V_b, which has a linear relationship with the amplitude of i_{p1} (i.e.,

I_{p1}). A larger I_p results in a larger V_b. Therefore, the battery charging current and charging voltage can be regulated by the outputs of the primary-side inverter [19]. Here, both the battery charging current and output voltage are fed back into the phase shift controller to regulate the primary-side inverter. The schematic waveforms of the switching signals, i.e., S_1, S_2, S_3, and S_4, are plotted as shown in Fig. 2. The switching signals of each bridge leg are complementary and with the duty ratio of 0.5. A phase shift angle between the diagonal switching signals (i.e., α) is controlled by the primary-side controller. In Fig. 2, S_1 and S_2 are the leading signals with respect to S_4 and S_3. Thus, Φ_1 and Φ_2 can be considered as the leading bridge leg, while Φ_3 and Φ_4 can be considered as the lagging bridge leg. Based on the sketchy waveforms (without considering the deadtime such that switching signals are complementary for one bridge leg), V_{p1} and I_{p1} can be calculated based on V_{dc} and I_{dc} using Fourier analysis as:

$$V_{p1} = \frac{4}{\pi}\cos\left(\frac{\alpha}{2}\right)V_{dc} \qquad (4.1)$$

$$I_{p1} = \frac{\pi}{2}\sec\left(\frac{\alpha}{2}\right)I_{dc} \qquad (4.2)$$

The phase shift angle can be controlled for V_p and I_p regulations, such that the charging current and voltage can track the references during the constant current (CC) and constant voltage (CV) charging modes.

The control block diagram of the primary-side CC and CV charging control based on the phase shift control is depicted, as shown in Fig. 3. The battery output voltage V_b is compared to a threshold voltage V_{val} to determine whether the WPT system operates in the CC or CV mode. Generally, the threshold voltage can be set as the as the reference voltage V_{bref}. If V_b is less than V_{val}, the output is 0 such that the phase shift angle is derived by the current controller (i.e., Controller2). The charging current I_b is controlled to track the current reference I_{bref}. The WPT system operates in the CC charging mode. On the contrary, when V_b is greater than V_{val}, the output is 1 such that the phase shift angle is derived by the voltage controller (i.e., Controller1). The charging voltage V_b is controlled to track the voltage reference V_{bref}. According to (3) and (4), both Controller1 and Controller2 can be linear controllers (e.g., proportional-integral (PI) controllers).

B. Operating Principles of the Known Full-Bridge Inverter with Phase Shift Control

Without losing generality, the equivalent impedance Z_{in} of the resonators and nonlinear loads can be modelled as a pure resistor when the harmonics of the resonator currents are small [20]. Thus, the transmitter current i_p is in phase with the input voltage of the transmitting resonator v_p. For WPT systems with light load conditions, the phase shift angle of the controller is generally large. Typical waveforms of i_p and v_p for a large phase shift angle are plotted, as shown in Fig. 2. During each full operating cycle of v_p from t_1 to t_{13}, the waveform of v_p comprises eight steady states (SS), i.e., SS1: $t_1 \leq t < t_2$, SS2: $t_3 \leq t < t_4$, SS3: $t_5 \leq t < t_6$, SS4: $t_6 \leq t < t_7$, SS5: $t_7 \leq t < t_8$, SS6: $t_9 \leq t < t_{10}$, SS7: $t_{11} \leq t < t_{12}$, and SS8: $t_{12} \leq t < t_{13}$, and four transient states (TS), i.e., TS1: $t_2 \leq t < t_3$, TS2: $t_4 \leq t < t_5$, TS3: $t_8 \leq t < t_9$, and TS4: $t_{10} \leq t < t_{11}$. The equivalent circuits of the full-bridge inverter with phase shift control during the twelve states are shown in Fig. 4. Here, the parasitic capacitances (i.e., C_1, C_2, C_3, and C_4) and diodes (i.e., D_1, D_2, D_3, and D_4) of the four power switches (i.e., Φ_1, Φ_2, Φ_3, and Φ_4) are assumed to be identical, although it will be appreciated that, in practice, there may be some minor discrepancies in parameters due to manufacturing tolerances.

Turning now to Fig. 4. the principles of operation of the power inverter in equivalent circuits of a known WPT system during one cycle will now be described. In the following discussion paragraph references – e.g. (a), (b), etc. – refer to the corresponding one of the individual circuit diagrams.

(a) At t_1, the switch Φ_3 is turned off, while the switch Φ_1 maintains the on-state and the switches Φ_2 and Φ_4 maintain off-state. The voltages across the parasitic capacitors C_2 and C_4 are V_{dc}, while the voltages across the parasitic capacitors C_1 and C_3 are 0. Due to the voltage cross the capacitor C_4 is V_{dc}, the diode D_3 is conducted. During the SS1 ($t_1 \leq t < t_2$), The transmitter current is continuous to be positive (i.e., i_p>0).

(b) At t_2, the switch Φ_4 is turned on, while the switch Φ_1 maintains the on-state and the switches Φ_2 and Φ_3 maintain off-state. During the TS1 ($t_2 \leq t < t_3$), The parasitic capacitor C_3 is charged, while the parasitic capacitor C_4 is discharged. Due to the existence of voltage across the capacitor C_4 (i.e., V_{ds4}>0), the switch Φ_4 is turned on with hard switching. During this period, the inverter current is still positive (i.e., i_p>0).

(c) At t_3, the parasitic capacitor C_4 is fully discharged and the parasitic capacitor C_3 is fully charged. The switches Φ_1 and Φ_4 are on-state, while the switches Φ_2 and Φ_3 are off-state. During the SS2 ($t_3 \leq t < t_4$), the voltages across the capacitors C_1 and C_4 are 0, while the voltages across the capacitors C_2 and C_3 are V_{dc}. The transmitter current remains positive (i.e., i_p>0).

(d) At t_4, the switch Φ_1 is turned off, while the switch Φ_4 maintains on-state and the switches Φ_2 and Φ_3 maintain off-state. The voltages across the parasitic capacitors C_3 and C_4 remains unchanged, while the parasitic capacitor C_1 is charged and the parasitic capacitor C_2 is discharged. During the TS2 ($t_4 \leq t < t_5$), the capacitor C_1 is charged from 0 to V_{dc}, while the capacitor C_2 is discharged from V_{dc} to 0. The transmitter current remains positive (i.e., i_p>0).

(e) At t_5, the parasitic capacitor C_2 is fully discharged and the parasitic capacitor C_1 is fully charged. Thus, the diode D_2 is conducted. During the SS3 ($t_5 \leq t < t_6$), the switch Φ_4 remains on-state, while the switches Φ_1, Φ_2, and Φ_3 are off-state. The transmitter current is positive (i.e., i_p>0).

(f) At t_6, the switch Φ_2 is turned on. The voltages across the parasitic capacitors C_1 and C_3 are V_{dc}, while the voltages across the parasitic capacitors C_2 and C_4 are 0. Therefore, the switch Φ_2 is turned on with ZVS. During the SS4 ($t_6 \leq t < t_7$), the switches Φ_2 and Φ_4 are on-state, while the switches Φ_1 and Φ_3 are off-state. The transmitter current is positive (i.e., i_p>0) during the first half period and negative (i.e., i_p<0) during the second half period.

(g) At t_7, the switch Φ_4 is turned off. The switch Φ_2 remains on-state, while the switches Φ_1 and Φ_3 remain off-state. The voltage across the parasitic capacitor C_4 is 0 and the transmitter current is negative (i.e., i_p<0). Hence, the diode D_4 is conducted during the SS5 ($t_7 \leq t < t_8$).

(h) At t_8, the switch Φ_3 is turned on. The switch Φ_2 remains on-state, while the switches Φ_1 and Φ_3 remain off-state. The voltages across the parasitic capacitors C_1 and C_3 are V_{dc}, while the voltages cross the parasitic capacitors C_2 and C_4 are 0. During the TS3 ($t_8 \leq t <$

t_9), the capacitor C_3 is discharged, while the capacitor C4 is charged. Due to the existence of voltage across the capacitor C_3 (i.e., V_{ds3}>0), Φ_3 is turned on with hard switching. The transmitter current is still negative (i.e., i_p<0).

(i) At t_9, the capacitor C_3 is fully discharged and the capacitor C_4 is fully charged. Hence, the voltages across the parasitic capacitors C_1 and C_4 are V_{dc}, while the voltages across the parasitic capacitors C_2 and C_3 are 0 at this moment. During the SS6 ($t_9 \leq t < t_{10}$), the switches Φ_2 and Φ_3 are on-state, while the switches Φ_1 and Φ_4 are off-state. The transmitter current remains negative (i.e., i_p<0).

(j) At t_{10}, the switch Φ_2 is turned off, while the switch Φ_3 maintains on-state and the switches Φ_1 and Φ_4 are still off-state. The voltages across the parasitic capacitors C_3 and C_4 remain unchanged, while the capacitor C_1 is discharged and the capacitor C_2 is charged. During the TS4 ($t_{10} \leq t < t_{11}$), the capacitor C_1 is discharged from V_{dc} to 0, while the capacitor C_2 is charged from 0 to V_{dc}. The transmitter current is still negative (i.e., i_p<0).

(k) At t_{11}, the parasitic capacitor C_2 is fully charged and the parasitic capacitor C_1 is fully discharged. Thus, the diode D_1 is conducted. During the SS7 ($t_{11} \leq t < t_{12}$), the switch Φ_3 is still on-state, while the switches Φ_1, Φ_2, and Φ_4 are off-state. The transmitter current is still negative (i.e., i_p<0).

(l) At t_{12}, the switch Φ_1 is turned on. The voltages across the parasitic capacitors C_2 and C_4 are V_{dc}, while the voltages across the parasitic capacitors C_1 and C_3 are 0. Therefore, Φ_1 is turned on with ZVS. During the SS8 ($t_{12} \leq t < t_{13}$), the switches Φ_1 and Φ_3 are on-state, while the switches Φ_2 and Φ_4 are off-state. The transmitter current is negative (i.e., i_p<0) during the first half period and positive (i.e., i_p>0) during the second half period.

It can be seen from the analysis that ZVS can be naturally achieved by the leading bridge legs of the inverter with the known phase shift control, whereas hard switching occurs on the switches of the lagging bridge leg during the transient periods TS1 ($t_2 \leq t < t_3$) and TS3 ($t_8 \leq t < t_9$). As a result, the EMI emission of the full-bridge inverter could be high,

especially the conducted EMI from 150 kHz to 30 MHz, which may violate the EMC standard EN55022.

Summary

Aspects of the invention are as set out in the independent claims. Some optional features are defined in the dependent claims.

Implementation of the techniques disclosed herein may provide significant technical advantages. For instance, as will be demonstrated below, zero-voltage switching (ZVS) can be achieved to enable airfares-shift modulator power inverter to enable all power switches to be soft-switched for all operating regions, including in the lagging bridge leg. Consequently, the power inverter can be operated with reduced switching power loss and attenuated electromagnetic interference. Thus, the converter can operate with a higher frequency while the EMI is still within the required boundaries.

In one arrangement, an "augmented passive circuit" comprises two diodes, two capacitors, and one inductor for a full-bridge inverter with known phase-shift control in wireless power transfer (WPT) systems. The operation may achieve soft switching and reduce the EMI radiation for a wide range of phase shift angles, up to the full range of phase shift angle from 0° to 180°. Such full-range ZVS operation may attained without any communication and/or coordinated control with the receiver circuit. Both simulation and experimental results show that ZVS can be achieved by the augmented circuit for a WPT system in both constant current (CC) and constant voltage (CV) control modes. Practical EMI tests demonstrate that the augmented circuit can mitigate the conducted EMI of the full-bridge inverter to meet the standard EN55022 with a full range of phase-shift angle from 0° to 180°. The proposed augmented circuit so adds soft-switching feature to a phase-shift inverter regardless of the types of resonant circuits in the WPT systems, therefore making it flexible for the inverter to drive different type of WPT systems in existing wireless charging standards.

Existing methods require more circuit components and cannot achieve soft switching for the entire operating range of the phase-shift-modulated inverter. The techniques disclosed herein have at least the following advantages:

- fewer circuit components than existing methods, with reduced cost.
- There is no active power switch and therefore does not need extra gate drive circuit for power switch.
- The augmented passive circuit can be added to existing phase-shift modulated power inverter.
- The augmented passive circuit enables a phase-shift modulated power inverter to achieve soft switching (through zero-voltage switching) for the entire operating range.

An augmented passive circuit (with connections shown in Fig. 5) comprises two diodes, two capacitors and one inductor for achieving soft switching in all the power switches in a power inverter under phase-shift modulation control.

The augmented passive circuit can be added to a power inverter to achieve soft switching under either fixed-frequency or variable-frequency operations of power inverter.

The augmented passive circuit can reduce the switching power stress and power losses to improve the lifetime and conversion efficiency of power inverters.

The augmented passive circuit can be used to modify existing designs of wireless power transfer systems compliant with the standards of the Wireless Power Consortium and Society of Automotive Engineers without changing the control algorithms.

A design method for the augmented passive circuit is also herein disclosed, based on the equations (25) to (27) set forth below.

Power inverters are widely used for a large range of modern commercial applications such as switched mode power supplies, battery chargers and wireless charging systems with markets in tens of billions of US dollars. The techniques can be applied to a wide variety of applications, but are particularly useful in wireless charging, including with mobile phones and mobile robotics such as robotic lawn mowers and robotic vacuum cleaners

Brief Description of the Drawings

The invention will now be described, by way of example only, and with reference to the accompanying drawings in which:

Fig. 1 is a schematic diagram of a typical SS-compensated WPT system;

Fig. 2 is a voltage- and current-time diagram illustrating schematic waveforms of the switching signals of a known power inverter for a WPT system;

Fig. 3 is a control block diagram of known phase shift control for WPT systems in achieving CC and CV charging as described in [19];

Fig. 4 is a series of equivalent circuit diagrams illustrating a cycle of operation of a power inverter of a known WPT system;

Fig. 5 is a circuit diagram of a power inverter implementing an exemplary passive augmented circuit in accordance with the techniques described herein;

Fig. 6 is a voltage- and current-time diagram illustrating schematic waveforms of the switching signals of a power inverter for a WPT system implementing an exemplary passive augmented circuit in accordance with the techniques described herein;

Fig. 7 is a series of equivalent circuit diagrams illustrating a cycle of operation of a power inverter implementing an augmented passive circuit in accordance with the techniques described herein;

Fig. 8 illustrates waveforms of I_b, I_{bref}, i_p, v_p, and switching signals of the WPT system (a) without the augmented circuit, and (b) with the augmented circuit in a simulation case 1;

Fig. 9 illustrates waveforms of drain currents and drain-to-source voltages of the four switches of the WPT system (a) without the augmented circuit and (b) with the augmented circuit in the simulation case 1;

Fig. 10 illustrates V_{ds}-I_d curves of the four switches of the WPT system without and with the augmented circuit in case 1;

Fig. 11 illustrates waveforms of V_b, V_{bref}, i_p, v_p, and switching signals of the WPT system (a) without the augmented circuit, and (b) with the augmented circuit in case 2;

Fig. 12 illustrates waveforms of drain currents and drain-to-source voltages of the four switches of the WPT system (a) without the augmented circuit and (b) with the augmented circuit in case 2;

Fig. 13 illustrates V_{ds}-I_d curves of the four switches of the WPT system without and with the augmented circuit in case 2;

Fig. 14 illustrates waveforms of v_{ds3}, i_{d3}, i_p, and v_p of WPT systems (a) without augmented circuit and (b) with augmented circuit for the current control;

Fig. 15 illustrates conducted EMI from full-bridge inverter (a) without augmented circuit and (b) with augmented circuit for the current control;

Fig. 16 illustrates magnified waveforms of v_{ds3} and i_{d3} of WPT systems (a) without augmented circuit and (b) with augmented circuit for the voltage control;

Fig. 17 illustrates conducted EMI from full-bridge inverter (a) without augmented circuit and (b) with augmented circuit for the voltage control;

Fig. 18 illustrates conducted EMI from full-bridge inverter without and with the augmented circuit when the phase shift angle is controlled at 120°, 90°, 60°, 30°, and 0°;

Fig. 19 illustrates background EMIs of the test chamber; and

Fig. 20 illustrates waveforms of v_{ds3}, i_{d3}, i_p, and v_p of the WPT system with and without the augmented circuit for different phase shift angles.

Detailed Description

The circuit diagram of a power inverter implementing an exemplary augmented passive circuit in accordance with the techniques herein disclosed is depicted as shown in Fig. 5. In this, the proposed augmented passive circuit comprises an inductor L_A, two diodes D_{A1} and D_{A2}, and two parallel-connected capacitors C_{A1} and C_{A2}. The circuit is termed an "augmented passive circuit" in as much as it is "passive" by not requiring any active switching components. The circuit "augments" a known phase-shift modulated full-bridge power inverter. In the example of Fig. 5, power inverter 500 is manufactured complete with the augmented passive circuit, however the augmented passive circuit may also be fitted (e.g. retro-fitted) to existing power inverters of known design.

As shown in Fig. 5, the phase-shift modulated full-bridge power inverter 500 comprises a leading bridge leg 502 comprising: a first power switch Φ_1, the first power switch having a first power switch parasitic capacitance C_1; and a second power switch Φ_2, the second power switch having a second power switch parasitic capacitance C_2. The first and second power switches Φ_1 and Φ_2 are connected in series with one another at leading bridge leg connection point A of leading bridge leg 502. Power inverter 500 further comprises a lagging bridge leg 504 comprising: a third power switch Φ_3, the third power switch having a third power switch parasitic capacitance C_3; and a fourth power switch Φ_4, the fourth power

switch having a fourth power switch parasitic capacitance C_4. The third and fourth power switches Φ_3 and Φ_4 are connected in series with one another at lagging bridge leg connection point B of lagging bridge leg 504.

Exemplary types of power switches include, as noted above, MOSFETs and IGBTs.

In the example of Fig. 5, power inverter 500 comprises a capacitor circuit branch 506 comprising first augmented circuit capacitor C_{A1} and second augmented circuit capacitor C_{A2} connected in series with one another at capacitor branch connection point X_1. Capacitor circuit branch 506 is connected in parallel with the leading bridge leg 502 and lagging bridge leg 504. Continuing in this example, the power inverter 500 comprises a diode circuit branch 508 comprising first augmented circuit diode D_{A1} and second augmented circuit diode D_{A2} connected in series with one another at diode branch connection point X_2. Diode circuit branch 508 is connected in parallel with the leading bridge leg 502 and lagging bridge leg 504. In this example, capacitor circuit branch connection point X_1 and diode circuit branch connection point X_2 are electrically connected with one another.

Leading bridge leg connection point A is connected to a first output terminal 510 of the power inverter for connection to a load Z, in this case a wireless power transfer charging load. Lagging bridge leg connection point B is connected to a second output terminal 512 of the power inverter for connection to the load Z. In operation, a load voltage V_p is developed across the load Z and a load current i_p flows through load Z.

Power inverter 500 further comprises augmented circuit inductor L_A connected on a first side (at a first inductor terminal) to the capacitor branch connection point X_1 and the diode branch connection point X_2. Inductor L_A is also connected on a second side (at the second inductor terminal) to one of the first and second output terminals 510, 512.

Together, augmented circuit inductor L_A, capacitor circuit branch 506 and diode circuit branch 508 together form an augmented passive circuit which operate to reduce or even remove discontinuous current which occurs, particularly when the phase-shift angle is large. In turn, this achieves soft-switching and reduces (or even removes) power loss and electromagnetic interference (EMI) arising from the switching of power switches.

The schematic waveforms of the switching signals, i_p and v_p of the WPT system with the augmented circuit are plotted as shown in Fig. 6. During each cycle (i.e., from t_1 to t_{13}), the waveform of v_p comprises eight steady states (SS), i.e., SS1: $t_2 \leq t < t_3$, SS2: $t_3 \leq t < t_4$, SS3: $t_5 \leq t < t_6$, SS4: $t_6 \leq t < t_7$, SS5: $t_8 \leq t < t_9$, SS6: $t_9 \leq t < t_{10}$, SS7: $t_{11} \leq t < t_{12}$, and SS8: $t_{12} \leq t < t_{13}$, and four transient states (TS), i.e., TS1: $t_1 \leq t < t_2$, TS2: $t_4 \leq t < t_5$, TS3: $t_7 \leq t < t_8$, TS4: $t_{10} \leq t < t_{11}$. The equivalent circuits during one cycle of operation are depicted, as shown in Fig. 7. In the following discussion paragraph references – e.g. (a), (b), etc. – refer to the corresponding one of the individual circuit diagrams.

(a) At t_1, the switch Φ_3 is turned off, while the switch Φ_1 is kept on-state and the switches Φ_2 and Φ_4 are kept off-state. The transmitter current is positive (i.e., i_p>0). The voltages across the parasitic capacitors C_2 and C_4 are V_{dc}, while the voltages across the parasitic capacitors C_1 and C_3 are 0. During the TS1 ($t_1 \leq t < t_2$), the capacitor C_3 is charged and the capacitor C_4 is discharged. The augmented inductor L_A and the parasitic capacitors C_3 and C_4 can form an *LC* resonator, such that the energy stored in the parasitic capacitor C_4 can be released before the switch Φ_4 is turned on.

So, it will be appreciated that Figs. 5 and 6 and associated text illustrate and describe a phase-shift modulated full-bridge power inverter 500 configured for use in a wireless power transfer system, the power inverter 500 comprising: a leading bridge leg 502 comprising: a first power switch Φ_1, the first power switch Φ_1 having a first power switch parasitic capacitance C_1; and a second power switch Φ_2, the second power switch Φ_2 having a second power switch parasitic capacitance C_2; a lagging bridge leg 504 comprising: a third power switch Φ_3, the third power Φ_3 switch having a third power switch parasitic capacitance C_3; and a fourth power switch Φ_4, the fourth power switch Φ_4 having a fourth power switch parasitic capacitance C_4; wherein the power inverter 500 is configured for each of the power switches to be switched on and off in a switching cycle; and wherein the power inverter further comprises: an augmented passive circuit comprising an inductor L_A, wherein the power inverter 500 is configured for the inductor L_A to combine with the third power switch parasitic capacitance C_3 and the fourth power switch capacitance C_4 to form a resonator when a first one of the third and fourth power switches Φ_3, Φ_4 (in this step (a), this is the third power switch Φ_3) is switched off and a second one of the third and fourth power switches Φ_3, Φ_4 (in this step (a), this is the fourth power switch Φ_4) is in a switched

off state, and for energy stored in the parasitic capacitance of the second one of the third and fourth power switches (in this step (a), this is C_4 of Φ_4) to be discharged before the second one of the third and fourth power switches (in this step (a), this is Φ_4) is switched on.

A corresponding method is also described.

The significance of this discharge of the energy stored in the parasitic capacitor C_4 will become evident from step (c) below. The discharge/release of the parasitic capacitor C_4 energy can be full or partial discharge.

According to the resonant circuit, the current flowing through the augmented inductor, and the voltages across the capacitors C_3 and C_4 can be expressed as

$$i_{\mathrm{LA}}(t) = \frac{V_{\mathrm{dc}}}{\sqrt{\frac{L_{\mathrm{A}}}{2C_{\mathrm{A}}}}} \cos\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t - t_1)\right] \quad (5)$$

$$v_{\mathrm{C3}}(t) = V_{\mathrm{dc}}\sqrt{\frac{C_{\mathrm{A}}}{C_{\mathrm{Q}}}} \sin\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t - t_1)\right] \quad (6)$$

$$v_{\mathrm{C4}}(t) = V_{\mathrm{dc}} - V_{\mathrm{dc}}\sqrt{\frac{C_{\mathrm{A}}}{C_{\mathrm{Q}}}} \sin\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t - t_1)\right] \quad (7)$$

Here, the transmitter current is mainly determined by the resonators of the WPT system, which will not affect the amplitudes and frequency of the augmented inductor current and the voltages across the capacitors. Besides, the amplitude of the augmented inductor current is determined by the previous state of the system circuit due to its continuity. The TS1 period can be calculated based on (6) or (7) as

$$\Delta t_{12} = \sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}} \sin^{-1}\left(\sqrt{\frac{C_{\mathrm{Q}}}{C_{\mathrm{A}}}}\right) \quad (8)$$

(b) At t_2, the parasitic capacitor C_3 is fully charged and the parasitic capacitor C_4 is fully discharged. The switch Φ_1 is turned on, while the switches Φ_2, Φ_3, and Φ_4 are turned off. The augmented inductor current can be calculated by substituting (8) into (5), as

$$i_{\mathrm{LA}}(t_2) = V_{\mathrm{dc}}\sqrt{\frac{2(C_{\mathrm{A}} - C_{\mathrm{Q}})}{L_{\mathrm{A}}}} \quad (9)$$

During the SS1 ($t_2 \leq t < t_3$), both the transmitter current and augmented inductor current are positive (i.e., i_p>0 and i_{LA}>0).

(c) At t_3, the switch Φ_4 is turned on. The switch Φ_1 is kept on-state and the switches Φ_2 and Φ_3 are kept off-state. The transmitter current is still positive (i.e., i_p>0). During the SS2 ($t_3 \leq t < t_4$), the augmented inductor current is decreased when the DC source is connected, as

$$i_{\mathrm{LA}}(t) = V_{\mathrm{dc}}\sqrt{\frac{2(C_{\mathrm{A}}-C_{\mathrm{Q}})}{L_{\mathrm{A}}}} - \frac{V_{\mathrm{dc}}}{L_{\mathrm{A}}}(t-t_3) \qquad (10)$$

Since the voltage across the capacitor C_4 is zero, Φ_4 is turned on with ZVS. Thus, the incorporation of the augmented passive circuit into power inverter 500 is significant in reducing or even removing the undesirable power loss and EMI from the power switch present in the prior art.

(d) At t_4, the switch Φ_1 is turned off. The switch Φ4 is kept on-state and the switches Φ_2 and Φ_3 are kept off-state. The voltages across the parasitic capacitors C_1 and C_4 are 0, while the voltages across the parasitic capacitors C_2 and C_3 are V_{dc}. The transmitter current is still positive (i.e., i_p>0). During the TS2 ($t_4 \leq t < t_5$), the augmented inductor current is further decreased based on (10). By assuming the transmitter current to be $I_{\mathrm{p}}\sin(\omega t+\theta)$, the voltages across the parasitic capacitors C_1 and C_2 can be expressed as

$$v_{\mathrm{C1}}(t) = -\frac{I_{\mathrm{p}}}{2\omega C_{\mathrm{Q}}}\cos(\omega t+\theta) \qquad (11)$$

$$v_{\mathrm{C2}}(t) = V_{\mathrm{dc}} + \frac{I_{\mathrm{p}}}{2\omega C_{\mathrm{Q}}}\cos(\omega t+\theta) \qquad (12)$$

Then, the TS2 period can be calculated by

$$\Delta t_{45} = \frac{\cos^{-1}\left(-\frac{2\omega C_{\mathrm{Q}}V_{\mathrm{dc}}}{I_{\mathrm{p}}}\right)-\frac{\pi}{2}}{\omega} \qquad (13)$$

(e) At t_5, since C_2 is fully discharged, the diode D_2 is conducted. During the SS3 ($t_5 \leq t < t_6$), the transmitter current is still positive (i.e., i_p>0) and the augmented inductor current is further decreased based on (10).

(f) At t_6, the switch Φ_2 is turned on, while the switch Φ_4 is kept on-state and the switches Φ_1 and Φ_3 are kept off-state. Since the voltage across the capacitor C_2 is zero, Φ_2 is turned on with ZVS. During the SS4 ($t_6 \leq t < t_7$), the transmitter current is positive during the first half period, while it is negative during the second half period. The augmented inductor current is further decreased based on (10). When the inductor current is reduced to 0, the diode D_{A1} is blocked. The inductor current becomes negative, which is the sum of the augmented capacitor currents (i.e., $I_{\mathrm{LA}} = I_{\mathrm{CA1}} + I_{\mathrm{CA2}}$), as shown in Fig. 7(f2). When the augmented capacitor C_{A1} is fully charged and the augmented capacitor C_{A2} is fully discharged, the diode D_{A2} is conducted and the augment inductor is kept unchanged at the minimum value as

$$i_{\mathrm{LA}}(t) = -\frac{V_{\mathrm{dc}}}{\sqrt{\frac{L_{\mathrm{A}}}{2C_{\mathrm{A}}}}} \qquad (14)$$

Thus, summarising at this juncture, the augmented passive circuit further comprises a diode circuit branch 508, the diode circuit branch comprising a first diode D_{A1} and a second diode D_{A2} connected in series with one another, the diode circuit branch 508 being connected in parallel to the leading bridge leg 502 and the lagging bridge leg 504, the power inverter 500 being configured for, when a first one of the first and second power switches (in this step (f), this is Φ_2) is switched on and a second one of the first and second power switches (in this step (f), this is Φ_1) is in a switched off state, the first one of the third and fourth power switches (in this step (f), this is Φ_3) is in a switched off state and a second one of the third and fourth power switches (in this step (f), this is Φ_4) is in a switched on state, , for a first one of the first and second diodes (in this step (f), this is D_{A1}) to be in a conductive state and a second one of the first and second diodes (in this step (f), this is D_{A2}) to be in a non-conductive state; and wherein the power inverter 500 is configured for current in the inductor L_A to become zero, and for the first one of the first and second diodes (in this step (f), this is D_{A1}) to be switched to a non-conductive state.

Further summarising, the augmented passive circuit further comprises a capacitor circuit branch 506, the capacitor circuit branch 506 comprising a first capacitor CA1 and a second capacitor C_{A2} connected in series with one another, the capacitor circuit branch 506 being connected in parallel to the leading bridge leg 502 and the lagging bridge leg 504, the power

inverter 500 being configured for a magnitude of the current in the inductor L_A to increase (in this step (f), the inductor current becomes negative after having been zero), for a first one of the first capacitor and the second capacitor (in this step (f), this is C_{A1}) to be fully charged and for a second one of the first capacitor and the second capacitor to be fully discharged (in this step (f), this is C_{A2}), and for the second one of the first and second diodes (in this step (f), this is D_{A2}) to be switched to a conductive state.

(g) At t_7, the switch Φ_4 is turned off, while the switch Φ_2 is kept on-state and the switches Φ_1 and Φ_3 are kept off-state. The transmitter current is negative (i.e., i_p<0). The voltage across the parasitic capacitors C_1 and C_3 are V_{dc}, while the voltages across the parasitic capacitors C_2 and C_4 are 0. During the TS3 ($t_7 \leq t < t_8$), the capacitor C_3 is discharged and the capacitor C_4 is charged. The augmented inductor L_A and the parasitic capacitors C_3 and C_4 can form an *LC* resonator, such that the energy stored in the parasitic capacitor C_3 can be released before the switch Φ_3 is turned on. The current flowing through the augmented inductor, and the voltages across the capacitors C_3 and C_4 can be expressed as

$$i_{\mathrm{LA}}(t) = -\frac{V_{\mathrm{dc}}}{\sqrt{\frac{L_{\mathrm{A}}}{2C_{\mathrm{A}}}}}\cos\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t-t_7)\right] \quad (15)$$

$$v_{\mathrm{C3}}(t) = V_{\mathrm{dc}} - V_{\mathrm{dc}}\sqrt{\frac{C_{\mathrm{A}}}{C_{\mathrm{Q}}}}\sin\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t-t_7)\right] \quad (16)$$

$$v_{\mathrm{C4}}(t) = V_{\mathrm{dc}}\sqrt{\frac{C_{\mathrm{A}}}{C_{\mathrm{Q}}}}\sin\left[\frac{1}{\sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}}(t-t_7)\right] \quad (17)$$

The TS3 period can be calculated based on (16) or (17) as

$$\Delta t_{78} = \sqrt{2L_{\mathrm{A}}C_{\mathrm{Q}}}\sin^{-1}\left(\sqrt{\frac{C_{\mathrm{Q}}}{C_{\mathrm{A}}}}\right) \quad (18)$$

Thus, in this step the augmented passive circuit again operates where the power inverter 500 is configured for the inductor L_A to combine with the third power switch parasitic capacitance C_3 and the fourth power switch capacitance C_4 to form a resonator, but the switching arrangement is the reverse of that described above in step (a), viz: when a first one of the third and fourth power switches Φ_3, Φ_4 (in this step (g), this is now the fourth power switch Φ_4) is switched off and a second one of the third and fourth power switches Φ_3, Φ_4 (now, in this step (g), the third power switch Φ_3) is in a switched off state, and for

energy stored in the parasitic capacitance of the second one of the third and fourth power switches (in this step (g), this is C_3 of Φ_3) to be discharged before the second one of the third and fourth power switches (in this step (g), this is Φ_3) is switched on.

(h) At t_8, the parasitic capacitor C_4 is fully charged and the parasitic capacitor C_3 is fully discharged. The switch Φ_2 is on-state, while the switches Φ_1, Φ_3, and Φ_4 are off-state. The augmented inductor current can be calculated by substituting (18) into (15), as

$$i_{\mathrm{LA}}(t_8) = -V_{\mathrm{dc}}\sqrt{\frac{2(C_{\mathrm{A}}-C_{\mathrm{Q}})}{L_{\mathrm{A}}}} \qquad (19)$$

During the SS5 ($t_8 \leq t < t_9$), both the transmitter current and augmented inductor current are negative (i.e., i_{p}<0 and i_{LA}<0).

(i) At t_9, the switch Φ_3 is turned on. The switch Φ_2 is kept on-state and the switches Φ_1 and Φ_4 are kept off-state. The transmitter current is still negative (i.e., i_{p}<0). During the SS6 ($t_9 \leq t < t_{10}$), the augmented inductor current is increased when the DC source is connected, as

$$i_{\mathrm{LA}}(t) = -V_{\mathrm{dc}}\sqrt{\frac{2(C_{\mathrm{A}}-C_{\mathrm{Q}})}{L_{\mathrm{A}}}} + \frac{V_{\mathrm{dc}}}{L_{\mathrm{A}}}(t-t_9) \qquad (20)$$

Since the voltage across the capacitor C_3 is zero, Φ_3 is turned on with ZVS.

(j) At t_{10}, the switch Φ_2 is turned off. The switch Φ_3 is kept on-state and the switches Φ_1 and Φ_4 are kept off-state. The voltages across the parasitic capacitors C_2 and C_3 are 0, while the voltages across the parasitic capacitors C_1 and C_4 are V_{dc}. The transmitter current is still negative (i.e., i_{p}<0). During the TS4 ($t_{10} \leq t < t_{11}$), the augmented inductor current is further increased based on (20). By assuming the transmitter current is $I_{\mathrm{p}}\sin(\omega t+\theta)$, the voltages across the capacitors C_1 and C_2 can be expressed as

$$v_{\mathrm{C1}}(t) = \frac{I_{\mathrm{p}}}{2\omega C_{\mathrm{Q}}}\cos(\omega t+\theta) \qquad (21)$$

$$v_{\mathrm{C2}}(t) = V_{\mathrm{dc}} - \frac{I_{\mathrm{p}}}{2\omega C_{\mathrm{Q}}}\cos(\omega t+\theta) \qquad (22)$$

Then, the TS4 period can be calculated as

$$\Delta t_{1011} = \frac{\frac{\pi}{2} - \cos^{-1}\left(\frac{2\omega C_{\mathrm{Q}} V_{\mathrm{dc}}}{I_{\mathrm{p}}}\right)}{\omega} \qquad (23)$$

(k) At t_{11}, since C_1 is fully discharged, the diode D_1 is conducted. During the SS7 ($t_{11} \leq t < t_{12}$), the transmitter current is still negative and the augmented inductor current is further increased based on (20).

(l) At t_{12}, the switch Φ_1 is turned on, while the switch Φ_3 is kept on-state and the switches Φ_2 and Φ_4 are kept off-state. Since the voltage across the capacitor C_1 is zero, Φ_1 is turned on with ZVS. During the SS8 ($t_{12} \leq t < t_{13}$), the transmitter current is negative during the first half period, while it is positive during the second half period. The augmented inductor current is further increased based on (20). When the inductor current is increased to 0, the diode D_{A2} is blocked. The inductor current becomes positive, which is the sum of the augmented capacitor currents (i.e., $I_{\mathrm{LA}} = I_{\mathrm{CA1}} + I_{\mathrm{CA2}}$), as shown in Fig. 7(l2). When the augmented capacitor C_{A1} is fully discharged and the augmented capacitor C_{A2} is fully charged, the diode D_{A1} is conducted and the augment inductor is kept unchanged at the maximum value as

$$i_{\mathrm{LA}}(t) = \frac{V_{\mathrm{dc}}}{\sqrt{\frac{L_{\mathrm{A}}}{2C_{\mathrm{A}}}}} \qquad (24)$$

Thus, summarising again at this juncture, it will be seen once more that the power inverter 500 is configured for, a first one of the first and second power switches (in this step (l), this is Φ_1) is switched on and a second one of the first and second power switches (in this step (l), this is Φ_2) is in a switched off state, the first one of the third and fourth power switches (in this step (l), this is Φ_4) is in a switched off state and a second one of the third and fourth power switches (in this step (l), this is Φ_3) is in a switched on state, for a first one of the first and second diodes (in this step (l), this is D_{A2}) to be in a conductive state and a second one of the first and second diodes (in this step (l), this is D_{A1}) to be in a non-conductive state; and wherein the power inverter 500 is configured for current in the inductor L_A to become zero, and for the first one of the first and second diodes (in this step (l), this is D_{A2}) to be switched to a non-conductive state.

Further summarising, it will be seen once more that the power inverter 500 is configured for a magnitude of the current in the inductor L_A to increase (in this step (I), the inductor current becomes positive after having been zero), for a first one of the first capacitor and the second capacitor (in this step (I), this is C_{A2}) to be fully charged and for a second one of the first capacitor and the second capacitor to be fully discharged (in this step (I), this is C_{A1}), and for the second one of the first and second diodes (in this step (I), this is D_{A1}) to be switched to a conductive state.

Obviously, the WPT system with the known phase shift control can implement ZVS for both bridge legs with the integration of the augmented circuit. As a result, the EMI emission, especially the conducted EMI can be reduced.

Assume that the augmented inductor current takes about $\frac{1}{N}$ switching cycle to increase from 0 to the maximum value (i.e., I_{max}), such as

$$\frac{\pi}{2}\sqrt{2L_{\mathrm{A}}C_{\mathrm{A}}} = \frac{T_{\mathrm{S}}}{N} \qquad (25)$$

Then, the parameters of the augmented inductor and capacitors can be calculated based on (24) and (25) as

$$L_{\mathrm{A}} = \frac{2V_{\mathrm{dc}}T_{\mathrm{S}}}{I_{\mathrm{max}}N\pi} \qquad (26)$$

$$C_{\mathrm{A}} = \frac{I_{\mathrm{max}}T_{\mathrm{S}}}{V_{\mathrm{dc}}N\pi} \qquad (27)$$

Therefore, a passive augmented circuit is disclosed that can turn a phase-shift power inverter into a fully soft-switched power inverter for the entire operating range (i.e. phase-shift angle from 0° to 180°. The proposed passive circuit has the following advantageous features:

- Independent of the compensation topologies of the transmitter (Tx) and receiver (Rx) circuits. For wireless power transfer systems, the leakage inductances of the transmitting and receiving coils require capacitive compensation. The compensation networks can be various types, i.e., series-series (capacitors in series for both Tx and Rx

coils), series-parallel (the capacitor in series with Tx coil and the capacitor in parallel with Rx coil), LCC-LCC, and so on;

- No requirement for the regulations of firing angles of the power switches or switching frequencies based on in-band or out-of-band communication between the Tx and Rx circuits;
- It may be implemented for full load operating conductions including light- and no-load conditions;
- It may be implemented for constant frequency operation of the inverter output voltage.

The proposed circuit has been tested for the full range of phase-shift angle from 0° to 180°. Practical measurements of the circuit waveforms and electromagnetic radiation are included to confirm its feasibility to achieve soft switching in the full operating range.

As noted above, the augmented passive circuit can be fitted (for example, retrofitted) to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system. Thus, a method of fitting (retrofitting) comprises connecting a capacitor circuit branch 506 in parallel to the leading bridge leg 502 and the lagging bridge leg 504, the capacitor circuit branch comprising a first capacitor C_{A1} and a second capacitor C_{A2} connected in series with one another at a capacitor branch connection point X_1; connecting a diode circuit branch 508 in parallel to the leading bridge leg 502 and the lagging bridge leg 504, the diode circuit branch 508 comprising a first diode D_{A1} and a second diode D_{A1} connected in series with one another at a diode branch connection point X_2; and connecting an inductor L_A at a first inductor terminal to the capacitor branch connection point X_1 and the diode branch connection point X_2 and connecting the inductor L_A at a second inductor terminal to one of the first and second output terminals 510, 512.

Components for the augmented passive circuit may be provided in the form of a kit of parts for fitting to a phase-shift modulated full-bridge power inverter configured for use any wireless power transfer system. Thus, a kit of augmented passive circuit parts for fitting to a phase-shift modulated full-bridge power inverter 500 configured for use in a wireless power transfer system, comprises: a first capacitor C_{A1} and a second capacitor C_{A2} to be connected in series with one another at a capacitor branch connection point X_1 in a capacitor circuit branch 506, the capacitor circuit branch 506 to be connected in parallel to a leading bridge

leg 502 and a lagging bridge leg 504 of the power inverter; a first diode D_{A1} and a second diode D_{A2} to be connected in series with one another at a diode branch connection point X_2 in a diode circuit branch 508 , the diode circuit branch 508 to be connected in parallel to the leading bridge leg 502 and the lagging bridge leg 504; and an inductor L_A to be connected at a first inductor terminal to the capacitor branch connection point X_1 and the diode branch connection point X_2 and to be connected at a second inductor terminal to one of power inverter first and second output terminals 510, 512.

Simulation Results

Simulations are carried out on a WPT system (schematic diagram as shown in Fig. 1) with the parameters given in Table 1 using Psim10.0. The battery load is modelled as a pure resistive load R_L without losing generality. The switching frequency is 100 kHz. The deadtime of the switching signal is 0.1 μs. PI controllers are adopted for both current and voltage control. The parameters of the current controller are K_{PI}=1 and K_{iI}=100000 and the parameters of the voltage controller are K_{PV}=0.1 and K_{iV}=10000. The output current and voltage references are I_{bref}=1.675A and V_{bref}=4.2V. Two cases are investigated in simulation. In case 1, the output current is controlled to track the current reference with the phase shift angle being greater than 120°. In case 2, the output voltage is controlled to track the voltage reference with the phase shift angle being greater than 165°, which means the on-pulse width of the input voltage of the transmitter (i.e., v_p) is less than 15°.

Parameters	Value	Parameters	Value
V_{dc}	24 V	L_p	48.4 μH
L_s	48.4 μH	M	7.1 μH
C_p	52.3 nF	C_s	52.3 nF
R_p	0.1 Ω	R_s	0.1 Ω
C_f	20 μF	R_L	10 Ω
C_1	1 nF	C_2	1 nF
C_3	1 nF	C_4	1 nF
C_{A1}	100 nF	C_{A2}	100 nF
L_A	1 μH		

TABLE 1. Main Parameters of WPT System in Simulation

For case 1, the waveforms of the output current (i.e., I_b), output current reference (i.e., I_{bref}), transmitter current (i.e., i_p), input voltage of the transmitting resonator (i.e., v_p), and the four switching signals (i.e., S_1, S_2, S_3, and S_4) of the WPT system without the augmented circuit (known WPT system) and with the augmented circuit are shown in Fig. 8. Both output currents are well-regulated to track the current reference (i.e., I_{bref}=1.675 A), and the transmitter currents are in phase with the input voltages of the transmitting resonators. The phase shift angles between the diagonal switching signals are controlled at 131.8° and 129.2° for the WPT systems without the augmented circuit and with the augmented circuit, respectively.

The waveforms of corresponding drain currents (i.e., I_{d1}, I_{d2}, I_{d3}, and I_{d4}) and drain-to-source voltages (i.e., V_{ds1}, V_{ds2}, V_{ds3}, and V_{ds4}) of the four switches are shown in Fig. 9. The four transient periods are labelled as TS_{A1}, TS_{A2}, TS_{A3}, and TS_{A4} for the WPT system without the augmented circuit, and the transient periods are labelled as TS_{B1}, TS_{B2}, TS_{B3}, and TS_{B4} for the WPT system with the augmented circuit. Apparently, hard switching occurs on the lagging bridge leg (i.e., Φ_3 and Φ_4) of the WPT system without the augmented circuit during TS_{A1} and TS_{A3}, respectively. However, ZVS can be implemented for all the four switches of the WPT system with the augmented circuit.

The corresponding V_{ds}-I_d curves of the switches of the WPT system without and with the augmented circuit are plotted, as shown in Fig. 10. It is clear to observe that the enclosed areas of Φ_3 and Φ_4 of the WPT system with the augmented circuit are significantly shrunk. The hard-switching issue of Φ_3 and Φ_4 for the known WPT system with phase shift control is addressed by incorporating the augmented circuit.

For case 2, the waveforms of the output voltage (i.e., V_b), output voltage reference (i.e., V_{bref}), transmitter current (i.e., i_p), input voltage of the transmitting resonator (i.e., v_p), and the four switching signals (i.e., S_1, S_2, S_3, and S_4) of the WPT system without the augmented circuit (known WPT system) and with the augmented circuit are shown in Fig. 11. He output voltages are regulated to track the reference (i.e., V_{bref}=4.2 V). The phase shift angle

between the diagonal switching signals is controlled at 165.4° and 169.2° for the WPT system without and with the augmented circuit, respectively.

The corresponding V_{ds}-I_d curves of the switches of the WPT system without and with the augmented circuit are plotted, are shown in Fig. 12. Similar to the results of case 1, hard switching occurs on the lagging bridge leg of the WPT system without the augmented circuit, while ZVS are implemented for all the switches of the WPT system with the augmented circuit.

The V_{ds}-I_d curves of the switches of the WPT system without and with the augmented circuit are also plotted, as shown in Fig. 13. Similar to the results of case 1, the enclosed areas of Φ_3 and Φ_4 of the WPT system with the augmented circuit are significantly shrunk.

Experimental Verification

Experiments are conducted on a WPT system with the same parameters, as given in Table 1. The frequency and deadtime of the switching signals of the full-bridge inverter are also identical to those being used in the simulation. The MOSFETs of the full-bridge inverter is Infineon's IRFP250M. Rogowski coils are adopted to measure the drain currents of the four DIP MOSFETs. The conducted EMI of the full-bridge inverter are measured by Advantest's spectrum analyzer R3261C. Background EMIs of the EMC chamber are shown in "Further Data, Section A" below. RIGOL's DP832 is adopted as the DC power supply for the WPT system. The controller is implemented using Texas Instrument (TI)'s digital signal processor (DSP) TMS320F28335. The parameters of the current controller are K_{PI}=0.00001 and K_{iI}=0.1 and the parameters of the voltage controller are K_{PV}=0.00001 and K_{iV}=10000. The output current and voltage references are also I_{bref}=1.675A and V_{bref}=4.2V. In experiment, both CC and CV control are studied.

First, the output current of the WPT system (i.e., I_b) is controlled to track the reference (i.e., I_{bref}) at 1.675 A. The waveforms of drain-to-source voltages and drain currents of the switch Φ_3 (i.e., v_{ds3} and i_{d3}), transmitter currents (i.e., i_p), and input voltages of the transmitting resonators (i.e., v_p) for the WPT system without and with the augmented circuit are shown in Fig. 16. The phase shift angles are controlled at 148.6° for the WPT system without the augmented circuit and at 148.2° for the WPT system with the augmented circuit. The

waveforms in Figs. 14(a2) and (b2) are magnified from the waveforms in Figs. 14(a1) and (b1), respectively. The waveforms in Figs. 14(a3) and (b3) are magnified from the waveforms in Figs. 14(a2) and (b2), respectively. The waveforms of v_{ds3} and i_{d3} in Fig. 14(a3) show that hard switching occurs for the known WPT system without the augmented circuit. However, ZVS can be achieved when the augmented circuit is integrated into the full-bridge inverter, as shown in Fig. 14(b3). Comparisons of conducted EMI from 150 kHz to 30 MHz between the full-bridge inverter without and with the augmented circuit are shown in Fig. 15. Apparently, the conducted EMI of the full-bridge inverter without the augmented circuit exceeds the upper limit of the standard EN55022. By incorporating the augmented circuit, the conducted EMI of the full-bridge inverter is significantly mitigated below the upper limit.

Then, the output voltage of the WPT system (i.e., V_b) is controlled to track the reference (i.e., V_{bref}) at 4.2 V. The phase shift angles are controlled at 166.2° and 169.8° for the WPT system without and with the augmented circuit, respectively. The comparisons of the magnified waveforms of v_{ds3} and i_{d3} within a 0.5μs transient state between the full-bridge inverters with and without the augmented circuit, are shown in Fig. 16. The magnified waveforms show that the hard switching occurs for the known WPT system without the augmented circuit, while ZVS can be achieved by integrating the augmented circuit, even if the phase shift angle has reached about 170° (i.e., the on-pulse width of v_p is only about 10°). Comparisons of conducted EMI from 150 kHz to 30 MHz between the full-bridge inverter without and with the augmented circuit are shown in Fig. 17. Obviously, the conducted EMI of the full-bridge inverter without the augmented circuit also exceeds the upper limit of the standard EN55022 for the voltage control. However, by integrating the augmented circuit, the EMI can be dramatically reduced.

Similar experiments are also conducted on the WPT system with the phase shift angle of 120°, 90°, 60°, 30°, and 0°, respectively. The corresponding waveforms of v_{ds3}, i_{d3}, i_p, and v_p for the WPT system without and with the augmented circuit are shown in "Further data, Section B" below. The results reveal that the augmented circuit can also achieve ZVS for heavy load conditions. The corresponding conducted EMI of the full-bridge inverter without and with the augmented circuit are presented in Fig. 18. Obviously, conducted EMIs are mitigated by the augmented circuit for the heavy load conditions. However, it is worthy to

note that the EMI reduction is more significant for the WPT system with a lager phase shift angle.

Further data

A. Background EMIs of the EMC Chamber

Since both the full-bridge inverter and controller circuit are placed inside the test chamber, four background EMIs, including (i) the conducted EMI without the power supplies for auxiliary circuits of the full-bridge inverter and the controller circuit, (ii) the conducted EMI with the power supplies for auxiliary circuits of the full-bridge inverter but without the controller circuit, (iii) the conducted EMI without the power supplies for auxiliary circuits of the full-bridge inverter but with the controller circuit, and (iv) the conducted EMI with the power supplies for auxiliary circuits of the full-bridge inverter, are measured as references, as shown in Fig. 19.

B. Waveforms of v_{ds3}, i_{d3}, i_p, and v_p of the WPT Systems with Different Phase Shift Angles

Experimental waveforms of v_{ds3}, i_{d3}, i_p, and v_p of the full-bridge inverter without and with the augmented circuit for the phase shift angle at 120°, 90°, 60°, 30°, and 0° are shown in Fig. 20.

It will be appreciated that the invention has been described by way of example only. Various modifications may be made to the techniques described herein without departing from the spirit and scope of the appended claims. The disclosed techniques comprise techniques which may be provided in a stand-alone manner, or in combination with one another. Therefore, features described with respect to one technique may also be presented in combination with another technique.

The current application also describes the following concepts.

1 An augmented passive circuit (with connections shown in Fig. 5) comprising two diodes, two capacitors and one inductor for achieving soft switching in all the power switches in a power inverter under phase-shift modulation control.

2 The augmented passive circuit can be added to a power inverter to achieve soft switching under either fixed-frequency or variable-frequency operations of power inverter.

3 The augmented passive circuit can reduce the switching power stress and power losses to improve the lifetime and conversion efficiency of power inverters.

4 The augmented passive circuit can be used to modify existing designs of wireless power transfer systems compliant with the standards of the Wireless Power Consortium and Society of Automotive Engineers without changing the control algorithms.

5 The augmented passive circuit can be transformed as an augmented active circuit by replacing the inductor with an actively-controlled current source or an equivalent current source, while still maintaining the functions described in the above points 2 to 4.

6 A design method for the augmented passive circuit based on the equations (25) to (27).

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Claims

1. A phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the power inverter comprising:

a leading bridge leg comprising:

a first power switch, the first power switch having a first power switch parasitic capacitance; and

a second power switch, the second power switch having a second power switch parasitic capacitance;

a lagging bridge leg comprising:

a third power switch, the third power switch having a third power switch parasitic capacitance; and

a fourth power switch, the fourth power switch having a fourth power switch parasitic capacitance; wherein

the power inverter is configured for each of the power switches to be switched on and off in a switching cycle; and wherein the power inverter further comprises:

an augmented passive circuit comprising an inductor, wherein the power inverter is configured for the inductor to combine with the third power switch parasitic capacitance and the fourth power switch capacitance to form a resonator when a first one of the third and fourth power switches is switched off and a second one of the third and fourth power switches is in a switched off state, and for energy stored in the parasitic capacitance of the second one of the third and fourth power switches to be discharged before the second one of the third and fourth power switches is switched on.

2. The power inverter of claim 1, the augmented passive circuit further comprising a diode circuit branch, the diode circuit branch comprising a first diode and a second diode connected in series with one another, the diode circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg, the power inverter being configured for, when:

a first one of the first and second power switches is switched on and a second one of the first and second power switches is in a switched off state;

the first one of the third and fourth power switches is in a switched off state and a second one of the third and fourth power switches is in a switched on state;

and

for a first one of the first and second diodes to be in a conductive state and a second one of the first and second diodes to be in a non-conductive state; and wherein the power inverter is configured for current in the inductor to become zero, and for the first one of the first and second diodes to be switched to a non-conductive state.

3. The power inverter of claim 2, the augmented passive circuit further comprising a capacitor circuit branch, the capacitor circuit branch comprising a first capacitor and a second capacitor connected in series with one another, the capacitor circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg, the power inverter being configured for a magnitude of the current in the inductor to increase, for a first one of the first capacitor and the second capacitor to be fully charged and for a second one of the first capacitor and the second capacitor to be fully discharged, and for the second one of the first and second diodes to be switched to a conductive state.

4. A phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the power inverter comprising:

a leading bridge leg;

a lagging bridge leg;

a first output terminal connected from a leading bridge leg connection point in the leading bridge leg;

a second output terminal connected from a lagging bridge leg connection point in the lagging bridge leg; and

an augmented passive circuit comprising:

a capacitor circuit branch, the capacitor circuit branch comprising a first capacitor and a second capacitor connected in series with one another at a capacitor branch connection point, the capacitor circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg;

a diode circuit branch, the diode circuit branch comprising a first diode and a second diode connected in series with one another at a diode branch connection point, the diode circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg; and

an inductor connected at a first inductor terminal to the capacitor branch connection point and the diode branch connection point and connected at a second inductor terminal to one of the first and second output terminals.

5. A method of operating a phase-shift modulated full-bridge power inverter in a wireless power transfer system, the power inverter comprising:

a leading bridge leg comprising:

a first power switch, the first power switch having a first power switch parasitic capacitance; and

a second power switch, the second power switch having a second power switch parasitic capacitance;

a lagging bridge leg comprising:

a third power switch, the third power switch having a third power switch parasitic capacitance;

a fourth power switch, the fourth power switch having a fourth power switch parasitic capacitance; and

an augmented passive circuit comprising an inductor;

the method comprising:

operating the power inverter so that each of the power switches is switched on and off in a switching cycle; and

switching a first one of the third and fourth power switches off when a second one of the third and fourth power switches is in a switched off state, for the inductor to combine with the third power switch parasitic capacitance and the fourth power switch capacitance to form a resonator and discharging energy stored in the parasitic capacitance of the second one of the third and fourth power switches before the second one of the third and fourth power switches is switched on.

6. The method of claim 5, wherein the augmented passive circuit further comprises a diode circuit branch, the diode circuit branch comprising a first diode and a second diode connected in series with one another, the diode circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg, the method further comprising:

switching a first one of the first and second power switches on when a second one of the first and second power switches is in a switched off state, and when the first one of

the third and fourth power switches is in a switched off state and a second one of the third and fourth power switches is in a switched on state; wherein a first one of the first and second diodes is in a conductive state and a second one of the first and second diodes is in a non-conductive state; wherein the power inverter current in the inductor becomes zero, the method further comprising switching the first one of the first and second diodes to a non-conductive state.

7. The method of claim 6, wherein the augmented passive circuit further comprises a capacitor circuit branch, the capacitor circuit branch comprising a first capacitor and a second capacitor connected in series with one another, the capacitor circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg, the method further comprising increasing a magnitude of the current in the inductor and charging fully a first one of the first capacitor and the second capacitor and discharging fully a second one of the first capacitor and the second capacitor, and switching the second one of the first and second diodes to a conductive state.

8. A method of fitting an augmented passive circuit to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the power inverter comprising:

a leading bridge leg;

a lagging bridge leg;

a first output terminal connected from a leading bridge leg connection point in the leading bridge leg; and

a second output terminal connected from a lagging bridge leg connection point in the lagging bridge leg; the method comprising:

connecting a capacitor circuit branch in parallel to the leading bridge leg and the lagging bridge leg, the capacitor circuit branch comprising a first capacitor and a second capacitor connected in series with one another at a capacitor branch connection point;

connecting a diode circuit branch in parallel to the leading bridge leg and the lagging bridge leg, the diode circuit branch comprising a first diode and a second diode connected in series with one another at a diode branch connection point; and

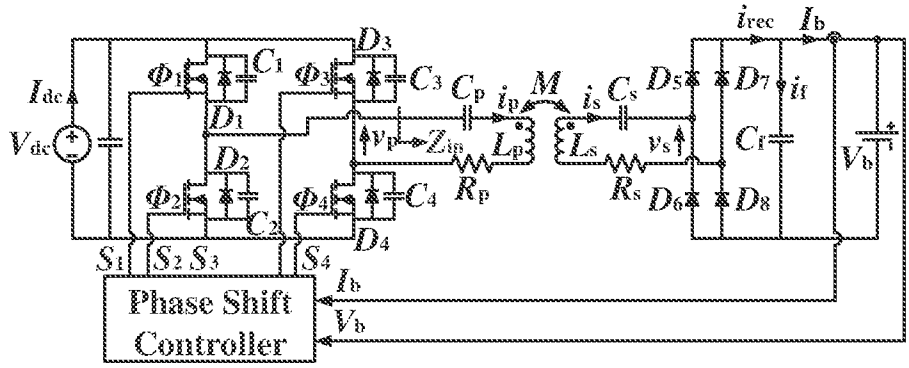
connecting an inductor at a first inductor terminal to the capacitor branch connection point and the diode branch connection point and connecting the inductor at a second inductor terminal to one of the first and second output terminals.

9. A kit of augmented passive circuit parts for fitting to a phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the kit of augmented passive circuit parts comprising:

a first capacitor and a second capacitor to be connected in series with one another at a capacitor branch connection point in a capacitor circuit branch, the capacitor circuit branch to be connected in parallel to a leading bridge leg and a lagging bridge leg of the power inverter;

a first diode and a second diode to be connected in series with one another at a diode branch connection point in a diode circuit branch, the diode circuit branch to be connected in parallel to the leading bridge leg and the lagging bridge leg; and

an inductor to be connected at a first inductor terminal to the capacitor branch connection point and the diode branch connection point and to be connected at a second inductor terminal to one of power inverter first and second output terminals.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I_b
I_{dc}
V_{dc}
Φ_1
C_1
D_1
Φ_3
D_3
C_3
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C_s
D_5
D_7
i_f
v_p
Z_{tp}
L_p
L_s
v_s
C_f
V_b
D_2
Φ_2
C_2
Φ_4
C_4
R_p
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S_1
S_2 S_3
S_4
I_b
V_b
Phase Shift Controller

Fig. 1

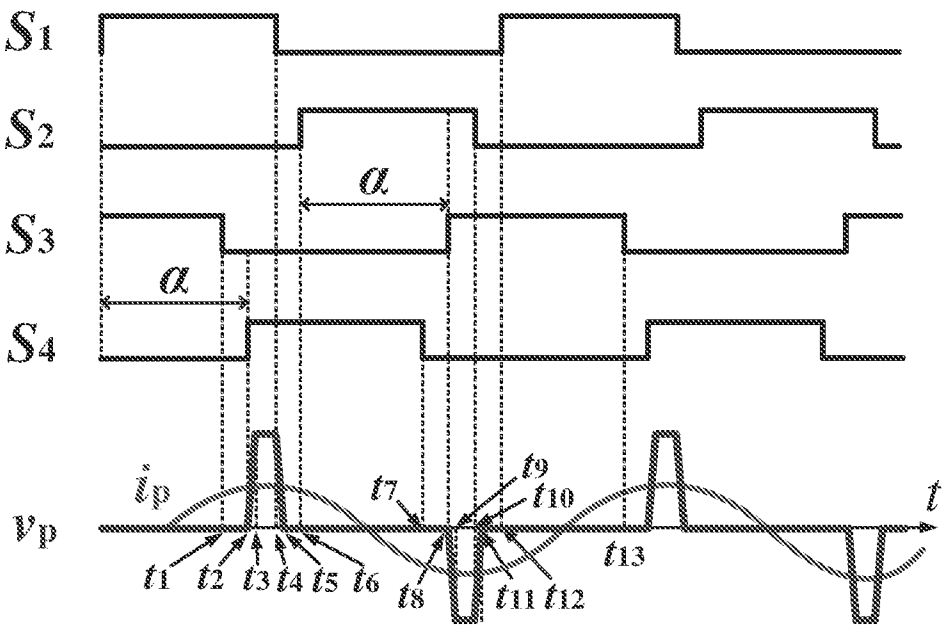
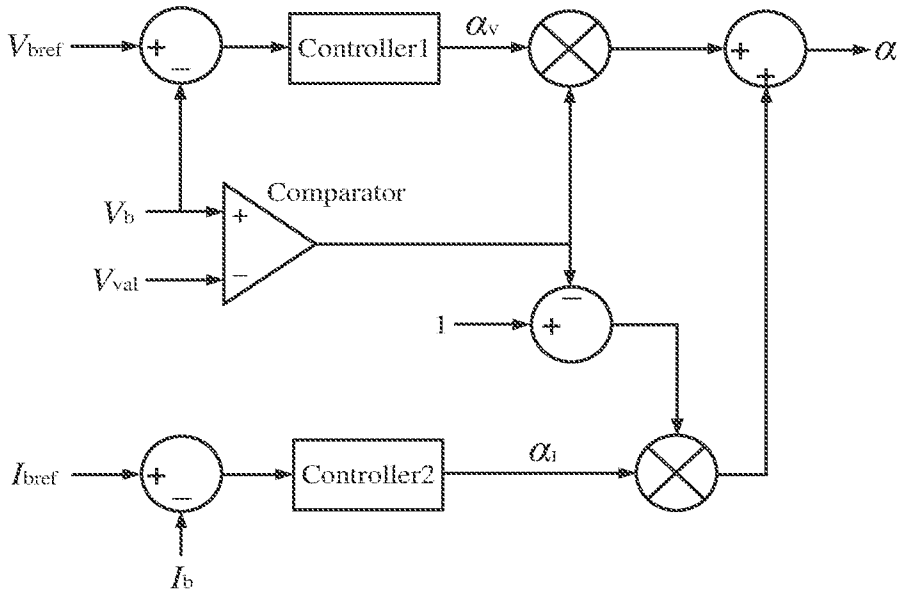

S_1
S_2
S_3
S_4
α
α
i_p
v_p
t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12} t_{13} t

Fig. 2


V_{bref}
Controller1
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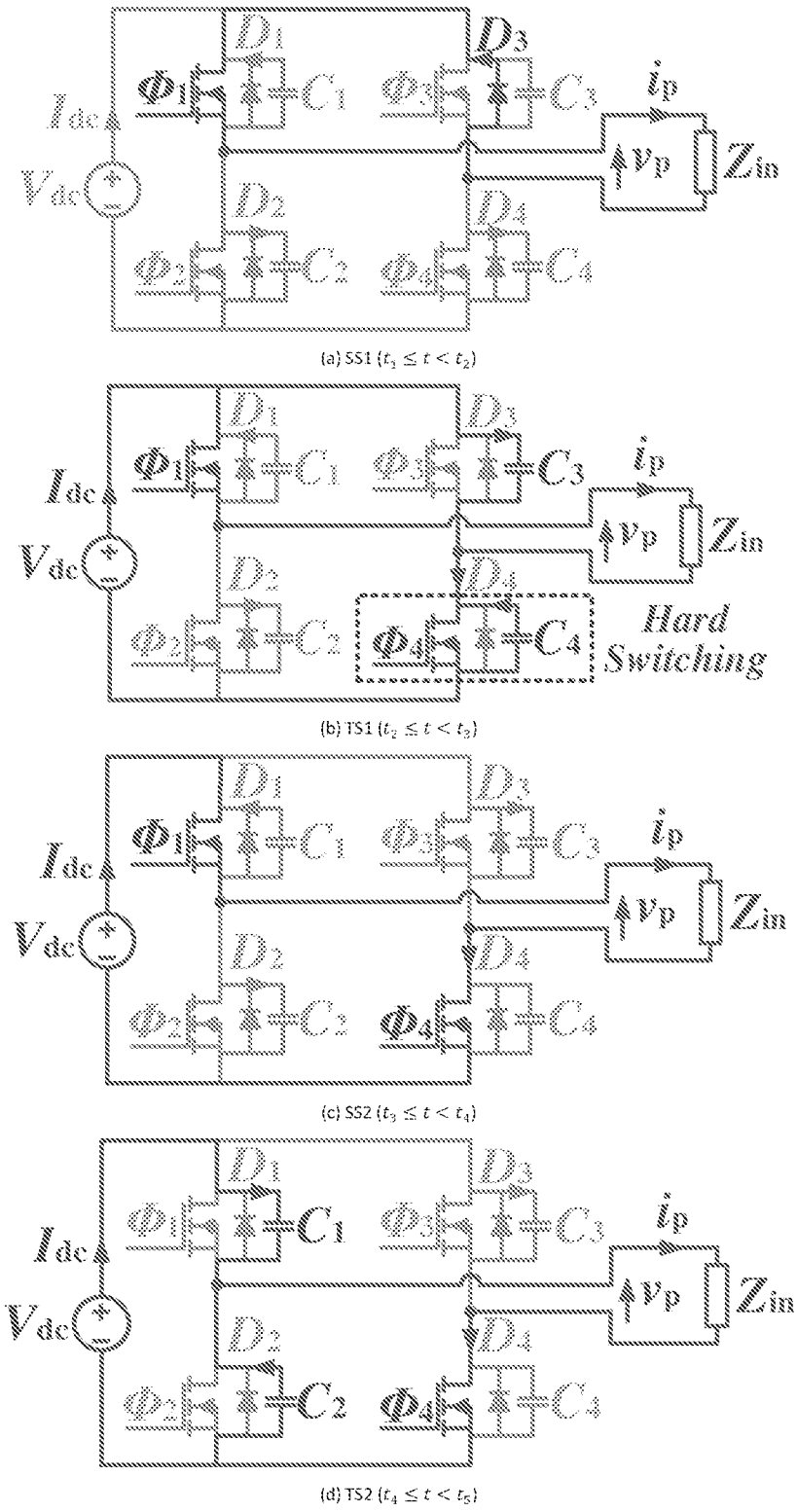
α
Comparator
V_b
V_{val}
1
I_{bref}
Controller2
α_i
I_b

Fig. 3



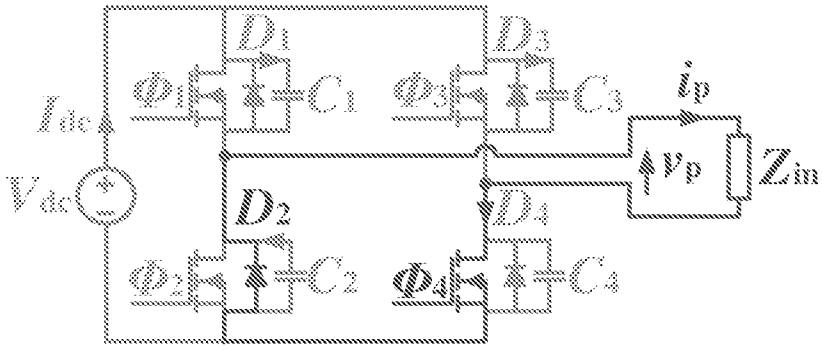
(a) SS1 ($t_1 \leq t < t_2$)

(b) TS1 ($t_2 \leq t < t_3$)

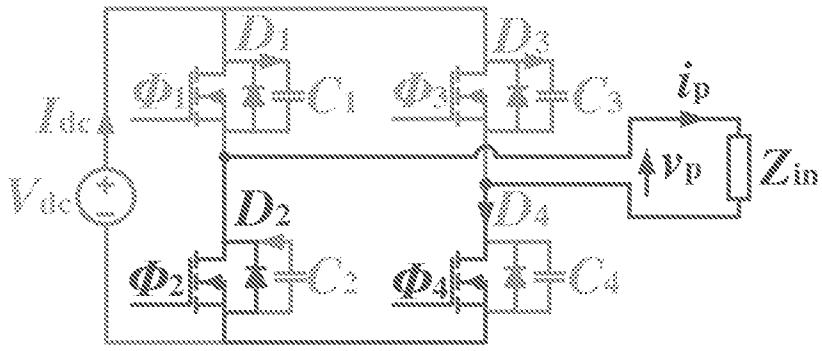
(c) SS2 ($t_3 \leq t < t_4$)

(d) TS2 ($t_4 \leq t < t_5$)

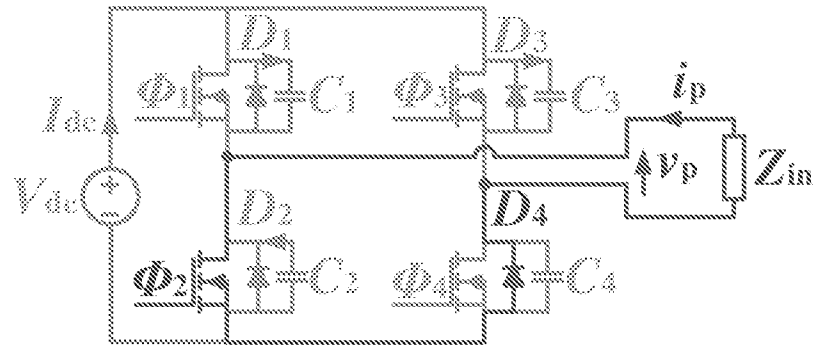
Fig. 4



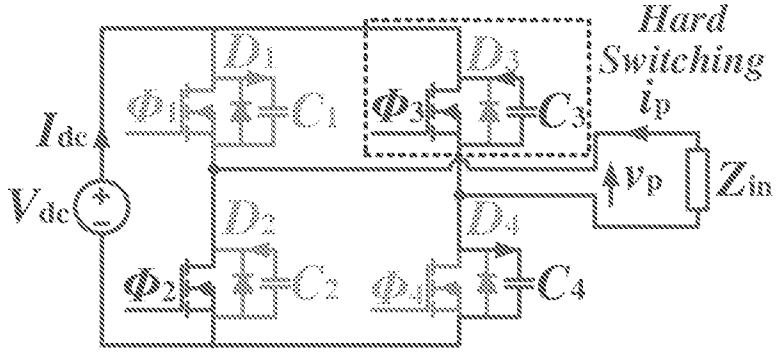
(e) SS3 ($t_5 \leq t < t_6$)



(f) SS4 ($t_6 \leq t < t_7$)

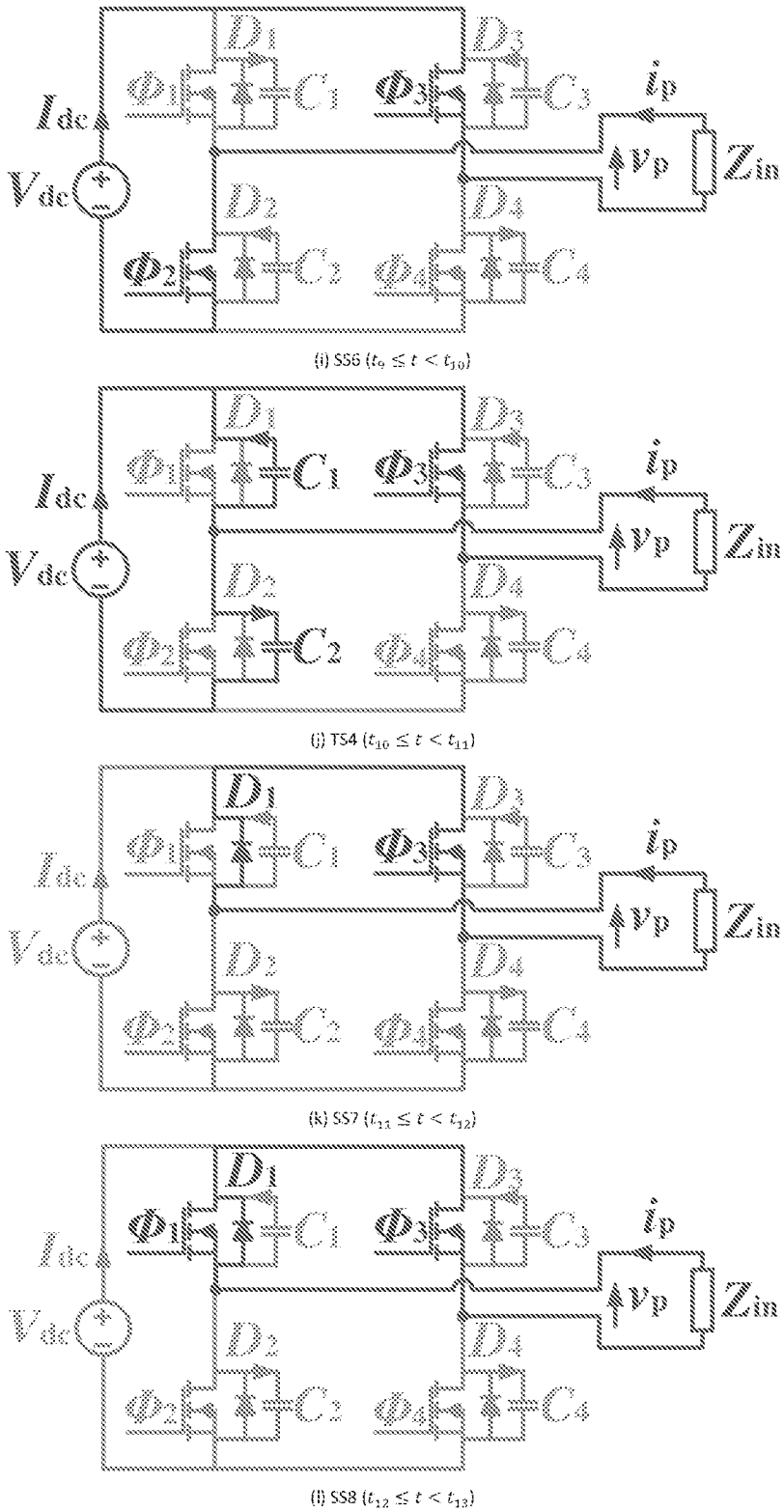


(g) SS5 ($t_7 \leq t < t_8$)



(h) TS3 ($t_8 \leq t < t_9$)

Fig. 4 (cont'd)



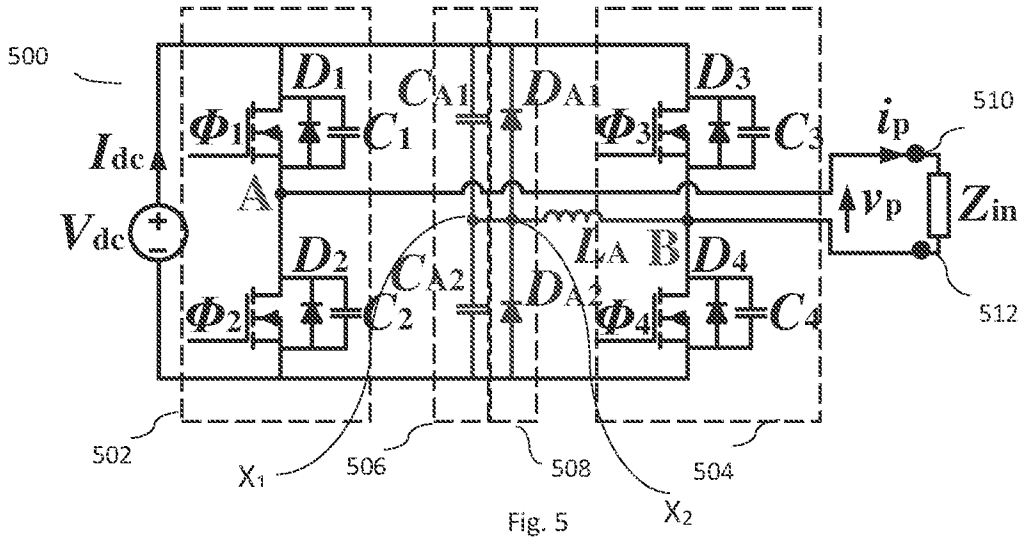
(i) SS6 ($t_9 \leq t < t_{10}$)

(j) TS4 ($t_{10} \leq t < t_{11}$)

(k) SS7 ($t_{11} \leq t < t_{12}$)

(l) SS8 ($t_{12} \leq t < t_{13}$)

Fig. 4 (cont'd)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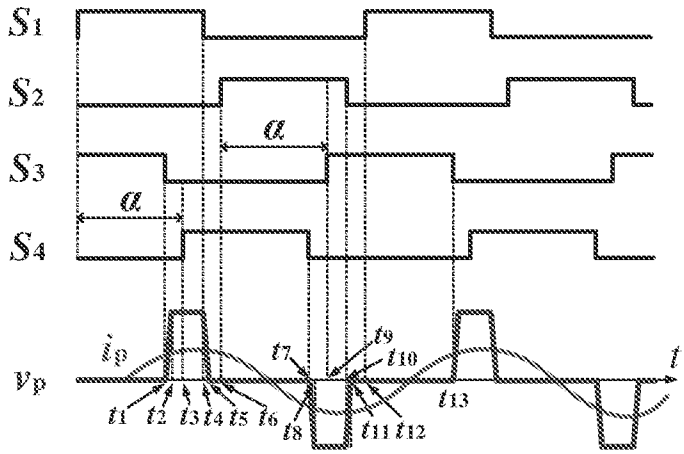
D_{A1}
D_3
Φ_1
C_1
Φ_3
C_3
i_p
510
I_{dc}
A
v_p
Z_{in}
V_{dc}
L_A
B
D_2
C_{A2}
D_{A2}
D_4
Φ_2
C_2
Φ_4
C_4
512
502
X_1
506
508
504
X_2

Fig. 5


S_1
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S_3
S_4
α
α
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v_p
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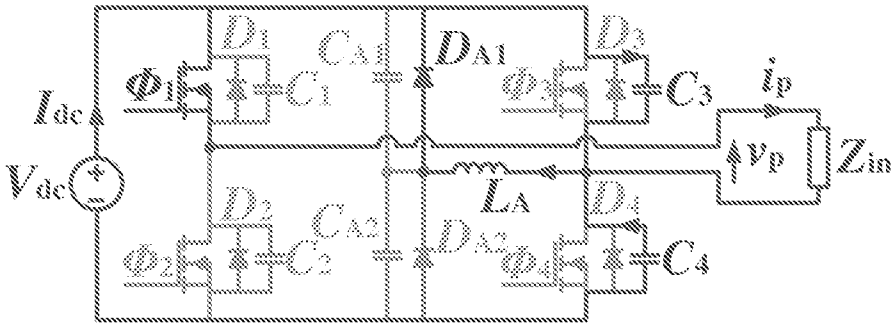
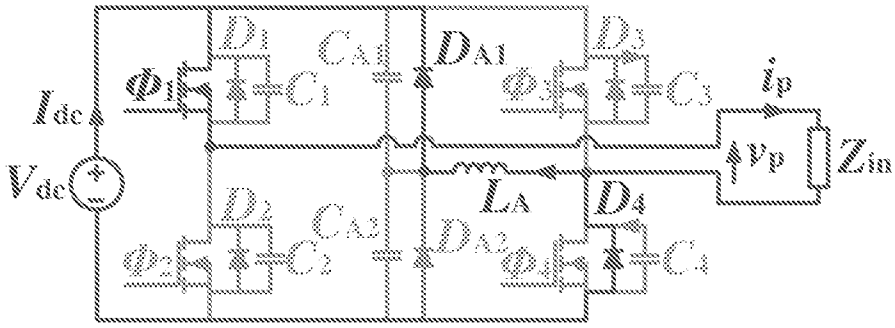
t

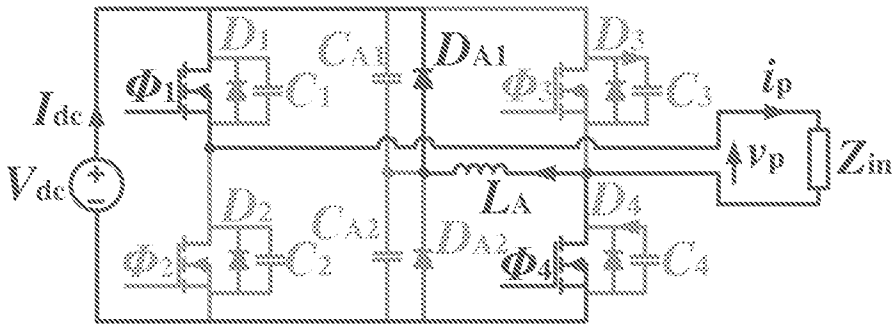
Fig. 6



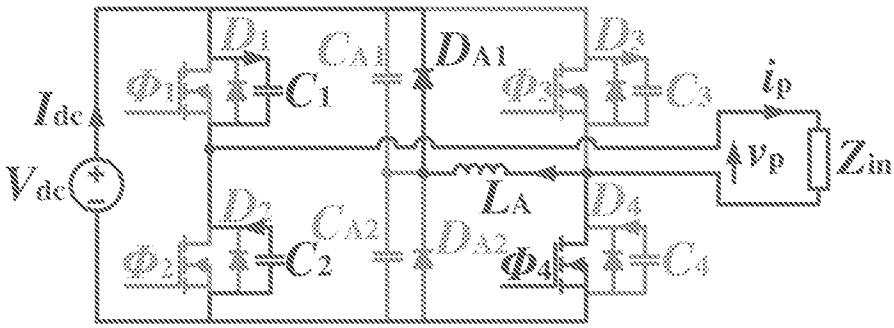
(a) TS1 ($t_1 \leq t < t_2$)



(b) SS1 ($t_2 \leq t < t_3$)

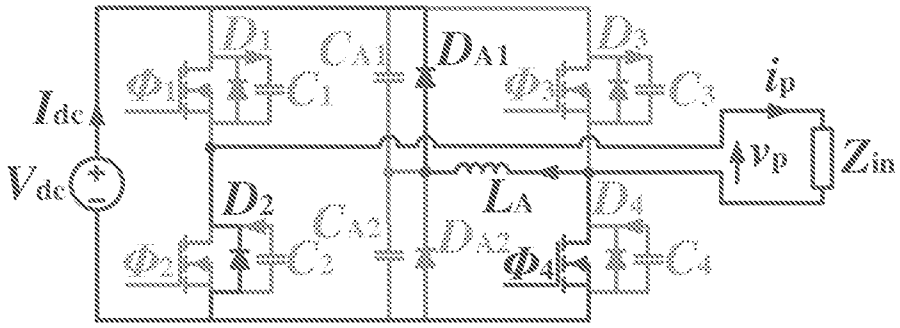


(c) SS2 ($t_3 \leq t < t_4$)

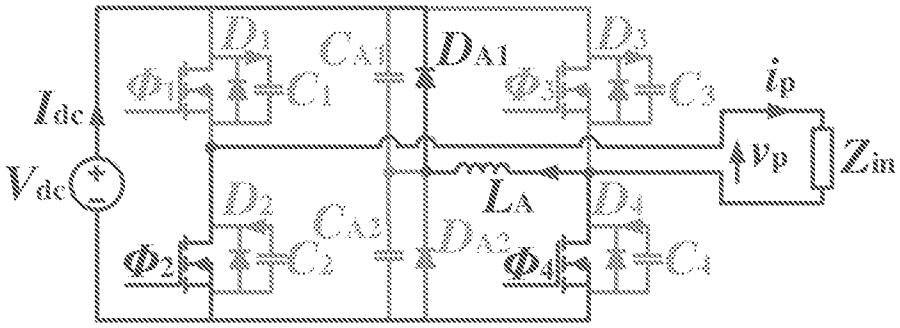


(d) TS2 ($t_4 \leq t < t_5$)

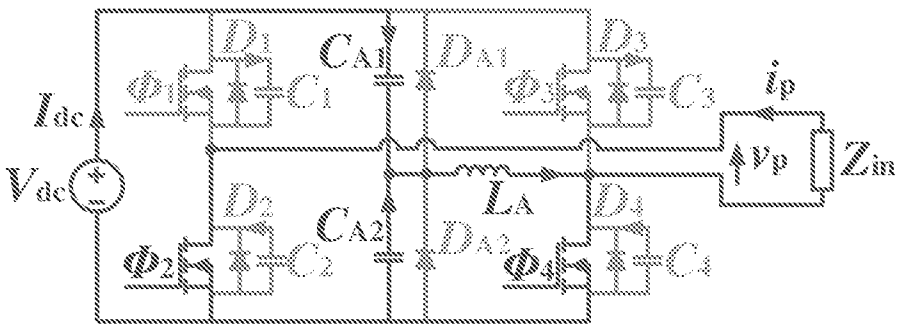
Fig. 7



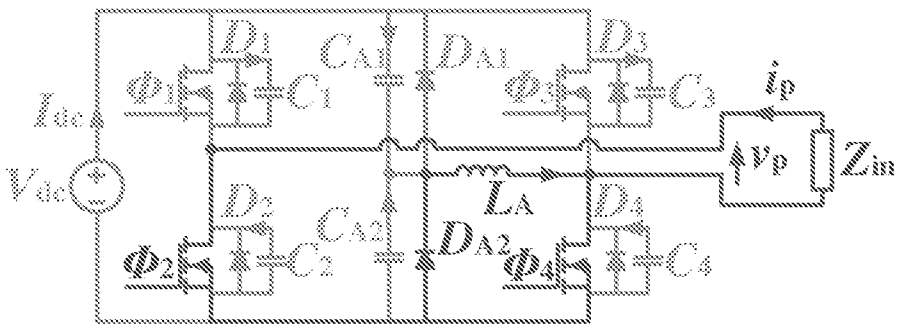
(e) SS3 ($t_5 \leq t < t_6$)



(f1) SS4 ($t_6 \leq t < t_7$)

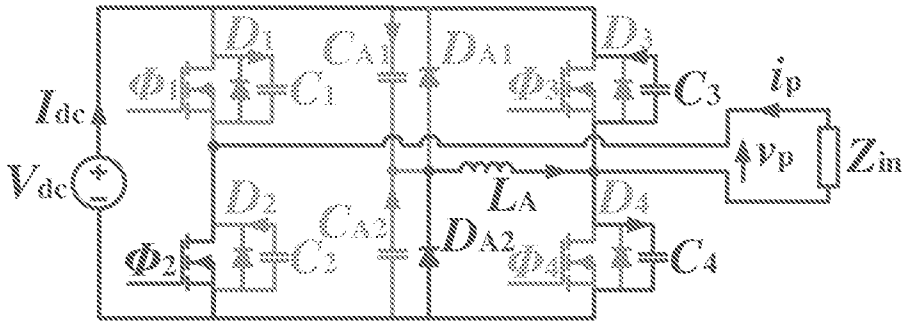


(f2) SS4 ($t_6 \leq t < t_7$)

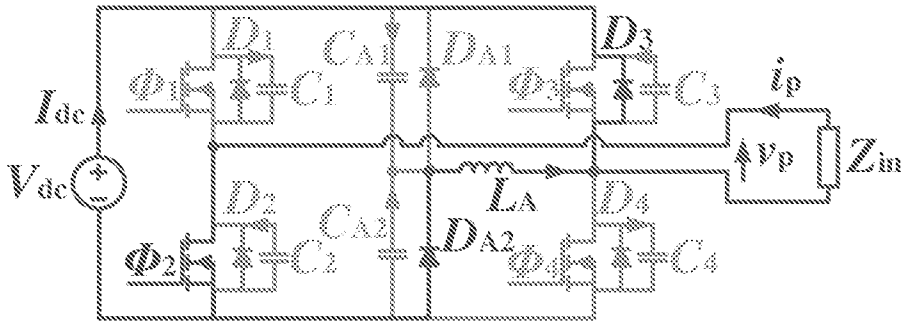


(f3) SS4 ($t_6 \leq t < t_7$)

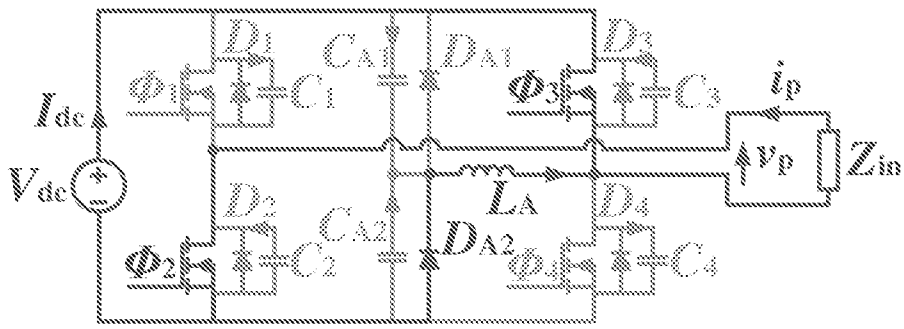
Fig. 7 (cont'd)



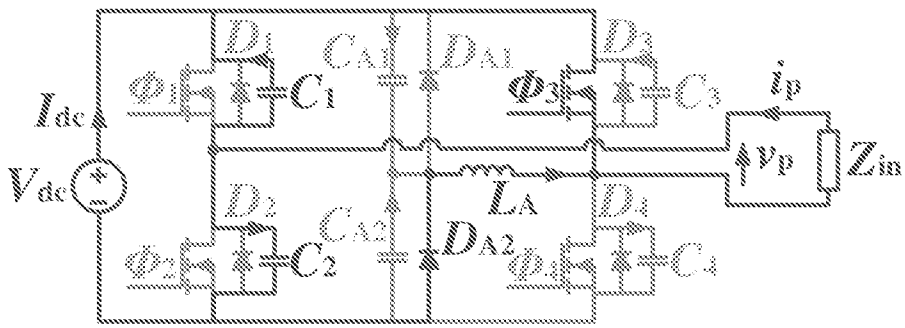
(g) TS3 ($t_7 \leq t < t_8$)



(h) SS5 ($t_8 \leq t < t_9$)

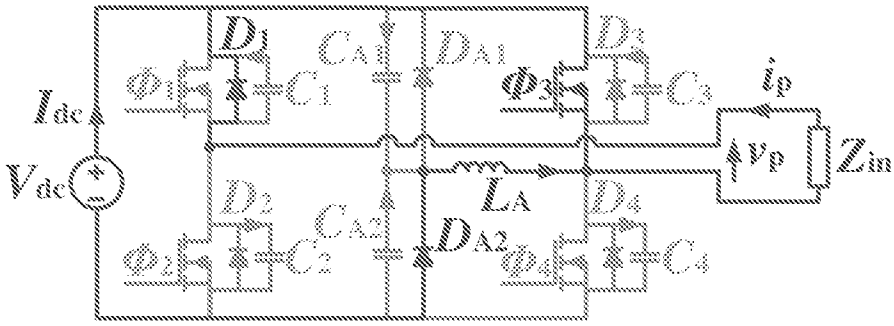


(i) SS6 ($t_9 \leq t < t_{10}$)

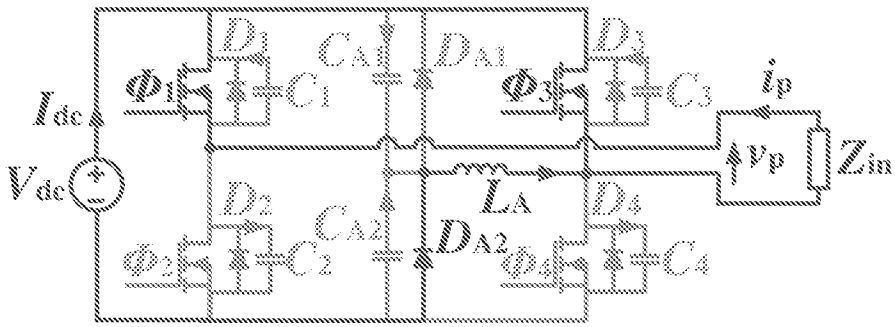


(j) TS4 ($t_{10} \leq t < t_{11}$)

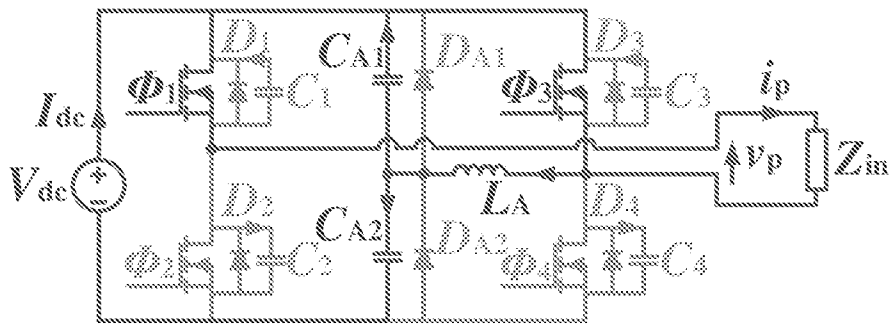
Fig. 7 (cont'd)



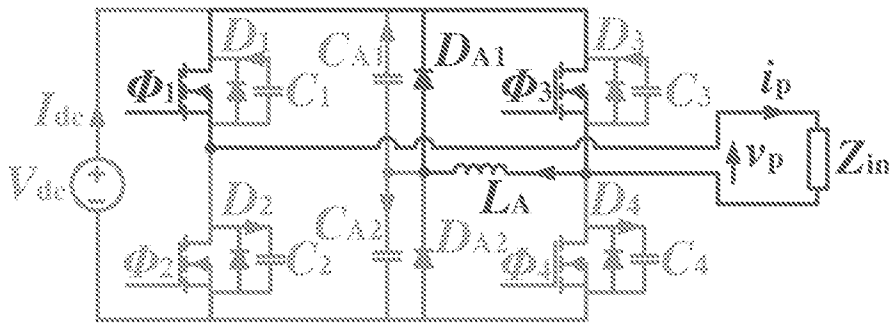
(k) SS7 ($t_{11} \leq t < t_{12}$)



(l1) SS8 ($t_{12} \leq t < t_{13}$)

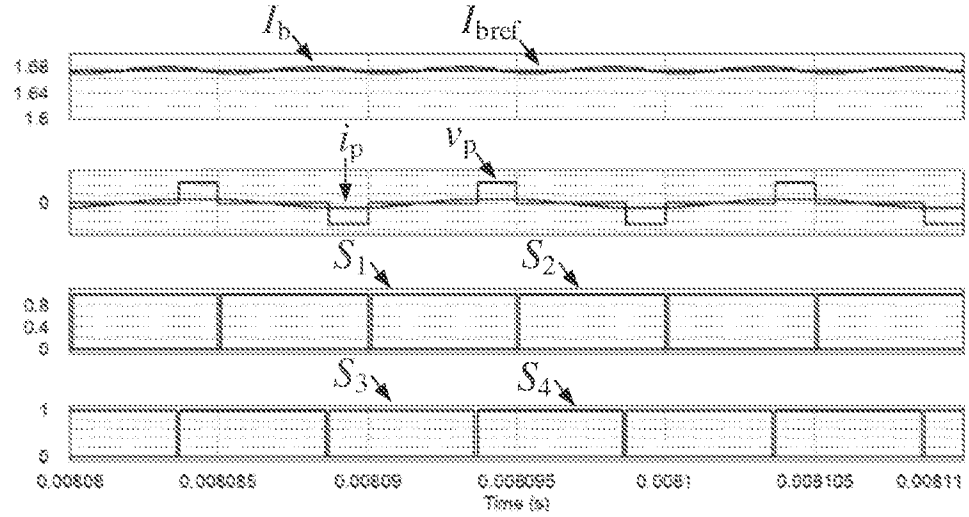


(l2) SS8 ($t_{12} \leq t < t_{13}$)

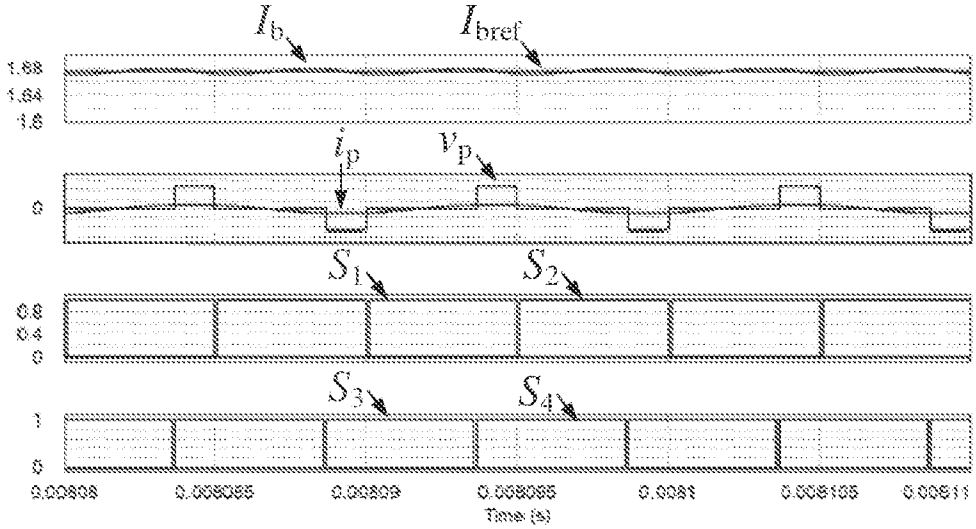


(l3) SS8 ($t_{12} \leq t < t_{13}$)

Fig. 7 (cont'd)


I_b
I_{bref}
1.68
1.64
1.6
i_p
v_p
0
S_1
S_2
0.8
0.4
0
S_3
S_4
1
0
0.00808
0.008085
0.00809
0.008095
0.0081
0.008105
0.00811
Time (s)

(a)


I_b
I_{bref}
1.68
1.64
1.6
i_p
v_p
0
S_1
S_2
0.8
0.4
0
S_3
S_4
1
0
0.00808
0.008085
0.00809
0.008095
0.0081
0.008105
0.00811
Time (s)

(b)

Fig. 8.

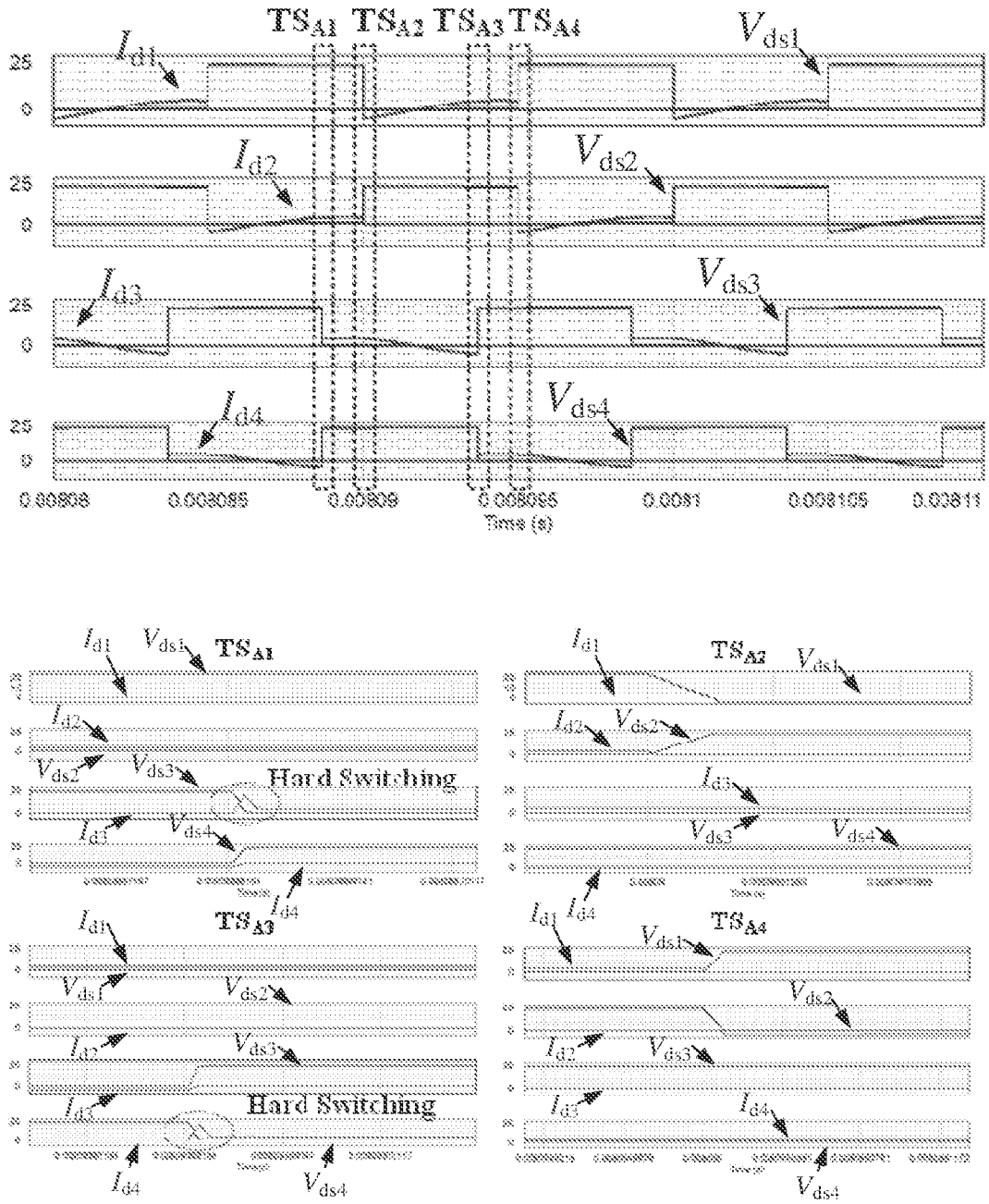

TSA1 TSA2 TSA3 TSA4
Id1
Vds1
Id2
Vds2
Id3
Vds3
Id4
Vds4
25
0
0.00808
0.008085
0.00809
0.008095
0.0081
0.008105
0.00811
Time (s)
TSA1
TSA2
TSA3
TSA4
Hard Switching
Hard Switching

Fig. 9(a)

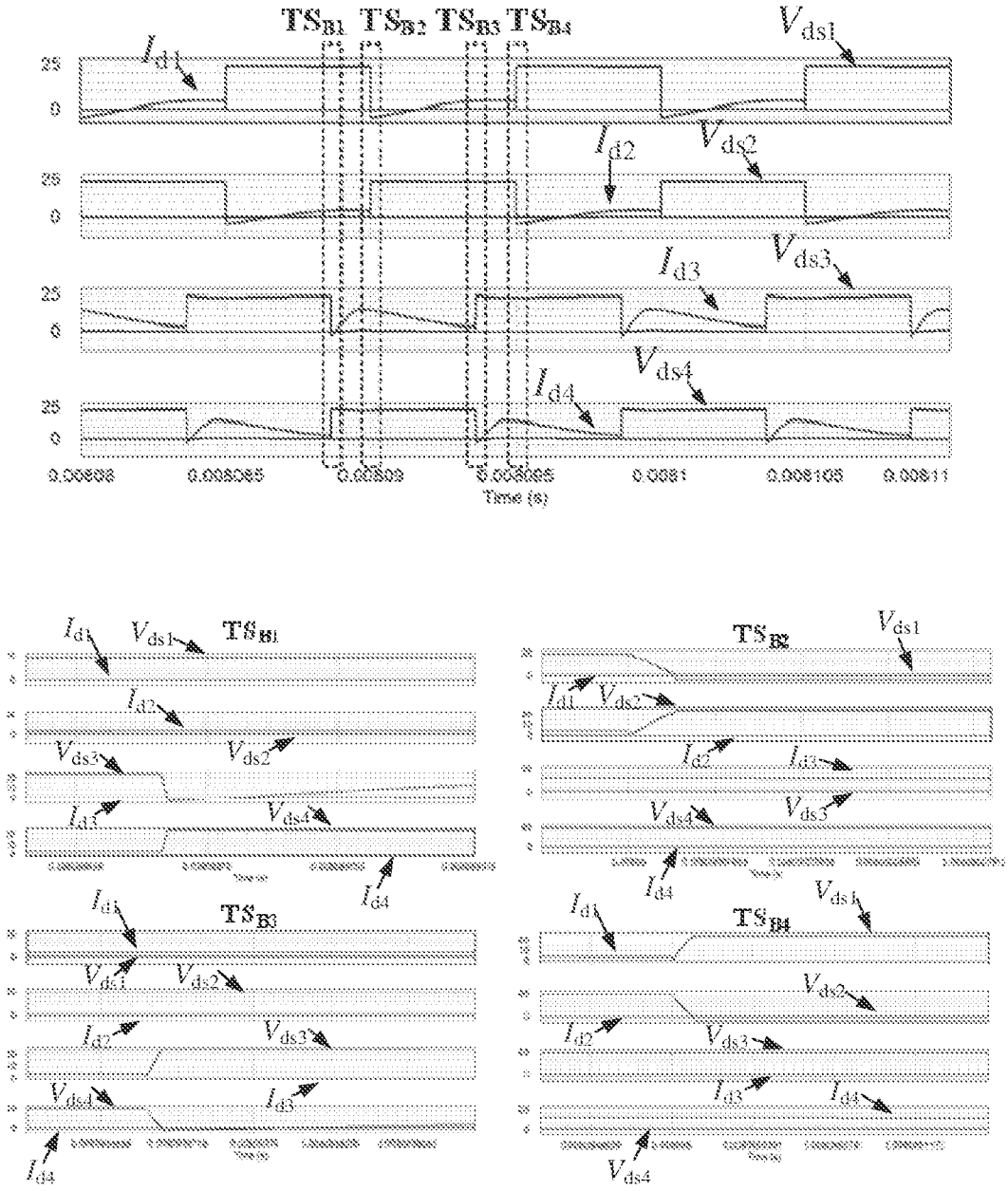

TS_B1
TS_B2
TS_B3
TS_B4
I_d1
V_ds1
I_d2
V_ds2
I_d3
V_ds3
I_d4
V_ds4
25
0
Time (s)

Fig. 9(b)

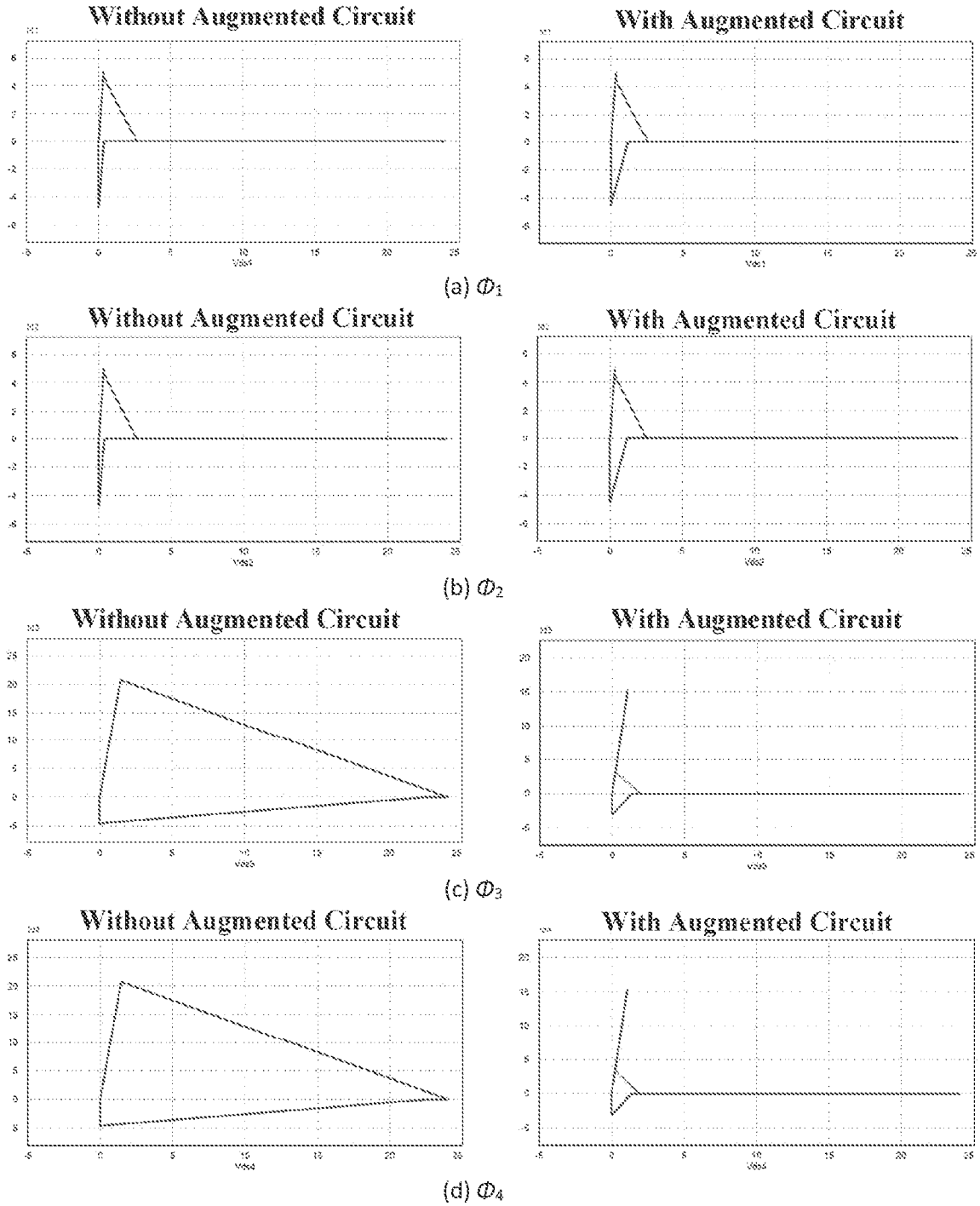
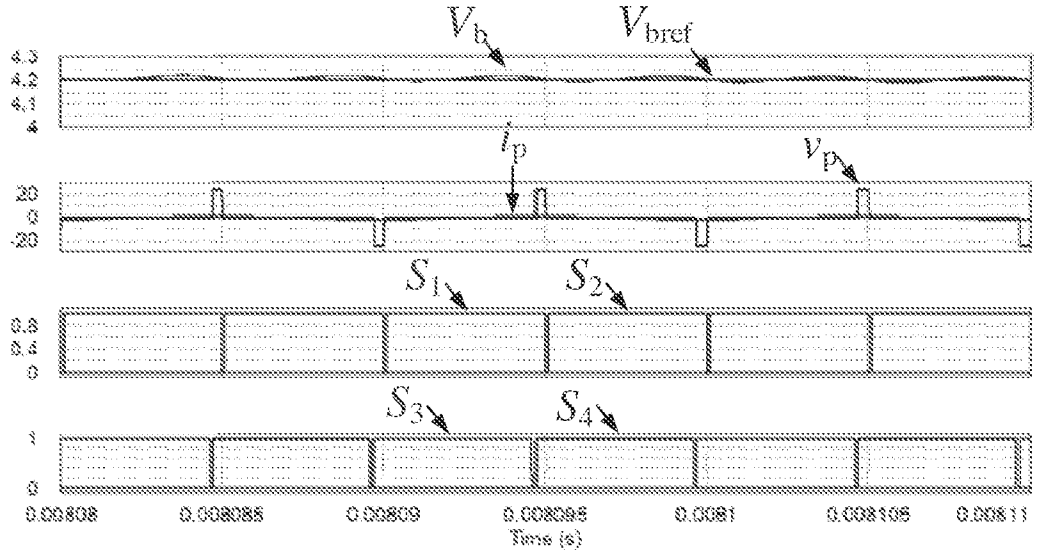
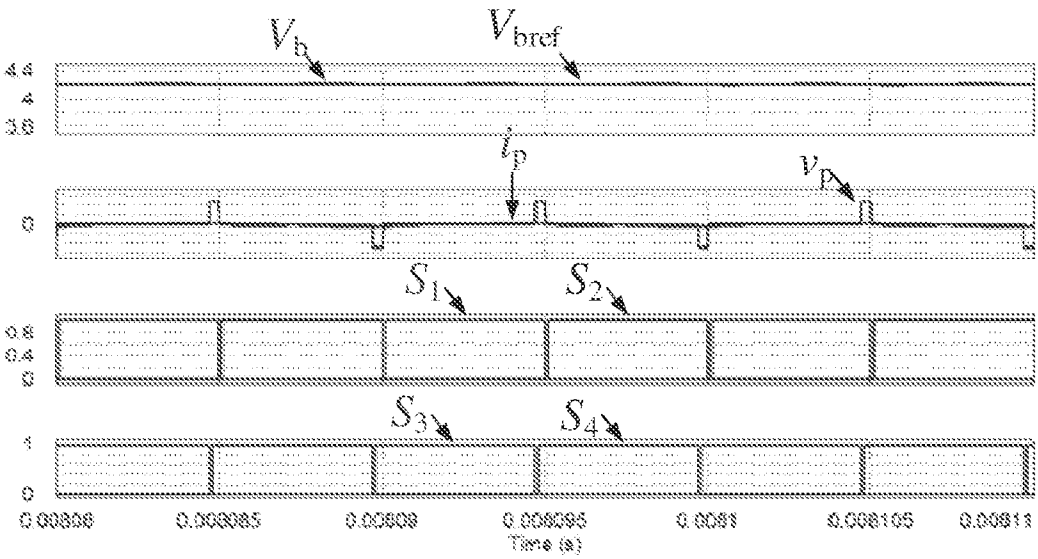

Without Augmented Circuit
With Augmented Circuit
(a) Φ_1
Without Augmented Circuit
With Augmented Circuit
(b) Φ_2
Without Augmented Circuit
With Augmented Circuit
(c) Φ_3
Without Augmented Circuit
With Augmented Circuit
(d) Φ_4

Fig. 10

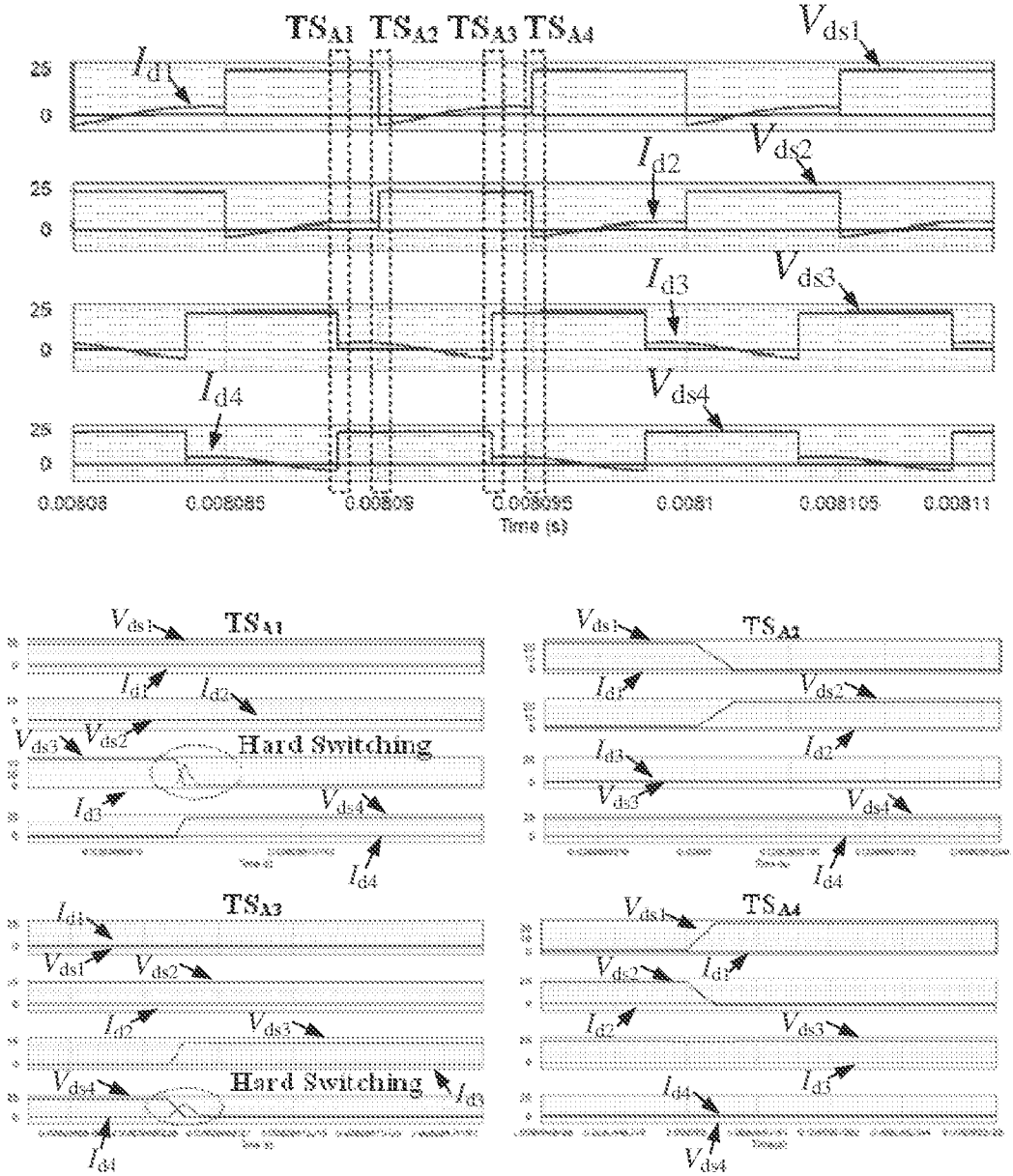

V_b
V_{bref}
4.3
4.2
4.1
4
i_p
v_p
20
0
-20
S_1
S_2
0.8
0.4
0
S_3
S_4
1
0
0.008085
0.00809
0.008095
0.0081
0.008105
0.00811
Time (s)

(a)


V_b
V_{bref}
4.4
4
3.6
i_p
v_p
0
S_1
S_2
0.8
0.4
0
S_3
S_4
1
0
0.008085
0.00809
0.008095
0.0081
0.008105
0.00811
Time (s)

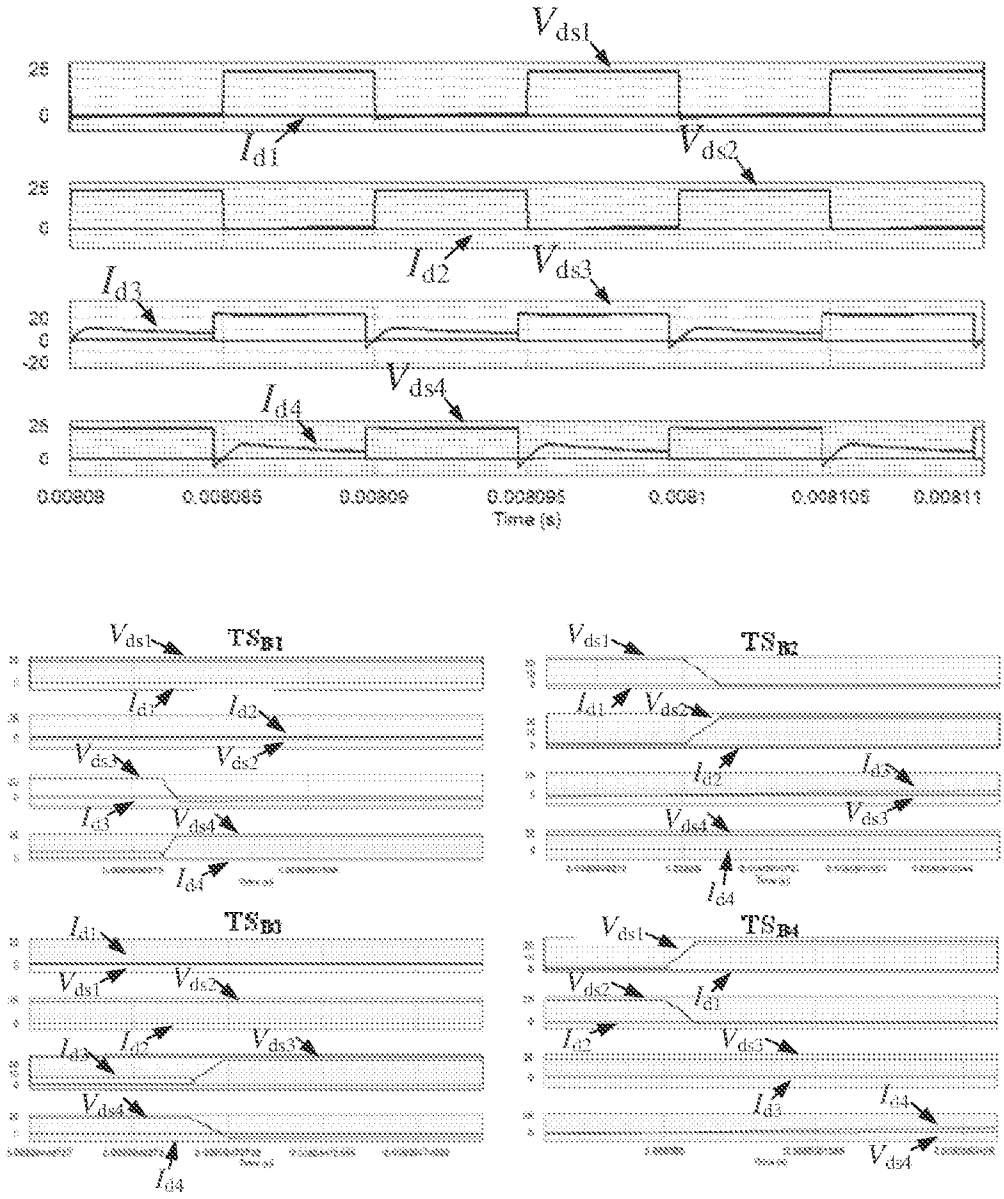
(b)

Fig. 11.


TSA1 TSA2 TSA3 TSA4
Vds1
Id1
Vds2
Id2
Vds3
Id3
Vds4
Id4
25
0
0.008088
0.008285
0.00829
0.008295
0.0081
0.008165
0.00811
Time (s)
TSA1
Hard Switching
TSA2
TSA3
Hard Switching
TSA4

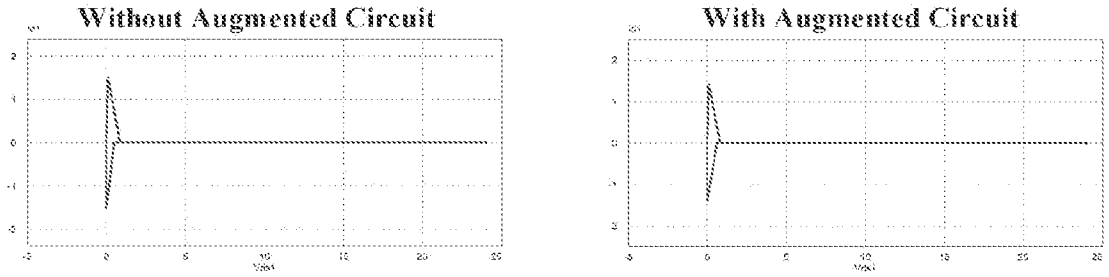
(a)

Fig. 12

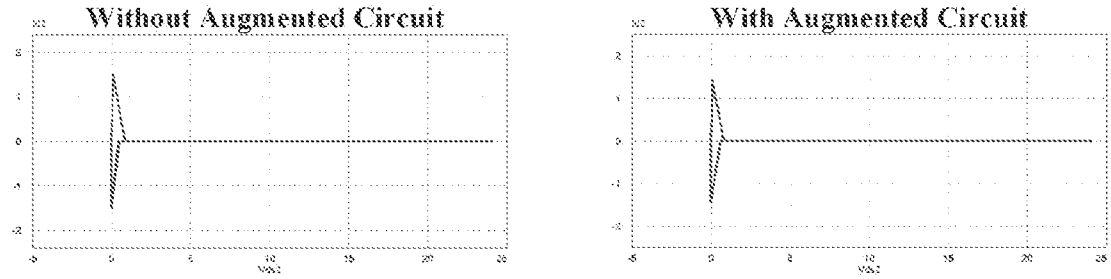


(b)

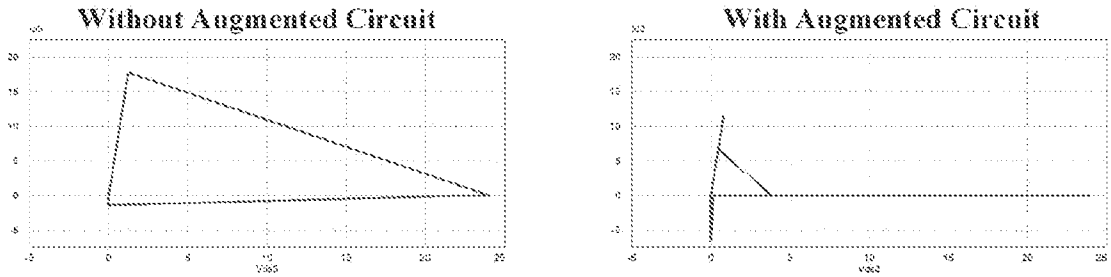
Fig. 12. (cont'd)



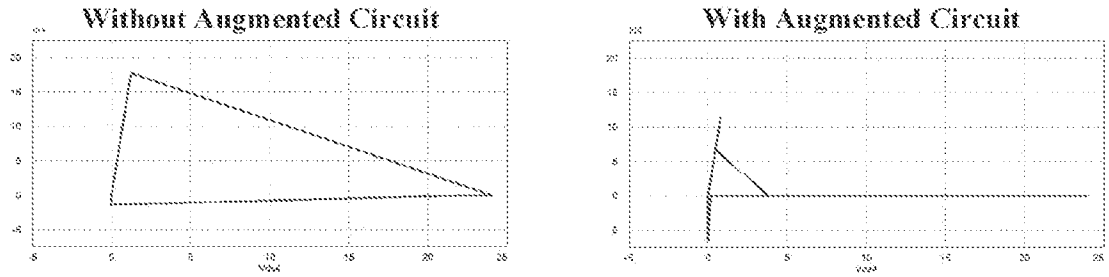
(a) Φ_1



(b) Φ_2

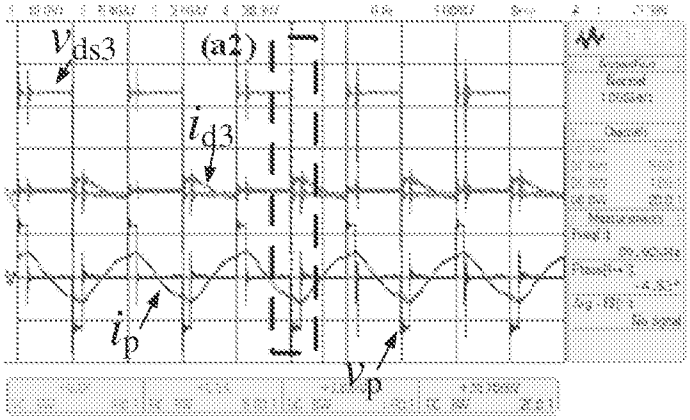


(c) Φ_3

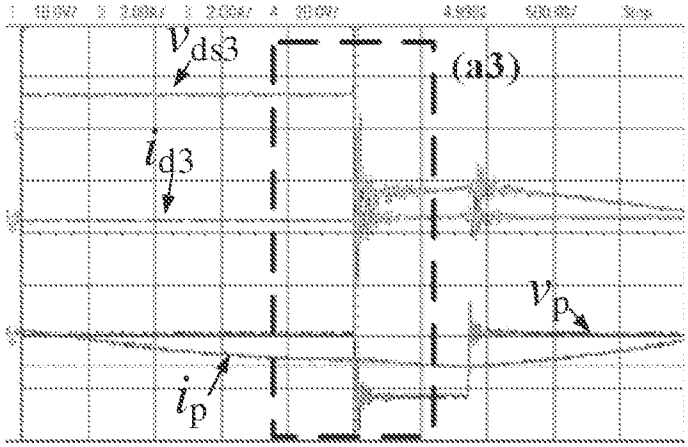


(d) Φ_4

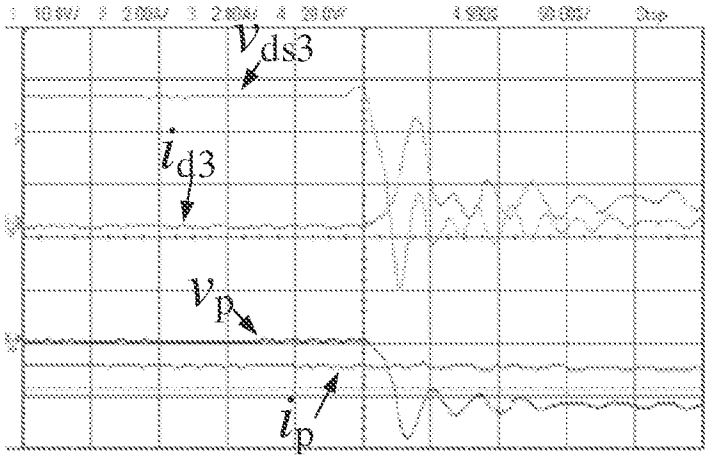
Fig. 13



(a1)

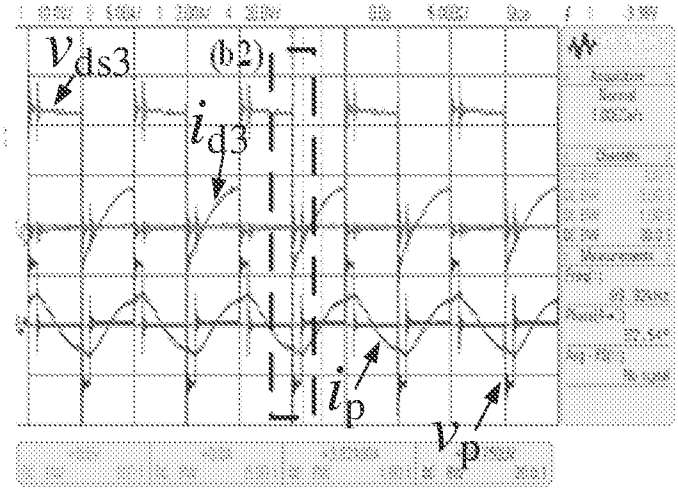


(a2)

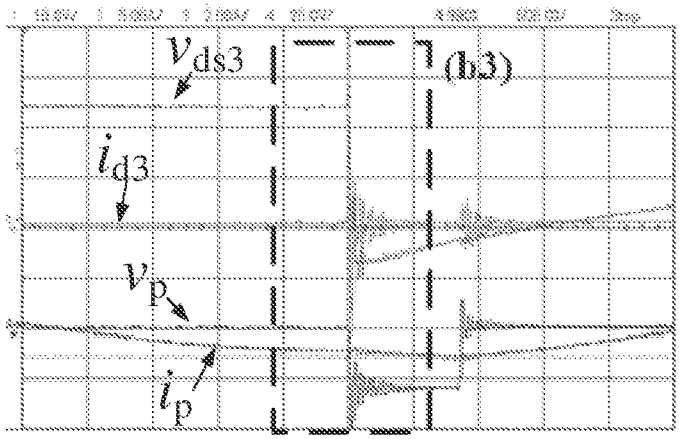


(a3)

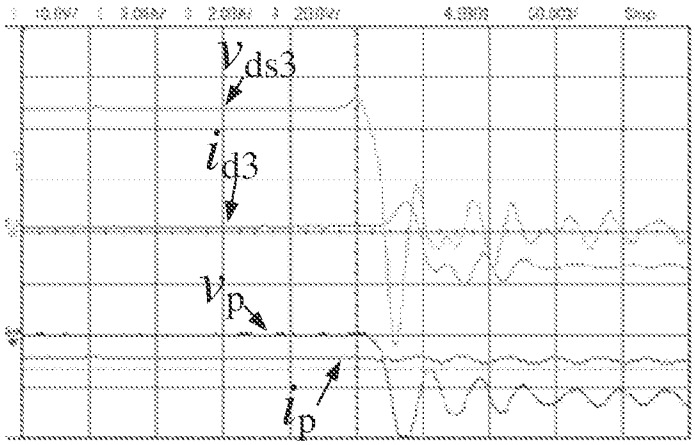
Fig. 14



(b1)

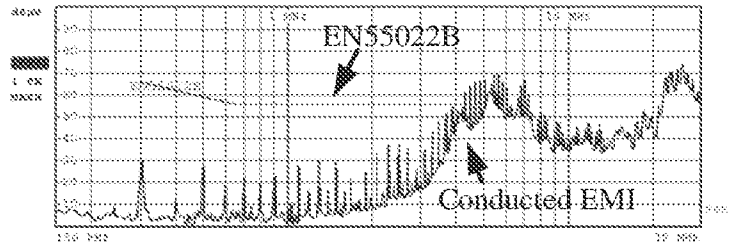


(b2)

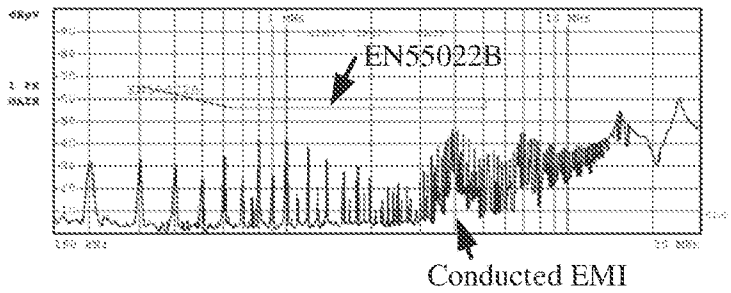


(b3)

Fig. 14 (cont'd)

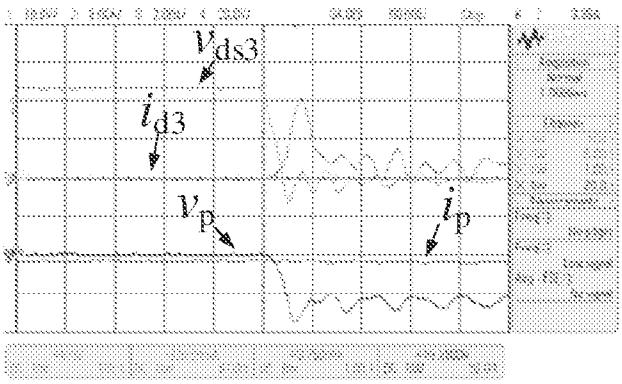


(a)

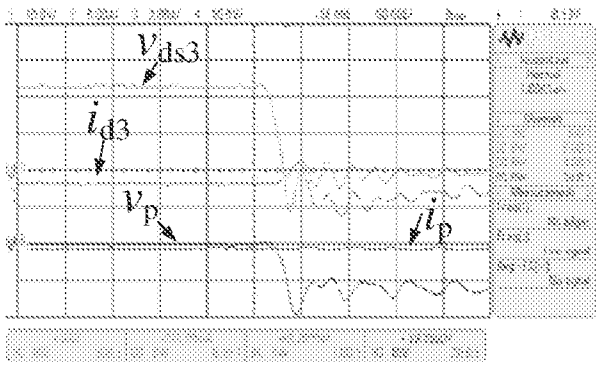


(b)

Fig. 15

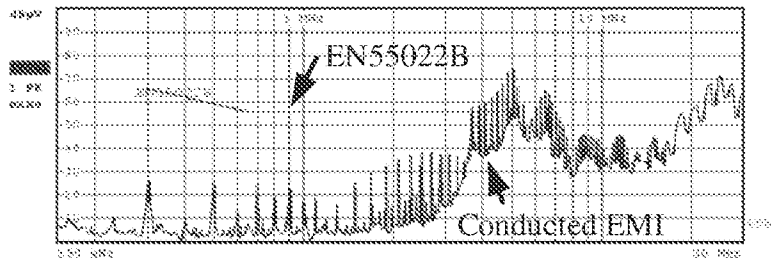


(a)

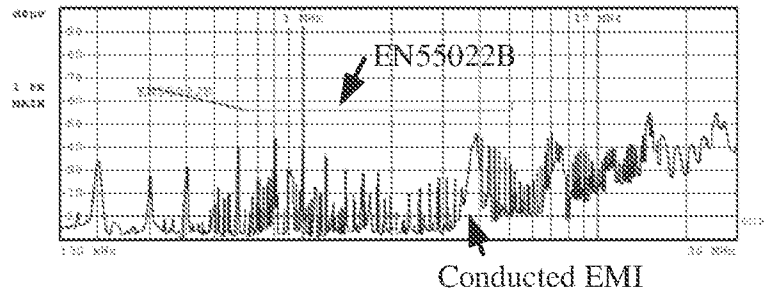


(b)

Fig. 16

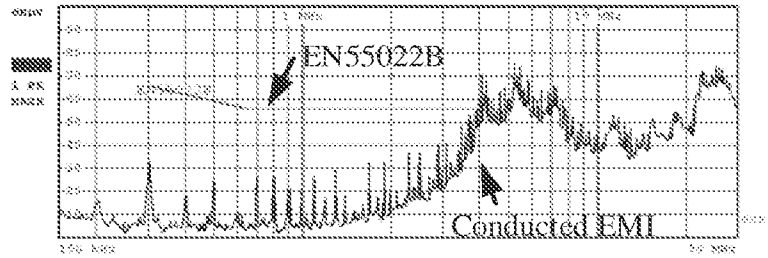


(a)

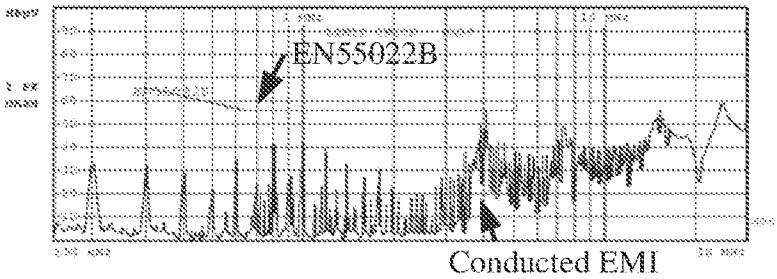


(b)

Fig. 17

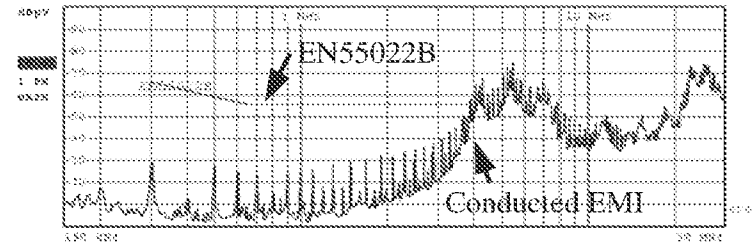


(a) α=120°, without augmented circuit

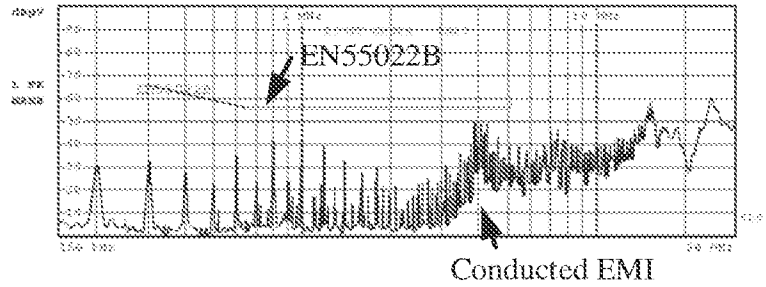


(b) α=120°, with augmented circuit

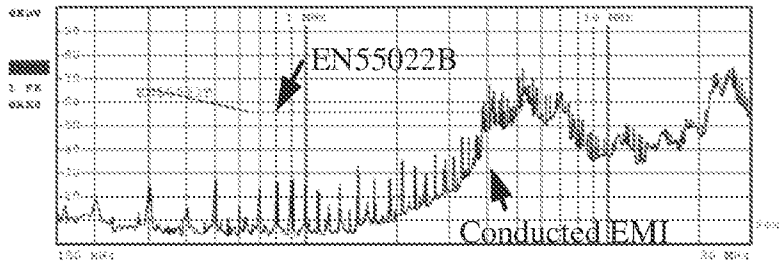
Fig. 18



(c) α=90°, without augmented circuit

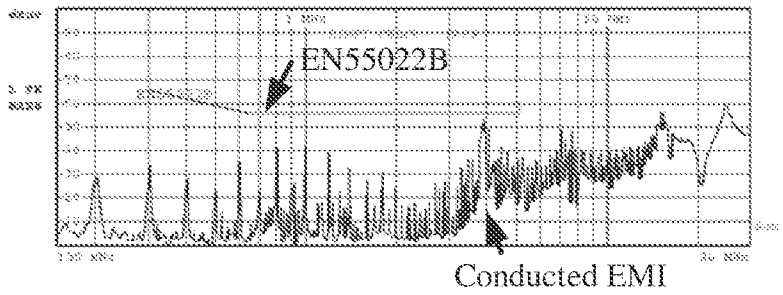


(d) α=90°, with augmented circuit



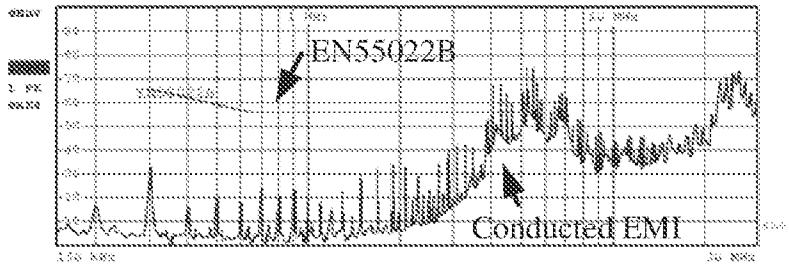
(e) α=60°, without augmented circuit

4

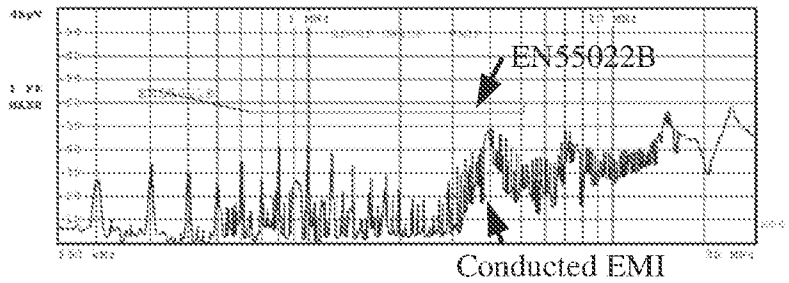


(f) α=60°, with augmented circuit

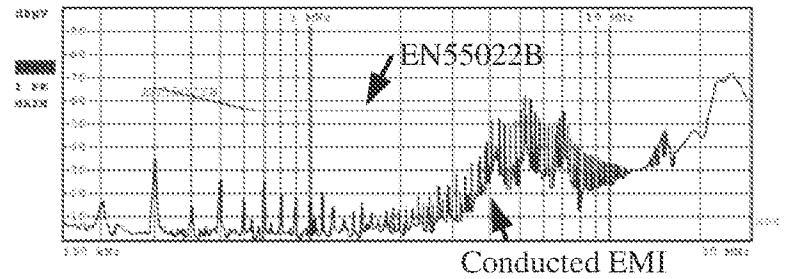
Fig. 18 (cont'd)



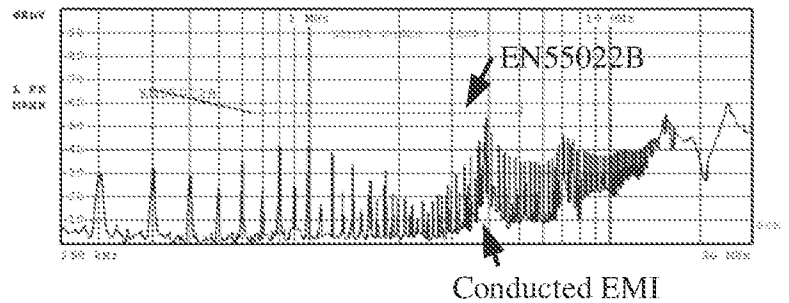
(g) α=30°, without augmented circuit



(h) α=30°, with augmented circuit

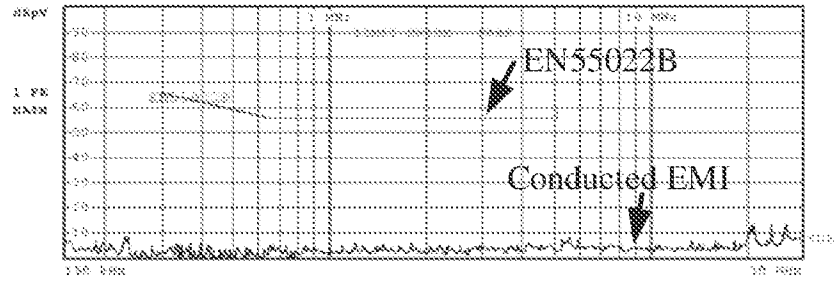


(i) α=0°, without augmented circuit

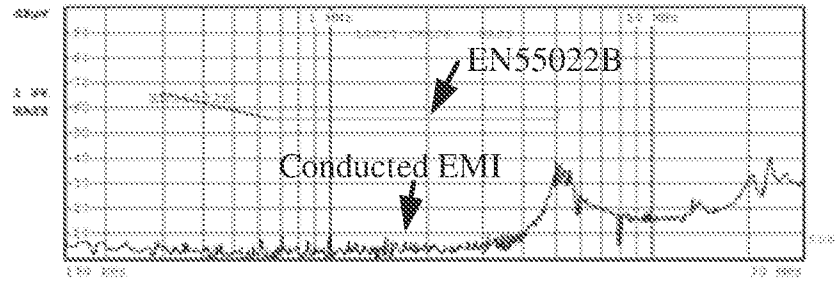


(j) α=0°, with augmented circuit

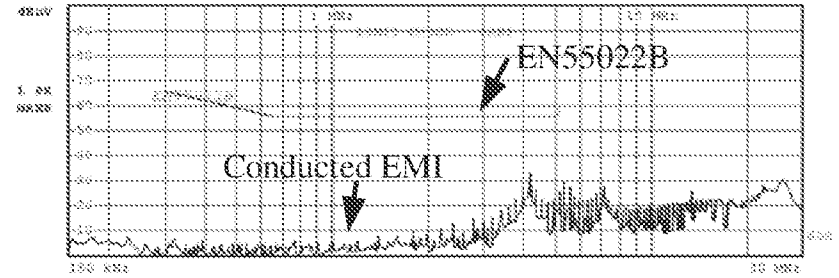
Fig. 18 (cont'd)



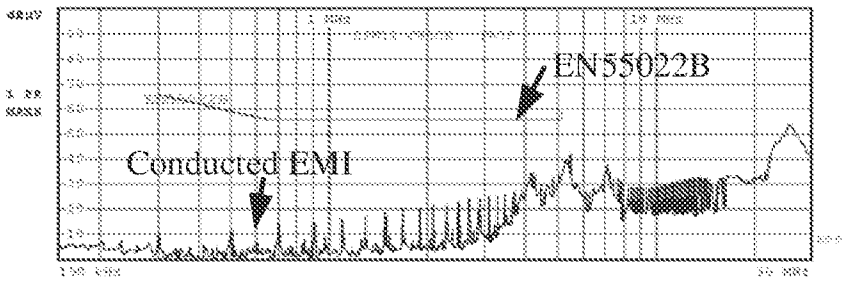
(a) without power supplies for both auxiliary circuits and DSP



(b) with power supplies for auxiliary circuits only

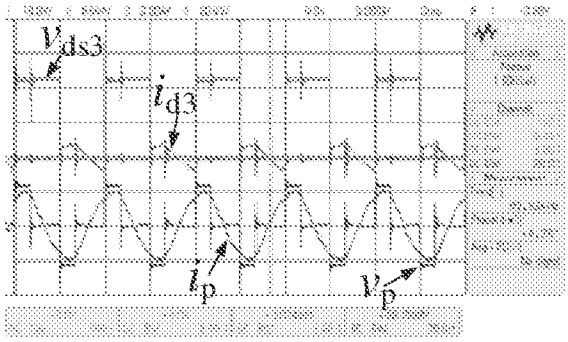


(c) with power supplies for DSP only

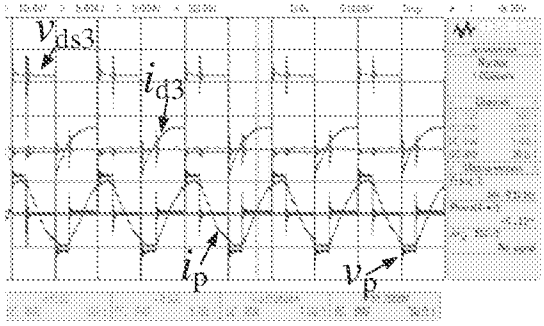


(d) with power supplies for both auxiliary circuits and DSP

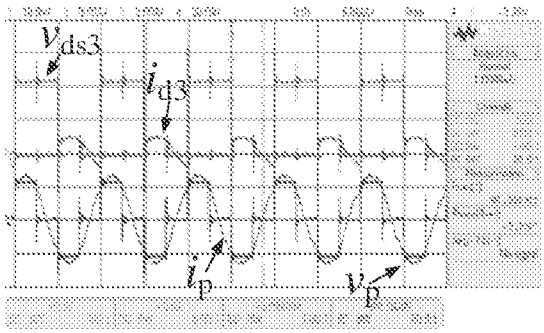
Fig. 19



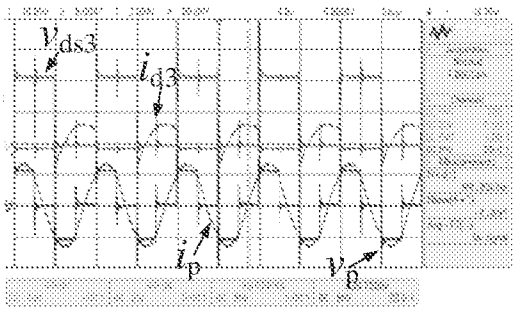
(a) α=120°, without augmented circuit



(b) α=120°, with augmented circuit

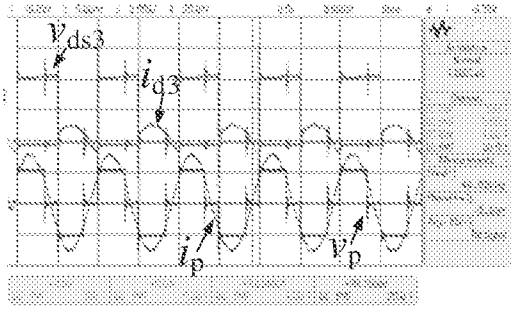


(c) α=90°, without augmented circuit

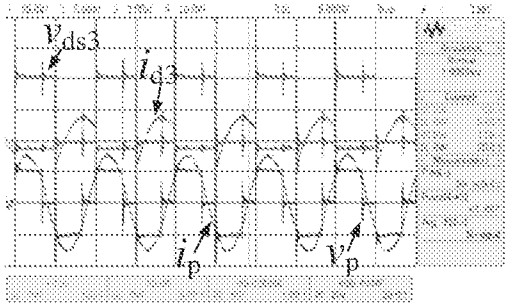


(d) α=90°, with augmented circuit

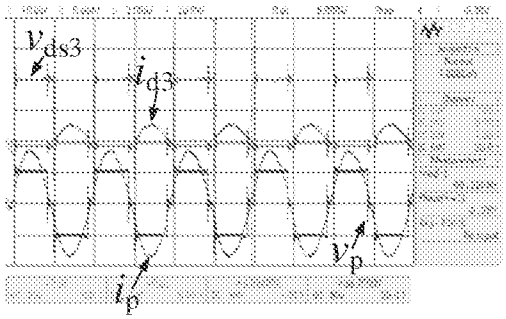
Fig. 20



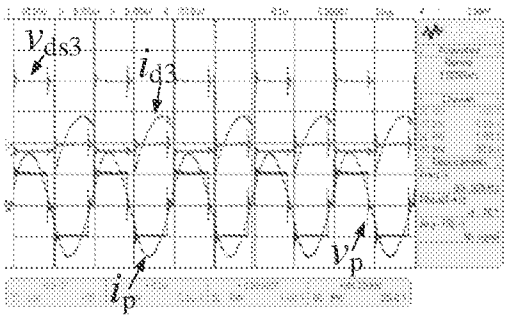
(e) α=60°, without augmented circuit



(f) α=60°, with augmented circuit

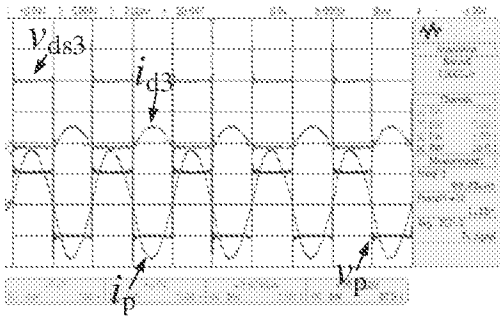


(g) α=30°, without augmented circuit

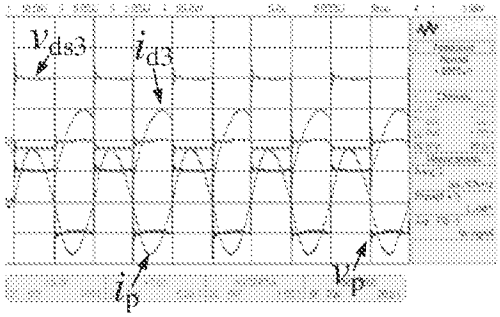


(h) α=30°, with augmented circuit

Fig. 20 (cont'd)



(i) α=0°, without augmented circuit



(j) α=0°, with augmented circuit

Fig. 20 (cont'd)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2023/050248

A. CLASSIFICATION OF SUBJECT MATTER

H02M 1/00 (2007.01) ***H02M 7/5387 (2007.01)*** ***H02J 50/00 (2016.01)***

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M, H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Fampat: phase shift, modulated, full bridge, inverter, augmented, boost, passive, inductor, capacitor, diode, series, wireless, transfer, charging, 相移, 调制, 全桥, 逆变, 增强, 无源, 电感, 电容, 二极管, 串联, 无线, 传输 and other related terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 106452080 A (INST ELECTRICAL ENG CAS) 22 February 2017 Para. [0004]-[0006], [0017], [0019], [0021]-[0024], [0027] and [0029], fig. 1 of the original non-English language document (a machine translation is enclosed **only** for your reference)	1-9
A	CN 108054947 A (UNIV TSINGHUA) 18 May 2018 Whole document of the original non-English language document (a machine translation is enclosed **only** for your reference)	
A	CN 109039091 A (UNIV SHANGHAI JIAOTONG) 18 December 2018 Whole document of the original non-English language document (a machine translation is enclosed **only** for your reference)	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

*Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26/09/2023 *(day/month/year)*	28/09/2023 *(day/month/year)*

Name and mailing address of the ISA/SG

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2023/050248

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:

   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:

   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:

   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please refer to Supplemental Box (Continuation of Box No. III).

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2023/050248

Supplemental Box
(Continuation of Box No. III)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I (claims 1-3 and 5-7): A phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the power inverter comprising: a leading bridge leg comprising: a first power switch, the first power switch having a first power switch parasitic capacitance; and a second power switch, the second power switch having a second power switch parasitic capacitance; a lagging bridge leg comprising: a third power switch, the third power switch having a third power switch parasitic capacitance; and a fourth power switch, the fourth power switch having a fourth power switch parasitic capacitance; wherein the power inverter is configured for each of the power switches to be switched on and off in a switching cycle; and wherein the power inverter further comprises: an augmented passive circuit comprising an inductor, wherein the power inverter is configured for the inductor to combine with the third power switch parasitic capacitance and the fourth power switch capacitance to form a resonator when a first one of the third and fourth power switches is switched off and a second one of the third and fourth power switches is in a switched off state, and for energy stored in the parasitic capacitance of the second one of the third and fourth power switches to be discharged before the second one of the third and fourth power switches is switched on, and corresponding operating method.

Group II (claims 4 and 8-9): A phase-shift modulated full-bridge power inverter configured for use in a wireless power transfer system, the power inverter comprising: a leading bridge leg; a lagging bridge leg; a first output terminal connected from a leading bridge leg connection point in the leading bridge leg; a second output terminal connected from a lagging bridge leg connection point in the lagging bridge leg; and an augmented passive circuit comprising: a capacitor circuit branch, the capacitor circuit branch comprising a first capacitor and a second capacitor connected in series with one another at a capacitor branch connection point, the capacitor circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg; a diode circuit branch, the diode circuit branch comprising a first diode and a second diode connected in series with one another at a diode branch connection point, the diode circuit branch being connected in parallel to the leading bridge leg and the lagging bridge leg; and an inductor connected at a first inductor terminal to the capacitor branch connection point and the diode branch connection point and connected at a second inductor terminal to one of the first and second output terminals, and corresponding fitting method and kit.

Please refer to **Box No. IV** of Written Opinion of The International Searching Authority (Form PCT/ISA/237) for detailed explanation.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2023/050248

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN 106452080 A	22/02/2017	NONE	
CN 108054947 A	18/05/2018	NONE	
CN 109039091 A	18/12/2018	NONE	