

June 23, 1959

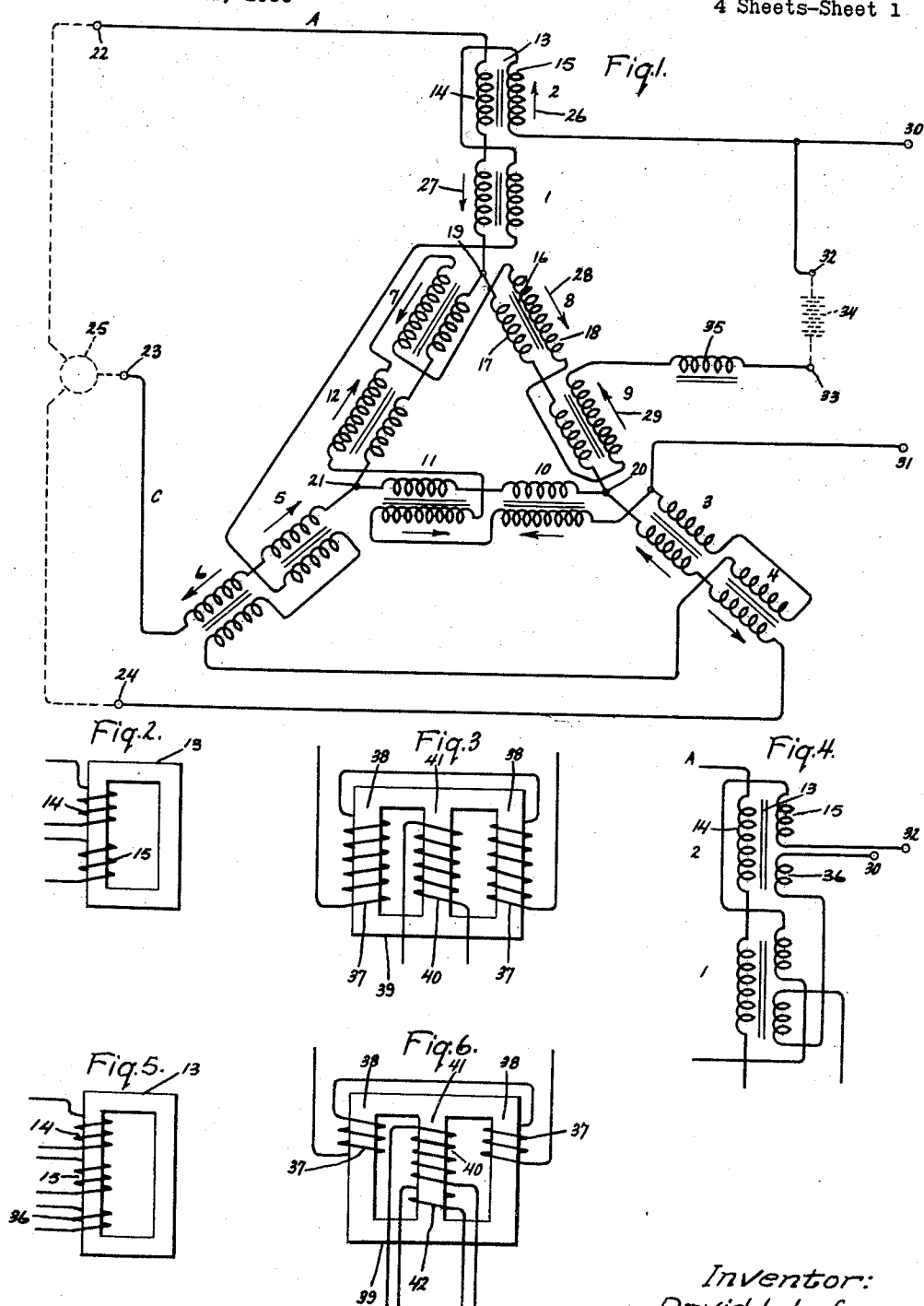
D. L. LA FUZE

2,892,141

FREQUENCY MULTIPLIER

Filed Nov. 27, 1956

4 Sheets-Sheet 1



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4 Sheets-Sheet 2

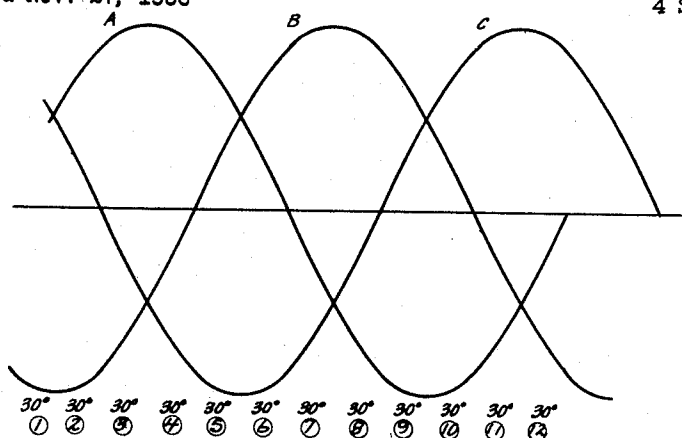


Fig. 7.

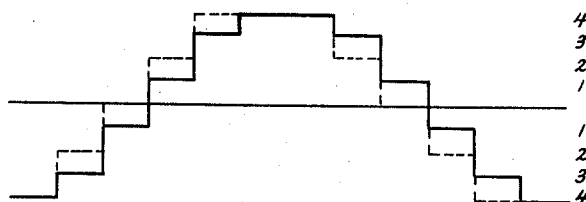


Fig. 8.

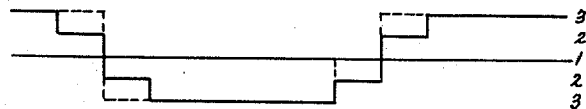


Fig. 9.

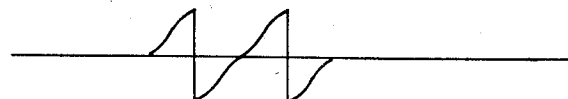
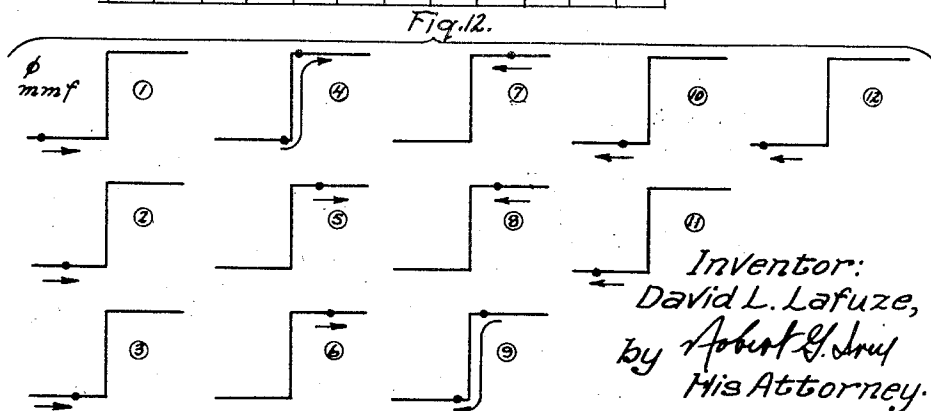


Fig. 10.

OUTPUT REACTOR	4	3	1	2	6	5	3	4	2	1	5	6
OUTPUT VOLTAGE	CB	BA	AB	CA	AC	CB	BC	AB	BA	AC	CA	BC
CURRENT LIMIT REACTOR	7,8	7,10	7,10	9,10	9,10	9,12	9,12	11,12	11,12	8,11	8,11	7,8
LOAD LIMIT REACTOR	3,10	1	2,9	6	5,12	3	4,11	2	1,8	5	6,7	4

Fig. 11.



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Fig. 13.

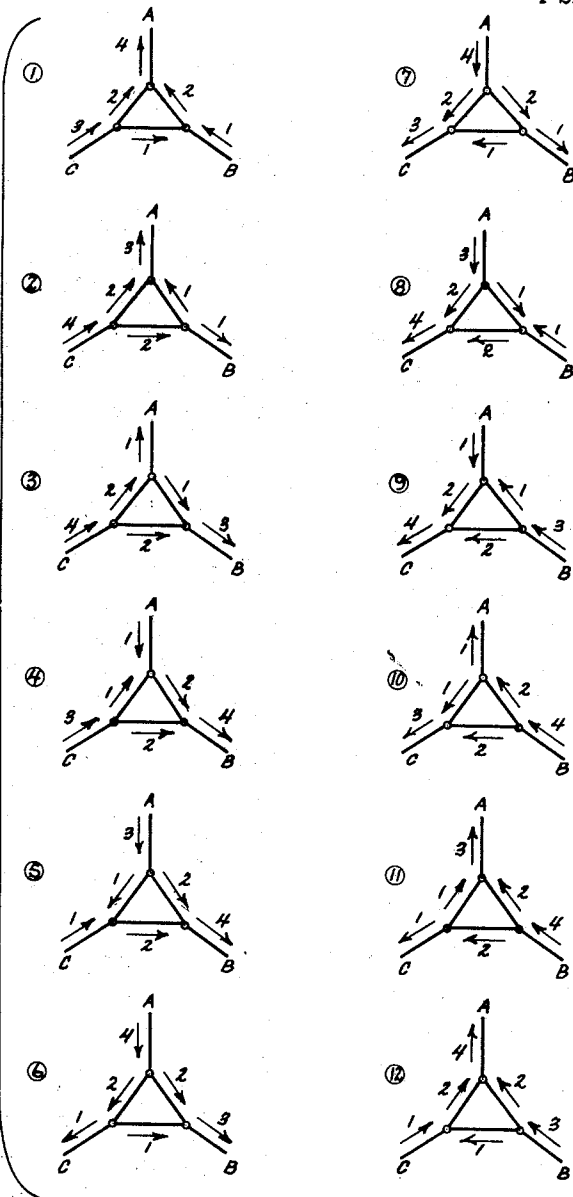


Fig. 14.

①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫
4		1		6		3		2		5	
	3		2		5		4		1		6

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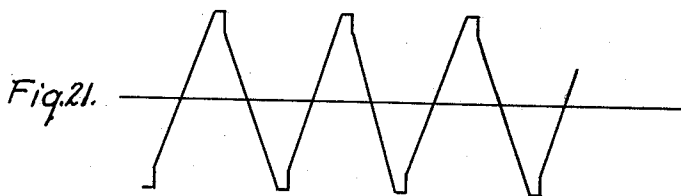
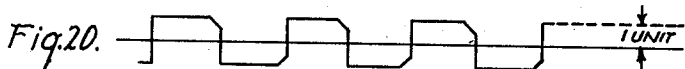
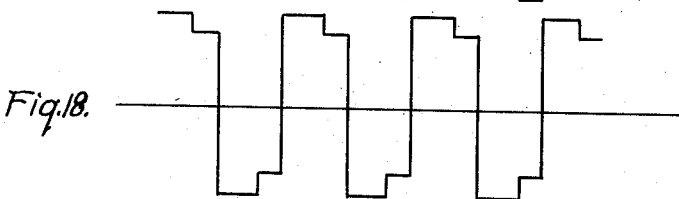
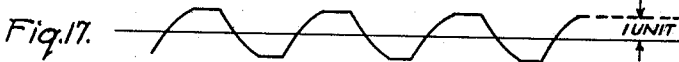
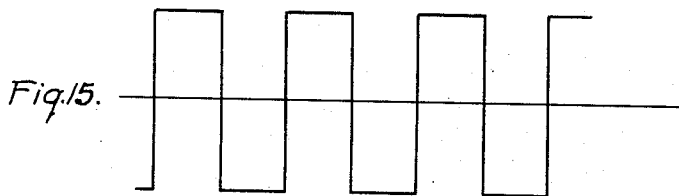
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4 Sheets-Sheet 4



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FREQUENCY MULTIPLIER

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Application November 27, 1956, Serial No. 624,532

13 Claims. (Cl. 321-7)

This invention relates to frequency multipliers and more particularly to static magnetic devices for converting three phase alternating current having a given frequency into single phase alternating current having a frequency six times the input frequency.

There are numerous instances where it has been found desirable to operate alternating current electrical apparatus from a power source having a frequency considerably higher than the frequency commonly provided by utilities, i.e., 60 cycles in the United States. It has been found, for example, that operation of fluorescent lamps at frequencies above 300 cycles permits the use of small and inexpensive capacitors as the ballast impedance for each lamp and that the lamps produce higher lumens per watt than they produce when operated at 60 cycles. These capacitive ballasts operating in higher frequency circuits do not produce the distorted lamp current wave form and high crest factor found in capacitive ballasted circuits operated at 60 cycles, which fact together with the high lumen output per watt is presumably attributable to the fact that at these higher frequencies the lamps stay ionized throughout a complete cycle, rather than going out each half-cycle thus necessitating restriking of the arc as in the case of operation at 60 cycles.

Alternating current at frequencies considerably above 60 cycles is also desirable for operation of other electrical apparatus such as magnetic amplifiers and motors as evidenced by the fact that virtually all alternating current aircraft electrical equipment is operated at 400 cycles, operation at the higher frequency permitting considerably reduced size and weight of the electrical components involved.

Alternating current power at higher frequencies has in the past conventionally been provided by rotating equipment, i.e., motor-generator sets. All rotating equipment, however, inherently requires maintenance and it is therefore desirable to provide static equipment for increasing the frequency of an alternating current source of power. Static frequency multipliers have been designed in the past, however, these multipliers generally required more than one stage to reach the desired output frequency and further did not provide particularly good overall utilization of the electrical components of the equipment.

Since the sixth harmonic of 60 cycles, i.e., 360 cycles is suitable for high frequency operation of fluorescent lamps and other equipment, such as magnetic amplifiers and motors, it is further desirable to provide a static single stage frequency multiplier for providing a 360 cycle output from a 60 cycle input.

It is therefore an object of this invention to provide an improved static single stage frequency multiplier for converting three phase alternating current having a given frequency into single phase alternating current having a frequency six times the original frequency.

Further objects and advantages of this invention will become apparent by reference to the following description and the accompanying drawings, and the features of novelty which characterize this invention will be

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pointed out with particularity in the claims annexed to and forming a part of this specification.

This invention in its broader aspects, provides three frequency doubling saturable core reactor circuits which are used to derive the output voltage at the multiplied frequency from a three phase alternating current source. Each frequency doubling reactor circuit is connected in the circuit with a different phase conductor of the three phase supply. In order to limit the current which would otherwise flow in excess amount between certain phase conductors of the supply circuit during certain intervals of operation of the frequency doubler reactor circuits, I provide three current limiting saturable core reactor circuits. These later circuits are connected in three phase delta relationship and the junction points of the delta are respectively connected to the terminals of the frequency doubling reactor circuits. Thus, the general arrangement of the network constitutes a form of Y-connection to the three phase supply circuit with a frequency doubling reactor circuit in each branch of the Y-connection and terminating in an internal neutral connection network constituted by the delta-connected current limiting reactor circuits.

Each frequency doubling circuit of this invention contains two reactor elements having core means with sharply saturating characteristics, the two reactor elements being respectively biased in opposite directions. Fundamentally, the frequency doubling circuits depend for their operation upon reversal of flux in the core of a reactor element from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of applied voltage, each such reversal inducing a half cycle of alternating current output voltage. Each interval of the twelve 30 degree intervals in a complete cycle of applied voltage thus produces a reversal of flux and a half cycle of output voltage in one frequency doubling reactor element. The individual half cycles of output voltage are then sequentially combined to produce a single phase alternating current output voltage having six times the frequency of the three phase applied voltage.

In accordance with one embodiment of the invention, each frequency doubling circuit contains two saturable core reactors, each having two windings, an alternating current winding connected in a leg of the Y-input circuit and a direct current saturating winding which also serves as an output winding. Similarly, each current limiting saturable core reactor circuit contains two saturable core reactors each having two windings, an alternating current winding connected in a leg of the delta connection and a direct current saturating winding. All of the direct current saturating windings are serially connected across a source of bias voltage with the saturating windings of each pair of frequency doubling and current limiting reactors being connected normally to saturate their associated cores in opposite directions. The direct current saturating windings of the frequency doubling or output reactors are further serially connected across the output circuit thereby providing the sequential combination of half cycles of output voltage referred to above.

In the drawings,

Fig. 1 is a schematic illustration of the preferred embodiment of this invention;

Fig. 2 is a schematic diagram of the core and coil arrangement of the reactors of the embodiment of Fig. 1;

Fig. 3 is a schematic diagram of an alternative core and coil arrangement;

Fig. 4 is a fragmentary schematic illustration showing one pair of output reactors of a modification of this invention;

Fig. 5 is a schematic diagram of the core and coil arrangement of the output reactors of Fig. 4;

Fig. 6 is a schematic diagram of an alternative core and coil arrangement for the reactors of Fig. 4;

Fig. 7 shows the phase relationships of the voltage waves impressed upon the input terminals of the circuit of Fig. 1;

Fig. 8 shows the magnitude and polarity of the phase current flowing in the output reactors of phase A of Fig. 1 during one complete cycle of impressed voltage;

Fig. 9 shows the magnitude and polarity of current flowing in the alternating current winding of one of the current limiting reactors during complete cycle of impressed voltage;

Fig. 10 shows the wave form of the voltage appearing across one of the current limiting reactors;

Fig. 11 is a chart showing the output reactors, the output voltage, the current limiting reactors, and the load limiting reactors which are effective during each 30 degree interval of impressed voltage in the circuit of Fig. 1;

Fig. 12 shows a series of typical saturation curves for one of the output reactors of Fig. 1 indicating the magnitude and direction of magnetization during each of the 30 degree intervals of Figs. 7 through 11;

Fig. 13 shows a series of schematic diagrams indicating the direction and magnitude of the currents flowing in the alternating current windings of the output and current limiting reactors of the circuit of Fig. 1 during each of the 30 degree intervals of Figs. 7 through 11;

Fig. 14 illustrates the output voltage wave and the output reactor providing such voltage for the circuit of Fig. 1 during each 30 degree interval of Figs. 7 through 11;

Figs. 15 and 16 show the output voltage and current waves respectively with an inductive load;

Figs. 17 and 18 show the output current and voltage waves respectively with an inductive load attempting to draw current exceeding the bias current;

Fig. 19 shows the output current wave with a capacitive load; and

Figs. 20 and 21 show output current and voltage waves respectively with a capacitive load attempting to draw current exceeding the bias current.

The preferred embodiment of this invention incorporates three pairs of output saturable core reactors 1 and 2, 3 and 4, and 5 and 6, each pair of output saturable core reactors constituting a frequency doubler circuit. Each of the output reactors 1 through 6 inclusive is provided with a core 13 with an alternating current winding 14 and a direct current saturating winding 15 thereon.

Three pairs of current limiting saturable core reactors 8 and 9, 10 and 11, and 12 and 7, are also provided, each of the current limiting saturable cores reactors 7 through 12 being provided with a core 16 with an alternating current winding 17 and a direct current saturating winding 18 thereon. The alternating current windings 17 of each pair of current limiting saturable core reactors 8 and 9, 10 and 11, and 12 and 7 are serially connected as shown, and the serially connected pairs are in turn delta-connected at points 19, 20 and 21.

The alternating current windings 14 of each pair of output saturable core reactors 1 and 2, 3 and 4, and 5 and 6 are serially connected as shown and each serially connected pair has one end connected to one of the junction points 19, 20 and 21 of the delta-connection of current limiting saturable core reactor alternating current windings 17. The other ends of the serially connected pairs of alternating current windings 14 of the output reactors 1 through 6 are respectively connected to three input terminals 22, 23 and 24 which in turn are adapted to be connected to an external source of three phase alternating current power, such as three phase generator 25 shown in dashed lines in Fig. 1. The direct current saturating windings 15 of the output reactors 1 through 6 and the direct current saturating windings 18 of the current limiting reactors 7 through 12 are serially connected with the direct current saturating windings 15 of

each pair of output reactors being connected normally to saturate their associated reactors in opposite directions and each of the direct current saturating windings 18 of the current limiting reactors being similarly connected normally to saturate their associated cores in opposite directions. Thus, direct current saturating windings 15 of output reactors 1 and 2 are connected to saturate their associated cores 13 in opposite directions as shown by arrows 26 and 27 and direct current saturating windings 13 of current limiting reactors 8 and 9 are likewise connected to saturate their associated cores 16 in opposite directions, as shown by arrows 28 and 29. The reversed direction of the direct current bias of each of the remaining pairs of output reactors and in each of the remaining current limiting reactors is similarly shown by arrows.

The serially connected direct current windings 15 of output reactors 1 through 6 are connected across output terminals 30 and 31 which are in turn adapted to be connected to the load desired to be operated by the circuit of Fig. 1, these output terminals delivering single phase alternating current having a frequency six times that of the frequency of the three phase alternating current applied to input terminals 22, 23 and 24, i.e., 360 cycles when three phase generator 25 is delivering 60 cycles. All of the serially connected direct current saturating windings 15 and 18 are serially connected across bias voltage terminals 32 and 33 to which a source of direct current bias voltage may be connected, such as battery 34 shown in dashed lines on Fig. 1. A reactor 35 is preferably connected in series with the direct current saturating windings 15 and 18 in order to suppress ripple in the direct current bias voltage supply circuit.

The output reactors 1 through 6 are of the sharply saturated type and have their cores 13 designed so that they can be driven from saturation aiding the direct current bias to saturation opposing the direct current bias in sequence, each in 30 degrees of one cycle of impressed voltage. The output reactors 1 through 6 can have equal turns on their alternating current windings 14 and direct current windings 15 or in the alternative, the alternating current and direct windings can have unequal turns; an output voltage higher than the input voltage can be secured by providing a greater number of turns on the direct current windings 15 than are on the alternating current windings 14. In the example, shown in Fig. 1 to be discussed more fully below, however, the alternating current windings 14 and direct current windings 15 of output reactors 1 through 6 are assumed to have substantially equal turns. It will be observed that in each of the pairs of output reactors, both reactors can not be unsaturated at the same time, i.e., if the reactor 1 becomes unsaturated, the reactor 2 by virtue of its reversed bias must be saturated.

The current limiting reactors 7 through 12 inclusive have their direct current saturating windings 18 arranged to provide substantially greater direct current biasing ampere turns than the bias ampere turns provided by direct current saturating windings 15 of the output reactors 1 through 6 and in an example shown in Fig. 1 and to be discussed more fully below, the direct current saturating windings 18 are assumed to have substantially twice the number of turns of the direct current saturating winding 15. As will become more readily apparent hereinafter, the current limiting reactors 7 through 12 can saturate only in the direction of direct current bias.

The output reactors 1 through 6 may be constructed as shown in Fig. 2 utilizing a closed O-shaped magnetic core formed of a plurality of relatively thin laminations of suitable magnetic material and with the alternating current winding 14 and the direct current saturating winding 15 arranged thereon in close coupled relationship, generally wound one over the other. The current limiting reactors 7 through 12 may be similarly constructed.

In order to explain the operation of the circuit of Fig. 1, reference will now be had to Figs. 7 through 14

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in addition to Fig. 1. In this explanation of the operation of the circuit of Fig. 1, the circuit of serially connected alternating current windings 14 of output reactors 1 and 2 connected to input terminal 22 is referred to as phase A, the circuit of the serially connected alternating current windings 14 of output reactors 3 and 4 connected to input terminal 24 is referred to as phase B, and the serially connected alternating current windings 14 of output reactors 5 and 6 connected to output terminal 23 is referred to as phase C. Positive current in each of the phases A, B, and C is defined as current flowing inward toward the center delta-connection of alternating current windings 17 of the current limiting reactors 7 through 12, and the direct current bias current is defined as one unit of current, i.e., a phase current in phase A flowing in alternating current windings 14 of output reactors 1 and 2 of four units is four times the bias current flowing in direct current saturating windings 15 of output reactors 1 and 2. In the circuit described, the output reactors 1 through 6 are designed to pass no more than four units of phase current respectively while the current limiting reactors 7 through 12 are designed to pass no more than two units of alternating current respectively.

If one unit of bias current is flowing in the circuit of the direct current saturating windings, direct current saturating windings 15 of the output reactors 1 through 6 will produce one unit of mmf in their respective cores 13. Considering now output reactors 1 and 2, let it be assumed that the phase A voltage is at a maximum positive, i.e., at the beginning of interval 4 in Fig. 7. At this instant, assuming that no load is connected across output terminals 30 and 31, and since alternating current windings 14 of output reactors 1 and 2 may be assumed to be pure inductance, the current flowing in alternating current windings 14 of output reactors 1 and 2 will be lagging the phase A voltage by 90 degrees and will thus be passing through zero going positive. Thus at this instant since there is no phase current flowing, the cores 13 of output reactors 1 and 2 will both be saturated in opposite directions and thus alternating current windings will therefore have low impedance. The phase A current will thus increase rapidly because of the low impedance in the circuit and being positive, aids the bias in output reactor 1 driving its core 13 further into saturation and opposes the bias in output reactor 2 driving its core 13 in the direction of unsaturation.

When the phase A current flowing in alternating current winding 14 of output reactor 2 reaches one unit, i.e., equal to the bias, core 13 of output reactor 2 will suddenly become unsaturated and its alternating current winding 14 will thus suddenly have high impedance. The phase A current will continue to increase, but now at a much slower rate which is determined by the greatly increased impedance of alternating current winding 14 of output reactor 2.

It will be remembered that the core 13 of output reactors 1 through 6 are of the sharply saturating type and are designed to be driven from saturation aiding the bias to saturation opposing the bias in 30 degrees of one cycle of impressed voltage. Here, at the beginning of interval 4, core 13 of output reactor 2 was saturated aiding the bias. The increase of current in alternating current winding 14 of output reactor 2 after the core 13 has become unsaturated continues until after the core 13 becomes saturated in the opposite direction, i.e., opposing the bias, this reversal of flux in the core 13 occurring in the 30 degrees of interval 4 of Fig. 7. This reversal of flux in core 13 is shown diagrammatically in interval 4 of Fig. 12. Alternating current winding 14 of output reactor 2 now again has low impedance and phase A current again increases rapidly to the value determined by the other reactors in the entire circuit as will be explained hereinafter. The initial rapid increase of phase A current, followed by a slow increase for 30 degrees of impressed voltage, and the subsequent

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rapid increase accounts for the stepped configuration of the diagram of Fig. 8.

Since direct current saturating winding 15 is coupled to alternating current winding 14, the reversal of flux in core 13 of output reactor 2 induces a half cycle of alternating voltage having a squarish wave form in direct current saturating winding 15. It is thus seen that a complete half cycle of output voltage has been produced in 30 degrees of a cycle of applied voltage. With the cores 13 of the output reactors 1 through 6 designed so that the reversal of their saturation respectively takes place during successive 30 degree intervals of a cycle of applied voltage, it will be seen in Fig. 7 that since there are twelve 30 degree intervals in a complete cycle of applied voltage, a reversal of flux in one of the output reactors being accomplished in each interval, the resulting half cycles of output voltage can be sequentially combined to produce a single phase alternating current output voltage across terminals 30 and 31 having six times the frequency of the three phase applied voltage.

The operation of the circuit of Fig. 1 during one complete cycle of applied voltage with no load connected across output terminals 30 and 31 will now be described. With one unit of bias current flowing in the bias circuit, during interval 1 of Fig. 7, four units of negative phase current will be flowing in phase A, as shown in Fig. 8, and one unit of positive phase current will be flowing in phase B, and three units of positive phase current will be flowing in phase C, as further shown in Fig. 13.

The units of phase current flowing in each of the phases B and C during any of the intervals of Figs. 7 and 8 can be determined from Fig. 8, which shows the magnitude and polarity of current flowing in phase A, in the following manner. Considering interval 1 of Fig. 7, in order to determine phase B current, the position of the phase B voltage wave of Fig. 7 during interval 1 is observed and the phase A voltage wave followed to its comparable position, in this case interval 9 at which it will be observed in Fig. 8, that the phase A current is one unit positive. Likewise, the phase C current in interval 1 is determined by observing the position of the phase C voltage wave in interval 1 and then following the phase A voltage wave to a comparable position, in this case interval 5 in which is shown in Fig. 8 the A current is three units positive.

The values and polarity of the phase B and C currents during each of the remaining intervals 2 through 12 are determined by the same manner and are shown diagrammatically in Fig. 13.

It will be recalled that the current limit reactors 7 through 12 inclusive are designed to pass no more than two units of current. Thus, in interval 1, reactors 7 and 12 are passing two units of current from phase C in the direction of phase A while reactors 11 and 10 are passing one unit of current from phase C toward phase B. The one unit of positive current in phase B combines with the one unit of positive current in current limit reactors 11 and 10 so that two units of current flow in current limit reactors 9 and 8 which in turn combine with the two units of current flow in reactors 12 and 7 to produce the four units of negative current flowing in phase A, as shown in interval 1 of Fig. 13.

It will thus be seen that in output reactor 2, four units of phase A current flowing in its alternating current winding 14 produces a corresponding four units of mmf in its core 13 aiding the one unit of mmf produced by the bias current in direct current saturating winding 15 so that core 13 is saturated with five units of mmf, as shown in interval 1 of Fig. 12, which shows the direction and degree of magnetization of output reactor 2 during a complete cycle of applied voltage. The four units of phase A current flowing in alternating current winding 14 of reactor 1 oppose the one unit of bias current so that there is a net mmf in core 13 of output reactor 1 of three units in a direction opposite from the bias which of course, causes core 13 of output reactor 1 to

be saturated since only one unit of mmf is required to saturate the core. It will be observed that cores 13 of output reactors 1 and 2 are both saturated in interval 1 and thus the alternating current windings 14 of output reactors 1 and 2 both have low impedance. The two units of current flowing in alternating current windings 17 of current limiting reactors 7 and 12 oppose the bias in current limiting reactor 7 and aid the bias in current limiting reactor 12. Here it will be recalled that the direct current saturating windings 18 of the current limiting reactors 7 through 12 provide twice the bias mmf provided by the direct current saturating windings of the output reactors 1 through 6 and therefore the one unit of bias current flowing in the direct current saturating windings 18 of current limiting reactors 7 and 12 produces two units of bias mmf in the cores 16 of these reactors. These two units of bias mmf oppose the two units of current flowing in alternating current winding 17 of current limiting reactor 7 so that its core 16 is unsaturated, and aids the two units of current flowing in alternating current winding 17 of current limiting reactor 12 so that its core 16 saturates. Alternating current winding 17 of current limiting reactor 12 is therefore low impedance while alternating current winding 17 of current limiting reactor 7 is high impedance.

The three units of positive current flowing in phase C oppose the one unit of bias in output reactor 6 producing a net mmf of two units which is still sufficient to saturate core 13 of output reactor 6 and aids the one unit of bias in output reactor 5 to produce a total of four units of bias mmf so that the core 13 of output reactor 5 is also saturated and thus alternating current windings 14 of output reactors 5 and 6 both have low impedance in interval 1. It is thus seen that across input terminals 22 and 23, alternating current windings 14 of output reactors 1, 2, 5 and 6 and alternating current winding 17 of current limiting reactor 12 have low impedance while alternating current winding 17 of current limiting reactor 7 has high impedance so that the input voltage impressed across terminals 22 and 23 will appear substantially across alternating current winding 17 of current limiting reactor 7. It will now be readily apparent that the current limiting reactors 7 through 12 are necessary in order to limit the current which would otherwise flow between the A and C phases in the conditions prevailing in interval 1.

The one unit of current flowing in alternating current windings 17 of current limiting reactors 11 and 10 aids the two units of bias mmf provided by the direct current saturating winding 18 of current limiting reactor 11 so that its core 16 is saturated, and opposes the two units of bias mmf in current limiting reactor 10, however, there is still one unit of mmf remaining so that core 16 of current limiting reactor 10 is still saturated and thus alternating current windings 17 of current limiting reactors 10 and 11 both have low impedance.

The one unit of current flowing in the phase B opposes the bias current in output reactor 4 so that its core 15 will be unsaturated and aids the bias current in output reactor 3 so that its core 13 will be saturated and thus it is seen that alternating current winding 14 of output reactor 3 is low impedance while alternating current winding 14 of output reactor 4 is high impedance. It is thus seen that since the cores of output reactors 3, 5, and 6 and current limiting reactors 10 and 11 are all saturated and thus their associated alternating current windings have low impedance, and since the core of output reactor 4 is unsaturated so that its alternating current winding 14 has high impedance, substantially all of the voltage impressed across terminals 23 and 24 will appear across alternating current winding 14 of output reactor 4. As explained above, when the current in phase B reaches one unit, core 13 of output reactor 4 will become unsaturated thereby suddenly increasing the impedance of its alternating current winding 14. This

condition will prevail for 30 degrees of a complete cycle of impressed voltage until the phase B current increase sufficiently above one unit to cause reversal of the flux in core 16 of output reactor 4 at which time the core is driven into saturation in opposite direction with its alternating current winding 14 again becoming of low impedance. This reversal of flux in the core 13 of output reactor 4 induces a square half wave of voltage in direct current saturating winding 15 of output reactor 4 which appears across output terminals 30 and 31.

It will also be seen that the two units of current flowing in alternating current windings 17 of current limiting reactors 8 and 9 respectively aid the bias in current limiting reactor 9 so that the core 16 of this reactor remains saturated, and cancels the bias in current limiting reactor 8 so that the core 16 of this reactor is unsaturated and its alternating current winding 17 thus is of high impedance. Since current limiting reactors 12, 11, 10, and 9 are saturated and thus their alternating current windings are of low impedance and since the cores of current limiting reactors 7 and 8 are unsaturated and thus their alternating current windings 17 are of high impedance, the same voltage will appear across the alternating current winding of current limiting reactor 8 also as appears across the alternating current winding of current limiting reactor 7 i.e., since the voltage across terminals 22 and 23 substantially appears across the alternating current winding 17 of current limiting reactor 7, this same voltage also appears across the alternating current winding 17 of current limiting reactor 8.

Fig. 11 summarizes the functioning of the circuit of Fig. 1 during interval 1 and in chart form indicates that during interval 1, output reactor 4 produces the half wave of induced voltage in the bias circuit which appears across output terminals 30 and 31, that the voltage appearing across the output reactor which in turn produces the voltage in direct current saturating winding 15 of output reactor 4 is the voltage across the C and B phases, and that the unsaturated and thus high impedance current limiting reactors are E and 8. There are five units of net mmf in the direction of the bias in core 13 of output reactor 2 and Fig. 13 shows the magnitude and direction of currents in the circuit of Fig. 1 during interval 1.

Referring now to interval 2 on Fig. 13, it will be seen that the phase A current has been reduced to three units negative, phase B current is one unit negative, and phase C current is four currents positive; two units of current flowing in current limiting reactors 7 and 12 toward phase A, two units of current flowing in current limiting reactors 11 and 10 toward phase B, and one unit of current flowing in current limiting reactors 8 and 9 toward phase A. Since the phase B current is one unit in the opposite direction from its direction in interval 1 of Fig. 13, it is readily seen that output reactor 3 will be unsaturated and will thus produce a half cycle of output voltage as its core 16 is driven from saturation in one direction to saturation in the other direction, this half cycle of output voltage being of opposite polarity from the half cycle of output voltage produced in output reactor 4 during interval 1. Reference to Fig. 11 indicates that the output voltage is produced in output reactors 3, that the voltage appearing across the output reactor 3 is across phases B and A, and that the effective current limiting reactors are 7 and 10. Fig. 12 indicates that during interval 2, core 13 of output reactor 2 is saturated with four units of mmf in the direction of the bias.

The functioning of the circuit of Fig. 1 through the remainder of a complete cycle of input voltage, i.e., intervals 3 through 12 of Fig. 7, can readily be ascertained by reference to Fig. 13 which shows the direction and magnitude of currents in each of the phases and in each leg of the delta-connected current limiting reactors of the circuit of Fig. 1. The remaining intervals of Fig. 11

indicate the output reactor which is effective during each interval, the phase voltages across the output reactor during the interval, and the current limiting reactors which are effective during the interval. The remaining intervals in Fig. 12 likewise indicate the direction and magnitude of the flux in the core 13 of output reactor 2, it being observed that the reversal of flux from saturation in one direction to saturation in the other direction provides the half wave of output voltage occurs during intervals 4 and 9. Fig. 14 likewise indicates the sequential induction of output voltages and the output reactor in which each half cycle is induced. As indicated previously, Fig. 8 indicates the polarity and magnitude of phase current flowing in phase A and it will be readily understood that the direction and magnitude of current flowing in the other two phases is the same as that flowing in phase A except phase displaced therefrom by 120 degrees in the case of phase C and 60 degrees in the case of phase B.

When a unity power factor load, such as a resistive load, is connected across output terminals 31, load current flows tending to oppose the bias in each of the output reactors, i.e., the mmf. produced by the load current subtracts from the normal bias. The system of Fig. 1 will carry load current up to a value equal to the bias current, however, a tendency to draw any higher load current will result in no output voltage and the system is therefore self-limiting to a value of load current not exceeding the bias current. Referring again to Figs. 1, 8, and 13, and particularly interval 1 of the latter two figures, let it be assumed that a unity power factor load current of one unit is flowing. Under these conditions, the current in the alternating current windings 14 of output reactors 3 and 4 in phase B will fall to zero while the current in alternating current windings 14 of output reactors 5 and 6 in phase C will increase to four units, so that the maximum permissible four units of phase current are still flowing in phase A. In the second interval, with one unit of unity power factor load current flowing, the phase B current will increase to two units negative with the phase A current falling to two units negative and the phase C current remaining at four units positive. Fig. 8 indicates in dotted lines the magnitude and polarity of the current in phase A with one unit of load current flowing and the corresponding currents and phases B and C can be readily determined in the same manner as the above-described determination of the corresponding phase current with no load applied across terminals 30 and 31.

The system is self-protecting, hence with more than one unit of load current flowing, and considering interval 1 for purposes of illustration, the bias of both output reactors 3 and 4 will be cancelled so that both reactors are unsaturated and thus both will have output voltages induced in their direct current saturating windings 15, these output voltages however cancelling so that no net output voltage will appear across terminals 30 and 31. The load limit reactors i.e., the reactors which become unsaturated to provide the self-protection or self-limiting feature in the case of interval 1 are output reactor 3 and current limiting reactor 10, current limiting reactor 10 also tending to become high impedance if there is a tendency to drive two units of current through its alternating current winding 17. Under these conditions, reactors 3 and 10 share the voltage across terminals 23 and 24, i.e., the voltage of phases C and B with reactor 4 so that reactors 3 and 10 tend to remove the voltage from reactor 4 which is the source of output voltage during the interval 1. A similar load current limiting action takes place during each succeeding interval and the effective load current limiting reactor or reactors are set forth in the bottom horizontal column of Fig. 11.

While the embodiment of Fig. 1 has been described

utilizing simple closed core reactors, as shown in Fig. 2, for the frequency doubling or output reactors 1 through 6 and the current limiting reactors 7 through 12, it will be readily apparent that other types of saturable core reactors can be used in either the frequency doubling or current limiting reactor circuits. In the case of the frequency doubling reactor circuits, alternating current winding means and other winding means which performs both biasing and output voltage inducing functions are required. At least a part of the other winding means must provide the biasing function and at least a part must provide the output voltage, i.e., one part can provide the biasing function and another part the output voltage function, or in the alternative, both functions can be provided by the same unitary means. In addition, the alternating current winding means must aid a part and oppose another part of both the biasing and output portions of the other winding means. Thus, if separate saturable core reactors are employed for the frequency doubling circuits, as in Figs. 1 and 2, alternating current windings 14 in each pair of reactors comprise the alternating current winding means and saturating windings 15 comprise the other winding means. Here, the bias voltage is applied to all of the other winding means, i.e., all of the windings 15, the alternating current windings 14 of each frequency doubling reactor circuit aiding a part thereof, i.e., one winding 15, and opposing another part, i.e., the other winding 15 by virtue of the reversed connection of windings 15 as shown in Fig. 2. Furthermore, all of the other winding means, i.e., all of the bias windings 15 are also serially connected in the output circuit and thus function both as bias windings and as output windings.

Each of the frequency doubling reactor circuits may comprise a single reactor as shown in Fig. 3 rather than the separate reactors as shown in Fig. 1. Here, alternating current windings 37 are arranged on the outer legs 38 of a three-legged core 39 with the direct current saturating winding 40 being arranged on the center leg 41 of the core. In this case, windings 37 form the alternating current winding means, one winding 37 aiding the bias provided by the other winding means, i.e., winding 40 in one outside leg 38 of core 39, and the other winding 37 opposing the bias in the other outside leg 38 of the core. All of the other winding means, i.e., windings 40, are also connected in the output circuit and thus again performs both biasing and output functions. It will also be readily apparent that the alternating current and direct current saturating windings may be reversed in the arrangement of Fig. 3, i.e., windings 37 may be the direct current saturating winding and winding 40 the alternating current winding.

The output reactors 1 through 6 of Fig. 1 may be provided with separate output windings as shown in Figs. 4 and 5. Here, with output reactors 1 and 2 only being shown the output reactors are again provided with alternating current windings 14 and direct current saturating windings 15 arranged on cores 13. However, in this case, separate output windings 36 are provided on each of the output reactors which are serially connected across output terminals 30 and 31. In this case, windings 14 of each pair of reactors again constitute the alternating current winding means with windings 15 and 36 constituting the other winding means. The bias voltage is impressed on a part of the other winding means, i.e., windings 15, and the alternating current winding means aids a part, i.e., one winding 15, and opposes another part i.e., the other winding 15 of the other winding means, again by virtue of the reverse connection of windings 15. The remaining part of the other winding means, i.e., windings 36, are serially connected in the output circuit, and like the bias windings 15, each pair is oppositely connected so that the alternating current windings 14 aid one winding 36 and oppose the other.

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The construction of Fig. 3 may also be provided with separate output windings as shown in Fig. 6 in which output winding 42 is arranged on the center leg 41 along with saturating winding 40. Here again, windings 37 comprise the alternating current winding means and winding 42 comprises the other winding means, one of the alternating current windings 37 aiding the bias provided by the other winding means, i.e., winding 40, in one outside leg 38 of core 39 and the other winding 37 opposing the bias in the other outside leg 38. The remaining part of the other windings means, i.e., winding 42, is serially connected with the other output windings in the output circuit. Here, again, windings 37 may be the direct current saturating winding and winding 40 the alternating current winding, in which case, a pair of output windings 42 would be provided on the outer legs 38 of core 39.

In the case of the current limiting saturable core reactor circuits, it is only necessary that there be provided alternating current winding means and bias winding means with the alternating current winding means aiding a part and opposing the remainder of the bias winding means. Thus, in the event that separate saturable core reactors are used for the current limiting reactor circuits as shown in Fig. 1, alternating current windings 17 of each pair of reactors collectively constitute the alternating current winding means, aiding one part of the bias winding means, i.e., one bias winding 18, and opposing the remainder, i.e., the other bias winding 18. As in the case of the frequency doubling reactor circuits, single reactors, as shown in Fig. 3, may be employed in the current limiting reactor circuits, in which case windings 37 form the alternating current winding means, one winding 37 aiding the bias provided by the bias winding means, i.e., winding 40, in one outside leg 38 of the core 39, and the other winding 37 opposing the bias in the other outside leg 38 of the core.

Figs. 15 through 21 inclusive, show output voltage and current waves with lagging and leading current loads. Fig. 1 shows the wave form of the voltage applied to either an inductive or a capacitive load drawing current which does not exceed the bias current; i.e., in the example given not exceeding one unit of current. If the crest of the current wave drawn by an inductive load does not exceed one unit, the current will have a wave form as shown in Fig. 16, it being observed that the output current lags the output voltage. If, however, the crest of the current wave tends to exceed one unit, a limiting action identical with that described hereinabove for a resistive load clips the top of the wave as shown in Fig. 17 thus, providing an output voltage wave as shown in Fig. 18.

It will be seen that because a finite time is required for the lagging load current to reverse from unit value of one polarity to unit value of the opposite polarity, the total value of the lagging current wave must always be less than the rectangular current wave supplied to a resistive or unitary power factor load. It will be further noted that when the clipping action occurs during the latter part of the current wave as shown in Fig. 17, the maximum output voltage does not appear across the load, as shown in Fig. 18. This is in contrast with the rectangular voltage wave which appears across the load when the current is less than one unit. The actual load voltage during the limiting or clipping action is the resistance of the load times the unit current, resulting in the final wave shape of the output voltage as shown in Fig. 18. It will now be seen that the maximum power which can be delivered to a lagging power factor load is less than that which can be delivered to a resistive load, not only because of the out-of-phase relationship of voltage and current, but also because either current or voltage is less than maximum except at the instant current limiting begins.

Considering now a capacitive or leading power factor

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load, the output voltage applied to the load when less than one unit of load current is being drawn is again shown in Fig. 15 while the wave form of the current is shown in Fig. 19. Currents change instantaneously in capacitive circuits so with the rectangular output voltage of Fig. 15, maximum current occurs at the reversal of the voltage and then decays as the capacitor charges up. It will be observed that the current wave of Fig. 19 leads the output voltage of Fig. 15.

When the capacitive load attempts to draw more than one unit of current, the current limiting action of the device clips the current peak as shown in Fig. 20. During the clipping interval the voltage changes at a constant rate corresponding to the rate of charge of the capacitor by a constant current. It will be observed that the unit current continues to flow much later in the cycle than does a current of such magnitude in Fig. 19. This phenomenon occurs because the current limiting action has delayed the build up of capacitor voltage. In the case of a long time constant load, unit current may flow for the entire half cycle. Again, as in the case of an inductive load, it is seen that the maximum voltage and current do not simultaneously occur for more than an instant and the maximum power deliverable to the load is therefore less than is possible with a resistive load.

The above discussion has assumed ideal core materials for the output reactors 1 through 6 with square knees to their B—H curves and flat post-saturation branches. Actually, however, known magnetic materials have appreciable slopes to the post-saturation branches of their B—H curves and the inductance of the reactor is proportional to this slope. Since the output current must be delivered to the load through five nominally saturated output reactors in series, the equivalent circuit of the output reactors may be represented by the voltage of the effective output reactor, i.e., the unsaturated output reactor, in series with the saturated impedance of the remaining output reactors. This saturated impedance is primarily inductive and non-linear because the B—H curve is non-linear. A leading current through this inductance results in a voltage in phase additive to the voltage of the effective reactor; it is well known that a transformer supplying a leading current load has a terminal voltage higher than its open circuit voltage. The terminal voltage of the multiplier with a capacitive load may therefore be higher than the no-load terminal voltage. Conversely, in the case of an inductive load the internal regulation of the multiplier is poorer. For this reason, in an actual device, a slightly capacitive load may be desirable.

It will now be readily apparent that this invention provides an improved frequency multiplying circuit for converting three phase alternating current of a given frequency into single phase alternating current having a frequency six times the input frequency, the circuit providing this frequency multiplication in a single stage composed of a minimum number of static elements. These elements are components having higher overall utilization and thus a unit of smaller overall size and weight in contrast with previous frequency multiplying circuits is provided.

A circuit according to Fig. 1 has been constructed and tested. In this circuit, the output reactors 1 through 6 were identical, each having a core formed of grain oriented magnetic steel with a high silicon content and having a sharply saturating characteristic. These cores were 8.00 inches long by 3.25 inches wide with a stack height of 1.12 inches and with their legs having a width of 1.00 inches and the ends having a width of 2.00 inches. The alternating current windings 14 were composed of 258 turns of Formex A.W.G. No. 12 wire and the direct current saturating windings 15 were composed of 416 turns of No. 17 wire with the alternating current windings 14 being wound over the direct current saturating windings 15. The current limiting reactors 7 through 12 were

also identical each having its core again formed of grain oriented magnetic steel having a high silicon content with a sharply saturating characteristic, the cores being 3.25 inches wide and 8.00 inches long with a stack height of 1.06 inches and with the leg being 1.00 inches wide. Here, the alternating current winding 17 had 164 turns of No. 12 wire and was wound over the direct current saturating winding 28 which had 548 turns of No. 18 wire. Choke 35 had an inductance of 0.91 henries. In the circuit tested, with source 25 providing three phase alternating current with 220 volts between phases at 60 cycles, an output voltage of 750 volts at 360 cycles was provided across terminals 30 and 31 with 2.00 amperes of bias current. This system would provide load current of up to 1.25 amperes at 600 volts to a unity power factor load.

While I have illustrated and described specific embodiments of this invention, further modifications and improvements will occur to those skilled in the art. I desire that it be understood therefore that this invention is not limited to the specific form shown and I intend in the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A static single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having bias winding means and alternating current winding means said alternating current winding means aiding a part and opposing the remainder of said bias winding means, said alternating current winding means being delta-connected, three frequency doubling saturable core reactor circuits each having alternating current winding means and other winding means, connections for impressing a bias voltage on said bias winding means and at least a part of each of said other winding means, an output circuit serially connecting at least a part of each of said other winding means, each of said last-named alternating current winding means aiding a part and opposing another part of its associated other winding means, said last-named alternating current winding means being respectively connected to the junctions of said delta-connection, and connections for impressing said three phase alternating current of predetermined frequency on said last-named alternating current winding means.

2. A static single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having core means with direct current bias winding means and alternating current winding means thereon, each of said direct current bias winding means being arranged normally to saturate its associated core means, each of said alternating current winding means aiding a part and opposing the remainder of its associated direct current bias winding means, said alternating current winding means being delta-connected, three frequency doubling saturable core reactor circuits each having core means with alternating current winding means and other winding means thereon, connections for impressing direct current on said direct current bias winding means and on at least a part of each of said other winding means, each of said other winding means being arranged normally to saturate its associated core means, an output circuit serially connecting at least a part of each of said other winding means, each of said last-named alternating current winding means aiding a part and opposing another part of its associated other winding means, said last-named alternating current winding means being respectively connected to the junctions

of said delta-connection, and connections for respectively impressing said three phase alternating current of predetermined frequency on said last-named alternating current winding means, said frequency doubling saturable core reactor circuits each having its said core means constructed to be driven from saturation in one direction to saturation in the opposite direction in 30 degree of a cycle of the alternating current voltage impressed on its alternating current winding means.

3. A static single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having bias winding means and alternating current winding means, said alternating current winding means aiding a part and opposing the remainder of said bias winding means, said alternating current winding means being delta-connected, three frequency doubling saturable core reactor circuits each having alternating current winding means and other winding means, connections for impressing a bias voltage on said bias winding means and on at least a part of each of said other winding means, an output circuit serially connecting at least a part of each of said other winding means, each of said last-named alternating current winding means aiding a part and opposing another part of its associated other winding means, said last-named alternating current winding means being respectively connected to the junctions of said delta-connection, and connections for impressing said three phase alternating current of predetermined frequency on said last-named alternating current winding means, said bias winding means being arranged to provide substantially greater bias ampere turns than said other winding means.

4. A static single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having core means with at least one alternating current winding and two direct current saturating windings thereon, each of said current limiting circuits having its direct current saturating windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and to oppose the other of its associated direct current saturating windings, said alternating current windings being delta-connected, three frequency doubling saturable core reactor circuits each having core means with at least one alternating current winding and a plurality of other windings thereon, each of said frequency doubling circuits having at least two of its other windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and oppose the other of said two other windings, connections for impressing direct current on said direct current saturating windings and said two other windings of each of said frequency doubling circuits, an output circuit serially connecting at least two of said other windings of each of said frequency doubling circuits, said last-named alternating current windings being respectively connected to the junctions of said delta-connection, connections for respectively impressing said three phase alternating current of predetermined frequency on said last-named alternating current windings, said frequency doubling saturable core reactor circuits each having its said core means arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding, each of said direct current saturating windings being arranged to provide substantially greater ampere turns than each of said first-named two other windings.

5. A static single stage frequency multiplier for con-

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verting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having core means with at least one alternating current winding and two direct current saturating windings thereon, each of said current limiting reactor circuits having its direct current saturating windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and to oppose the other of its associated direct current saturating windings, said alternating current windings being delta-connected; three frequency doubling saturable core reactor circuits each having core means with at least one alternating current winding, two direct current saturating windings and two secondary windings thereon; each of said frequency doubling circuits having its direct current saturating windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and opposing the other of its associated direct current saturating windings, connections for impressing direct current on said direct current saturating windings, an output circuit serially connecting said secondary windings, said last-named alternating current windings being respectively connected to the junctions of said delta-connection, and connections for impressing said three phase alternating current of predetermined frequency on said last-named alternating current windings, said frequency doubling saturable core reactor circuits each having its core means arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding, said first-named direct current saturating windings being arranged to provide substantially greater ampere turns than said last-named direct current saturating windings.

6. A static single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times said predetermined frequency comprising three current limiting saturable core reactor circuits each having core means with at least one alternating current winding and two direct current saturating windings thereon, each of said current limiting circuits having its direct current saturating windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and to oppose the other of its associated direct current saturating windings, said alternating current windings being delta-connected, three frequency doubling saturable core reactor circuits each having core means with at least one alternating current winding and two direct current saturating windings thereon, each of said frequency doubling circuits having its direct current saturating windings arranged normally to saturate said core means adjacent thereto and its alternating current winding arranged to aid one and oppose the other of its direct current saturating windings, connections for impressing direct current on said direct current saturating windings, an output circuit serially connected to said last-named direct current saturating windings, said last-named alternating current windings being respectively connected to the junctions of said delta-connection, and connections for impressing said three phase alternating current of predetermined frequency on said last-named alternating current windings, said frequency doubling saturable core reactor circuits each having its core means arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding, said first-named direct current saturating windings being arranged to provide substantially greater ampere turns and said last-named direct current saturating windings.

7. A single stage frequency multiplier for converting

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three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times the predetermined frequency comprising three input terminals for connection to a source of three phase alternating current, three pairs of current limiting saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, said direct current windings of each of said pairs of current limiting reactors being arranged normally to saturate their associated cores respectively in opposite directions, each pair of said current limiting reactors having its alternating current windings serially connected, said serially connected pairs of alternating current windings being delta-connected, three pairs of frequency doubling output saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, each pair of said output reactors having its alternating current windings serially connected, said last-named serially connected pairs of alternating current windings being respectively connected between said input terminals and the junction points of said delta-connection, said direct current windings of each of said pairs of output reactors being arranged normally to saturate their associated cores respectively in opposite directions, a pair of output terminals, said direct current windings of said output reactors being serially connected across said output terminals, and connections for impressing direct current on all of said direct current windings, said direct current windings of said current limiting reactors having substantially greater ampere turns than the ampere turns of said direct current windings of said output reactors, each of said output reactors having its core arranged to be driven from saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding.

8. A single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times the predetermined frequency comprising three input terminals for connection to the source of three phase alternating current, three pairs of current limiting saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, said direct current windings of each of said pairs of current limiting reactors being arranged normally to saturate their associated cores respectively in opposite directions, each pair of said current limiting reactors having its alternating current windings serially connected, said serially connected pairs of alternating current windings being delta-connected, three pairs of frequency doubling output saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, each pair of said output reactors having its alternating current windings serially connected, said last-named serially connected pairs of alternating current windings being respectively connected between said input terminals and the junction points of said delta-connection, said direct current windings of each of said pairs of output reactors being arranged normally to saturate their associated cores respectively in opposite directions, said direct current windings of said current limiting reactors having substantially greater ampere turns than the ampere turns of said direct current windings of said output reactors, all of said direct current windings being connected in series, connections for impressing direct current on said serially connected direct current windings, a pair of output terminals, said serially connected direct current windings of said output reactors being connected across said output terminals, each of said output reactors having its core arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding.

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9. A single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times the predetermined frequency comprising three input terminals for connection to the source of three phase alternating current, three pairs of current limiting saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, said direct current windings of each of said pairs of current limiting reactors being arranged normally to saturate their associated cores respectively in the opposite directions, each pair of said current limiting reactors having its alternating current winding serially connected, said serially connected pairs of alternating current windings being delta-connected, three pairs of frequency doubling output saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, each pair of said output reactors having its alternating current windings serially connected, said last-named serially connected pairs of alternating current windings being respectively connected between said input terminals and the junction points of said delta-connection, said direct current windings of each of said pairs of output reactors being arranged normally to saturate their associated cores respectively in opposite directions, said direct current windings of said current limiting reactors having substantially greater ampere turns than the ampere turns of said direct current windings of said output reactors, all of said direct current windings being connected in series, connections for impressing direct current on said serially connected direct current windings, a pair of output terminals, said serially connected direct current windings of said output reactors being connected across said output terminals, each of said output reactors having its core arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding, and a choke connected in series with said direct current windings of said current limiting reactors.

10. A single stage frequency multiplier for converting three phase alternating current having a predetermined frequency into single phase alternating current having a frequency six times the predetermined frequency comprising three input terminals for connection to the source of three phase alternating current, three pairs of current limiting saturable core reactors each having a core with an alternating current winding and a direct current saturating winding thereon, said direct current windings of each of said pairs of current limiting reactors being arranged normally to saturate their associated cores respectively in the opposite directions, each pair of said current limiting reactors having its alternating current windings serially connected, said serially connected pairs of alternating current windings being delta-connected, three pairs of frequency doubling output saturable core reactors each having a core with an alternating current winding and a direct current saturating winding, each pair of said output reactors having its alternating current windings serially connected, said last-named serially connected pairs of alternating current windings being respectively connected between said input terminals and the junction points of said delta-connection, said direct current windings of each of said pairs of output reactors being arranged normally to saturate their associated cores respectively in opposite directions, said direct current windings of said current limiting reactors having at least substantially twice the ampere turns of said direct current windings of said output reactors, all of said direct current windings being connected in series, connections for impressing direct current on said serially connected direct current windings, and a pair of output terminals, said serially connected direct current windings of said output reactors being connected across said output terminals, each of said output

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reactors having its core arranged to be driven from saturation in one direction to saturation in the opposite direction in 30 degrees of a cycle of the alternating current voltage impressed on its alternating current winding.

11. A static single stage frequency multiplier for converting polyphase alternating current having a predetermined frequency into a single phase alternating current having a frequency which is said predetermined frequency multiplied by double the number of the phases of said polyphase current, comprising: a plurality of biased frequency doubling saturable core reactor circuits each having alternating current winding means, each of said alternating current winding means being connected to a different phase conductor of the source of said polyphase alternating current, each of said frequency doubling saturable core reactor circuits having output winding means; an output circuit including all of said output winding means; and an internal neutral network connecting the alternating current winding means of said frequency doubling saturable core reactor circuits, said neutral network comprising a plurality of biased current limiting saturable core reactor circuits connected in a mesh polygon relationship, and said alternating current winding means being respectively connected to the junctions of said network.

12. A static single stage frequency multiplier for converting polyphase alternating current having a predetermined frequency into single phase alternating current having a frequency which is said predetermined frequency multiplied by double the number of the phases of said polyphase current, comprising: a plurality of frequency doubling saturable core reactor circuits each having alternating current winding means and other winding means; connections for impressing a bias voltage on at least a part of each of said other winding means; an output circuit serially connecting at least a part of each of said other winding means; each of said alternating current winding means aiding a part and opposing another part of its associated other winding means; connections for respectively connecting each of said alternating current winding means in circuit with a different phase conductor of the source of said polyphase alternating current; and an internal neutral network connecting said alternating current winding means, said internal neutral network comprising a plurality of current limiting saturable core reactor circuits each having bias winding means and alternating current winding means, said last mentioned alternating current winding means aiding a part and opposing the remainder of said bias winding means and being connected in a mesh polygon network relationship, said alternating current winding means of said frequency doubling reactors being connected respectively to the junctions of said network, and connections for impressing a bias voltage on said bias winding means.

13. A static single stage frequency multiplier for converting polyphase alternating current having a predetermined frequency into single phase alternating current having a frequency which is said predetermined frequency multiplied by double the number of the phases of said polyphase current, comprising: a plurality of input terminals adapted to be respectively connected to a source of polyphase alternating current; a plurality of pairs of frequency doubling output saturable core reactors equal in number to the number of phases of said source and each having a core with an alternating current winding and a direct current saturating winding, each pair of said output reactors having its alternating current windings serially connected, each of said serially connected pairs of alternating current windings having one end connected to a respective input terminal, said direct current windings of each of said pairs of output reactors being arranged normally to saturate their associated cores respectively in opposite directions; a plurality of pairs of current limiting saturable core reactors equal in number to the number of phases of said source and each having a core with an alternating current winding and a

direct current saturating winding thereon, said direct current windings of each of said pairs of current limiting reactors being arranged normally to saturate their cores respectively in opposite directions, each pair of said current limiting reactors having its alternating current windings serially connected, and the serially connected pairs of alternating current windings being connected in a mesh polygon relationship to form an internal neutral network; the serially connected alternating current windings of said pairs of output reactors being connected respectively to the junctions of said network, and all of said direct current windings being connected in series; connections including a series choke for impressing direct current on

said serially connected direct current windings; and a pair of output terminals, said serially connected direct current windings of said output reactors being connected across said output terminals.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 2,892,141

June 23, 1959

David L. La Fuze

It is hereby certified that error appears in the printed specification of the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 8, line 40, for "reactors are E" read -- reactors are 7 --; column 11, line 11, for "windings" read -- winding --; column 13, line 57, for "curent" read -- current --; line 69, for "associate" read -- associated --; column 14, line 7, for "degree" read -- degrees --.

Signed and sealed this 18th day of October 1960.

(SEAL)

Attest:

KARL H. AXLINE

Attesting Officer

ROBERT C. WATSON

Commissioner of Patents

UNITED STATES PATENT OFFICE
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