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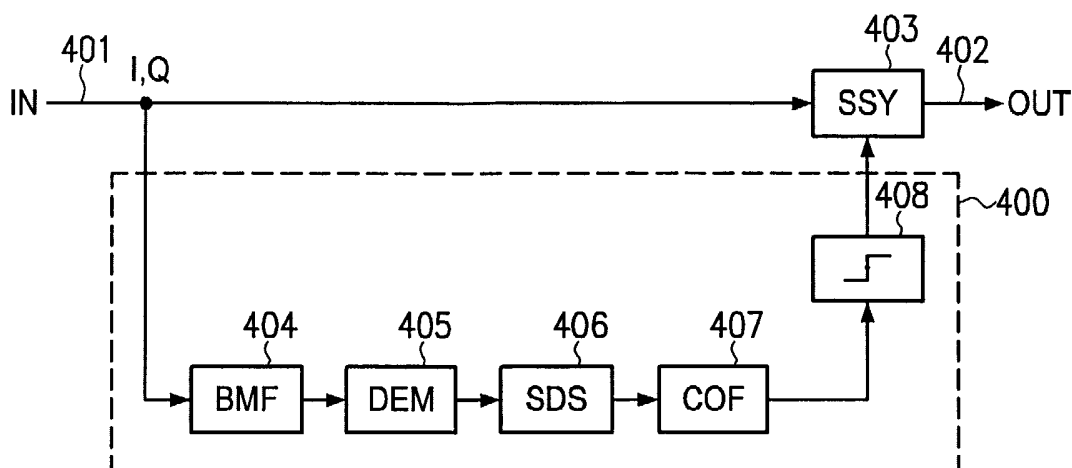
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(54) Title: SYNCHRONIZATION DATA DETECTION UNIT AND METHOD



(57) **Abstract:** A synchronization data detecting unit is provided in a communication system for detecting predetermined synchronization data. The synchronization data are sent in a transmission frame in a communication signal of the communication system. The synchronization data include a sequence of identical binary symbols which are transmitted after scrambling. The synchronization detection unit comprises a descrambler (406) for descrambling the received communication and for producing an output data sequence having multi-level signal values. The multi-level signal values of the descrambler output are smoothed in a filter unit (407). The smoothed signal is compared with a predetermined threshold value. If the smoothed signal exceeds the predefined threshold value, a detection of said synchronized data is indicated.



WO 03/084119 A1

SYNCHRONIZATION DATA DETECTION UNIT AND METHOD

Technical Field

The invention generally relates to a synchronization data detection unit and a method for detecting predetermined synchronization data, and in particular to a receiver and a receiving method in a wireless local area network (WLAN) communication system.

Background Art

In a communication system such as a wireless local area network (WLAN) system, it is important for a receiver to be synchronized to the transmitter so that messages can successfully be exchanged between the transmitter and the receiver. A wireless local area network system is a flexible data communication system implemented as an extension to or an alternative for a wired LAN. WLAN systems transmit and receive data over the air using radio frequency or infrared technology to minimize the need for wired connections. Thus, WLAN systems combine data connectivity with user mobility.

Most WLAN systems use spread spectrum technology, a wide-band radio frequency technique developed for use in a reliable and secure communication system. The spread spectrum technology is designed to trade-off bandwidth efficiency for reliability, integrity and security. Two types of spread spectrum radio systems are frequently used: frequency hopping and direct sequence systems.

In direct sequence spread spectrum systems, spreading is achieved by encoding each data bit using a code word or symbol that has a much higher frequency and information bit rate. The resultant "spreading" of the signal across a wider frequency bandwidth results in a comparatively lower power spectrum density, so that other communication systems are less likely to suffer interference from the device that transmits the direct sequence spread spectrum signal. Direct sequence spread spectrum employs a pseudo random noise code word known to the transmitter and receiver to spread the data. The code word consists of a sequence of "chips" that are multiplied by (or exclusive-ORed) with the information bits to be transmitted. Many wireless networks conform the IEEE 802.11 standard which employs the well-known Barker code word to encode and spread the data. The Barker code word consists of a predefined sequence of eleven chips. One entire Barker code word sequence is transmitted at the time period occupied by an information-containing symbol.

To allow higher data rate transmissions, the IEEE 802.11 standard was extended to IEEE 802.11b. In addition to the 11-bit Barker chip, the 802.11b standard uses an 8-bit complementary code keying (CCK) algorithm for high data rate transmission.

The data transfer rate may also be improved above the symbol rate by employing higher order modulation techniques, including quadrature phase-shift keying (QPSK) modulation. According to such modulation techniques, each bit is represented by a higher number of possible phases. The transmitter therefore generates two signals, the first signal is called the "in-phase" (I) signal or "I channel" and the second signal is called the

“quadrature” (Q) signal or “Q channel” for a 90 degree phase-shifted sinusoidal carrier at the same frequency.

The IEEE 802.11 standard for wireless LANs using direct sequence spread spectrum techniques employ a training preamble to train a receiver to a transmitter. Each transmitted data message comprises an initial training preamble followed by a data field. The preamble includes a synchronization field to ensure that the receiver can perform the necessary operations for synchronization. For the preamble length, two options have been defined, namely a long and a short preamble. All compliant 802.11b systems have to support the long preamble. The short preamble option is provided in the standard to improve the efficiency of the network throughput when transmitting special data such as voice or video. The synchronization field of a preamble consists of 128 one bits for a long preamble and 56 zero bits for a short preamble.

A receiver detects the synchronization symbols and aligns the receiver's internal clock with the symbols in the synchronization field in order to establish a fixed reference time frame with which it interprets the fields in the transmission frame structure following the preamble. The preamble, including the synchronization field, is transmitted with the start of every message (data packet).

The purpose of a preamble detection unit is to continuously monitor the incoming signal for the preamble and to indicate if the preamble has been detected. The boundaries between consecutive Barker symbols or CCK symbols are determined and the forwarding of the symbols is to be synchronized to the receiver's processing schedule. Based on the preamble detection and a timing offset between a symbol arrival and a processing schedule of the following modules, the incoming signal is synchronized to the receiver's processing schedule.

Referring now to Fig. 1, a detection process for detecting a preamble in a communication signal is illustrated. A preamble detection step 101 is performed after receiving a communication signal 100 and before subjecting the received communication signal to further processing, in particular to descrambling 102.

The configuration of a conventional preamble detector 200 is illustrated in Fig. 2. The received communication signal 201 consisting of an in-phase and a quadrature component is provided to preamble detector 200. In the preamble detector 200, the received communication signal 201 is first applied to a despreader 204, in particular a Barker matched filter (BMF). The despread communication signal is supplied to a demodulator (DEM) 205 for demodulating the despread communication signal. The demodulated signal consists of a sequence of “hard” decisions of the received bit sequence, i.e. each data value of the demodulated signal takes one of both possible binary values. The demodulated bit stream is monitored for detecting the predefined preamble data. Typically, a correlator is used to detect the preamble. The correlator is essentially a matched filter for the preamble sequence. The correlator produces an output with a large magnitude when the preamble is present. Preamble detection is normally declared when the magnitude of the correlation exceeds a predefined threshold.

After preamble detection, the demodulated communication signal is applied to a (digital) descrambler (DDS). An example of a prior art descrambler 300 is illustrated in Fig. 3. The incoming signal 301a is supplied to delay blocks 304, 305 denoting a time delay of several units in accordance with a predefined descrambling rule. The delayed signals are fed back and combined using a multiplier or exclusive-OR gate 306. The output is fed back to the incoming signal 301b and combined using a multiplier or exclusive-OR gate 303 to produce a descrambled

output 302.

Synchronization data detecting units still have a number of problems. One problem is that noise may degrade the signal quality so that the synchronization unit, in particular the preamble detector, fails to declare a preamble even though a preamble is present in the received communication signal. Noise may also produce an output exceeding the threshold when an actual preamble is not present.

Disclosure of Invention

An improved synchronization detection unit and method are provided that enable a less error prone detection of predefined synchronization data.

- 10 In one aspect of the invention, a synchronization data detection unit is provided in a communication system for detecting predetermined synchronization data of a transmission frame in a communication signal. The synchronization data include a sequence of identical binary symbols which are transmitted after being sent through a scrambler. The synchronization data detection unit comprises a descrambler for descrambling the received communication signal and for producing an output data sequence having multi-level signal values. The multi-level
15 signal values are applied to a filter means for smoothing the descrambler output. The smoothed signal is supplied to a threshold means. The threshold means compares the smoothed output of the filter means with a predetermined threshold value. If the output of the filter means exceeds the predefined threshold value, the threshold means indicates the detection of said synchronization data.

In a further embodiment said filter means is a comb filter.

- 20 In a further embodiment said comb filter comprises a predetermined number of identical delay portions for sequentially delaying a received input signal an accumulation means for accumulating the output signal of each of the delay portions and the input signal.

In a further embodiment said comb filter further comprises normalizing means for dividing the accumulation result by the number (n) of accumulated signals.

- 25 In a further embodiment each of said delay portions consists of a predetermined number of registers in series connection.

In a further embodiment said predetermined number of registers is larger than 5.

In a further embodiment said comb filter comprises at least nine delay portions.

- 30 In a further embodiment said threshold means are adapted to indicate a detection of said synchronization data after determining that a predetermined number of subsequent accumulation results exceeds said predetermined threshold (Th).

In a further embodiment said predefined number of subsequent accumulation results is a number between 5 and 20.

In a further embodiment said predefined number of subsequent accumulation results is larger than 10.

5 In a further embodiment said threshold means provides at least two threshold values (Th_1 , Th_2) to discriminate and detect synchronization data of different lengths in said communication signal.

In a further embodiment said threshold means comprises a first threshold value (Th_1) for detecting synchronization data of a longer length and a second threshold value (Th_2) for detecting synchronization data of a shorter length.

In a further embodiment said first and second threshold values (Th_1 , Th_2) have the same absolute value but different signs.

10 In a further embodiment said communication system is adapted for employing a direct sequence spread spectrum transmission scheme for transmission of said communication signal and said synchronization data detection unit further comprises

a despreading unit for despreading the received

communication signal, and a demodulating unit for demodulating the despread communication signal.

In a further embodiment said communication system is a wireless local area network (WLAN) system.

15 In a further embodiment a wireless LAN receiver comprising a synchronization data detection unit according to any of the above embodiments.

In still another aspect of the invention, a method for receiving synchronization data is provided for use in a communication system. The predetermined synchronization data are included in a transmission frame of a communication signal. The synchronization data comprise a sequence of identical binary symbols which are
20 transmitted after scrambling. The received communication signal is descrambled to produce a sequence of multi-level output signal values. The multi-level output signal values are smoothed and the smoothed signal is compared to a predetermined threshold value. If the smoothed signal exceeds the predetermined threshold, said synchronization data are detected.

In one embodiment said smoothing step averages the signal values of the received descrambled signal.

25 In a further embodiment said averaging step comprises the steps of:

subsequently delaying the received input signal a plurality of times,

accumulating each of the delayed signal portions and the input signal, and

outputting the accumulated signal.

30 In a further embodiment said output signal being normalized by dividing the accumulated signal by the number of accumulated signal portions.

In a further embodiment said first and said second threshold values (Th_1, Th_2) have the same absolute value but different signs.

In a further embodiment said communication signal is transmitted using a direct sequence spread spectrum transmission scheme and said communication signal being despread and demodulated before being descrambled.

- 5 In a further embodiment a method for receiving a communication signal in a communication system comprises the steps of detecting synchronization data in accordance with the methods described above.

Brief Description of Drawings

- 10 The accompanying drawings are incorporated into and form a part of the specification for the purpose of explaining the principles of the invention. The drawings are not to be construed as limiting the invention to only the illustrated and described examples of how the invention can be made and used. Further features and advantages will become apparent from the following and more particular description of the invention, as illustrated in the accompanying drawings, wherein:

- Fig. 1 is a flow-chart illustrating a preamble detection procedure;
- 15 Fig. 2 is a block diagram illustrating a preamble detector for detecting a preamble in a communication signal;
- Fig. 3 is a block diagram illustrating the configuration of a descrambler incorporated into a preamble detector as shown in Fig. 2;
- Fig. 4 is a block diagram illustrating a synchronization data detection unit;
- Fig. 5 is a block diagram illustrating a configuration of a half-soft descrambling module incorporated in the
20 configuration as shown in Fig. 4;
- Fig. 6 is a block diagram illustrating a more detailed embodiment of the descrambling module shown in Fig. 5;
- Fig. 7 is a block diagram illustrating a configuration of a filter module as shown in the configuration of Fig. 4;
- Fig. 8 is a block diagram illustrating another configuration of a filter module as shown in Fig. 6;
- Fig. 9 is a flow-chart illustrating a preamble detection processing procedure;
- 25 Fig. 10 is a flow-chart illustrating a threshold comparison procedure for detecting predetermined synchronization data in a communication signal; and
- Fig. 11 is a flow-chart illustrating a more detailed threshold comparison procedure for detecting two different kinds of preambles in a communication signal.

Modes of Carrying Out the Invention

The illustrative embodiments of the present invention will be described with reference to the figure drawings.

Referring now to the drawings and in particular to Fig. 4, which illustrates a synchronization data detecting unit for detecting synchronization data, in particular a predefined preamble, as described herewith. The configuration as shown in Fig. 4 consists of a synchronization data detecting module 400 and a synchronizing module 403. The synchronization data detecting module 400 detects a preamble and may also provide a timing offset between a symbol arrival and the processing schedule of the following modules. The symbol synchronizer 403 will use the timing offset information to synchronize the data stream to the processing schedule.

The synchronization data detecting module 400 comprises the following modules: a Barker matched filter (BMF) module 404, a differential BPSK demodulator (DEM) module 405, and a soft descrambler (SDS) module 406. These modules, i.e. BMF, DEM, and SDS, form together a non-coherent receiver. Further, the synchronization data detecting module 400 comprises a comb filter (COF) module 407 for smoothing the descrambler output. For evaluating the smoothed data to detect the predefined preamble data the synchronization data detecting module 400 contains a threshold controller 408. Details of the above-identified modules are described below.

The Barker matched filter module 404 receives the communication signal 401 input to the synchronization data detecting module 400 and computes a correlation between the Barker sequence and the samples of the input signal. The Barker code word consists of eleven chips which comprise the sequence "01001000111" or "+1,-1,+1,+1,-1,+1,+1,+1,-1,-1,-1" (non-return-to-zero - NRZ), in which the leftmost chip is output first in time. One entire Barker code word sequence is received in the time period occupied by an information-containing symbol. Thus, if the symbol rate is 1 Mbaud, the underlying chip rate for the eleven chips of the Barker sequence is 11 MHz. By using the 11 MHz chip rate signal, the spectrum occupied by the transmitting signal is eleven times greater. In an exemplary implementation, the Barker sequence is extended from eleven samples to twenty-two samples due to an input sample rate of 22 Msps. This is achieved by stuffing zeros between the original elements of the Barker sequence.

The input samples of the I channel and the Q channel are correlated with the Barker sequence, respectively. A complex correlation sample is computed for each complex input sample. This may be implemented by a "sliding-window" algorithm known in the art.

The despread communication signal is applied to demodulator module 405. In a specific implementation, the demodulator module 405 is a differential BPSK demodulator.

Turning now to Fig. 5 and Fig. 6, which illustrate particular implementations for a descrambler module 406. The descrambler module 406 may be implemented as a soft-descrambler outputting multi-value samples. In contrast to digital demodulators, in a soft descrambler multi-value input signals are not subjected to a "hard" binarization, but the descrambled output values are aligned around the expected binary values.

In other embodiments described herein, a “half-soft” descrambler is used for descrambling the demodulated signal. Examples of a configuration of a “half-soft” descrambler module 500 are shown in Fig. 5 and Fig. 6. A half-soft descrambler differs from a soft descrambler in that the input signal 501a applied to a “delay portion” 504-506 in said descrambler is binarized whereas the other branch of the input signal 501b is maintained as multi-value signal. In descrambler 500 of Fig. 5, the received input signal 501a is applied to a binarization portion 503 for converting a multi-value input sample value into a binary value.

The descrambler 500 is configured in accordance with a predefined generating polynomial, e.g. given by $1 + x^a + x^b$ wherein x^a and x^b denote predefined time delays. The delayed signals are fed back and added to the input signal using a multiplication or exclusive-OR gate to produce the descrambled output. As shown in Fig. 6, the delay elements 504, 505 comprise a plurality of one bit registers 601-606, each denoting a time delay of one unit. The half-soft descrambler outputs a sequence of soft-symbols aligned around the expected binary values.

The half-soft descrambler arrangement of Fig. 5 and Fig. 6 may have the advantage that the hardware effort for providing multi-level output samples is considerably reduced compared to conventional soft descramblers.

When receiving preamble data, the multi-level output sample values of a soft or half-soft descrambler all have the same sign. In order to reduce an influence of random deviations in the output sample values, the output sample values are averaged by means of a comb filter 407. Implementation examples for a comb filter are shown in Fig. 7 and Fig. 8.

Referring now to Fig. 7, the incoming real and imaginary data symbols 701 are applied to a multiplier 705 to be weighted with a weight W_1 . The weighed signal is added to a fed back and delayed output signal 702 using a delay element 704 and an adder 703. Before adding the fed back output signal and the input signal, the delayed fed back signal is also weighted using a multiplier 706 with a weight W_2 .

According to a particular embodiment, the incoming data symbols 701 are multiplied in multiplier 705 with a fixed-point equivalent of 0.2 and the delayed “averaged” values provided by delay element 704 are multiplied with a fixed-point equivalent of 0.8. Although the algorithm of this embodiment is described with reference to weighting values of 0.2 and 0.8, respectively, those skilled in the art will appreciate that the weighting algorithm may be implemented to the same effect using a variety of weighting value combinations W_1 and W_2 . A noise reduction of the input sample values 701 may be increased by reducing the amount of weight W_1 and increasing the amount of weight W_2 . In contrast, the accuracy of the received data symbols in time may be increased by increasing the amount of the first weight W_1 and decreasing the amount of the second weight W_2 .

Another embodiment of a comb filter configuration is shown in Fig. 8. Each output of the depicted comb filter represents an average of n chip samples that are spaced by eleven or twenty-two samples (depending on the employed input sample rate). As those skilled in the art will appreciate, the number of averaged samples is set to be appropriate for a sufficient noise reduction. Noise will be reduced more efficiently when increasing the number n . In a specific example of this embodiment, the number n of averaged samples is 10. An averaged amplitude is computed separately for the in-phase channel I and the quadrature channel Q . This may be achieved in the specific embodiment by implementing the following formulas:

$$f_I(k) = \frac{1}{10} \sum_{i=0}^9 d_I(k - 22i)$$

$$f_Q(k) = \frac{1}{10} \sum_{i=0}^9 d_Q(k - 22i)$$

wherein $f(k)$ represents the comb filter output and $d(k-22i)$ represents the descrambler output when employing a Barker sequence of 22 samples, as mentioned above.

Both filter outputs f_I and f_Q will be used to decide if a preamble is currently received. In a specific embodiment, both outputs are added to counter the influence of the frequency offset of the signal:

$$S(kT) = f_I(kT) + f_Q(kT)$$

wherein S represents the sum of both outputs and f_I and f_Q represent the averaged comb filter output of the respective channel.

Referring back to Fig. 8, comb filter 800 comprises a plurality of delay elements 804, an adder 803 and a divider 805. The incoming descrambler output 801 is applied to the adder 803 and branched to a first one of the identical delay elements 804. The output of each of the delay elements 804 is applied to adder 803 and to the input of a subsequent one of the delay elements 804. Adder 803 receives a predetermined number n of input signals which are accumulated and provided to divider 805. The number n of inputs and a corresponding number of $n-1$ of delay elements 804 is set in accordance with the above described considerations. Divider 805 normalizes the accumulated sum provided by adder 803.

Fig. 9 schematically shows an example of how to detect a preamble in an incoming communication signal. After receiving (step 900) the communication signal, the communication signal is subjected to a soft descrambling process 901 and the descrambled output is smoothed in order to reduce the influence of random deviations in the communication signal (902). The preamble is detected in the output signal on the basis of the output signal values of the averaged descrambler output in step 903. The preamble detection is performed by comparing the comb filter output against a predefined threshold value. Details of the process performed by threshold controller 408 are illustrated in Fig. 10.

As shown in Fig. 10, each obtained comb filter sum S (step 1001) is compared during preamble search against a predefined threshold Th in step 1002. When the comb filter output exceeds the predefined threshold Th , a preamble may have been detected (step 1003) and the preamble detection procedure enters a "preamble detecting state". Threshold controller 408 will remain in this state while fetching two more chips to determine if subsequent descrambler outputs are even larger.

After comparing these two further sample values, the threshold controller will periodically confirm the comparison result, i.e. to determine whether or not a descrambler peek re-appears after a symbol duration. The comb filter output has to exceed the predefined threshold T_h a predetermined number of times before a preamble detection is definitely declared (steps 1004, 1005). The “locked state” (in case of a preamble detection) is entered after the comparator result in step 1002 is confirmed a predetermined number of times T_N . In one implementation, T_N is 15, i.e. requiring to confirm a preamble detection 15 times. Those skilled in the art will appreciate that any other number of times may be implemented to the same effect, e.g. a number T_N between 10 and 20 times.

In accordance with the IEEE 802.11b standard for wireless LANs, the threshold controller 408 may be adapted to detect a long and a short preamble. As both preambles not only differ by their lengths but also differ by the binary value of the preamble sequence, these preambles may be distinguished by employing different threshold values corresponding the binary preamble values.

A threshold comparison process able to detect a long and a short preamble in accordance with the wireless LAN standard is illustrated in Fig. 11. The preamble detection procedure employs a first threshold T_{h1} and a second threshold T_{h2} . In accordance with the expected descrambler output values $+1/-1$ both threshold values only differ by the sign.

After having first detected a long or short preamble in step 1102 or in step 1107, a “reliability check” is performed for each of the preambles repeatedly either by steps 1103-1106 or by steps 1108-1111. In case the detected long or short preamble cannot be confirmed in one of the confirmation loops formed by steps 1103-1106 for a long preamble confirmation or by steps 1108-1111 for a short preamble confirmation, the threshold comparator returns to step 1101.

After a preamble has been detected and confirmed and a timing offset between symbol arrival and symbol processing in the following data modules is known, the symbol synchronizer module 403 will release the data such that symbol release and symbol processing are matched.

According to the various embodiments described above, the decision for each sent symbol is shifted from the demodulator's output to the comb filter's output. According to a specific embodiment, a half-soft descrambler is employed which introduces a binarization in the descrambler “delay path” comprising a plurality of one bit width registers. The output of the half-soft descrambler is a sequence of soft symbols which are aligned around the expected value of $+1$ (long preamble consisting of sent ones) or -1 (short preamble consisting of sent zeros) based on the sent preamble sequence.

The embodiments described above may provide a more reliable and improved preamble detection without increasing the hardware complexity. By shifting the preamble detecting step to a subsequent processing stage, the preamble detection of the various embodiments described herein reduce the occurrence of failure to detect a preamble or to wrongly detect a preamble.

Industrial Applicability

Evidently, the present invention may advantageously be used in industrial processes and products.

CLAIMS

1. A synchronization data detection unit in a communication system for detecting predetermined synchronization data of a transmission frame in a communication signal, said synchronization data including a sequence of identical binary symbols which are transmitted after scrambling, comprising:
 - a descrambler (406) for descrambling the received communication signal (501) and producing output data symbols (502) having multi-level signal values,
 - a filter means (407) for smoothing the descrambled output data symbols (502), and
 - a threshold means (408) for comparing the smoothed output (802) of said filter means (407) with a predetermined threshold value (Th) and indicating a detection of said synchronization data if the output (802) of the filter means (408) exceeds said predetermined threshold value (Th).
2. The synchronization data detection unit according to claim 1, wherein said descrambler (500) comprising:
 - a binarization portion (503) for converting a received multi-level input signal (501a) into a binary signal,
 - a delay portion (504-506) delaying the binary signal in accordance with a predefined descrambling rule,
 - a multiplication portion (502) for multiplying the multi-level input signal (501b) with the binary signal output from the delay portion (504-506) and outputting a descrambled signal.
3. The synchronization data detection unit according to claim 2, wherein said delay portion (504-506) consists of a plurality of delay sections (504, 505) and at least one signal combining portion (506) for combining binary signals having a different delay in accordance with a predefined descrambling rule.
4. The synchronization data detection unit according to claim 2, wherein the delay portion (504, 505) comprises a plurality of delay registers (601-606) having a one bit width.
5. The synchronization data detection unit according to claim 1, wherein the descrambled signal output has at least a two bit width.
6. A method for detecting predetermined synchronization data of a transmission frame in a communication signal, said synchronization data including a sequence of identical binary symbols which are transmitted after scrambling, the method comprising the steps of:
 - descrambling (901) the received communication signal and producing an output data sequence having multi-level signal values,
 - smoothing (902) the multi-level signal values of the descrambled signal, and

comparing (903) the multi-level signal values of the smoothed signal with a predetermined threshold value (T_h) and detecting said synchronization data if the smoothed signal exceeds the predetermined threshold value (T_h).

- 5 7. The method for detecting predetermined synchronization data according to claim 6, wherein said descrambling step (901) comprises the steps of:

converting the received multi-level input signal into a binary signal,

delaying the binary signal in accordance with a predefined descrambling rule,

multiplying the multi-level input signal with the binary signal, and

outputting the descrambled signal.

- 10 8. The method for detecting predetermined synchronization data according to claim 7, wherein the step of delaying the binary signal comprises the steps of delaying the binary signal and combining the delayed binary signal with a further delayed binary signal in accordance with the predetermined descrambling rule.

- 15 9. The method for detecting predetermined synchronization data according to claim 6, wherein said comparing step (903) further comprises the step of indicating a detection of said synchronization data after determining (1001-1005) that said accumulation result subsequently exceeds said predetermined threshold (T_h) a predetermined number of times (T_N).

10. The method for detecting predetermined synchronization data according to claim 9 wherein said comparing step comprises the step of:

20 comparing (1104) the accumulation result with a first threshold value (T_{h1}) for detecting synchronization data of a longer length, and

comparing (1107) said accumulation result with a second threshold value (T_{h2}) for detecting synchronization data of a shorter length.

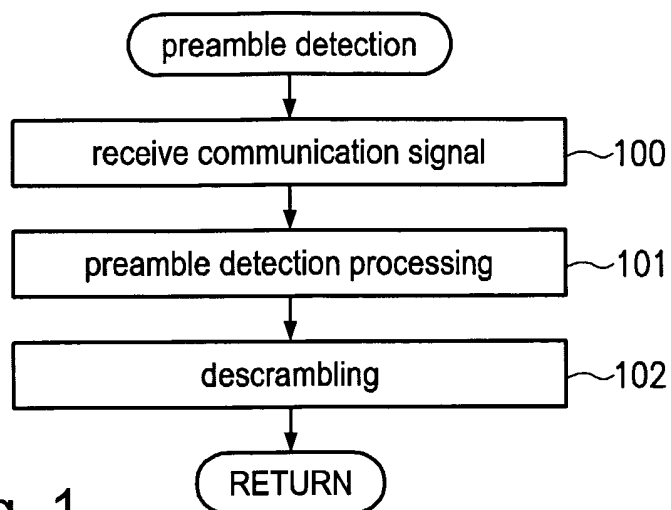


Fig. 1
(Prior Art)

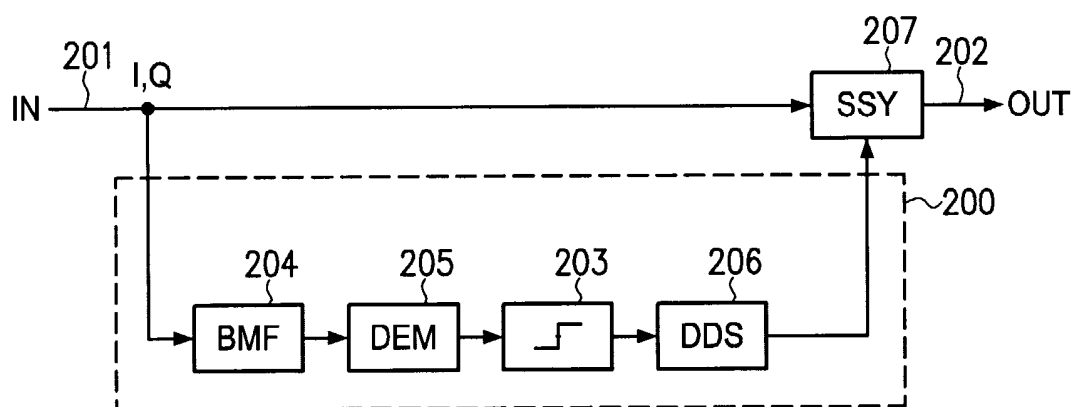


Fig. 2
(Prior Art)

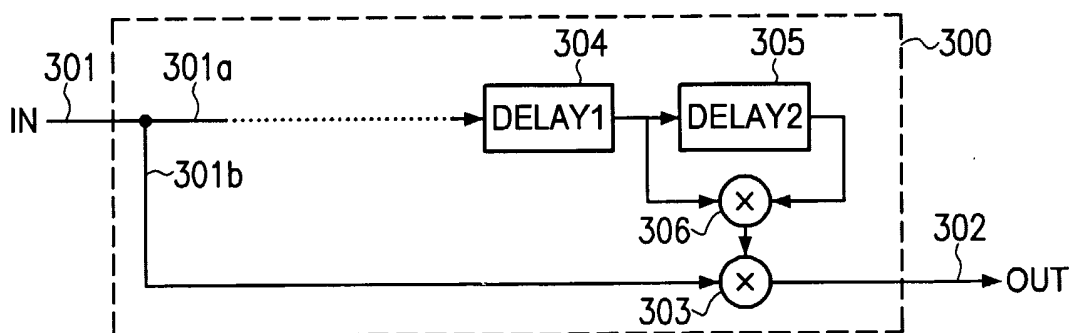


Fig. 3
(Prior Art)

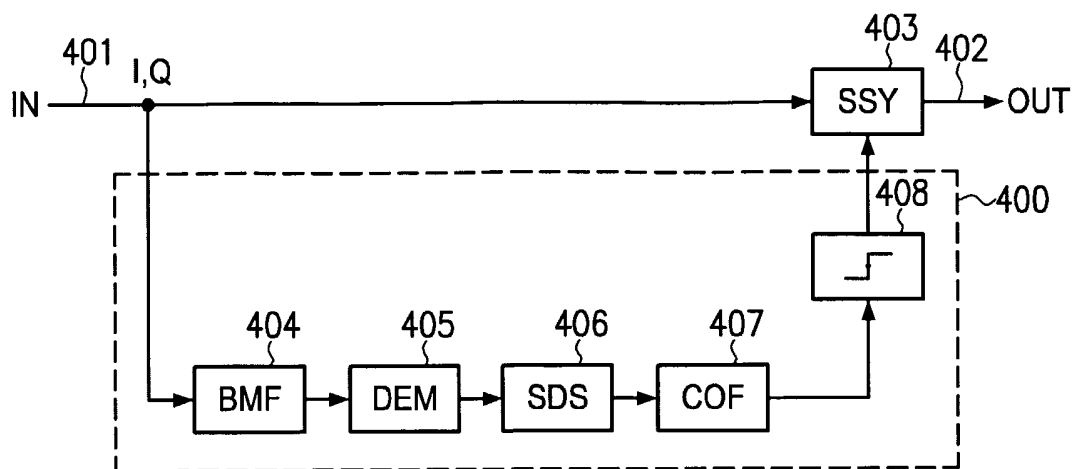


Fig. 4

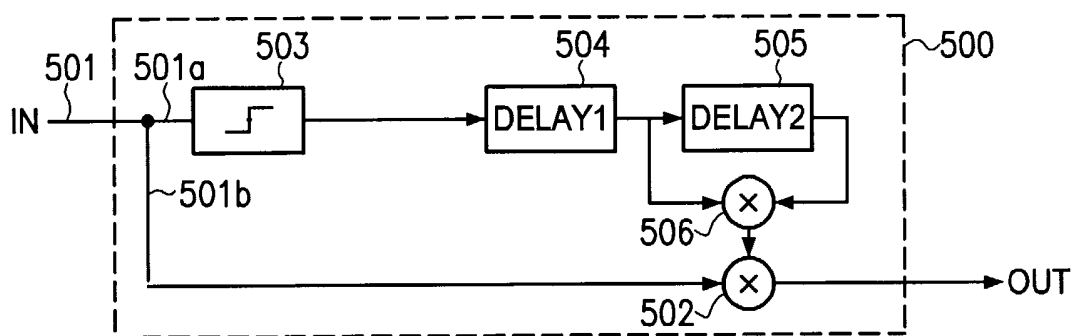


Fig. 5

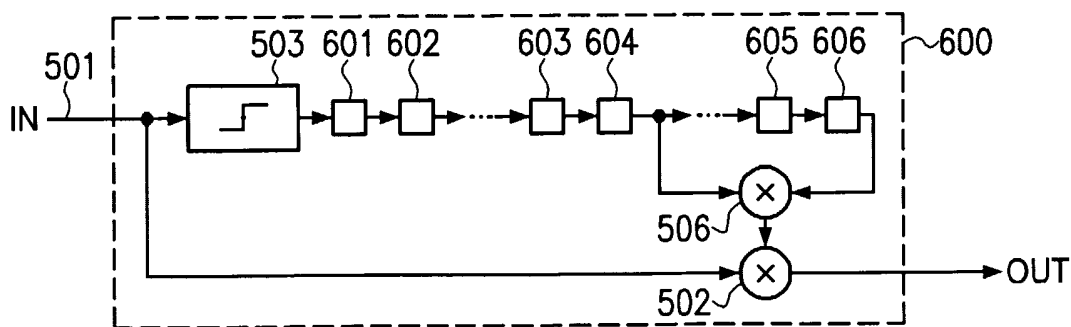


Fig. 6

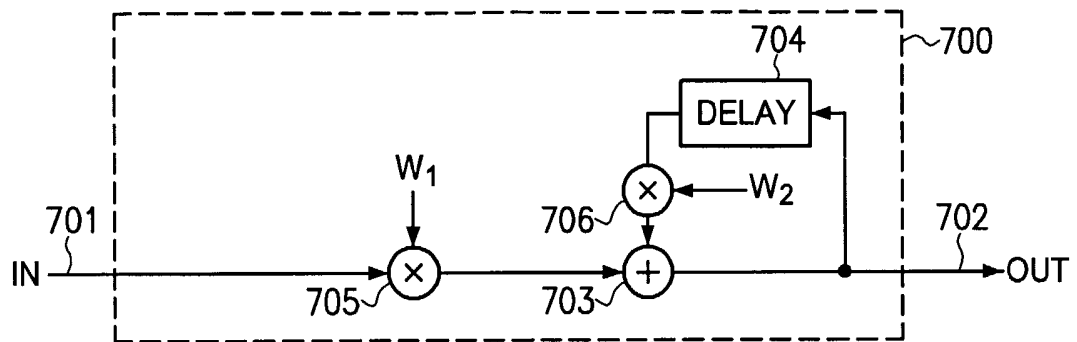


Fig. 7

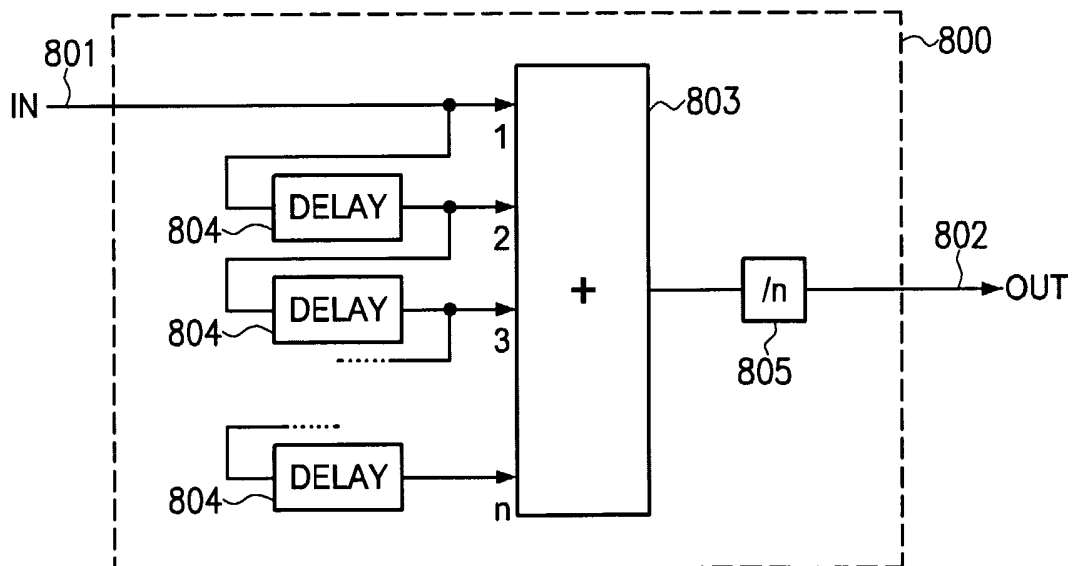


Fig. 8

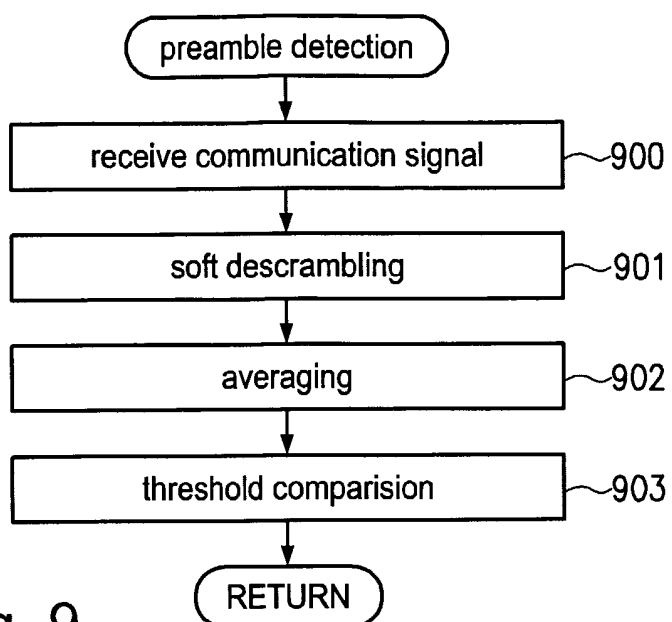


Fig. 9

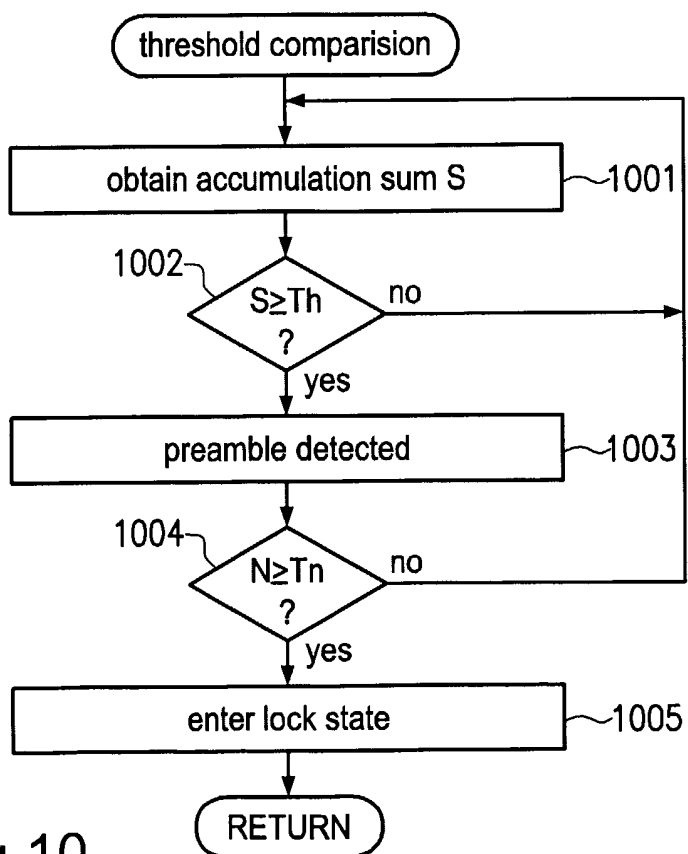


Fig.10

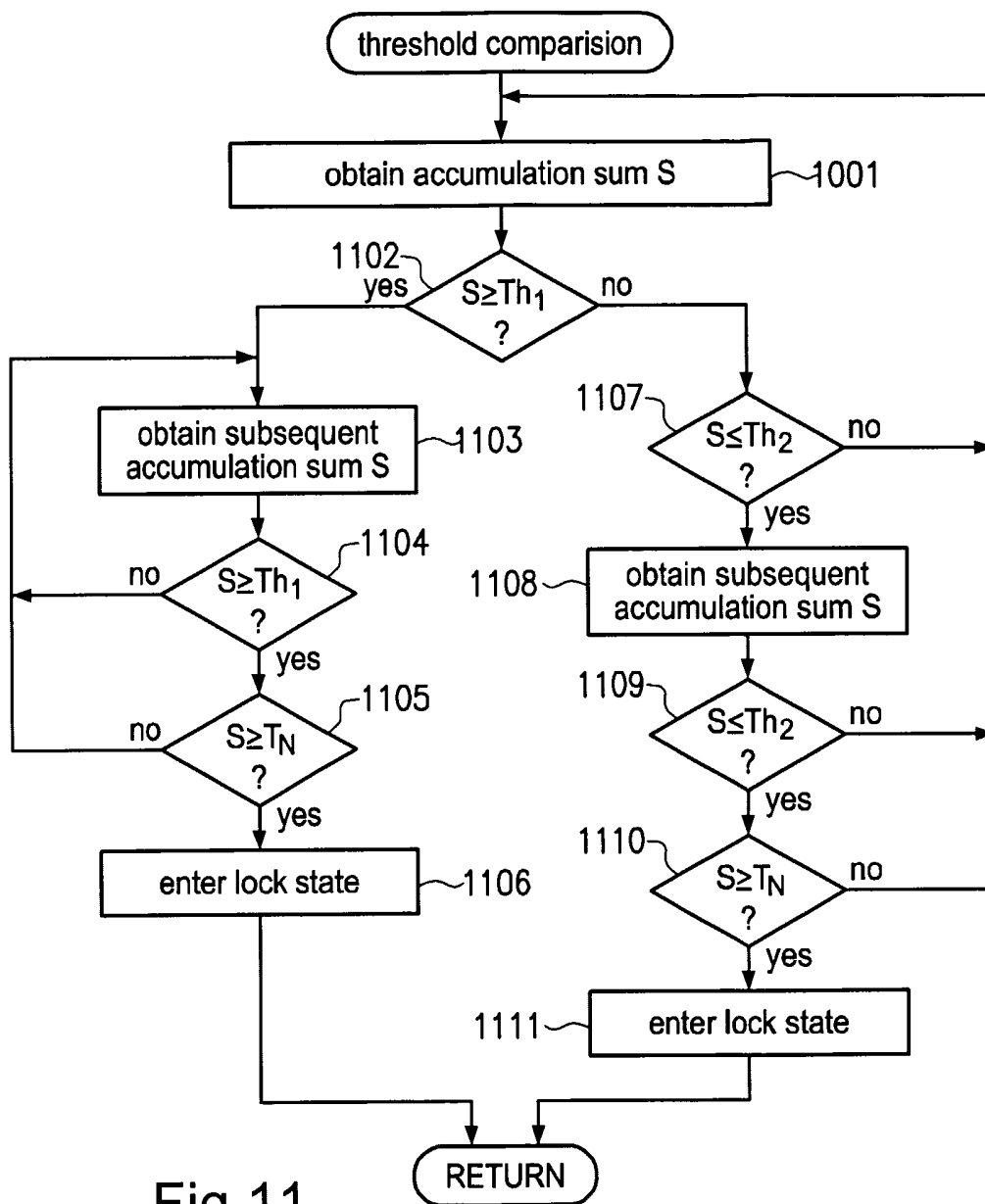


Fig.11

INTERNATIONAL SEARCH REPORT

 Internati pplication No
 PCT/US 03/06259

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 H04L7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR 2 493 646 A (THOMSON CSF) 7 May 1982 (1982-05-07) page 1, line 21 -page 3, line 21 page 4, line 1 -page 6, line 19; figure 1 ---	1-10
A	MIZOGUCHI M ET AL: "A fast burst synchronization scheme for OFDM" UNIVERSAL PERSONAL COMMUNICATIONS, 1998. ICUPC '98. IEEE 1998 INTERNATIONAL CONFERENCE ON FLORENCE, ITALY 5-9 OCT. 1998, NEW YORK, NY, USA, IEEE, US, 5 October 1998 (1998-10-05), pages 125-129, XP010314868 ISBN: 0-7803-5106-1 paragraphs '0III!', '00IV!; figures 2-7 --- -/--	1-10



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

19 June 2003

Date of mailing of the international search report

27/06/2003

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	"802.11b: Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Higher-Speed Physical Layer Extension in the 2.4GHz Band" IEEE STD 802.11B-1999, XX, XX, 1999, XP002240048 cited in the application paragraphs '18.2.3.8!-'18.2.4!; figure 132 -----	1

Initiation on patent family members

PCT/US 03/06259

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
FR 2493646	A	07-05-1982	FR 2493646 A1	07-05-1982