United States Patent

Budzynski et al.

[15] **3,665,401**

[45] **May 23, 1972**

[54] SWITCHING CIRCUITS AND METHOD FOR RESISTOR ELEMENTS IN CONDUCTOR SELECTION MATRICES

[72] Inventors: **Leonard M. Budzynski; Donald D. Leuck,** both of Toledo, Ohio

[73] Assignee: **Owens-Illinois Inc.**

[22] Filed: **Apr. 19, 1971**

[21] Appl. No.: **135,023**

[52] **U.S. Cl.** .....**340/166 R,** 315/169

[51] **Int. Cl.** **H04q 9/00**

[58] **Field of Search**.....340/166; 315/169

[56] **References Cited**

UNITED STATES PATENTS

3,555,511 1/1971 Filippazzi.....340/166

3,573,542 4/1971 Mayer et al.....315/169

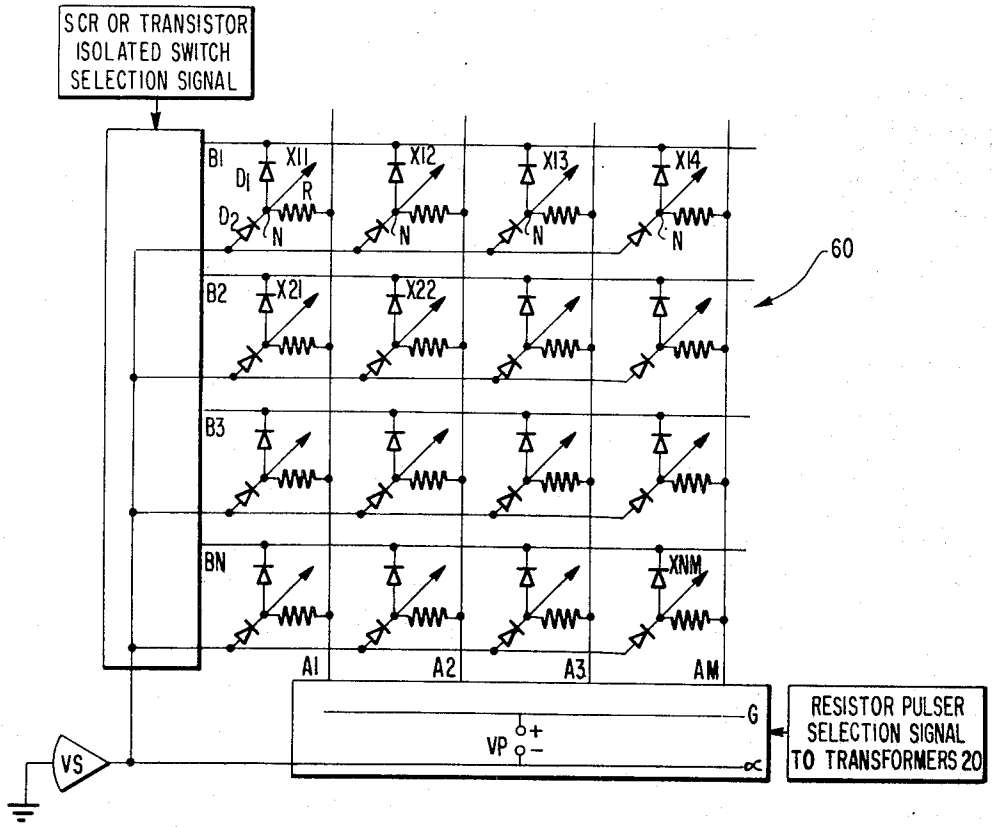
Primary Examiner—Donald J. Yusko

Attorney—Donald K. Wedding and E. J. Holler

[57] **ABSTRACT**

A gas discharge display and memory panel having parallel row and parallel column conductor arrays wherein the conductors in the arrays are connected to selection and addressing resistor-diode matrix circuitry having non-inductive switch means for rendering nodal points in said matrix effective to change a discharge condition at selected sites of the panel. An NPN transistor switch is used to connect a high voltage source to the resistors in the matrices to thereby pulse the nodal points. The circuits are reversible to accomodate negative and positive type pulses.

4 Claims, 9 Drawing Figures



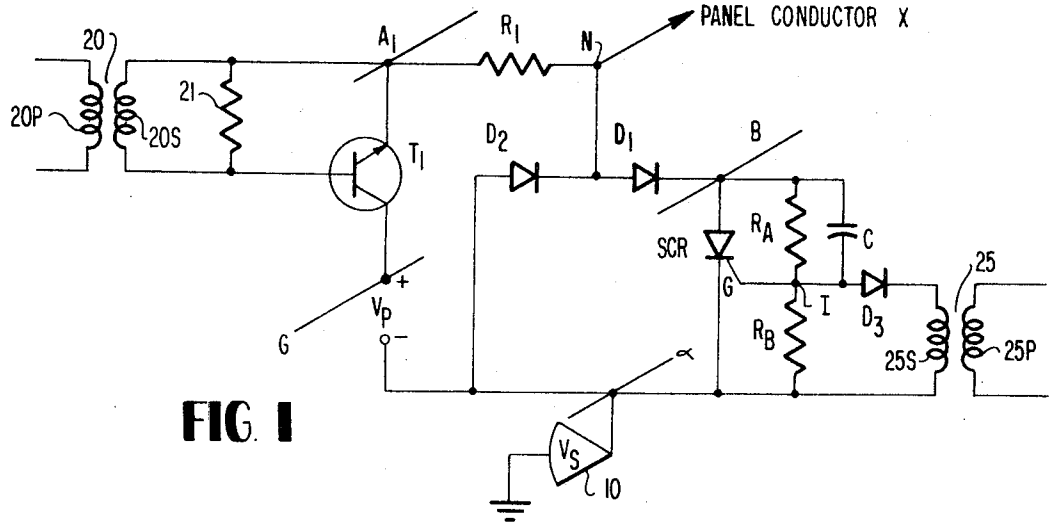


FIG. 1

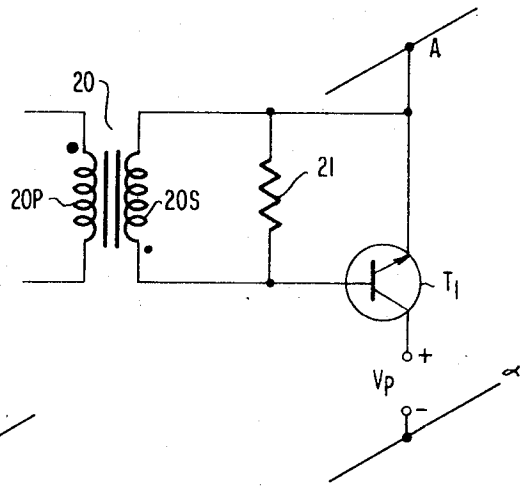
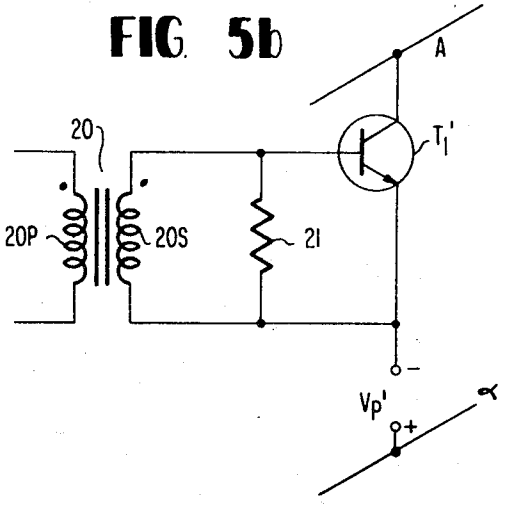


FIG. 5a

FIG. 5b



INVENTOR
DONALD D LUECK & LEONARD M BUDZYNSKI

BY Donald K. Wedding et
E. J. Holler

ATTORNEYS

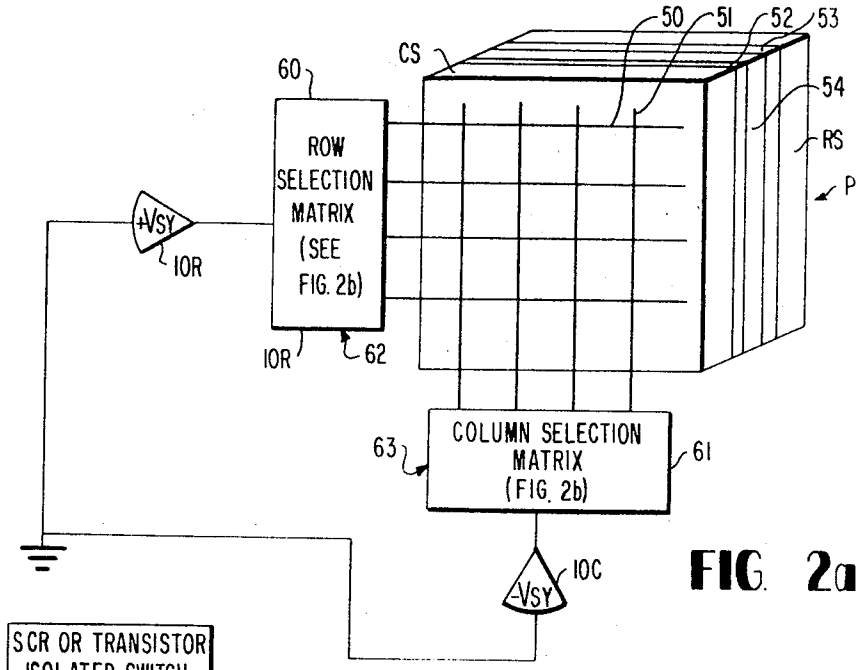

50
51
52
53
54
CS
60
ROW SELECTION MATRIX (SEE FIG. 2b)
RS
P
+VSY
IOR
IOR
62
63
COLUMN SELECTION MATRIX (FIG. 2b)
61
-VSY
IOC

FIG. 2a

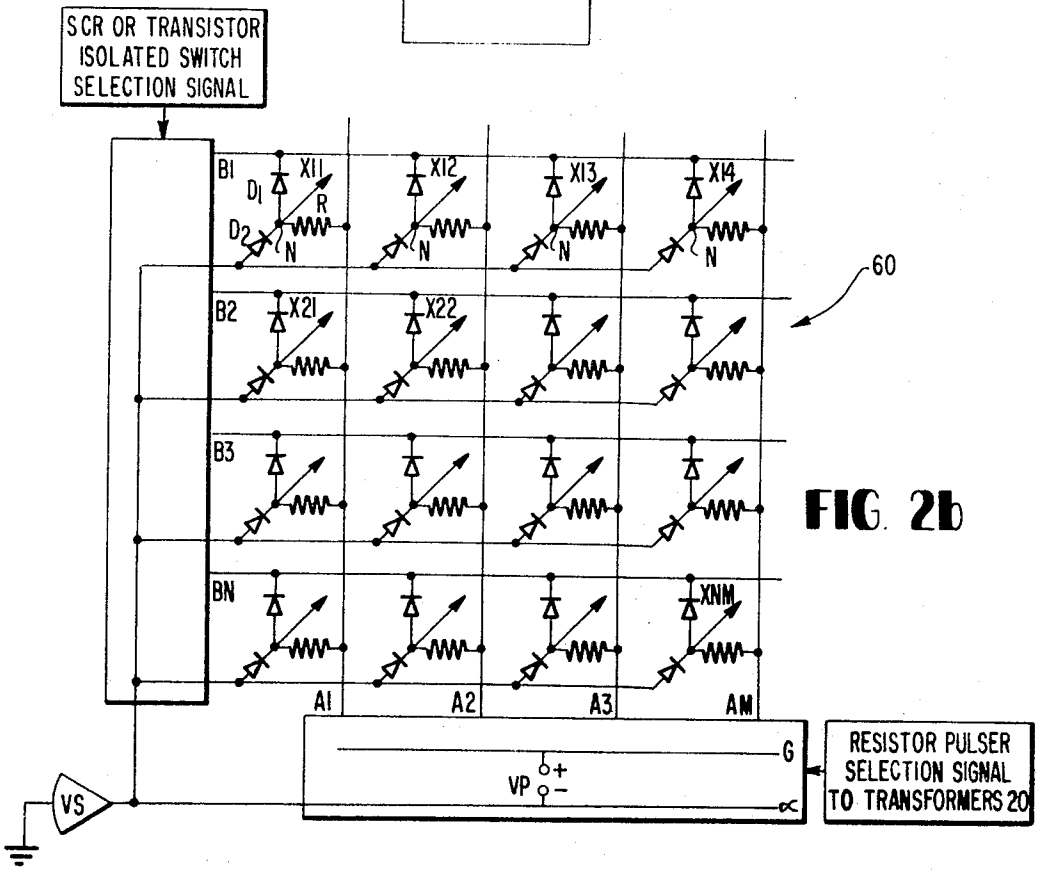

SCR OR TRANSISTOR ISOLATED SWITCH SELECTION SIGNAL
B1
D1
D2
R
N
X11
X12
X13
X14
60
B2
X21
X22
B3
BN
XNM
A1
A2
A3
AM
G
VP
VS
RESISTOR PULSER SELECTION SIGNAL TO TRANSFORMERS 20

FIG. 2b

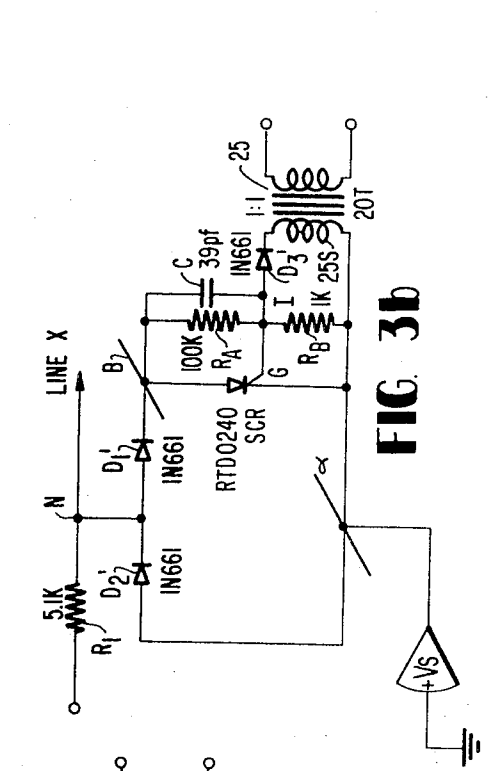


FIG. 3b

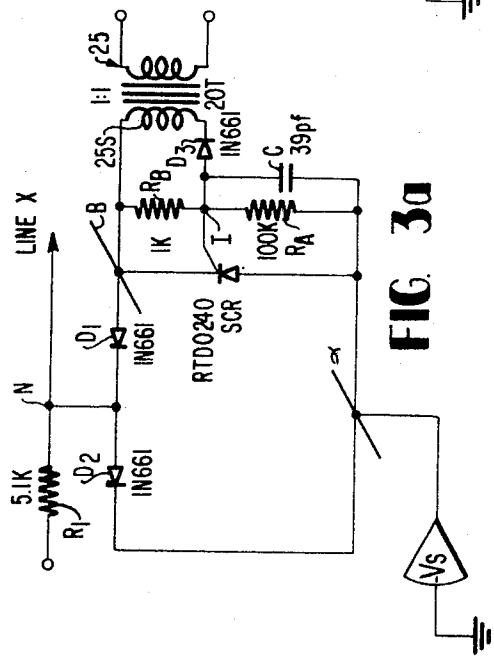


FIG. 3a

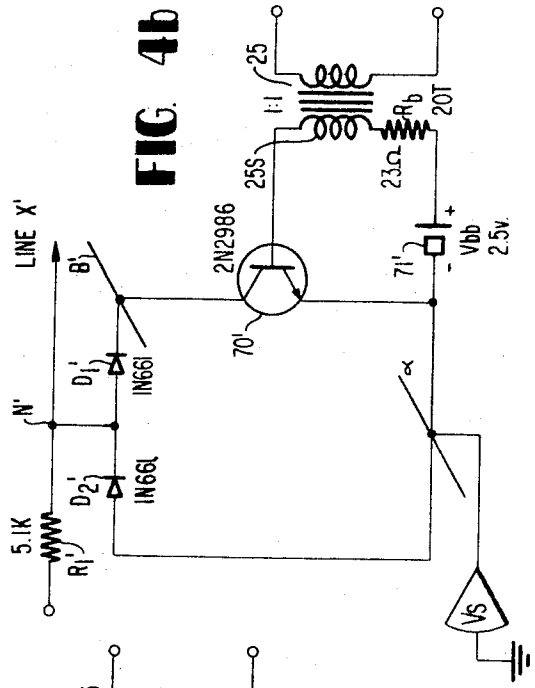


FIG. 4b

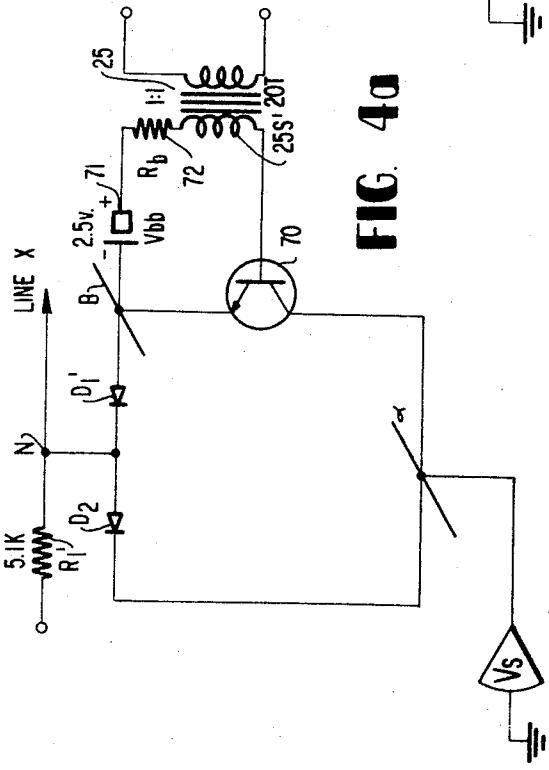


FIG. 4a

SWITCHING CIRCUITS AND METHOD FOR RESISTOR ELEMENTS IN CONDUCTOR SELECTION MATRICES

BACKGROUND OF THE INVENTION

The present invention relates to improvement in resistor pulsing circuits for matrices used to address conductors, particularly in gas discharge display and memory panels of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167, issued March 3, 1970, and Bitzer et al. U.S. Pat. No. 3,559,199. In the Baker et al. patent, there is disclosed a gas discharge display/memory device in which a pair of rectangular glass plate members are joined in spaced apart relation, the gas plate members carrying dielectrically coated multiple conductor arrays, with the row and column conductor arrays in the active panel area being comprised of linear conductors extending parallel to the long direction in the plates, respectively. The plates are joined by a spacer sealant with their long axes transverse to each other and with the conductor ends extending beyond the point where the plates are spacedly joined towards both edges of the plates, respectively.

This invention is directed towards improvements in resistor pulsing systems and circuits used in a diode-resistor multiplexed addressing matrix as disclosed in application Ser. No. 60,402, of William E. Johnson, filed Aug. 5, 1970, and entitled "Selection and Addressing Circuitry for Matrix Type Gas Display Panel", and application Ser. No. 62,015 of Larry S. Schmersal, filed Aug. 7, 1970 and entitled "Improvements in Gas Discharge Display Memory Panels and Selection and Addressing Circuits Therefor". In accordance with the present invention, the resistors in such selection circuits are not driven by a transformer winding, for example. An isolated, non-inductive switching circuit is provided in the form of an NPN transistor with a circuit for applying a small control signal to the base electrode of the transistor switch. These non-inductive switches are, in effect, isolated current switching devices so that the repetition rates are much faster, the power dissipation rates are better than prior art transformer circuits or active solid state pulsing circuits used in such matrix selection systems. Moreover, the circuits are reversible to accommodate negative and positive type pulsers circuits.

This invention removes the need for high voltage level transformers in addressing matrices for gas discharge panels in particular and makes use of a low-power transformer, or other logic isolation device, to control an isolated transistor switch. Thus, a transistor may be used in a floating matrix (floating relative to the sustainer for discharge panels) rather than having to insert a high-power transformer. This reduces to easily managable proportions, the requirements of core material and overall size as well as capacitances. Furthermore, the waveforms of the addressing pulses are free from problems of inductive kickback and transformer recovery.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages, and features of the invention will become more apparent from the following specification and drawings, wherein:

FIG. 1 illustrates basic diode-resistor address/selection circuitry or matrix element for a conductor in either of row or column conductor arrays as disclosed in the aforementioned Johnson patent Application Ser. No. 60,402.

FIG. 2A illustrates a system configuration wherein the group select diodes and bit select resistors are positioned on the left hand edge extension of a panel plate member for the row conductors and the sustainer bypass diodes are positioned on the right hand edge extension of the panel, and the column select diodes and the column select resistors are mounted on the upper plate edge extension along with the pulsing circuits, whereas the sustainer bypass diodes for the column conductors are on the lower plate extension as disclosed in the aforementioned Schmersal patent application Ser. No. 62,015; and FIG. 2B illustrates the selection matrix for a row or column conductor array or portions thereof, respectively;

FIG. 3A and FIG. 3B illustrate positive and negative SCR pulsers for the diodes in accordance with the invention;

FIG. 4A and FIG. 4B illustrate the positive and negative transistor pulses for the diodes in accordance with the invention;

FIG. 5A and 5B illustrate transistor pulser circuits for pulsing the matrix resistors in the selection matrices, respectively.

In FIG. 2A, the panel P is a display panel constituted by a row and column conductor support plates RS and CS respectively carrying row conductors **50** and and column conductors **51**, respectively. The conductors are coated with a dielectric or insulating coating or layer **52** and **53** respectively and the plates are joined in spaced relation by a spacer sealant **54** to form a thin gas chamber in which is placed a working or electroresponsive gas medium under pressure. It will be appreciated that other electrorespective mediums may be used, but the preferred embodiment disclosed herein uses a gas as the working medium between the transverse conductor arrays **50** and **51**, Selection signals are applied to the selection matrices as indicated by the input arrows **62** and **63** respectively, and may be from a computer, for example.

One or more row conductors are selected by row selection circuit **60** and one or more column conductors are selected by column selection circuit **61** each of which floats on the sustainer voltages from sources **10R** and **10C**, which are connected to a common ground reference. It will be appreciated that the illustrated positive and negative relationship may be reversed so that a positive sustainer source and selection matrix may be used for the column conductors and the opposite polarity sustainer and selection matrix used for the row conductors.

Referring now to FIG. **1**, the basic matrix circuit element is the same circuit as is disclosed in Johnson application Ser. No. 60,402, filed Aug. 3, 1970, and entitled "Selection and Addressing Circuitry for Matrix Type Gas Display Panel", and as shown, the entire selection and address system floats on the sustainer voltage wave form from sustainer voltage generator **10**, which may be square wave, sinusoidal, trapezoidal, or any other periodic wave form. As described in the aforementioned Johnson application, the voltage from sustainer generator **10** may constitute one-half of the sustaining voltage necessary to operate the panel, the remaining one-half at 180° phase or opposite polarity may be supplied to the other conductors in the opposite array. Thus, one-half the sustainer potential is applied to the row conductors and one-half the sustainer potential at 180° phase relationship, is applied to the column conductors for the panel.

Resistor R and diodes D1 and D2 constitute a matrix selection or multiplexing element having a nodal point N. There is one such element for each panel conductor line with the panel conductor lines being connected to their respective nodal points N (See FIG. 2B). The end of resistor R opposite from the nodal point N is adopted to have applied thereto a voltage pulse of magnitude which, combined with the sustainer potential, is effective to manipulate the discharge conditions of a discharge site in the panel P as located by a selected row conductor and a selected column conductor. Such a voltage is derived from a direct current voltage source VP which, in the embodiment shown in FIG. 1 has its positive output terminal connected, via bus conductor G, to the collector electrode of transistor T1 with the emitter electrode of transistor T1 connected essentially to a bus conductor A1, which in turn, connects to a plurality of resistor ends for selecting or pulsing groups of resistors. For example, as illustrated in FIG. 2B all of the resistors in the vertical first row of the vertical columns of the selection matrix are pulsed by bus A1, and in the second row by bus A2 and son on to the last resistor pulsing. The high voltage supply VP may be used as indicated to commonly serve all resistor pulsers. Transistors T1 are normally non-conductive and are rendered conductive by a pulse from resistor selection transformer coupler **20**, the voltage at the transformer secondary **20S** is developed across resistor **21** and applied to the base-emiter electrode of transistor T1 to thereby render this transistor conductive. Conduction of transistor T1 thereby apply the full potential from source +VP to the end of

resistor R1 and hence, in the absence of a low impedance at the nodal point, this potential appears or rises at nodal point N and is therefore applied to panel conductor X. As also illustrated, diode D1 is poled in such a direction that it presents a low impedance to the voltage from source VP.

In accordance with the present invention, a non-inductive switching device is provided in this path to present either a high impedance or a very low impedance to thereby permit the addition of the voltage appearing at nodal point N to the sustainer potential which is applied at a common point α in the circuit. It will be noted that the line is common to the anode electrodes of all of the diodes D2 for the purposes of accommodating the sustainer currents as disclosed more fully in the above mentioned Johnson patent application Ser. No. 60,402 and referenced in said Johnson application as a sustainer bypass diode.

A number of different types of circuits may be connected between bus lines B and common point α as is shown in FIGS. 3A, 3B, 4A and 4B, the circuit shown in FIG. 3B being the circuit shown in FIG. 1. In this case, a Silicon Controlled Rectifier (SCR) has its anode electrode connected to bus line B and its cathode electrode connected to the common point or line α. A turn on network includes voltage divider constituted by resistors RA and RB has its intermediate point I thereof connected to control the gate electrode G of the SCR. A speed-up capacitor C is connected in shunt with resistor RA.

When the potential at nodal point N begins to rise due to the conduction of transistor T1, this same voltage begins to rise at point (or conductor bus) B and is coupled through resistor RA and capactior C to the gate electrode G of the SCR. This small rise in potential is sufficient to trigger or gate on the SCR and permit a heavy conduction of current so that there is no further rise in potential at nodal point N and hence no rise in potential on the panel conductor X connected to nodal point N. However, for the purposes of preventing the voltage appearing at nodal point N from dropping to zero and hence not being applied to panel conductor connected thereto e.g. the selection of a particular conductor X, simultaneously with or just prior to (but not after) the conduction of transistor T1, a voltage pulse is applied to the gate electrode G of the SCR to thereby prevent it from conducting. Thus, since the SCR gate is back biased by this voltage pulse,, the voltage appearing at nodal point N is applied to the panel conductor. It will be appreciated, as was indicated above, that the voltage appearing at point N at this time is added to the voltage from sustaining generator **10**. The selection signal from the block labeled "SCR or transistor isolated switch selection signal" is applied to transformer **25**, diode D3 in series with secondary winding **25S** blocks spurious polarity signals from the gate electrode of the SCR.

It will be apparent that all other diodes D1 which have their cathode electrodes connected to bus line B will be similarly back biased and hence, in the event their resistors R1 have been pulsed in a manner described earlier herein, such nodal points will also then be raised in potential in accordance with the sum of the voltage VP and the voltages from the sustaining generator **10** in that time interval. Although not shown, sustaining generators VS could have their potentials controlled in synchronism with the application of pulsing potentials to transistors T1 and SCR.

Except for polarity considerations, the circuit illustrated in FIG. 3A, is identical in all respects to the circuit shown in FIG. 3B. Note that the diodes D1 and D2 have been reversed and in this instance, the anode electrode of the SCR is connected to the common point or bus whereas the cathode electrode thereof is connected to the anode of the diode D1. Representative component values and types are shown in FIGS. 3A and 3B; it being understood that this is by way of illustration and not limitation.

Although the preferred embodiment of the non-inductive isolated switching circuits are shown in FIGS. 3A and 3B, instead of SCR type switches, transistors may be used as is shown in FIGS. 4A and 4B. FIG. 4A illustrates a negative pulse transistor pulser and FIG. 4B illustrates a positive pulse transistor pulser. In FIG. 4A, transistor switch **70** has its emitter connected to the anode of diode D and its collector connected to common point or bus α. A bias source **71** (VBB) is required in order to normally bias this transistor on or conductive, such bias potential being applied via the secondary **25S'** of selection transformer **25** and a small current limiting resistor **72**. In order to select line or bus B in this embodiment, a pulse voltage induced in the secondary winding **25S**, as in the embodiment of FIG. 3A is used to overcome the bias voltage **71** and render transistor switch **70** non-conductive and thereby present a high impedance at bus line B and all diodes D1 connected thereto, which in turn permits the potential at any corresponding nodal point to be applied to the panel conductor line connected thereto.

It will be noted that as in the case of the SCR circuits, the transistor circuits are likewise reversible, thus permitting the use of the NPN transistors. Moreover, both circuit types act as isolated switches. The positive and negative resistor pulsing circuits shown in FIGS. 5A and 5B are substantially identical, it being noted that the transistors in both circuits are NPN types but can be PNP types as well as mixes in complementary circuit arrangements to make the negative and positive pulsers symmetrical. The transformers, however, have their secondaries wound or connected so as to supply or have induced therein proper polarity pulse signals for application to the base circuits of the transistors to render same conductive for the time intervals of said pulse signals.

The invention is not to be limited to the exact form shown in the embodiment disclosed herein as a number of obvious changes may be made and be within the scope of the following claims:

WHAT IS CLAIMED IS:

1. In a system for supplying operating potentials to a load device having row and column conductor arrays, including a first selection matrix for selecting the row conductors and a second selection matrix for selecting the column conductor, each said selection matrix including a plurality of multiplexing elements, each multiplexing element having a common nodal point connected to a conductor in one of said arrays and at least three electrical paths to said nodal point, there being a resistive impedance element in one of said paths, and means for applying a pulse potential between the end of said impedance element remote from said nodal point and a common point, a undirectioned conducting device in each of the other paths of said multiplexing element, one of said undirectional conducting devices being connected directly between said nodal point and said common point, a non-inductive switching device between the end of said other unidirectional conducting device and said common point, and circuit means for applying a switching signal to said non-inductive switching device to cause same to exhibit a high impedance during the time of said switching signal, the improvement in each said means for applying a pulse potential between said resistive impedance element and said common point, respectively, comprising a direct current voltage source, means connecting one terminal of said direct current voltage source to said common point, a normally non-conductive transistor having its collector-emitter circuit connected between the other terminal of said direct current voltage source and said remote end of said resistive impedance element, and means for selectively supplying a pulse voltage to the base of said transistor to render same conductive.

2. The invention defined in claim 1 wherein the transistors for pulsing the row conductor matrix resistors are of the same type as the transistors for pulsing the column conductor matrix resistors.

3. The invention defined in claim 2 wherein said transistors are of the NPN type.

4. The invention defined in claim 2 wherein each said means for selectively supplying a pulse voltage to the base of a transistor includes a low-power signalling transformer, having secondary windings connected between base and emitter electrodes of said transistors.

* * * * *