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- [54] **METHOD OF MAKING A CHIP CARRIER WITH TERMINATING RESISTIVE ELEMENTS**
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- [22] Filed: **Dec. 11, 1991**

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Reissue of:

- [64] Patent No.: **4,949,453**
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- Appl. No.: **366,604**
- Filed: **Jun. 15, 1989**

- [51] Int. Cl.⁵ **H01C 17/06**
- [52] U.S. Cl. **29/620; 29/846;**
29/847; 427/101; 361/765
- [58] Field of Search 29/620, 846, 847, 850;
361/400, 402, 421; 174/260; 357/70, 80;
427/101; 437/180

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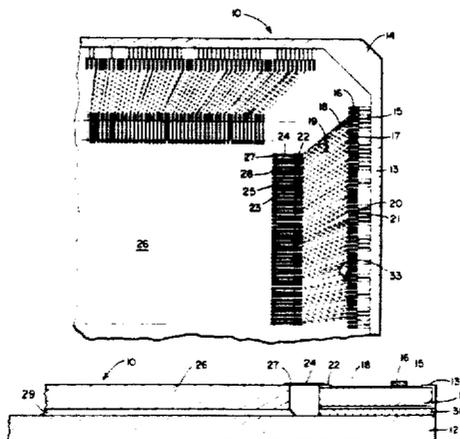
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ABSTRACT

[57] A generic chip carrier is described which includes, as integral parts, a voltage bus and a plurality of terminating resistors connected between the voltage bus and signal traces on the carrier. The voltage bus wraps around the chip carrier, thus providing a large area of metal. Through the selective use of the terminating resistors, the generic carrier can be customized for a particular type of integrated circuit, i.e., source or destination termination of signals. A signal trace may be customized by "opening" the terminating resistor with a current spike applied by a standard electrical probe. Spare bonding pads and terminating resistors are placed at intervals about the periphery of the carrier as insurance against defective or mistakenly removed terminating resistors.

6 Claims, 3 Drawing Sheets



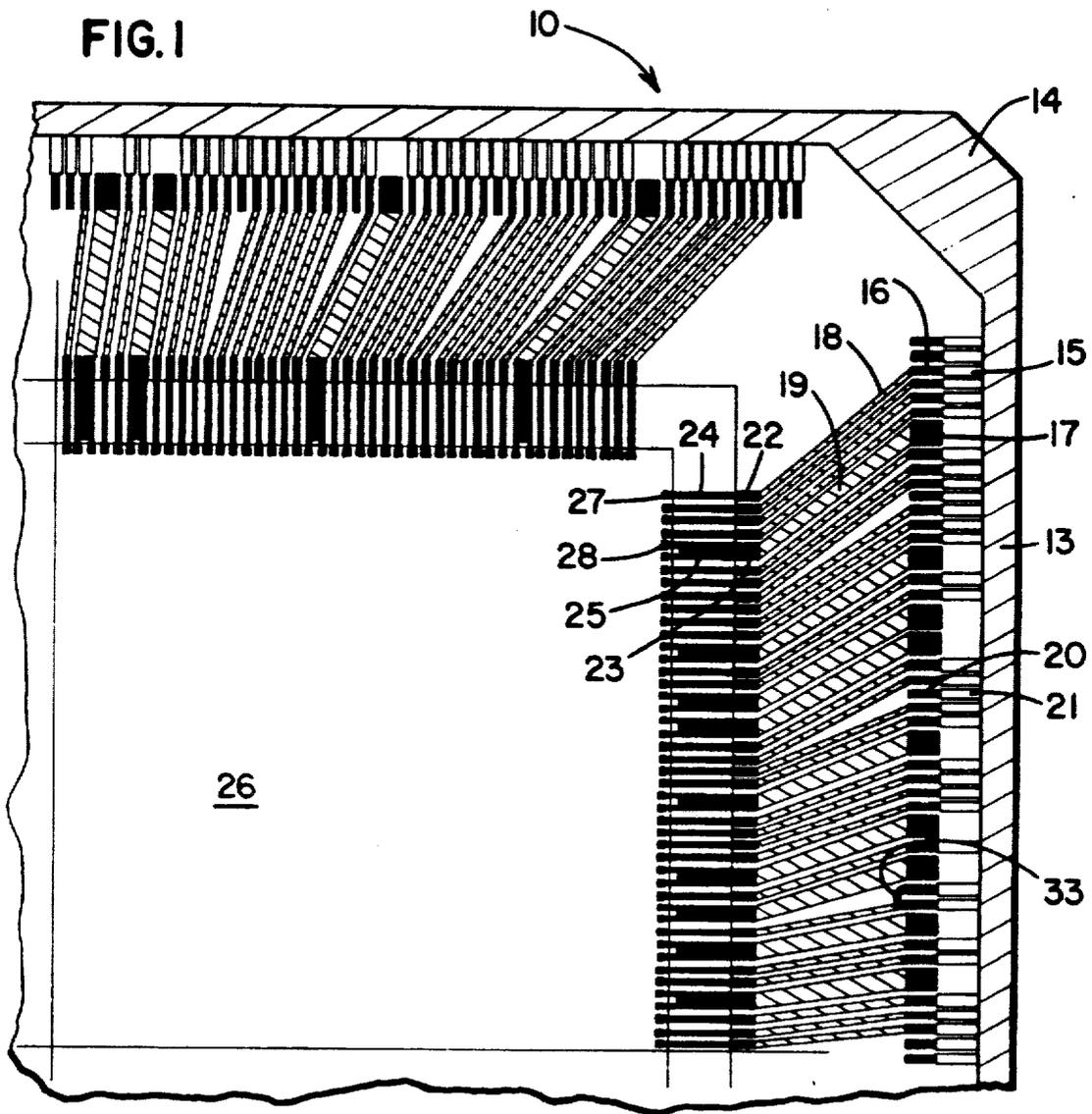


FIG.2

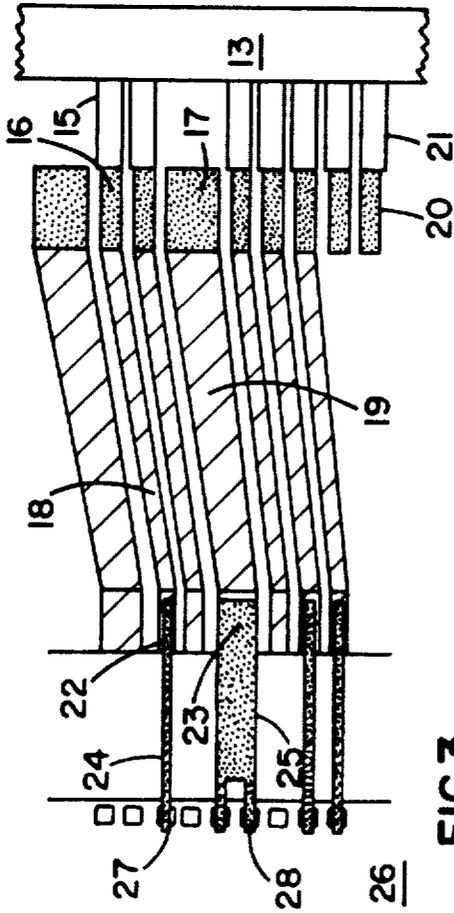
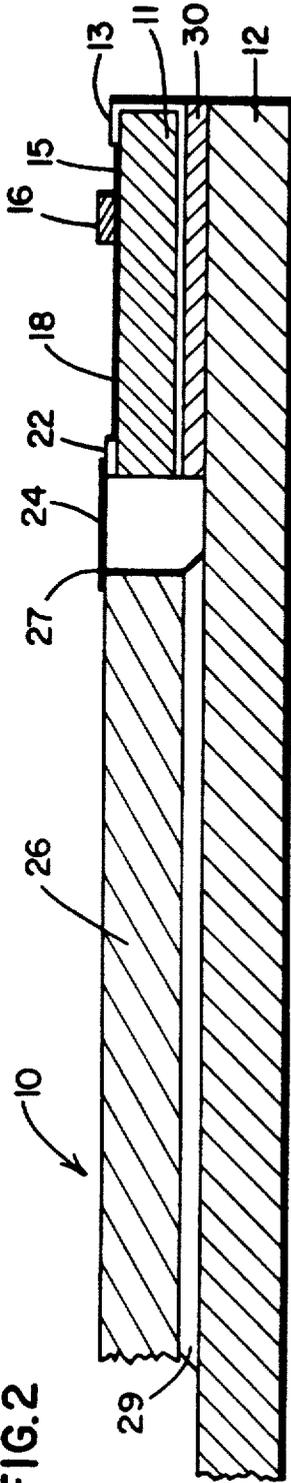
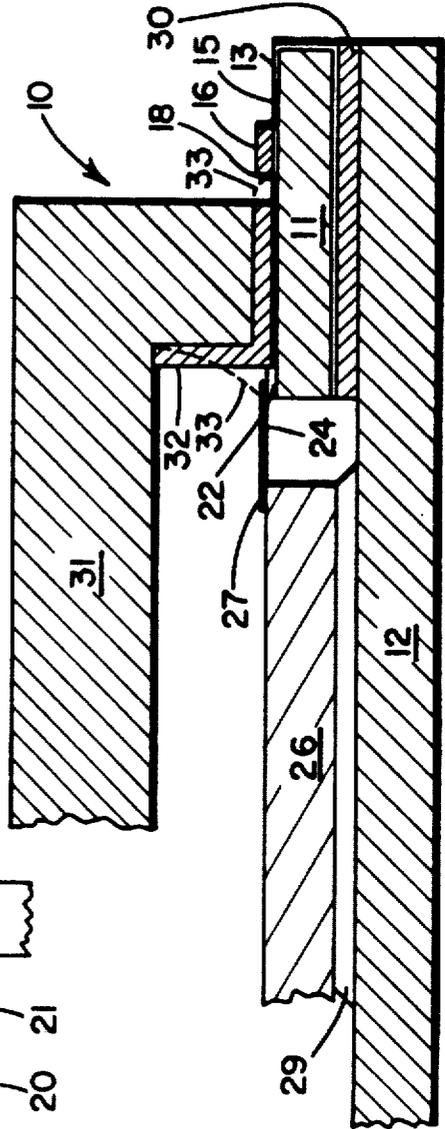


FIG.3

FIG.4



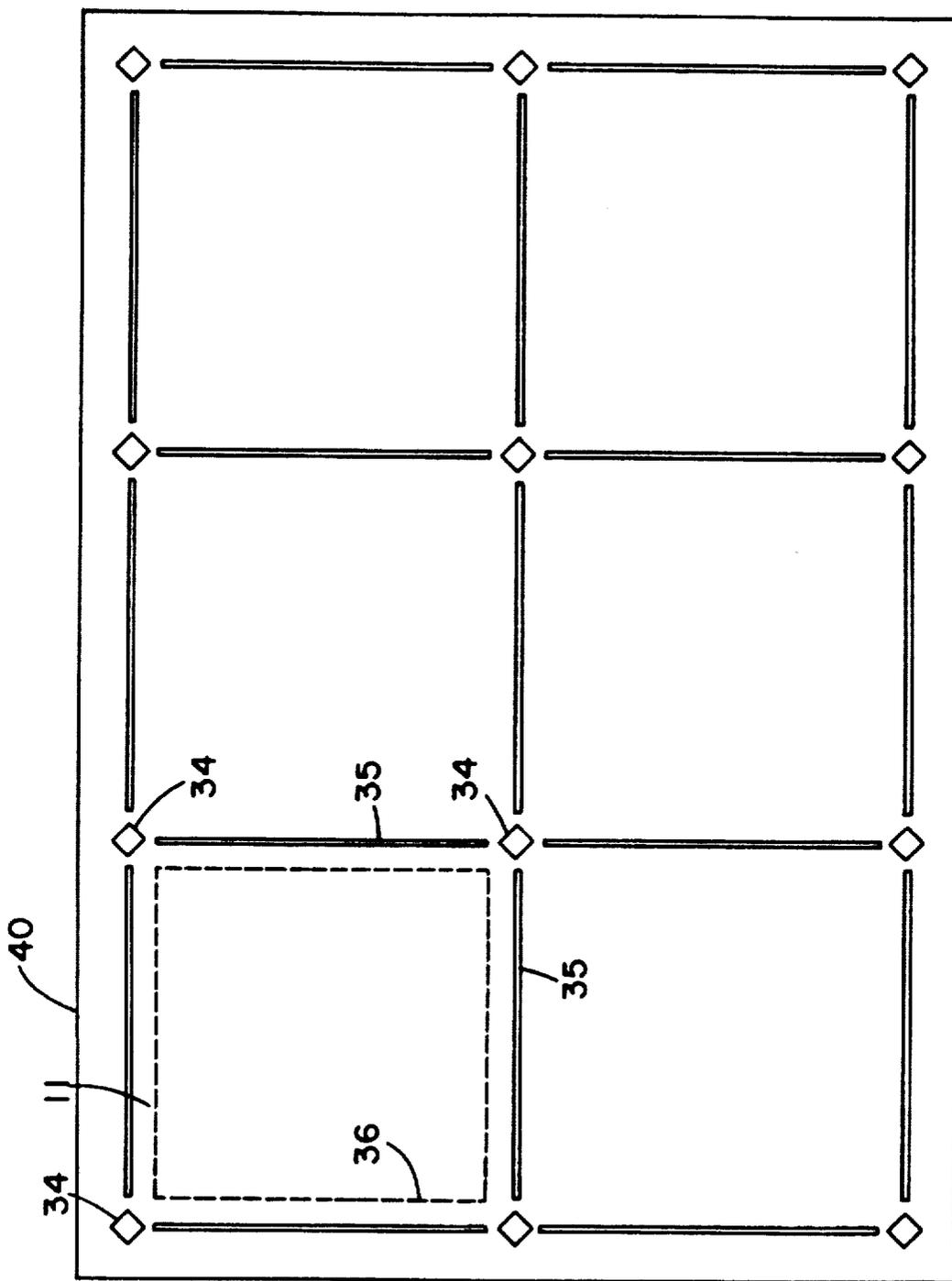


FIG.5

METHOD OF MAKING A CHIP CARRIER WITH TERMINATING RESISTIVE ELEMENTS

Matter enclosed in heavy brackets [] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

This application is a reissue of Ser. No. 07/366,604, filed Jun. 15, 1989, now U.S. Pat. No. 4,949,453.

FIELD OF THE INVENTION

This invention relates generally to a method of fabricating integrated circuit carriers. In particular, it is directed to a generic integrated circuit carrier which contains resistive elements that selectively perform source or destination termination.

BACKGROUND OF THE INVENTION

At high frequency communication rates, conductive paths such as coaxial wire, twisted pair wire, and circuit board traces, take on a characteristic impedance which must be matched with either source or destination termination resistors to ensure minimal signal reflection. In high speed supercomputers, such as the type manufactured by Cray Research, Inc., the Assignee of the present invention, nearly all conductive paths require such source or destination termination. A significant problem with source or destination termination is that a large portion of the circuit board surface is taken up by resistor components.

In high speed supercomputers, nearly all available space on circuit boards must be given over to logic elements. To maximize speed, the length of conductive paths between logic elements must be short to minimize signal propagation delay. Therefore, integrated circuits must be mounted close together on circuit boards. In the prior art, terminating resistor components are wasteful of circuit board space. Thus, there is a need for integrated circuit packages which contain, as an integral component, terminating resistors of either the source or destination type. The inclusion of terminating resistors must not increase the overall size of the integrated circuit package. Minimizing the "footprint" of each integrated circuit on a circuit board remains a primary goal.

SUMMARY OF THE INVENTION

The present invention solves the aforementioned problems in the prior art and has other advantages which will be readily recognizable by those skilled in the art. One object of the present invention is to provide a method of fabricating generic chip carriers such that its conductive paths may be customized by the selective use of terminating resistors that are an integral part of the carrier. Another object of the present invention is to minimize the footprints of the carrier and associated circuit board by including terminating resistors within the carrier rather than mounting the resistors as separate devices on a circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, where like numerals refer to like elements throughout the several views,

FIG. 1 is a top-down view of the upper right quadrant of an integrated circuit seated in a carrier accord-

ing to the preferred embodiment of the present invention;

FIG. 2 is a cross-sectional side view of the integrated circuit bonded to the carrier;

FIG. 3 is an enlarged view of the conductive paths between the integrated circuit and the carrier;

FIG. 4 is a cross-sectional side view of the integrated circuit bonded to the carrier and hermetically sealed by the carrier lid; and

FIG. 5 shows the blank ceramic substrate prior to the metallization process that creates a wraparound voltage bus.

DETAIL DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following Detailed Description of the Preferred Embodiment, reference is made to the accompanying Drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized without departing from the scope of the present invention.

FIG. 1 is a top-down view of the upper right quadrant of an integrated circuit 26 seated in a carrier 10, according to the present invention. In a preferred use of the present invention 10, the integrated circuit 26 is an ECL gate array seated in the center of the carrier 10. The outer periphery of the integrated circuit 26 is lined with bonding pads 27 and 28. Bonding pads 27 are used for signal paths; bonding pads 28 are used for voltage supply paths. Tape Automated Bonding (TAB) traces 24 and 25 electrically connect bonding pads 27 and 28 on the integrated circuit 26 to bonding pads 22 and 23 lining the inner periphery of the carrier 10. Inner bonding pads 22 are used for signal paths; inner bonding pads 23 are used for voltage supply paths. From the inner bonding pads 22 and 23, the electrical connections are brought out by traces 18 and 19 to outer bonding pads 16 and 17 lining the outer periphery of the carrier 10. Outer bonding pads 16 are used for signal paths; outer bonding pads 17 are used for voltage supply paths. The outer bonding pads 16 and 17 are larger and less densely packed than the inner bonding pads 22 and 23, because they connect, by Tape Automated Bonding (TAB) means, to large, bulky, electrical traces on a printed circuit board (not shown). The electrical traces on integrated circuits and their carriers, on the other hand, are usually very small and densely packed. Thus, the traces 18 and 19 fan-out from inner bonding pads 22 and 23 to outer bonding pads 16 and 17 to facilitate electrical connection between the integrated circuit 26 and a printed circuit board.

In the preferred embodiment of the chip carrier 10, a "wraparound" voltage bus 13 is formed as an integral part of the carrier 10. A large area 14 of the voltage bus 13 is exposed in the upper right hand corner of FIG. 1. This exposed area 14 permits connection between the voltage bus 13 and a voltage bus on a printed circuit board. The beveled corner area 14 provides a large, low impedance, bonding pad for connecting the voltage bus 13 on the carrier 10 to a voltage bus on the printed circuit board. A terminating resistive element 15 electrically connects an outer bonding pad 16 on the carrier 10 to the voltage bus 13. The "wraparound" feature of the voltage bus 13 is provided to facilitate additional and/or continuous connection between the voltage bus on the printed circuit board, and the voltage bus 13 on the chip

carrier 10, thereby reducing the inductance of the connective path.

The outer bonding pads 17 are not connected to terminating resistive elements 15. The outer bonding pads 17 are dedicated to voltage supply paths. In the preferred embodiment, regardless of chip type, these outer bonding pads 17 and traces 19 must always be used for the supply voltages. The remaining outer bonding pads 16 can be used for any input or output signal. Thus, the present invention provides a generic carrier 10 in which many types of integrated circuits can be placed.

By selective use of the terminating resistors 15, the generic carrier 10 can be customized for a particular type of integrated circuit. For example, the generic carrier 10 can be used for integrated circuits which require destination termination for their input signals. Those skilled in the art will recognize that source termination could be substituted for destination termination. In destination termination only, every input signal is terminated by a resistor; output signals are not terminated. To customize the generic carrier 10, the resistive elements 15 are removed from signals that do not require them. An electrical probe could be used to "open" the resistive elements 15, by means of a large current spike caused to flow between the voltage bus 13 and the bonding pad 16. Alternatively, a laser could be used to open the resistive elements 15.

Spare outer bonding pads 20 and terminating resistive elements 21 are placed at intervals about the periphery of carrier 10. These spares provide some security in case one of the outer bonding pads 16 or resistive elements 15 becomes defective, either because of fabrication problems or because of mistaken removal. In the preferred embodiment, the spare outer bonding pads 20 and resistive elements 21 are placed at intervals of every eight outer bonding pads 16 and 17. Alternative embodiments could choose different intervals. A jumper TAB trace or wire bond 33 can be used to connect the spare outer bonding pad 20 to the desired outer bonding pad 16 or, alternatively, an inner bonding pad 22.

FIG. 2 is a side view of a portion of the carrier 10. Referring to both FIGS. 1 and 2, the carrier 10 in the preferred embodiment is fabricated from two layers of ceramic. A flat, substantially square, ceramic substrate 12 provides a base for a second ceramic substrate 11. The second substrate 11 is shaped to define a central aperture or cavity for receiving the integrated circuit 26. The upper substrate 11 is bonded to the base substrate 12 by a 5 mil thick glass seal 30. The integrated circuit 26 rests on the base substrate 12 and is bonded thereto by means of die bonding adhesive 29. The pads 16, 17, 20, 22, and 23, reside on the surface of the upper substrate 11, and are comprised of conductive bumps. These conductive bumps are built up by sputter-depositing, photolithography, and electroplating as described herein later. Resistive elements 15, made of tantalum nitride or other resistive materials well known to those skilled in the art, are deposited on the upper substrate 11 using thin film techniques and connect the outer bonding pads 16 to the voltage bus 13. Signal traces 18 are deposited on the upper substrate 11 using thin film techniques and connect the outer bonding pads 16 to the inner bonding pads 22. Supply voltage traces 19 are deposited on the upper substrate 11 using thin film techniques and connect the outer bonding pads 17 to the inner bonding pads 23. The TAB traces 24 form conductive paths which span the open space between the integrated circuit 26 and the inner edge of the upper

substrate 11, thereby connecting the inner bonding pads 22 to the bonding pads 27 on the integrated circuit 26. The TAB traces 25 also form conductive paths which span the open space between the integrated circuit 26 and the inner edge of the upper substrate 11, thereby connecting the inner bonding pads 23 to the bonding pads 28 on the integrated circuit 26. Those skilled in the art will readily recognize that wire bonds may be substituted for the TAB traces 24 or 25.

FIG. 2 also illustrates the geometry of the wrap-around voltage bus 13. By wrapping the voltage bus 13 around the upper substrate 11, a larger area of metal is available. This large area of metal provides a low impedance voltage bus for the terminating resistors 15, thereby sinking or supplying a large amount of current for the integrated circuit 26 during plural termination of signals.

When a large number of signals require termination, it is important that a sufficient number of electrons be close by on a low impedance voltage bus or ground bus. Otherwise, during plural termination, the local area may be swamped or depleted of electrons. This in turn causes a change in the termination ability of the resistive elements 15, which could result in unwanted reflections on the signal paths. In high-density ECL circuits, these factors become important in terms of timing and noise problems. As the termination voltage shifts, timing delays or errors can occur. In addition, noise problems abound. Often times intermittent faults will result from sequences that are data-dependent and cannot be easily re-created due to insufficient termination on signal paths.

FIG. 3 is an enlarged view of the critical elements discussed in FIG. 1. The bonding pads 27 and 28 on the integrated circuit 26 are typically 2 mils square with conductive bumps of slightly smaller dimensions built upon the pads to facilitate TAB bonding. The bonding pads 27 and 28 are typically placed on a 4 mil pitch. The bonding pads 27 are connected to the inner bonding pads 22 by 2 mil wide TAB traces 24. The bonding pads 28 are connected to the inner bonding pads 23 by 6 mil wide TAB traces 25.

The inner bonding pads 22 are substantially rectangular, measuring 3 mils by 11 mils with a gold bump 1 mil high thereon. The runner bonding pads 22 are separated from adjacent pads by a distance of 1.5 mils. The inner bonding pads 22 are connected to the outer bonding pads 16 by 2 mil wide traces 18.

The inner bonding pads 23 are substantially rectangular, measuring 7.5 mils by 10 mils with a gold bump 1 mil high thereon. The inner bonding pads 23 are separated from adjacent pads by a distance of 1.5 mils. The inner bonding pads 23 are connected to the outer bonding pads 17 by 6 mil wide traces 19.

The traces 18 and 19 are tapered to fan-out from the width dimension of the inner bonding pads 22 and inner 23 to the width dimension of the outer bonding pads 16 and 17, respectively.

The outer bonding pads 16 and 20 are substantially rectangular, measuring 3 mils by 11 mils with a gold bump 1 mil high thereon. The outer bonding pads 16 and 20 are separated from adjacent pads by a distance of 1.5 mils.

The outer bonding pads 17 are substantially rectangular, measuring 7.5 mils by 10 mils with a gold bump 1 mil high thereon. The outer bonding pads 17 are separated from adjacent pads by a distance of 1.5 mils.

The resistive elements 15 and 21 are substantially rectangular, measuring 3.5 mils by 12 mils long, as measured along the inner-to-outer periphery axis.

In FIG. 4, a lid 31 is shown hermetically sealed to the upper substrate 11 by a glass seal 33 which starts out as a glass frit 32 before heating. The glass frit 32 is initially bonded to the bottom lip and inside wall of the lid 31. The glass frit 32 extends horizontally over the traces 18 and 19 and vertically abuts the inner bonding pads 22 and 23. When the glass frit 32 is heated, it flows downward over the inner bonding pads 22 and 23 to form the glass seal 33. The flow of glass is indicated generally by the dotted lines labeled with reference number 33. The resulting vertical seal 33 is thin at the top and broad at the base. Those skilled in the art will recognize that non-hermetic sealing may be used, such as an epoxy seal or a "glob-top" adhesive.

FIG. 5 is a top view of the upper substrate 11 of the carrier 10 prior to fabrication. The fabrication process of the carrier 10 begins with a sheet 40 of blank "green" (unfired) ceramic material. Diamond-shaped holes 34 and elongated, rectangular holes 35 are punched into the soft "green" ceramic sheet 40. The diamond-shaped holes define the beveled corners of the upper substrate 11, discussed herein before in conjunction with FIG. 1. The elongated, rectangular holes 35 define the edges of the upper substrate 11. In an alternative embodiment, the edges could be defined by a plurality of smaller and more numerous segments.

After the "green" ceramic sheet 40 is fired, the metallization of the pads, traces, resistive elements, and voltage bus is performed. Those skilled in the art will recognize that a number of techniques could be used to deposit these elements on the ceramic sheet 40, including electroplating, sputtering, or electroless plating.

In the preferred embodiment, the fired ceramic sheet 40 is first coated with a base metal by sputter-depositing means. The base metal coats the top and bottom surfaces of the fired ceramic sheet 40. The base metal also coats through the holes 34 and 35 of the fired ceramic sheet 40. This provides one uniform, electrically conductive, voltage bus 13 across all surfaces of the ceramic sheet 40. Sputter-depositing the base metal provides a strong bond between the base metal and the ceramic sheet 40.

A photoresist is placed over the coated ceramic sheet 40, a mask is placed over the uncured photoresist, and the photoresist is exposed to light. Those skilled in the art will readily recognize that a positive or negative photoresist may be used. The photoresist is either acid-etched or plasma-etched to provide openings and to expose the portions of the coated ceramic sheet 40 which correspond to the required pads, traces, resistive elements, and voltage bus on the ceramic substrate. The sputter-deposited base metal beneath the photoresist is used as the anode in the electroplating step to build up the voltage bus and the metal traces on the ceramic substrate. Note that the conductive bumps on the pads are further built up by additional sputter-depositing or electroplating means.

Upon completion of the fabrication process, a complete pattern exists, including resistive elements, bonding pads, and the voltage bus. The photoresist is then removed and the substrate is subjected to a mild acid bath to remove the exposed base metal, leaving intact the electroplated metal.

The upper substrate 11 is removed from the ceramic sheet 40 by snapping the sheet 40 along the edges made

by the elongated, rectangular holes 35. The center area 36 is cut out with a laser to form the aperture or cavity for the integrated circuit.

Although a specific configuration has been illustrated and described for the preferred embodiment of the present invention set forth herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the preferred embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, although the preferred dimensions of the elements of the present inventions are discussed herein, alternative dimensions could be substituted. Also, the integrated circuit need not be placed in a cavity, but could be placed on the same surface as the traces and resistive elements. In addition, wire bonding, ribbon bonding, or TAB (Tape Automated Bonding) could be used to attach the integrated circuit bonding pads to the connections on the chip carrier. Therefore, it is manifestly intended that this invention be limited only by the claims and equivalents thereof.

What is claimed is:

1. A method of fabricating an integrated circuit chip carrier, comprising the steps of:

- a) providing a first substrate having a location defined for receiving the integrated circuit;
- b) [metallizing a portion] depositing a metal layer on at least two surfaces of said first substrate such that a voltage bus with a large surface area is created;
- c) defining at least one conductive signal path on said first substrate; and
- d) depositing at least one resistive element on said first substrate such that said resistive element is connected between said conductive signal path and said voltage bus.

[2. The method of claim 1, wherein the metallizing step (b) further comprises depositing a metal layer onto a plurality of surfaces of said first substrate, such that said voltage bus occupies a large surface area.]

3. The method of claim 1, further comprising the step of opening said resistive element with an excessive electrical current.

4. The method of claim 1, further comprising the step of opening said resistive element with a laser.

5. [The method of claim 1, further comprising the step of] A method of fabricating an integrated circuit chip carrier, comprising the steps of:

- (a) providing a first substrate having a location defined for receiving the integrated circuit;
- (b) metallizing a portion of said first substrate such that a voltage bus is created;
- (c) defining at least one conductive signal path on said first substrate;
- (d) depositing at least one resistive element on said first substrate such that said resistive element is connected between said conductive signal path and said voltage bus; and
- (e) adding at least one uncommitted resistive element connected to said voltage bus on said first substrate, thereby providing a spare resistive element.

6. The method of claim 5, further comprising the step of connecting said uncommitted resistive element to said conductive signal path when said resistive element is unavailable.

7. The method of claim 1 wherein the steps are performed in any order.

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