Title: FIELD EFFECT TRANSISTOR AND METHOD

Abstract: A field-effect transistor (FET) includes a plurality of semiconductor layers, a source electrode and a drain electrode contacting one of the semiconductor layers, a first dielectric layer on a portion of a top semiconductor surface between the source and drain electrodes, a first trench extending through the first dielectric layer and having a bottom located on a top surface or within one of the semiconductor layers, a second dielectric layer lining the first trench and covering a portion of the first dielectric layer, a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer, a second trench extending through the third dielectric layer and having a bottom located in the first trench on the second dielectric layer and extending over a portion of the second dielectric, and a gate electrode filling the second trench.
FIELD EFFECT TRANSISTOR AND METHOD

CROSS REFERENCE TO RELATED APPLICATIONS


STATEMENT REGARDING FEDERAL FUNDING

[0002] This invention was made under U.S. Government contract DE-AR-0000117. The U.S. Government has certain rights in this invention.

TECHNICAL FIELD

[0003] This disclosure relates to III-Nitride field effect transistors (FETs) and in particular to insulated gates for FETs. Otherwise stated, this writing pertains to III-Nitride insulating-gate transistors with passivation.

BACKGROUND

[0004] III-nitride transistors are promising for high-speed and high-power applications, such as power switches, which may be used for motor drivers and power supplies, among other applications.

[0005] Many of these applications require the transistor to operate in normally-off mode. Normally-off mode operation can be realized by a number of approaches, but typically at the penalty of higher on-resistance and lower output-current.

transistor and a method for making a normally-off FET.


[0008] High-power applications with normally-off III-nitride transistors need an insulated gate to achieve low leakage current, and an effective passivation dielectric to achieve minimal trapping effects.

[0009] The best-suited gate insulator and the best-suited passivation dielectric are usually different materials, which may cause processing compatibility problems. For example, plasma-enhanced chemical vapor deposition (PECVD) SiN film is a known good passivation material, while metal organic chemical vapor deposition (MOCVD) AlN is a known good gate insulator material.

[0010] Unfortunately, the process of forming MOCVD AlN can degrade a PECVD SiN film that is already deposited on the semiconductor.

[0011] What is needed is a device structure and method of making the device that resolves this process incompatibility and that has a high breakdown voltage and low on resistance. The embodiments of the present writing consider these and other needs.

SUMMARY

[0012] In a first embodiment disclosed herein, a field-effect transistor (FET) comprises a plurality of semiconductor layers, a source electrode contacting at least one of the semiconductor layers, a drain electrode contacting at least one of the semiconductor layers, a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode, a first trench extending
through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers, a second dielectric layer lining the first trench and covering a portion of the first dielectric layer, a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer, a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric, and a gate electrode filling the second trench.

[0013] In another embodiment disclosed herein, a method of fabricating a field-effect transistor (FET) comprises forming a plurality of semiconductor layers, forming a source electrode contacting at least one of the semiconductor layers, forming a drain electrode contacting at least one of the semiconductor layers, forming a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode, forming a first trench extending through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers, forming a second dielectric layer lining the first trench and covering a portion of the first dielectric layer, forming a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer, forming a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric, and forming a gate electrode filling the second trench.

[0014] These and other features and advantages will become
further apparent from the detailed description and accompanying figures that follow. In the figures and description, numerals indicate the various features, like numerals referring to like features throughout both the drawings and the description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 shows a diagram of III-nitride field effect transistor in accordance with the present disclosure;

[0016] FIG. 2 shows a typical off-state current voltage (IV) characteristic of a FET in accordance with the present disclosure;

[0017] FIG. 3 shows a typical dynamic current voltage (IV) characteristic of a FET in accordance with the present disclosure;

[0018] FIG. 4 shows a diagram of another field effect transistor in accordance with the present disclosure;

[0019] FIG. 5 shows a diagram of yet another field effect transistor in accordance with the present disclosure;

[0020] FIG. 6 shows a diagram of still another field effect transistor in accordance with the present disclosure; and

[0021] FIG. 7 shows a diagram of a gate insulator stack in accordance with the present disclosure.

DETAILED DESCRIPTION

[0022] In the following description, numerous specific details are set forth to clearly describe various specific embodiments disclosed herein. One skilled in the art, however, will understand that the presently claimed invention may be practiced without all of the specific details discussed below. In other instances, well known features have not been described so as not to obscure the invention.

[0023] FIG. 1 shows a diagram of III-nitride field effect
transistor (FET) in accordance with the present disclosure. The FET has a buffer layer 14 formed on a substrate 12. A channel layer 16 is formed on the buffer layer 14 and a barrier layer 18, is formed on the channel layer 16.

[0024] The substrate 12 material may be silicon (Si), silicon carbide (SiC), sapphire (Al₂O₃), gallium nitride (GaN), or aluminum nitride (AlN).

[0025] The buffer layer 14 may be a stack of III-Nitride materials grown on the substrate 12 by chemical vapor deposition or molecular beam epitaxy.

[0026] The channel layer 16 may be a III-Nitride material, such as GaN, grown on the buffer layer 14 by chemical vapor deposition or molecular beam epitaxy. Typically the channel layer 16 is an undoped GaN layer with the thickness ranging from 5 nanometers to a few micrometers.

[0027] The barrier layer 18 may be 1-30 nanometers thick and may typically be only 5 nm thick. The barrier layer 18 may be AlGaN, with a 25% Al composition.

[0028] A source electrode 20 and a drain electrode 22 are in contact with the channel layer 16 and extend through the the barrier layer 18. The source electrode 20 and drain electrode 22 are on opposite ends of the channel layer 16.

[0029] A dielectric layer 30, which may be 1nm to 100nm thick and is typically 10nm thick, and which may be SiN, is deposited by metal organic chemical vapor deposition (MOCVD) on top of the AlGaN barrier layer 18. In a preferred embodiment the dielectric layer 30 is deposited by MOCVD at a temperature higher than 600 degrees C, and typically at 900 degrees C.

[0030] The dielectric layer 30 is patterned to be on top of the AlGaN barrier layer 18 in a gate area for a distance of Ls2, Ls1, Lg, Ld1 and Ld2, as shown in FIG. 1, between the source 20 and drain 22. In the embodiment of FIG. 1, the dielectric layer
30 is not in contact with either the source 20 or the drain 22.  

A first gate trench 32 with a length of \( L_g \), as shown in FIG. 1, is formed through the dielectric layer 30 and the barrier layer 18. The bottom 38 of the gate trench 32 is located within the channel layer 16, and extends below the barrier layer 18 and into the channel layer 16 by a vertical distance 36. This vertical distance 36 is between an interface of the barrier layer 18 and channel layer 16 and the bottom 38 of the gate trench 32, and is typically between 0 and 10 nanometers (nm). The vertical distance 36 needs to be equal or greater than 0 nm for normally-off operation, and needs to be as small as possible to in order to minimize the on-resistance.  

A gate insulator 33 is formed in the gate trench 32 and over the dielectric layer 30. As shown in FIG. 7, the gate insulator 33 may include a stack of: a layer of single-crystalline AlN 104 at the bottom of the gate trench 32, which may be up to 2nm thick and typically 1nm thick; a layer of polycrystalline AlN 102 on the single crystalline AlN layer, which is 1nm to 50nm thick and typically 10nm thick; and an insulating layer of SiN 100, which may be 1nm to 50nm thick and typically 10nm thick, formed on the polycrystalline AlN layer.  

The single crystalline AlN 104 is preferably grown at a temperature greater than 600C, and less than 1100C. A preferred temperature for growing the single crystalline AlN 104 is 900C. The polycrystalline AlN 102 is preferably grown at a temperature greater than 300C, and less than 900C, and a preferred temperature is 600C.  

The gate insulator 33 stack makes the FET a normally off FET. Under a positive gate bias the FET has a very low gate leakage, and a high-mobility electron channel is formed at the interface between the barrier layer 18 and the channel layer 16.  

The single-crystalline AlN layer 104 of the gate
insulator stack 33 provides a high-quality interface for electron transport in the channel layer 16. Furthermore, the single crystalline AlN layer 104 provides an energy barrier to prevent electron trapping into the poly-crystalline AlN layer 102. The thickness of the single crystalline AlN layer 104 is chosen to be thin enough, typically below 2nm, to avoid accumulation of channel electrons in absence of a positive gate bias.

[0036] The SiN layer 100 serves as a blocking layer to leakage paths through grain boundaries of the polycrystalline AlN layer 102.

[0037] The gate insulator 33 is formed in the trench 32 and over the dielectric layer 30. The gate insulator 33 and the dielectric layer 30 are removed in regions beyond the gate area of Ls2, Ls1, Lg, Ld1 and Ld2, as shown in FIG. 1.

[0038] A passivation dielectric 34, which may be SiN and have a thickness of 10nm to 500nm with a typical thickness of 100nm, is deposited by plasma-enhanced chemical vapor deposition (PECVD) over the barrier layer 18 between the source 20 and the drain 22, over the gate insulator 33 in the trench 32, and over the gate insulator 33 on the dielectric layer 30. In a preferred embodiment the passivation dielectric 34 is deposited by PECVD at a temperature lower than 500 degrees C, and typically at 300 degrees C.

[0039] A second gate trench 40 is formed in passivation dielectric 34 by etching and may have a length of the sum of Lg, Ls1 and Ld1, as shown in FIG. 1. The second gate trench 40 extends to the gate insulator 33 in the gate trench 32 and overlaps the gate insulator 33 on the dielectric layer 30 by a distance Ls1 and Ld1, as shown in FIG. 1. The gate insulator 33 on the dielectric layer 30 for distance Ls2 and Ld2 on either side of Ls1 and Ld1, as shown in FIG. 1, remains covered by the
passivation layer 34.

[0040] A gate electrode 24 is formed within the second gate trench 40 and may extend over the passivation layer 34 partially toward the source electrode 20 by a distance Ls3, as shown in FIG. 1, and partially toward the drain electrode 22 by a distance Ld3, as shown in FIG. 1, to form an integrated gate field-plate. The gate electrode 24 may be any suitable metal.

[0041] As shown in FIG. 1, two types of dielectric are in contact with the AlGaN barrier layer 18 in the gate to drain region. The two types of dielectric are: a dielectric layer 30, which may be a SiN layer deposited by metal organic chemical vapor deposition (MOCVD), and a passivation dielectric layer 34, which may be a SiN layer deposited by plasma-enhanced chemical vapor deposition (PECVD).

[0042] Dielectric layer 30 is deposited prior to the deposition of the gate insulator layer stack 33. The dielectric layer 30 serves as a etch stop layer for the patterning of the gate insulator layer stack 33, and dielectric layer 30 can survive subsequent high-temperature steps, such as the deposition of gate insulator layer stack 33 and the alloying of source 20 and drain 22 contacts.

[0043] Dielectric layer 34 serves the purpose of mitigating trapping behaviors. Dielectric layer 34 is deposited after the deposition of gate insulator layer stack 33, to avoid the impact of high-temperature processing on the properties of dielectric layer 34.

[0044] FIG. 2 shows a typical off-state current voltage (IV) characteristic of a FET in accordance with the present disclosure. As shown in FIG. 2, the off-state current is very low even at 600 volts, demonstrating the breakdown voltage is greater than 600 volts.

[0045] FIG. 3 shows a typical dynamic current voltage (IV)
characteristic of a FET in accordance with the present disclosure, and the graph demonstrates that the on-resistance for a FET is only minimally degraded.

[0046] FIG. 4 shows a diagram of another field effect transistor in accordance with the present disclosure. The embodiment of FIG. 4 is similar to the embodiment of FIG. 1. However, in the embodiment of FIG. 4 the dielectric layer 30, which may be 1nm to 100nm thick and is typically 10nm thick, and which may be SiN, is deposited by metal organic chemical vapor deposition (MOCVD) on top of the AlGaN barrier layer 18 and extends from the source 20 to the drain 22, as shown in FIG. 4, rather than just in the gate area as shown in FIG. 1.

[0047] FIG. 5 shows a diagram of yet another field effect transistor in accordance with the present disclosure. The embodiment of FIG. 5 is similar to the embodiment of FIG. 4. However, in the embodiment of FIG. 5 the gate insulator stack 33 extends from the source 20 to the drain 22, as shown in FIG. 5, rather than just in the gate area as shown in FIG. 4.

[0048] FIG. 6 shows a diagram of still another field effect transistor in accordance with the present disclosure. The embodiment of FIG. 6 is similar to the embodiment of FIG. 1. However, in the embodiment of FIG. 6 the bottom 38 of the gate trench 32 is located within the barrier layer 18, and does not extend below the barrier layer 18 into the channel layer 16. The gate trench 32 may also be only to the top surface of the barrier layer 18. Variations of the embodiment of FIG. 6 may also include an embodiment where the dielectric layer 30 extends from the source 20 to the drain 22, and another embodiment where both the dielectric layer 30 and the gate insulator stand extend from the source 20 to the drain 22.

[0049] Having now described the invention in accordance with the requirements of the patent statutes, those skilled in this
art will understand how to make changes and modifications to the present invention to meet their specific requirements or conditions. Such changes and modifications may be made without departing from the scope of the invention as disclosed herein. 

[0050] The foregoing Detailed Description of exemplary and preferred embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean “one and only one” unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the Claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase “means for. . .” and no
method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "comprising the step(s) of . . . ."

[0051] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

[0052] Broadly, this writing discloses at least the following:

A field-effect transistor (FET) includes a plurality of semiconductor layers, a source electrode and a drain electrode contacting one of the semiconductor layers, a first dielectric layer on a portion of a top semiconductor surface between the source and drain electrodes, a first trench extending through the first dielectric layer and having a bottom located on a top surface or within one of the semiconductor layers, a second dielectric layer lining the first trench and covering a portion of the first dielectric layer, a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer, a second trench extending through the third dielectric layer and having a bottom located in the first trench on the second dielectric layer and extending over a portion of the second dielectric, and a gate electrode filling the second trench.

[0053] CONCEPTS

This writing also presents at least the following concepts.

Concept 1. A field-effect transistor (FET) comprising:
   a plurality of semiconductor layers;
   a source electrode contacting at least one of the
semiconductor layers;
  a drain electrode contacting at least one of the semiconductor layers;
  a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode;
  a first trench extending through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers;
  a second dielectric layer lining the first trench and covering a portion of the first dielectric layer;
  a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer;
  a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric; and
  a gate electrode filling the second trench.

Concept 2. The FET of concept 1 further comprising:
  a substrate comprising silicon (Si), silicon carbide (SiC), sapphire (Al₂O₃), gallium nitride (GaN), or aluminum nitride (AlN);
  wherein the plurality of semiconductor layers comprise:
    a III-nitride channel layer; and
    a barrier layer over the channel layer.

Concept 3. The FET of concept 2 wherein:
  the channel layer comprises GaN and has a thickness ranging from 5 nanometers to a few micrometers; and
  the barrier layer comprises AlGaN having a thickness
ranging from 1-30 nanometers and having a 25% Al composition.

Concept 4. The FET of concept 2 wherein:

a distance between an interface of the channel layer and the barrier layer and the bottom of the first trench is equal to or greater than 0 nanometers and less than or equal to 10 nanometers.

Concept 5. The FET of concept 1, 2, 3 or 4 wherein:

the first dielectric layer is deposited by metal organic chemical vapor deposition; and

the third dielectric layer is deposited by plasma-enhanced chemical vapor deposition.

Concept 6. The FET of concept 1, 2, 3 or 4 wherein:

the first dielectric layer comprises SiN deposited at a temperature greater than 600 degrees centigrade by metal organic chemical vapor deposition; and

the third dielectric layer comprises SiN deposited at a temperature lower than 500 degrees centigrade by plasma-enhanced chemical vapor deposition.

Concept 7. The FET of concept 1, 2, 3 or 4 wherein:

the gate electrode extends over the third dielectric partially toward the source electrode and the drain electrode to form an integrated gate field-plate.

Concept 8. The FET of concept 1, 2, 3 or 4 wherein:

the first dielectric layer comprises SiN having a thickness of 1nm to 100nm; and

the third dielectric layer comprises SiN having a thickness of 10nm to 500nm.
Concept 9. The FET of concept 1, 2, 3 or 4 wherein the second dielectric comprises:

- a single-crystalline AlN layer at the bottom of the gate trench;
- a polycrystalline AlN layer on the single crystalline AlN layer; and
- an insulating layer comprising SiN on the polycrystalline AlN layer.

Concept 10. The FET of concept 9 wherein:

- the single crystalline AlN is grown at a temperature greater than 600°C and less than 1100°C;
- the poly crystalline AlN is grown at a temperature greater than 300°C and less than 900°C.

Concept 11. The FET of concept 9 wherein:

- the single crystalline AlN layer is up to 2nm thick;
- the polycrystalline AlN layer is 1nm to 50nm thick; and
- the insulating layer is 1nm to 50nm thick.

Concept 12. The FET of concept 1, 2, 3 or 4 wherein:

- the first dielectric is only in a gate area and the second dielectric covers the first dielectric in the gate area; or
- the first dielectric extends from the source electrode to the drain electrode and the second dielectric covers the first dielectric only in the gate area; or
- the first dielectric extends from the source electrode to the drain electrode and the second dielectric covers the first dielectric and extends from the source electrode to the drain electrode.
Concept 13. A method of fabricating a field-effect transistor (FET) comprising:
  forming a plurality of semiconductor layers;
  forming a source electrode contacting at least one of the semiconductor layers;
  forming a drain electrode contacting at least one of the semiconductor layers;
  forming a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode;
  forming a first trench extending through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers;
  forming a second dielectric layer lining the first trench and covering a portion of the first dielectric layer;
  forming a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer;
  forming a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric; and
  forming a gate electrode filling the second trench.

Concept 14. The method of concept 13 further comprising:
  providing a substrate comprising silicon (Si), silicon carbide (SiC), sapphire (Al₂O₃), gallium nitride (GaN), or aluminum nitride (AlN);
  wherein the plurality of semiconductor layers comprise:
    a III-nitride channel layer; and
a barrier layer over the channel layer.

Concept 15. The method of concept 14 wherein:
the channel layer comprises GaN and has a thickness ranging from 5 nanometers to a few micrometers; and
the barrier layer comprises AlGaN having a thickness ranging from 1-30 nanometers and having a 25% Al composition.

Concept 16. The method of concept 14 wherein:
a distance between an interface of the channel layer and the barrier layer and the bottom of the first trench is equal to or greater than 0 nanometers and less than or equal to 10 nanometers.

Concept 17. The method of concept 13, 14, 15 or 16 wherein:
forming the first dielectric layer comprises depositing the first dielectric layer by metal organic chemical vapor deposition; and
forming the third dielectric layer comprises depositing the third dielectric layer by plasma-enhanced chemical vapor deposition.

Concept 18. The method of concept 13, 14, 15 or 16 wherein:
the first dielectric layer comprises SiN deposited at a temperature greater than 600 degrees centigrade by metal organic chemical vapor deposition; and
the third dielectric layer comprises SiN deposited at a temperature lower than 500 degrees centigrade by plasma-enhanced chemical vapor deposition.

Concept 19. The method of concept 13, 14, 15 or 16 further comprising:
forming the gate electrode to extend over the third
dielectric partially toward the source electrode and the drain
electrode to form an integrated gate field-plate.

Concept 20. The method of concept 13, 14, 15 or 16 wherein:
the first dielectric layer comprises SiN having a thickness
of 1nm to 100nm; and
the third dielectric layer comprises SiN having a thickness
of 10nm to 500nm.

Concept 21. The method of concept 13, 14, 15 or 16 wherein the
forming the second dielectric comprises:
forming a single-crystalline AlN layer at the bottom of the
gate trench;
forming a polycrystalline AlN layer on the single
crystalline AlN layer; and
forming an insulating layer comprising SiN on the
polycrystalline AlN layer.

Concept 22. The method of concept 21 wherein:
the single crystalline AlN is grown at a temperature
greater than 600C and less than 1100C;
the poly crystalline AlN is grown at a temperature greater
than 300C and less than 900C.

Concept 23. The method of concept 21 wherein:
the single crystalline AlN layer is up to 2nm thick;
the polycrystalline AlN layer is 1nm to 50nm thick; and
the insulating layer is 1nm to 50nm thick.

Concept 24. The method of concept 13, 14, 15 or 16 wherein:
the first dielectric is only formed in a gate area and the
second dielectric covers the first dielectric in the gate area; or

the first dielectric is formed to extend from the source electrode to the drain electrode and the second dielectric covers the first dielectric only in the gate area; or

the first dielectric is formed to extend from the source electrode to the drain electrode and the second dielectric covers the first dielectric and extends from the source electrode to the drain electrode.

Concept 25. The method of concept 13, 14, 15 or 16 wherein:

the first dielectric layer provides an etch stop for patterning of the second dielectric layer.

Concept 26. The method of concept 13, 14, 15 or 16 wherein:

forming the first trench comprises etching; and

forming the third trench comprises etching and the second dielectric provides an etch stop.
WHAT IS CLAIMED IS:

1. A field-effect transistor (FET) comprising:
   a plurality of semiconductor layers;
   a source electrode contacting at least one of the semiconductor layers;
   a drain electrode contacting at least one of the semiconductor layers;
   a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode;
   a first trench extending through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers;
   a second dielectric layer lining the first trench and covering a portion of the first dielectric layer;
   a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer;
   a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric; and
   a gate electrode filling the second trench.

2. The FET of claim 1 further comprising:
   a substrate comprising silicon (Si), silicon carbide (SiC), sapphire (Al₂O₃), gallium nitride (GaN), or aluminum nitride (AlN);
   wherein the plurality of semiconductor layers comprise:
   a III-nitride channel layer; and
   a barrier layer over the channel layer.
3. The FET of claim 2 wherein:
   the channel layer comprises GaN and has a thickness ranging
   from 5 nanometers to a few micrometers; and
   the barrier layer comprises AlGaN having a thickness
   ranging from 1-30 nanometers and having a 25% Al composition.

4. The FET of claim 2 wherein:
   a distance between an interface of the channel layer and
   the barrier layer and the bottom of the first trench is equal to
   or greater than 0 nanometers and less than or equal to 10
   nanometers.

5. The FET of claim 1 wherein:
   the first dielectric layer is deposited by metal organic
   chemical vapor deposition; and
   the third dielectric layer is deposited by plasma-enhanced
   chemical vapor deposition.

6. The FET of claim 1 wherein:
   the first dielectric layer comprises SiN deposited at a
   temperature greater than 600 degrees centigrade by metal organic
   chemical vapor deposition; and
   the third dielectric layer comprises SiN deposited at a
   temperature lower than 500 degrees centigrade by plasma-enhanced
   chemical vapor deposition.

7. The FET of claim 1 wherein:
   the gate electrode extends over the third dielectric
   partially toward the source electrode and the drain electrode to
   form an integrated gate field-plate.
8. The FET of claim 1 wherein:
   the first dielectric layer comprises SiN having a thickness of 1nm to 100nm; and
   the third dielectric layer comprises SiN having a thickness of 10nm to 500nm.

9. The FET of claim 1 wherein the second dielectric comprises:
   a single-crystalline AlN layer at the bottom of the gate trench;
   a polycrystalline AlN layer on the single crystalline AlN layer; and
   an insulating layer comprising SiN on the polycrystalline AlN layer.

10. The FET of claim 9 wherein:
    the single crystalline AlN is grown at a temperature greater than 600C and less than 1100C;
    the poly crystalline AlN is grown at a temperature greater than 300C and less than 900C.

11. The FET of claim 9 wherein:
    the single crystalline AlN layer is up to 2nm thick;
    the polycrystalline AlN layer is 1nm to 50nm thick; and
    the insulating layer is 1nm to 50nm thick.

12. The FET of claim 1 wherein:
    the first dielectric is only in a gate area and the second dielectric covers the first dielectric in the gate area; or
    the first dielectric extends from the source electrode to the drain electrode and the second dielectric covers the first dielectric only in the gate area; or
    the first dielectric extends from the source electrode to
the drain electrode and the second dielectric covers the first dielectric and extends from the source electrode to the drain electrode.

13. A method of fabricating a field-effect transistor (FET) comprising:
    forming a plurality of semiconductor layers;
    forming a source electrode contacting at least one of the semiconductor layers;
    forming a drain electrode contacting at least one of the semiconductor layers;
    forming a first dielectric layer covering a portion of semiconductor top surface between the source electrode and the drain electrode;
    forming a first trench extending through the first dielectric layer and having a bottom located on a top surface of the semiconductor layers or within one of the semiconductor layers;
    forming a second dielectric layer lining the first trench and covering a portion of the first dielectric layer;
    forming a third dielectric layer over the semiconductor layers, the first dielectric layer, and the second dielectric layer;
    forming a second trench extending through the third dielectric layer and having a bottom located in the first trench on the surface of or within the second dielectric layer, and extending over a portion of the second dielectric on the first dielectric; and
    forming a gate electrode filling the second trench.

14. The method of claim 13 further comprising:
    providing a substrate comprising silicon (Si), silicon
carbide (SiC), sapphire (Al₂O₃), gallium nitride (GaN), or aluminum nitride (AlN);
wherein the plurality of semiconductor layers comprise:
    a III-nitride channel layer; and
    a barrier layer over the channel layer.

15. The method of claim 14 wherein:
    the channel layer comprises GaN and has a thickness ranging from 5 nanometers to a few micrometers; and
    the barrier layer comprises AlGaN having a thickness ranging from 1-30 nanometers and having a 25% Al composition.

16. The method of claim 14 wherein:
    a distance between an interface of the channel layer and the barrier layer and the bottom of the first trench is equal to or greater than 0 nanometers and less than or equal to 10 nanometers.

17. The method of claim 13 wherein:
    forming the first dielectric layer comprises depositing the first dielectric layer by metal organic chemical vapor deposition; and
    forming the third dielectric layer comprises depositing the third dielectric layer by plasma-enhanced chemical vapor deposition.

18. The method of claim 13 wherein:
    the first dielectric layer comprises SiN deposited at a temperature greater than 600 degrees centigrade by metal organic chemical vapor deposition; and
    the third dielectric layer comprises SiN deposited at a temperature lower than 500 degrees centigrade by plasma-enhanced
chemical vapor deposition.

19. The method of claim 13 further comprising:
   forming the gate electrode to extend over the third
dielectric partially toward the source electrode and the drain
electrode to form an integrated gate field-plate.

20. The method of claim 13 wherein:
   the first dielectric layer comprises SiN having a thickness
   of 1nm to 100nm; and
   the third dielectric layer comprises SiN having a thickness
   of 10nm to 500nm.

21. The method of claim 13 wherein the forming the second
dielectric comprises:
   forming a single-crystalline AlN layer at the bottom of the
gate trench;
   forming a polycrystalline AlN layer on the single
   crystalline AlN layer; and
   forming an insulating layer comprising SiN on the
   polycrystalline AlN layer.

22. The method of claim 21 wherein:
   the single crystalline AlN is grown at a temperature
greater than 600C and less than 1100C;
   the poly crystalline AlN is grown at a temperature greater
   than 300C and less than 900C.

23. The method of claim 21 wherein:
   the single crystalline AlN layer is up to 2nm thick;
   the polycrystalline AlN layer is 1nm to 50nm thick; and
   the insulating layer is 1nm to 50nm thick.
24. The method of claim 13 wherein:
   the first dielectric is only formed in a gate area and the second dielectric covers the first dielectric in the gate area; or
   the first dielectric is formed to extend from the source electrode to the drain electrode and the second dielectric covers the first dielectric only in the gate area; or
   the first dielectric is formed to extend from the source electrode to the drain electrode and the second dielectric covers the first dielectric and extends from the source electrode to the drain electrode.

25. The method of claim 13 wherein:
   the first dielectric layer provides an etch stop for patterning of the second dielectric layer.

26. The method of claim 13 wherein:
   forming the first trench comprises etching; and
   forming the third trench comprises etching and the second dielectric provides an etch stop.
A. CLASSIFICATION OF SUBJECT MATTER
H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 29/778; H01L 21/18; H01L 21/338; H01L 21/335; H01L 29/812; H01L 29/423; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: field-effect transistor, source, drain, trench, dielectric, gate, nitride, MOCVD, PECVD

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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See paragraphs [0021]–[0029], claims 1-24 and figure 2. | 1-26 |
See abstract, paragraphs [0002]–[0030], claims 10,22 and figure 1. | 1-26 |
| A         | US 2010-0090251 A1 (ANNE LORENZ et al.) 15 April 2010
See paragraphs [0052]–[0080], claims 1-17 and figures 1-2. | 1-26 |
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| A         | US 2010-0025730 A1 (STEN HEHRMAN et al.) 04 February 2010
See paragraphs [0079]–[0095] and figures 7A-9B. | 1-26 |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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**P** document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report
22 December 2014 (22.12.2014)

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