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[72] Inventors **Julius Gluck**
Glenbrook;
Warren R. Wines, Norwalk; Joseph J. Laszlo, West Redding; Nanjundiah N. Murthy, West Redding, Conn.; Klaus E. Grund, Ann Arbor, Mich.

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[73] Assignee **Sperry Rand Corporation**
New York, N.Y.

[54] **OSCILLATOR KEYBOARD WITH ROLL AND DOUBLE-STRIKE CONTROL**
12 Claims, 8 Drawing Figs.

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[51] **Int. Cl.** **G08b 29/00**
[50] **Field of Search** ..... 340/365, 345; 178/81, 101, 17 C; 197/98, 101, 1, 13; 235/128, 145

[56] **References Cited**
UNITED STATES PATENTS

2,718,633	9/1955	Fennessy	340/345
2,737,647	3/1956	Oliwa	340/345
3,091,320	5/1963	Mertn	197/13
3,456,077	7/1969	Jones	178/17
3,483,553	12/1969	Blankenbaker	178/17

Primary Examiner—Robert L. Griffin
Assistant Examiner—John C. Martin
Attorneys—Marshall M. Truex, Thomas P. Murphy and H. Walter Clum

ABSTRACT: A solid-state keyboard for producing a coded output to an associated data processor. Depression of any single key activates an encoder and a circuit which produces a signal for gating the encoder output into the processor. A further circuit detects when a second key is depressed before a first key is released and, if the time between depression of the keys is less than a fixed interval, an alarm is sounded. If the time between depression of the two keys is greater than the fixed interval, the gating signal for the data represented by the second key is inhibited until after the first key is released.

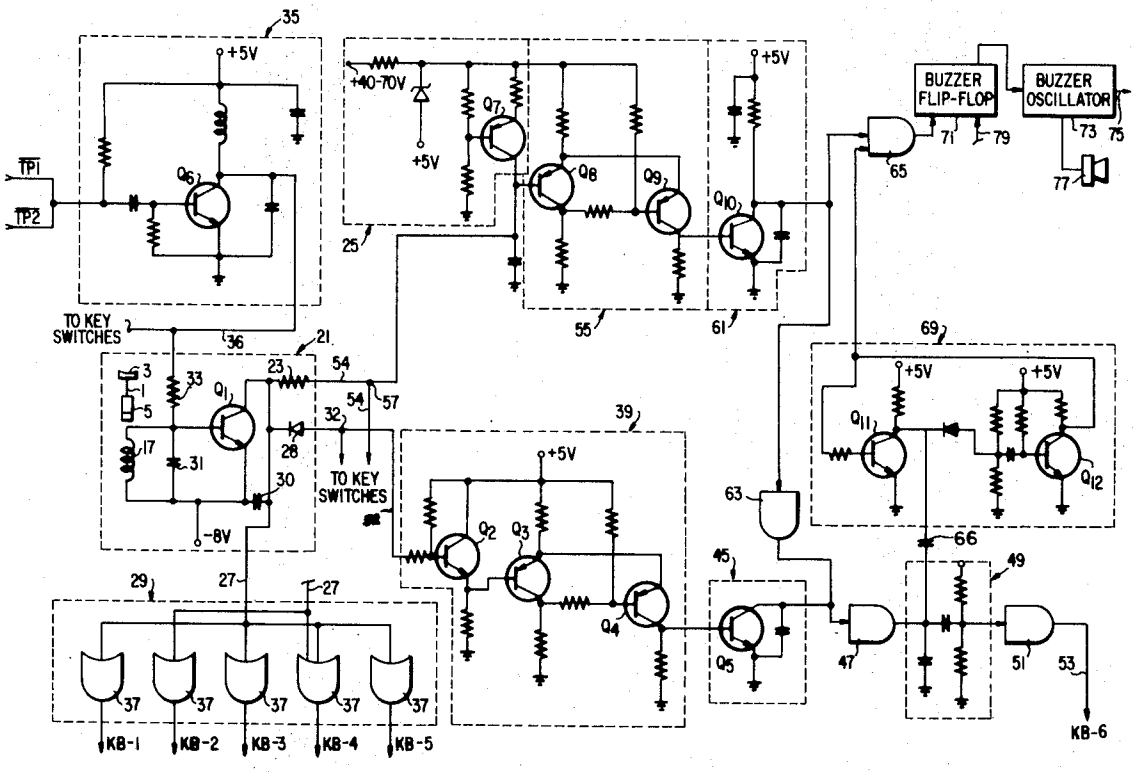
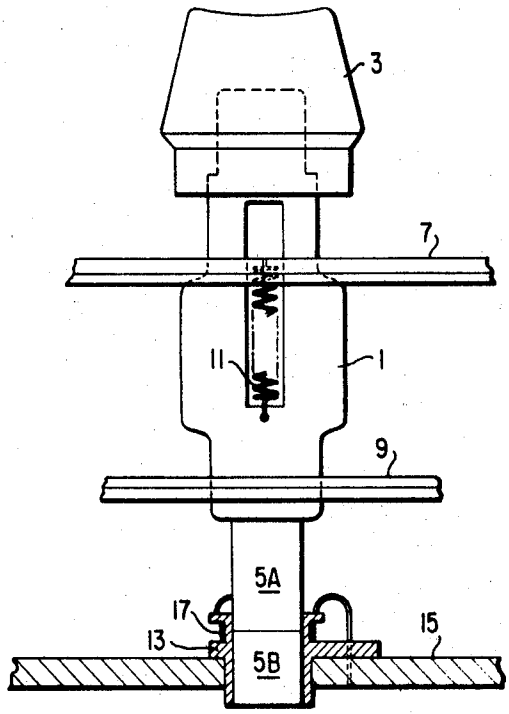


FIG. 1



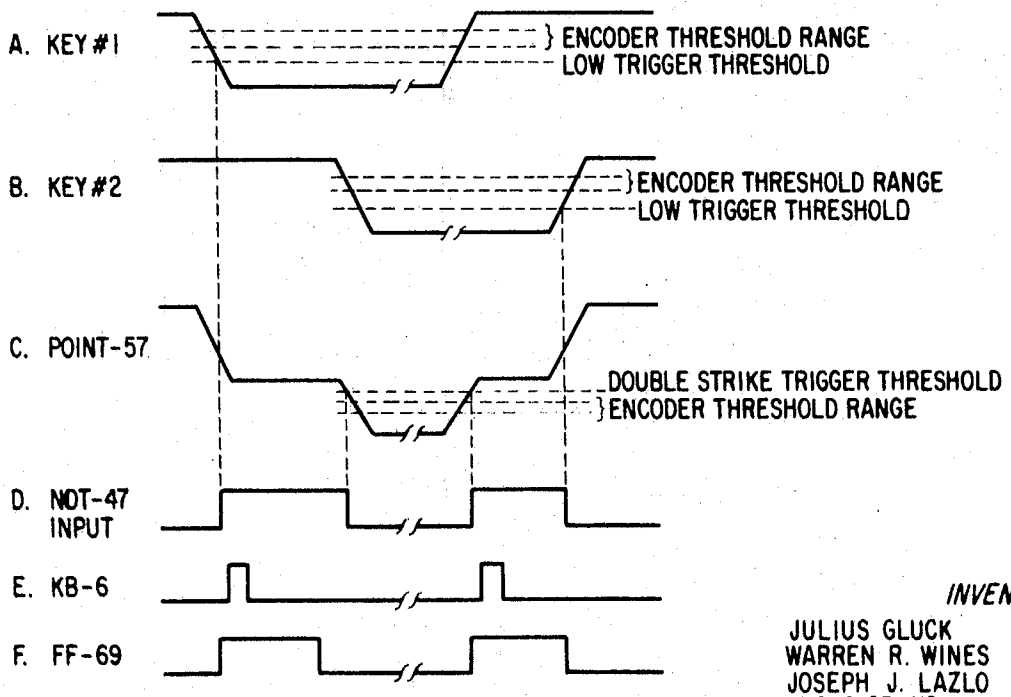
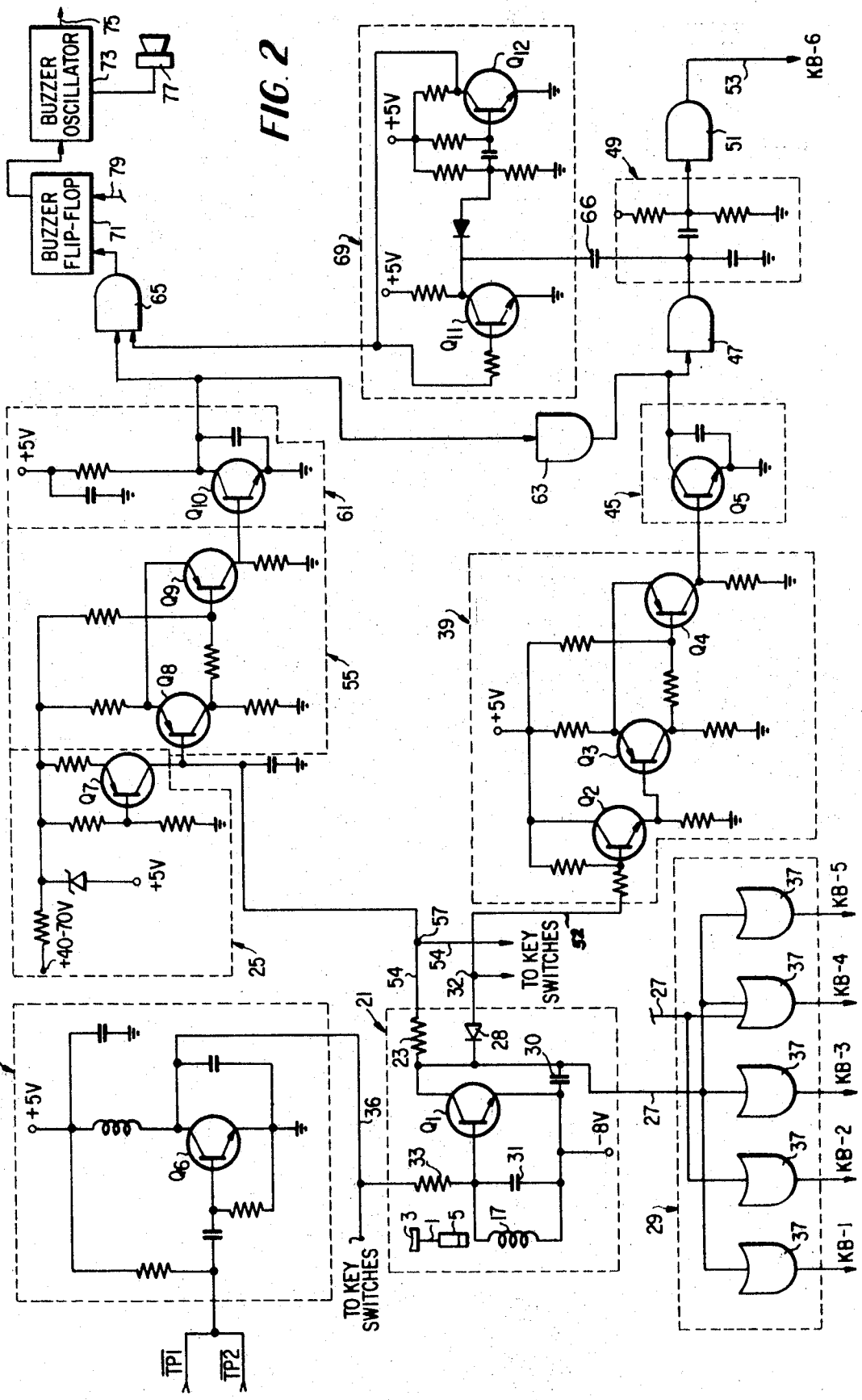


FIG. 3

INVENTORS

JULIUS GLUCK
WARREN R. WINES
JOSEPH J. LAZLO
KLAUS GRUND
NANJUNDIAH N. MURTHY

FIG. 2


BUZZER OSCILLATOR
BUZZER FLIP-FLOP
+5V
+40-70V
-8V
TO KEY SWITCHES
KB-1
KB-2
KB-3
KB-4
KB-5
KB-6
TP1
TP2

OSCILLATOR KEYBOARD WITH ROLL AND DOUBLE-STRIKE CONTROL

PRIOR ART

Keyboards having mechanical interlocks for preventing double strikes are well known in the art. The interlocks in these devices are such that rolling, i.e., depression of a second key before complete release of a previously depressed key, is permissible to a certain degree but double strikes, i.e., depression of two keys to the operative position at or near the same time, is not. Mechanical interlocks tend to wear and eventually become a source of trouble.

At least one prior art keyboard is known which has no mechanical interlocks but instead provides means for detecting when a double strike occurs. This keyboard does not permit rolling to the degree that a second key may be depressed before a previously depressed key has been released from the operative position. This, of course, reduces the speed at which an operator may operate a keyboard.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide a solid-state keyboard having means for producing an error signal upon occurrence of a double strike yet permits correct entry of data even though keys are rolled to the extent that a second key is moved to the operative position before a prior key is released from the operative position.

An object of the invention is to provide a keyboard having means for detecting when two keys are simultaneously in the operative position, means for determining if the elapsed time between depression of the two keys is greater than a predetermined minimum interval of time, and means for producing an error signal when said elapsed time is less than the predetermined minimum interval of time.

An object of the invention is to provide a keyboard having a plurality of keys, a solid-state switch associated with each of said keys and activated by depression of the associated key, an encoder responsive to said switches for producing an output code in response to the depression of said keys, means normally responsive to depression of a key for producing a gating signal, means for sensing when a second switch is activated before a first switch is inactivated, and means responsive to said sensing means for inhibiting the gating signal for the second depressed key until after the first depressed key is released.

A feature of the invention is the provision of a constant current generator, a plurality of key switches connected in parallel circuits to said constant current generator, and means for sensing the voltage at the output of said constant current source to determine when at least two of the key switches are concurrently active. All key switches control an encoder and a gating pulse generator. The sensing means acts when a second key switch is activated to inhibit generation of a second gating signal until after a first key switch is deactivated. Each gating signal initiates a timing signal that is compared with the sensing means to thereby produce an error signal if the time elapsing between activation of two keys does not exceed a predetermined minimum time.

Other objects of the invention and its mode of operation will become apparent from consideration of the following description and the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows the structure of a typical key.

FIG. 2 is a schematic circuit diagram of a preferred embodiment of the invention.

FIGS. 3A through 3F are waveforms illustrating the operation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is adapted for use in a keyboard having a full complement of keys, the exact number of keys being a matter of choice depending upon the intended use. A typical key is shown in FIG. 1. The key comprises a key stem 1 having a key cap 3 attached to its upper extremity and a core 5 staked or otherwise attached to its lower extremity. The core comprises a ferrite portion 5*a* and a brass portion 5*b*. The key stem is supported for vertical movement in first and second keyboard guide plates 7 and 9. A key return spring 11 is attached between the key stem and guide plate 7 and normally biases the key upwardly in the position shown with a shoulder of the key stem abutting guide plate 7.

The core 5 extends into a bobbin 13 mounted in a printed circuit board 15. A coil 17 is wound on the bobbin. The coil has a first inductance when the key is not depressed and the brass core 5*b* is within the coil. Upon depression of the key, the ferrite core portion moves downwardly into the bobbin and changes the inductance of the coil 17.

Each key is associated with a solid-state switch 21. Although only one solid-state switch 21 is shown in FIG. 2, it will be understood that the number of switches varies depending upon the number of keys on the keyboard. Each key switch comprises a transistor Q1 having its collector connected through a resistor 23 to a constant current generator 25. The collector of each transistor is connected by a lead 27 to the input of a keyboard encoder matrix 29. Also, the collector of each transistor is connected through a diode 28 to a junction point 32. A capacitor 30 is connected between the collector and emitter of each transistor and the emitters are connected to a −0.8 volt source. A tank circuit comprising the inductance 17 and a capacitor 31 is connected between the −0.8 volt source and the base of the transistor. The base of each transistor is connected through an isolating resistor 33 to the output of a 2 megahertz controlled oscillator 35.

The oscillator 35 comprises an RF amplifier of conventional design that is pulsed at a 2 megahertz rate by 1 megahertz clock pulses $\overline{TP1}$ and $\overline{TP2}$ derived from the data processor associated with the keyboard.

The output of oscillator 35 appearing on lead 36 is continuously applied through resistors 33 to the tank circuits of all the key switches 21. When a particular key is not depressed, the brass core portion 5*b* is within the coil 17 and detunes the tank circuit thereby attenuating the signal at the transistor base to the point where the transistor will not turn on. When the transistor Q1 is off, its collector potential is approximately +7.4 volts.

When a key is depressed, the ferrite core portion 5*b* is moved within the coil 17 thus tuning the tank circuit. In the tuned condition, the tank circuit parallel impedance increases thus causing an increase in the voltage at the base of Q1. The transistor switches on and off at a 2 megahertz rate but the capacitor at its output settles to the near 0 volt level. Capacitor 30 performs a smoothing function during this interval. The output from the transistor is a ramp function (FIG. 3A) and the slope of the ramp will depend upon the rate at which the key is depressed to move the ferrite portion of the core 5 into coil 17. However, as will be evident from the following discussion, the present invention functions properly regardless of the rate at which a key is depressed.

The zero potential at the collector is passed by way of lead 27 to the input of encoder 29. The encoder comprises a plurality of transistor NOR gates 37 each having one or more inputs connected to the collector of one or more key switch transistors. Since a NOR gate performs a single inversion, each depression of a single key results in positive output signals from one or more of the NOR gates. These signals are designated KB–1 through KB–5 and are fed into the processor with which the disclosed embodiment is associated. However, the encoder output signals KB–1 through KB–5 are not automatically fed into the processor but are gated by a further signal KB–6 for reasons which will become apparent from the subsequent description.

All the transistor NOR gates in the encoder 29 cannot be exactly matched. Therefore, all of them will not have the same firing threshold and will not fire at the same time. A short interval of time is allowed for the outputs KB–1 and KB–5 to sta-

bilize before the KB–6 signal is produced to gate the encoder outputs into the processor.

The circuit for producing the KB–6 gating signal comprises a Schmitt trigger **39**, an inverter **45**, a NOT-circuit **47**, a shaper delay **49**, and a NOT-circuit **51**.

The Schmitt trigger **39** is of conventional design and comprises three transistors Q2, Q3, and Q4. The base of input transistor Q2 is connected by way of lead **52**, and through each of the diodes **28**, to the collectors of the transistors in the key switches. The trigger **39** is designed to be triggered by a voltage which is slightly lower than the voltage range within which the NOR gates of the encoder are fired. This is illustrated in FIG. 3A which shows the waveform of the output from switch **21** when a key is depressed and subsequently released. Therefore, when a key is depressed and the collector of the corresponding key switch transistor drops to zero potential, the NOR gates of the encoder and the trigger **39** receive an input signal but the NOR gates are set before the trigger activated. The trigger output transistor Q4 is normally on, but upon activation of the trigger, the transistor is turned off and its output drops to zero potential thus cutting off the inverter **45**. When inverter **45** is cut off, its output rises to the logic one level of +5 volts and this signal is inverted to a logic zero or 0-volt signal by NOT-circuit **47**.

The delay element **49**, which is also of conventional design, shapes the output of NOT-**47** into a 0.2 millisecond pulse and delays it 0.5 microsecond. The output of delay element **49** is then inverted by NOT **51** to produce a logic one signal on lead **53**. This signal, which is the KB–6 signal, is fed to the data processor to control the gating of signals KB–1 through KB–5 into the processor.

It should be noted that NOT-circuits **47** and **51** in combination with shaper delay **49** comprise a waveshaper which shapes the KB–6 signal from the leading edge of the output signal from trigger **39**. When a key is depressed and its corresponding key switch activated, the voltage at point **32** drops below the firing threshold of the trigger **39** and the trigger fires. The trigger remains fired until the key is released and the voltage at point **32** rises back to its normal value. If succeeding keys should be depressed before preceding keys are released then the trigger will continuously fire until all keys have been released.

A feature of the invention is the provision of means for permitting keys to be rolled. Rolled as used herein relates to the tendency of a keyboard operator to begin depressing a second key before a previously depressed key is completely returned to its at rest position. Thus, when keys are rolled, it is possible to have two keys in a depressed position such that two key switches **21** produce output signals simultaneously. The present invention permits the operator to roll keys provided the key depressions are spaced by an elapsed time interval of some fixed duration. In the disclosed embodiment, this interval is 12 milliseconds. If two keys are depressed within a 12millisecond interval, it is known as a double strike and represents an error condition. The circuits about to be described serve to distinguish between a roll and a double strike. If a double strike occurs, an alarm is sounded to indicate a possible false entry of data. If a roll occurs, the data for the first key is entered in the normal way as described above, but the KB–6 signal necessary for gating into the processor the data represented by the second key is blocked until the first key is released. The second KB–6 signal is then key to gate into the processor the data represented by the second key.

A second Schmitt trigger **55** has an input connected to the point **57** intermediate the constant current generator **25** and the resistors **23** of the key switches **21**. The output of trigger **55** is connected through an inverter **61** and a NOT circuit **63** to the input of NOT-circuit **47**.

The output of inverter **61** is connected to one input of a NAND-gate **65**. The output from NOT-circuit **47** is connected through a capacitor **66** to the input of a monostable delay flip-flop **69**. The output of the delay flip-flop is connected to the second input of NAND **65**.

The output of NAND **65** is connected to the set input of a buzzer flip-flop **71**. A 1 kilohertz buzzer oscillator **73** is connected to the output of flip-flop **71** and provides a signal on lead **75** to drive a loudspeaker **77**.

The constant current generator **25** is the common collector load supply for all the key switch transistors Q1. When no keys are depressed, no transistors Q1 are on and the current source is open. The collector load voltage (i.e., point **57**) is at about +7.4 volts. When one key is depressed, a current of about 2 milliamp flows through corresponding transistor Q1 thus dropping the voltage at point **57** to about 4.5 volts. When two keys are depressed, the 2 milliamp constant current divides between two transistors Q1 reducing the load resistance and causing the voltage at point **57** to drop to about 2.8 volts. Since the transistor Q1 and resistors **23** form a plurality of parallel paths between point **57** and the −0.8 volt source, it is obvious that the voltage at point **57** depends on the number of transistors that are on.

The double-strike Schmitt trigger **55** monitors the common collector supply voltage at point **57**. The trigger is designed to fire at a voltage input level which is between 2.8 volts and 4.5 volts. Furthermore, as shown by the waveform of FIG. 3C, the trigger **55** fires before the encoder threshold range is reached as the key switch output drops.

Trigger **55** is of conventional design and comprises two transistors Q8 Q9. Q8 is normally off and Q9 is normally on so that the output of the trigger is normally about +0.7 volts. The output of inverter **61** is normally about +0.1 volt corresponding to the logic zero. The logic zero is inverted by NOT-circuit **63** so that the output of NOT circuit is normally a logic one.

Referring now to the waveforms of FIGS. 3A–3F, the circuit of FIG. 2 operates in the following manner in order to properly enter data into the processor when two keys are rolled. When the first key is depressed, the corresponding key switch **21** is activated to thereby activate the encoder outputs KB–1 through KB–5, and generate the gating signal KB–6, all as described above.

When the second key is depressed, the voltage at point **57** drops below the threshold value of double-strike trigger **55** and the trigger is activated. The collector voltage at Q9 drops to 0-volts thereby turning off transistor Q10 in the inverter **61**. The output of the inverter rises to logic one level and this signal is inverted by NOT-circuit **63** to drive the input of NOT-circuit **47** to the logic zero level. This is true even though the trigger **39** is still activated as a result of the first key being held in the depressed state. Furthermore, since two keys are simultaneously depressed, there are two key switches **21** providing inputs to the encoder **29** so that the output of the encoder during this interval is a logical sum of the two coded characters corresponding to the keys being depressed.

The conditions just described remain stable until the key that was first depressed is released. When the key is released, the key switch for that key stops producing an output signal to the encoder **29** so that the output signals KB–1 through KB–5 change to represent only the character corresponding to the second depressed key. When the first depressed key is released, the voltage at point **32** does not rise, because the second depressed key is still depressed. Thus, the voltage at point **32** holds trigger **39** off. However, the voltage at point **57** does rise above the threshold value of trigger **55** when the first key is released, so that the trigger **55** is turned off and its output rises sufficiently to turn on transistor Q10 in inverter **61**. The output of inverter **61** drops to the logic zero level and this signal is inverted by NOT-circuit **63** so that the output of NOT-circuit **63** rises to the logic one level. Since the trigger **39** is still activated, its output is at the logic zero level so that the output of inverter **45** is at the logic level. Therefore, NOT-circuit **49** is activated to produce a logic zero output that is delayed by delay element **49** and inverted by NOT-circuit **51** to become a KB–6 signal on lead **53**. This KB–6 signal is then used to gate the output of the encoder, representing the character corresponding to the second depressed key, into the data processor. When the second depressed key is released, the switch **21** corresponding thereto is cut off and the voltage

at point 57 rises above the firing threshold of trigger 39 provided a further key is not depressed before the second key is released.

If two keys are depressed at exactly the same instant or within about 12 milliseconds of each other, the data represented by the keys may be erroneously supplied to the data processor. The present invention provides means for warning an operator when such a double strike has occurred. For example, consider the immediately preceding illustration but assume that the second key is depressed within 12 milliseconds of the time the first key is depressed. The operation of the circuit is exactly the same as described in the illustration. However, an alarm is also sounded.

At the time the first key is depressed and the first KB–6 signal is generated to gate the output of the encoder into the data processor, the output of NOT-circuit 47 is differentiated by capacitor 66 and triggers the multivibrator 69. This multivibrator is designed so that it produces a logic one output signal of 12 milliseconds duration in response to each signal it receives through the capacitor 66. Therefore, for an interval of approximately 12 milliseconds after the first key is depressed, one input of NAND-gate 65 is conditioned by a logic one output from the multivibrator.

When the second key is depressed to fire the trigger 55, the output of the trigger drops to the logic zero level. The logic zero signal is inverted by inverter 61 and applied as a logic one signal to the second input of NAND-gate 65. With both inputs conditioned, the NAND gate produces an output signal to set the buzzer flip-flop 71. The buzzer flip-flop produces an output signal to activate the buzzer oscillator 73 which drives the loudspeaker. The operator, upon hearing the audio signal generated by the loudspeaker, knows that data may have been erroneously entered into the data processor. This data may be cleared from the processor by means of a clear key on the keyboard. Such a key may also provide a signal on the lead 79 to reset the buzzer flip-flop and stop the buzzer oscillator.

The multivibrator 69 is activated so as to apply a 12 millisecond input signal to NAND-gate 65 each time a KB–6 signal is generated. However, if a second key is not depressed within 12 milliseconds of a first key, the output of the multivibrator drops to a logic zero signal before trigger 55 is activated to condition the second input of NAND-gate 65.

From the preceding description, it is seen that the present invention provides a novel keyboard input for a data processor, said keyboard providing correct entry of data into the processor even though the keys may be rolled by the operator, while at the same time providing means for indicating to the operator when a double strike has occurred and data may have erroneously been entered into the processor. The keyboard is of solid-state construction and requires no moving parts other than the key itself. The keyboard is rugged, reliable, and not subject to switch bounce as in some keyboards of the prior art. Furthermore, it is not sensitive to magnetic fields as are some prior art keyboards employing reed switches.

While a specific embodiment has been shown for the purpose of illustration, it will be understood that various modifications and substitutions may be made in the embodiment shown without departing from the spirit and scope of the invention as defined by the appended claims. For example, the diodes 28 may be eliminated and the trigger 39 connected to the point 57. In this case, the trigger 39 should be modified so as to be triggered by the voltage at point 57 as any one or more of the key switches is/are operated.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

We claim:

1. In an electronic keyboard having a plurality of selective actable keys, the improvement comprising:
- a constant current generator;
- a plurality of switch circuits each actuated by one of said keys;
- a plurality of parallel current conducting paths connected to the output of said constant current generator, each of said parallel paths including one of said switch circuits;
- first means responsive to said switch circuits for producing encoded output signals for application to data processing means according to which of said switch circuits are actuated;
- said means for sensing when at least one of said switch circuits is actuated, said second means producing an output signal as long as at least one of said switch circuits is actuated; and,
- third means responsive to each output signal from said second means for producing a gating signal of fixed duration for gating said encoded output signals into said data processing means.

2. The improvement as claimed in claim 1 and further comprising:
- fourth means connected to the output of said constant current generator for sensing when at least two of said switch circuits are actuated, said fourth means producing an output signal as long as at least two of said switch circuits are actuated; and,
- means responsive to the output signal of said fourth means for inhibiting the output signal of said second means.

3. The improvement as claimed in claim 2 and further comprising:
- a timing circuit responsive to said second means for producing a timing signal of predetermined duration; and,
- a comparison circuit responsive to said timing circuit and said fourth means for producing an error signal if said fourth means produces an output signal while said timing signal is being produced.

4. The improvement as claimed in claim 3 and further comprising:
- a loudspeaker; and,
- means responsive to said error signal for feeding an audio signal to said loudspeaker.

5. The improvement as claimed in claim 4 wherein said fourth means includes trigger means for sensing the voltage at the output of said constant current generator and said second means includes trigger means for sensing the voltages in individual ones of said parallel paths.

6. The improvement as claimed in claim 2, wherein said third means includes pulse forming circuitry for producing said gating signal in predetermined timed relation to the leading edge portion of each output signal from said second means, the termination of said output signal from said fourth means, while one of said switching circuits remains actuated, being operative to provide, in effect, an additional output signal from said second means.

7. In an electronic keyboard having a plurality of selectively operable keys, the improvement comprising:
- an oscillator;
- a constant current generator having an output;
- a voltage source;
- a plurality of switch circuits, one for each of said keys, and each comprising,
- a transistor having an emitter connected to a voltage source,
- a collector connected through a resistor to the output of said constant current generator, and,
- a parallel resonant circuit including a coil and a capacitor connected between said voltage source and the base of the transistor,
- means connecting said oscillator to the base of each of said transistors;
- means mounted on each said key for selectively tuning or detuning the parallel resonant circuit of the corresponding key switch to thereby turn on the corresponding transistor whereby parallel current paths are established between said voltage source and said constant current generator when a plurality of said keys are operated; and,
- means electrically connected to said transistors for producing an indication corresponding to the operated keys.

8. The improvement as claimed in claim 7 and further comprising:
- first means including first trigger means for producing a first signal as long as any one of said transistors is on;

second means including second trigger means for producing a second signal as long as any two or more of said transistors is on; and,

third means responsive to said second means for inhibiting said first signal as long as any two or more of said transistors is on.

9. The improvement as claimed in claim **8** wherein said second trigger means is connected between the output of said constant current source and said resistors to sense the voltage thereat.

10. The improvement as claimed in claim **9** and further comprising:

further means responsive to said first and third means for producing a gating pulse of fixed duration each time said first signal is initiated.

11. The improvement as claimed in claim **10** and further comprising:

timing means responsive to said further means for producing a timing signal of predetermined duration each time a said gating signal is produced; and,

means responsive to said timing means and said second means for producing an error signal occurs during a said timing signal.

12. The improvement as claimed in claim **11** where in each switch circuit includes a diode said first trigger means being connected through said diodes to the collectors of each of said transistors to sense the voltages thereat.

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