(54) Title: AUTOMATIC GAIN CONTROL FOR RECEIVED SIGNAL STRENGTH INDICATION
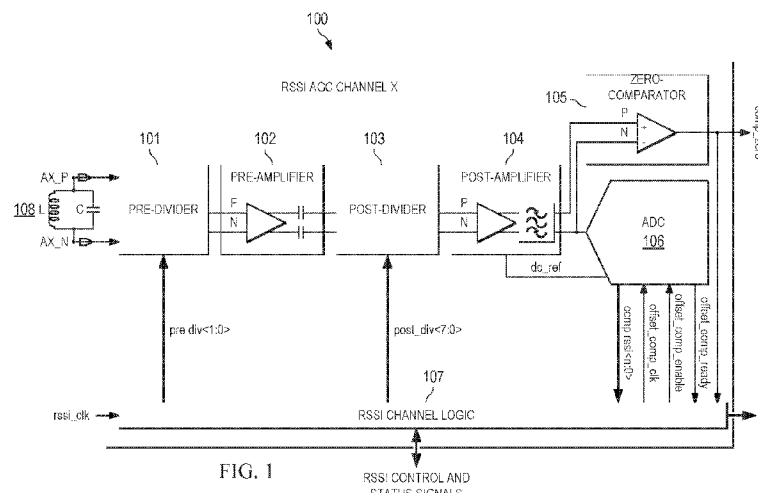
FIG. 1

(57) Abstract: In some implementations, an automatic gain control (AGC) circuit comprises: a pre-divider circuit operable to pre-divide an input signal according to a pre-divider circuit setting and output a pre-divided signal; a pre-amplifier operable to pre-amplify the pre-divided signal and output a pre-amplified signal; a post-divider circuit operable to post-divide the pre-amplified signal according to a post-divider circuit setting; an analog-to-digital converter (ADC) operable to generate a digital data stream from the post-divided signal; logic operable to sample the digital data stream; determine a pre-divider circuit setting and a post-divider circuit setting based on the sampled data stream; set the pre-divider circuit and the post-divider circuit based on the determined settings; and generate a received signal strength value based on the pre-divider circuit setting and the post-divider circuit setting.

AUTOMATIC GAIN CONTROL FOR
RECEIVED SIGNAL STRENGTH INDICATION

TECHNICAL FIELD

[0001]   The subject matter of this disclosure relates generally to determining received signal strength of magnetic fields.

BACKGROUND

[0002]   A received signal strength indicator (RSSI) of enforced electro-magnetic or pure magnetic fields can be used in vehicle access or passive-entry-go (PEG) systems to determine the distance between a transmitter located in the vehicle and a receiving system located in a key fob. The RSSI can be determined by measuring the voltage of a continuous waveform (CW) signal that is transformed from an electro-magnetic or pure magnetic field by an antenna or a coil. If the CW signal is corrupted by distortion the constant envelope of the CW signal starts to vary, leading to inaccurate RSSI information and an inaccurate distance measurement.

SUMMARY

[0003]   In some implementations, an automatic gain control (AGC) circuit comprises: a pre-divider circuit operable to pre-divide an input signal according to a pre-divider circuit setting and output a pre-divided signal; a pre-amplifier operable to pre-amplify the pre-divided signal and output a pre-amplified signal; a post-divider circuit operable to post-divide the pre-amplified signal according to a post-divider circuit setting; an analog-to-digital converter (ADC) operable to generate a digital data stream from the post-divided signal; and logic operable to: sample the digital data stream; determine a pre-divider circuit setting and a post-divider circuit setting based on the sampled data stream; set the pre-divider circuit and the post-divider circuit based on the determined settings; and generate a received signal strength value based on the pre-divider circuit setting and the post-divider circuit setting.

[0004]   In some implementations, a method of automatic gain control (AGC) performed by an AGC circuit comprises: pre-dividing, by a pre-divider circuit, an input signal according to a pre-divider circuit setting and outputting a pre-divided signal; pre-amplifying, by a pre-amplifier, the pre-divided signal and outputting a pre-amplified signal; post-dividing, by a post-divider circuit, the pre-amplified signal according to a post-divider circuit setting; generating, by an analog-to-digital converter (ADC), a digital data stream from the post-divided signal; sampling the digital data stream; determining a pre-divider circuit setting and a post-divider circuit setting based on the sampled data stream; setting the pre-divider circuit and the post-

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divider circuit based on the determined settings; and generating a received signal strength value based on the pre-divider circuit setting and the post-divider circuit setting.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005]   FIG. 1 is a block diagram of an example AGC circuit for RSSI, according to an embodiment.

[0006]   FIG. 2 is a schematic diagram of an example pre-divider circuit, according to an embodiment.

[0007]   FIG. 3 is a schematic diagram of an example pre-amplifier circuit, according to an embodiment.

[0008]   FIG. 4 is a schematic diagram of an example post-divider circuit, according to an embodiment.

[0009]   FIG. 5 is a schematic diagram of an example post-amplifier, according to an embodiment.

[0010]   FIG. 6 is a schematic diagram of an example subranging analog-to-digital converter (ADC), according to an embodiment.

[0011]   FIG. 7 illustrates example waveforms of the subranging ADC of FIG. 6 operating in an automatic offset compensation mode, according to an embodiment.

[0012]   FIGS. 8 and 9 illustrate an example operating mode of the subranging ADC of FIG. 6 after an automatic offset compensation process, according to an embodiment.

[0013]   FIGS. 10-11 illustrate an example zero comparator, according to an embodiment.

[0014]   FIGS. 12-20 illustrate example digital control circuit, according to an embodiment.

[0015]   FIGS. 21-26 illustrate AGC circuit performance, according to an embodiment.

[0016]   FIG. 27 is a flow diagram of an example process performed by an AGC circuit, according to an embodiment.

DETAILED DESCRIPTION

Example System

[0017]   FIG. 1 is a block diagram of an example digital AGC circuit 100 for received RSSI, according to an embodiment. AGC circuit 100 allows fast tracking of an envelope of CW input signals (AX_P, AX_N). AGC circuit 100 can be implemented in a single ended configuration or a symmetrical configuration. In the embodiment shown, AGC circuit 100 is

implemented in a symmetrical configuration and AX_P, AX_N are positive (P) and negative (N) symmetrical CW input signals, respectively. In the figures that follow, only the P side of the circuitry is shown. For a symmetrical configuration the N side is complemented by mirroring the positive side circuitry at a ground line. AGC circuit 100 is for a single RSSI AGC channel X. In an embodiment, the CW input signals are transformed from an electromagnetic or pure magnetic field by transducer 108, which can be, for example, an antenna or coil.

[0018]   In an embodiment, AGC circuit 100 includes pre-divider circuit 101, pre-amplifier 102, post-divider circuit 103, post-amplifier 104, zero comparator 105, subranging ADC 106 and RSSI channel logic 107. Each of these components will be described in detail in the description that follows.

[0019]   AGC circuit 100 provides several advantages over other systems and methods for generating RSSI values, including but not limited to: I) divider and amplifier partitioning into a chain of pre-divider, pre-amplifier, post-divider and post-amplifier to improve CNR and INL thus improving measurement accuracy; ii) the pre-divider tap is unchanged until the CW input signals reach a defined level so noise due to pre-divider attenuation is not increased while the CW input signals increase; iii) for low CW input signals, the pre-divider circuit includes a bypass setting so that low CW input signals are amplified prior to undergoing further voltage division by the post-divider circuit; iv) the pre-divider circuit operates directly at the coil and has a high impedance because it operates with a low number of taps that are loaded by parasitic capacitances; v) a higher degree of freedom to adjust circuit parameters for low noise and high linearity; vi) a subranging ADC in the feedback path instead of feedback based on a comparator, which provides fast envelope tracking (fast measurement update rate) to allow averaging of more measurement values in the same measurement period resulting in better accuracy; vii) allows capture of an amplitude modulated signal; and viii) settling time duration is shorter and better defined.

Example Pre-Divider Circuit

[0020]   FIG. 2 is a schematic diagram of an example pre-divider circuit 101, according to an embodiment. Pre-divider circuit 101 attenuates a strong CW input signal using a resistive divider in a single ended or symmetrical configuration. For clarity of discussion, only the positive side for processing AX_P <pre_div_in_p> is shown in FIG. 2. Pre-divider circuit 101 includes resistive divider 200 comprising a number of resistive elements coupled in series to provide 4 tap points, which are selectively coupled to the output of multiplexer (MUX) 203 by

switches. In other embodiments, a capacitive divider or resistive/capacitive ladder network can be used to divide low frequency CW input signals and a PI or TEE attenuator can be used to divide high frequency CW input signals.

[0021]   MUX 203 includes a series of switches and a decoder (not shown) that activates one tap point depending on a decoded setting (pre_div). In an embodiment, pre_div is a control word (pre_div<1:0>) provided by RSSI channel logic 107 in FIG. 1. MUX 203 also includes a bypass switch for bypassing the division of weak CW input signals. The output of MUX 203 (pre_div_out_p) is a divided AX_P or an undivided AX_P if pre-divider circuit 101 is configured in a bypass mode. Although resistive divider 200 is shown as including 4 tap points, any desired number of tap points can be used in resistive divider 200 by using an appropriate number of resistive elements and sizing pre_div accordingly. In some implementations, the range of attenuation is given by Equation [1]:

$$a\_prediv_{range} = \frac{V_{pre\_div\_out}}{V_{pre\_div\_in}}.$$

[1]

Example Pre-Amplifier

[0022]   FIG. 3 is a schematic diagram of an example pre-amplifier 102, according to an embodiment. Pre-amplifier 102 is a low noise, high linearity gain amplifier that can be implemented in a single ended or symmetrical configuration. Pre-amplifier 102 can include one or more stages with fixed gain. The input impedance of pre-amplifier 102 can be matched to an antenna impedance to reduce noise. In an embodiment, pre-amplifier 102 can include an operational amplifier 300 and capacitors 301a, 301b coupled to the outputs of operational amplifier 300 to provide DC decoupling when pre-amplifier 102 is resistively loaded (e.g., by post-divider 103). For high frequency signals, pre-amplifier 300 can be replaced by a frequency conversion circuit. The pre-amplifier gain is given by Equation [2]:

$$Gain_{pre\_amp} = \frac{V_{pre\_amp\_out}}{V_{pre\_amp\_in}}.$$

[2]

Example Post-Divider Circuit

[0023]   FIG. 4 is a schematic diagram of an example post-divider circuit 103, according to an embodiment. Post-divider circuit 103 can be implemented in a single ended or symmetrical configuration. FIG. 400 shows only the P side circuitry. Post-divider circuit 103 attenuates the output of pre-amplifier 300 for measurement purposes using resistive divider 400. Resistive divider 400 includes a number of resistive elements coupled in series to provide 256 tap points, which are selectively coupled to the output of multiplexer (MUX) 402 by switches. A decoder in post-divider 103 (not shown) activates one tap point depending on setting post_div. In an embodiment, post_div can be a control word (post_div <7:0>) provided by RSSI channel logic 107. Post-divider circuit 103 also includes a bypass switch for bypassing weak CW input signals.   In other embodiments, a capacitive divider, resistive/capacitive ladder network can be used to divide low frequency CW input signals and a PI or TEE attenuator can be used to divide high frequency CW input signals. Although resistive divider 400 is shown as including 256 taps, any desired number of taps can be used in resistive divider 200 by using an appropriate number of resistive elements and sizing the selection signal accordingly.

[0024]   In an embodiment, a post-divider ratio α_{post_div} can be determined by taking a logarithm of a ratio of the post-divider input voltage ($V_{post\_div\_in}$) and the post-divider output voltage ($V_{post\_div\_out\_p}$), where the post-divider ratio α_{post_div} is given by:

$$\alpha_{post\_div} = \frac{V_{post\_div\_out}}{V_{post\_div\_in}} = B^{-post\_div},$$

[3]

$$post\_div = log_B \left(\frac{V_{post\_div\_in}}{V_{post\_div\_out}} \right),$$

[4]

where base B determines the measurement resolution (e.g., B=1.02345).   In another embodiment, other post-divider ratio can be used to achieve different measurement resolutions (e.g., cubic root).

Example Post-Amplifier Circuit

[0025]   FIG. 5 is a schematic diagram of an example post-amplifier 104, according to an embodiment. Post-amplifier 104 is a low noise, high linearity gain amplifier that can be implemented in a single ended or symmetrical configuration. Post-amplifier 104 can include one or more stages with fixed gain. The input impedance of post-amplifier 104 can be matched

to the post-divider impedance to reduce noise. In an embodiment, post-amplifier 104 can include operational amplifier 500 having an output coupled to band pass filter 501 to limit bandwidth to achieve low total root-mean-square (RMS) noise. Band pass filter 501 can be configured to exhibit low group delay to allow fast operation of the AGC loop. Band pass filter 501 can be located in its own block or distributed into gain stages by resistive-capacitive (RC) loading (low pass) and capacitive series feedback (high pass). The post-amplifier gain is given by Equation [5]:

$$Gain_{post\_amp} = \frac{V_{post\_amp\_out}}{V_{post\_amp\_in}}.$$

[5]

Example Subranging ADC and Zero-Comparator Circuit

[0026]   FIG. 6 is a schematic diagram of an example subranging analog-to-digital converter (ADC) 106, according to an embodiment. In the embodiment shown, ADC 106 is a 5-bit flash ADC with automated offset compensation. In another embodiment, a successive approximation (SAR) ADC can be used. In the embodiment shown, ADC 106 operates in a unipolar configuration to reduce chip size by reducing the number of components (e.g., comparators). In another embodiment, a bipolar configuration can be used. In the embodiment shown, ADC 106 is DC coupled to preceding post-amplifier 104. In another embodiment, ADC 106 and post-amplifier 104 can be DC decoupled.

[0027]   Referring to FIG. 6, ADC 106 includes reference voltage stage 601 and comparator stage 602. Reference voltage stage 601 generates reference voltages (Vref_0-Vref_n) for comparators 603_0 to 603_n (e.g. n=31) in comparator stage 602. In the example embodiment of FIG. 6, there are n +1 comparators and only comparator 603_0 and comparator 603_n are shown. Reference voltage stage 601 includes operational amplifier 604 with a non-inverting input coupled to a DC reference (dc_ref) and an inverting input coupled to an offset voltage (VDC) that occurs across resistor 605 (RDC). The voltage output of operational amplifier 604 steers a voltage controlled current source 610 that acts on resistive ladder 606, which includes resistive elements R0...Rn (e.g., R0-R31) to generate reference voltages and resistor 605 to generate the offset voltage VDC that is controlled in a feedback loop.

[0028]   A first input of each of comparators 603_0 to 603_n is coupled to the ADC input (adc_in_n) by corresponding series switches 607_0 to 607_n. A second input of each comparator 603_0 to 603_n is coupled to a tap point of resistive ladder 606. Series switches

607_0 to 607_n are controlled by an offset compensation enable signal (offset_comp_enable) generated by RSSI channel logic 107. Parallel switches 608_0 to 608_n couple the inputs of comparators 603_0 to 603_n together, resulting in offset voltages to appear at the outputs of comparators 603_0 to 603_n. The outputs of comparators 603_0 to 603_n are compensated RSSI values (comp_rssi_0 to comp_rssi_n), which are input into offset compensation logic 609.

[0029]   In an embodiment, offset compensation logic 609 includes circuitry for generating offset calibration signals (offset_cal_0 to offset_cal_n) for comparators 603_0 to 603_n based on the compensated RSSI values (comp_rssi_0 to comp_rssi_n) received from the outputs of comparators 603_0 to 603_n. For example, during an offset compensation mode, series switches 607_0 to 607_n are opened to disconnect comparators 603_0 to 603_n from the ADC input (adc_in_n) and parallel switches 608_0 to 608_n are closed to short together inputs of comparators 603_0 to 603_n. This causes voltage offsets to appear at the outputs of comparators 603_0 to 603_n. The voltage offsets are input to offset compensation logic 609, which includes circuitry for generating and providing offset calibration values (offset_cal_0 to offset_cal_n) based on the voltage offsets. The offset calibration values are used to compensate for the offset voltages. When offset compensation is completed, offset compensation logic 609 generates an offset compensation ready signal (offset_comp_ready), which is sent to RSSI channel logic 107, as shown in FIG. 1. Offset compensation logic 609 is coupled to an offset compensation clock (offset_comp_clk) generated by RSSI channel logic 107.

[0030]   FIG. 7 illustrates example waveforms related to the automated offset compensation mode, according to an embodiment. Before any measurement can be started an offset compensation is carried out by disabling the inputs of comparators 603_0 to 603_n from adc_in_n by series switches 607_0 to 606_n and connecting for each comparator 603_0 to 603_n both inputs to Vref_x by parallel switches 608_0 to 608_n via signal offset_comp_enable. Each of comparators 603_0 to 603_n has the ability to program an artificial offset voltage between its inputs within a certain range (e.g., +/- 40mV) by enforcing an imbalance via signal offset_cal_x<n:0>. The step width of the artificial offset voltage is binary weighted (e.g., 40, 20, 10, 5, 2.5 and 1.25 mV). Offset compensation logic 609 controls the compensation process flow using a successive approximation procedure that is activated by signal offset_comp_enable. For each comparator 603_0 to 603_n the largest step is activated with the first falling edge of signal offset_comp_clk (e.g. via offset_cal_x<5>). The second falling edge offset_cal_x<5> is kept high if comparator output stays logically high, otherwise it is set back to logically low and the state of offset_cal_x<5> is latched until

offset_comp_ready is cleared. This offset compensation procedure is repeated for the next lower offset_cal_x bits in a sequential manner. If all offset_cal_x bits are processed signal flag offset_comp_ready is set.

[0031] FIGS. 8 and 9 illustrate an example operating mode of subranging ADC 106 of FIG. 6 after an offset compensation process, according to an embodiment. In operating mode after offset compensation process has finished shorted parallel switches 608_0 to 608_n are opened and series switches 607_0 to 607_n are closed. All comparators 603_0 to 603_n where reference voltages Vref_0 to Vref_n are exceeded by the amplitude of input signal adc_in_n are set to logical high. In an embodiment, the comparator output signals comp_rssi<n:0> are a quantized data stream of thermometer codes related to the instantaneous amplitude value of adc_in_n (quantization only). Sampling of the thermometer codes is performed in RSSI channel logic 107.

[0032] Reference voltage stage 601 includes voltage controlled current source 609 that feeds resistive ladder 606 and operational amplifier 604 that operates in a feedback loop. Vdc across a lowest resistor R0 is sensed and compared to Vdc_ref that is provided by post-amplifier 104 via signal input dc_ref. The voltage difference between both potentials controls current source 610 in a way that after a settling time operating current will produce a voltage drop across resistor R_{DC} with Vdc = Vdc_ref. The reference voltages Vref_x are based on this operating current and the divider ratios for different tap points. The divider ratios are chosen to match to post-divider ratios (e.g., a logarithmic type). In this embodiment, using a 5-bit subranging ADC 106 at Vref_15, the AGC loop operates in its equilibrium state where no post-divider correction occurs:

$$V_{ac} = V_{ac\_eq} = V_{ref\_15} - V_{dc_{ref}}.$$

[6]

[0033] The divider ratio is derived from the relative change of the CW input signal:

$$\Delta V_{ac\_rel_x} = \frac{V_{ref\_x} - V_{ref\_15}}{V_{ac\_eq}} = B^{post\_div\_corr\_x},$$

[7]

with base B is the value chosen for post-divider circuit 103 (e.g., B=1.02345 e.g.).

[0034]   For AC voltages beyond AGC loop equilibrium post-divider correction is linear stepped if Vac is close to equilibrium for accuracy reasons and nonlinear stepped for speed reasons. Referring to FIGS. 8 and 9, example post-divider correction words are given by Equation [8]:

$$post\_div\_corr_x = \begin{cases} -24 & x = 0 \\ -18 & x = 1 \\ \pm(x - 15) & for\ 2 \leq x \leq 29 \\ 18 & x = 30 \\ 24 & x = 31, \end{cases}$$

[8]

with x=15 being the equilibrium state in this example.

[0035]   The post-divider correction word (post_div_corr) is calculated in RSSI channel logic 107 based on signal comp_rssi<31:0> (assuming 32 comparators) delivered from subranging ADC 106, but has been introduced here to make the overall functionality of AGC circuit 100 more clear.

[0036]   FIG. 10 illustrates an example zero-comparator 105, according to an embodiment. Parallel to subranging ADC comparators 603_0-603_n is zero-comparator 105 offset compensated before any measurement can be started (not shown). During operation symmetrical AC output signal of post-amplifier 104 is connected to P and N inputs of zero-comparator 105, as shown in FIG. 1. The positive edge of output signal comp_zero represents the zero phase of the symmetrical AC signal at its input, as shown in FIG. 11.

Example RSSI Channel Logic Circuit

[0037]   Referring again to FIG. 1, RSSI channel logic 107 fulfills several functions within AGC circuit 100. RSSI channel logic 107 performs peak detection by sampling a quantized data stream comp_rssi<n:0> delivered from subranging ADC 106 and finding the peak value therein. RSSI channel logic 107 controls the settings of pre-divider circuit 101 and post-divider circuit 103 depending on the detected peak value. RSSI channel logic 107 calculates RSSI result words rssi<k:0> and streams the RSSI result words to results registers or further calculation units (e.g. averaging units). RSSI channel logic 107 provides clocks derived from master clock rssi_clk (e.g. offset_comp_clk). RSSI channel logic 107 includes a state machine to control overall measurement flow, provide correction procedure and handle communication to a master state machine.

[0038]   FIGS. 12 and 13 illustrate example peak detection performed by RSSI channel logic 107 of FIG. 1, according to an embodiment. RSSI channel logic 107 samples the quantized data stream comp_rssi and finds the peak value therein. Note that to make the peak detection procedure more clear, FIGS. 12 and 13 show a continuous sine wave on adc_in_n instead of a quantized data stream on comp_rssi at the output of ADC 106 where sampling actually occurs. The 0° of the continuous sine wave at adc_in_n is indicated in FIGS. 12 and 13 by a positive edge of comp_zero. Other phases of the sine wave at adc_in_n can be determined by counting clock edges of rssi_clk. For example, with a 125kHz sine wave and a 6MHz clock the 13th and 19th negative edge of rssi_clk corresponds to time points 90° and 135°. In a maximum hold mode (MHM), envelope or non-coherent detection is performed. Starting from 0° until 135° at each negative edge of rssi_clk the highest bits of comp_rssi showing a logical high will be latched. The last sample taken indicates the peak value. In a maximum sample mode (MSM), quasi coherent detection is performed. At 90° a sample of comp_rssi will be taken and the highest bit with a logical high indicates peak value. Both modes allow for divider change within one period of the sine wave if calculation delay and analog settling (group delay) < 270°(MSM)/225°(MHM).

[0039]   Detected peak values will be converted into post-divider correction values (post_div_corr) according to Equation [8] and added together from sample measurement to sample measurement to evaluate the post_div word that adjusts post-divider 103:

$$post\_div_i = \sum_i post\_div\_corr_i$$

[9]

with i being the number of sample measurements and initial condition post_div_corr$_0$ =0.

[0040]   FIGS. 14-17 illustrate an example static operation of divider control performed by RSSI channel logic of FIG. 1, according to an embodiment. With logarithmic AGC loop in equilibrium the transfer function of Vin to Vac_eq can be solved and reordered for post_div value that depends on range setting of pre-divider 101 using Equations [1]-[3] and [5]:

$$post\_div_{range} = log_B \left(\frac{V_{in} \cdot a\_pre\_div_{range} \cdot Gain_{pre\_amp} \cdot Gain_{post\_amp}}{V_{ac\_eq}} \right),$$

[10]

with $0 \leq post\_div_{range} \leq 255$ and $0 \leq range \leq 3$.

[0041]   With the sensitivity defined as smallest detectable voltage Equation [11] gives:

$$V_{sens} = \frac{V_{ac\_eq}}{Gain_{pre\_amp} \cdot Gain_{post\_amp}}.$$

[11]

[0042]   With the pre-divider ratio expressed as a shift of post-divider value, Equation [12] gives:

$$pre\_div_{range} = log_B \left(\frac{1}{a\_pre\_div_{range}} \right).$$

[12]

[0043]   Or expressed as a relative shift from one range to a next range Equation [13] gives:

$$pre\_div_{range} = pre\_div_{0,1} + \cdots + pre\_div_{(range-1),range}.$$

[13]

[0044]   Due to post-divider curve overlap for certain V_{in} values a calibration procedure is able to find initially unknown pre-divider ratios by measuring post_div values while keeping V_{in} constant and forcing the range setting to range and (range-1) successively as shown in FIG. 15:

$$pre\_div_{(range-1),range} = post\_div_{range} - post\_div_{(range-1)}.$$

[14]

[0045]   Although the physical pre-divider ratio remains unchanged by this calibration procedure it is useful for calculating correct RSSI words from post_div and calibrated pre_div words as described in further detail below.

[0046]   Due to post-divider curve overlap there is also a certain flexibility when to change from (range-1) to actual range and can be used to operate on the most accurate part of the post divider curve. For small post_div values (<100) strong noise influence by the resistive divider occurs. To prevent distortion due to the pre-divider switching the ranges can be

changed only during a short tracking period (initial settling of AGC) and in rising direction for Vin changes, afterwards post-divider can act on curve defined by the range setting. In FIG. 16, when post_div value exceeds 207 to achieve equilibrium in range 1, pre_div is changed by 1 step thus reducing post_div by 89 steps. After AGC settling, post_div is acting on a fixed curve giving a headroom of 48 steps upwards and 118 steps downward for any Vin changes during capture phase. The RSSI value is calculated from post_div, range and pre_div according to Equation [15]:

$$rssi = \begin{cases} post\_div & range = 0 \\ post\_div + \sum_{i=1}^{range} pre\_div_{(i-1),i} & range > 0. \end{cases}$$

[15]

[0047]   FIGS. 18-19 illustrate an example dynamic operation of divider control performed by RSSI channel logic 107 of FIG. 1, according to an embodiment. The AGC principle is dedicated to measure the envelope of bursted AC input voltages. During programmable tracking time ($T_{tracking}$) the AGC circuit tries to follow the envelope's rising edge thereby changing the post-divider value and range setting accordingly to an instantaneous peak amplitude of the input voltage. After any range change has occurred a programmable wait time (T_{range_delay}) keeps the divider settings unchanged so that the analog circuitry within the AGC loop settles before any new divider settings can be performed. If bursted AC input voltage has become a stable continuous wave signal (CW) capturing of momentary RSSI values starts within a programmable length ($T_{capture}$) for further processing (e.g. averaging). During capture time the last range setting of the tracking phase will be kept constant and only post-divider 103 is working to refresh RSSI values.

[0048]   FIG. 20 illustrates an example state machine implemented by RSSI channel logic 107 of FIG. 1, according to an embodiment. With signal agc_enable AGC circuit 100 will be started. After a wait time T1 for settling of the analog part (e.g., amplifier, filter, etc.) offset compensation can be started via signal offset_comp_enable. Clock offset_comp_clk that is derived from rssi_clk for offset compensation will be started. Within wait time T2 a successive approximation procedure is executed to compensate for offsets and its end is indicated by flag offset_comp_ready. With flag offset_com_ready set one or more measurements can be initiated by signal measurement_enable. If an AC voltage burst is active at AGC input AGC circuit 100 tracks its envelope during a tracking phase and takes samples of the envelope during a capturing phase. While both dividers can be regulated during the

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tracking phase, post-divider 103 can be regulated during the capture phase. Signal comp_zero is available during tracking and capturing time.

Performance

[0049]   FIGS. 21-22 illustrate analog performance of AGC circuit 100, according to an embodiment. From input to post-amplifier output analog performance is determined as static integrated non-linearity (INL_static) and carrier-to-noise ratio (CNR) for a closed AGC loop in equilibrium. INL_static is defined as the deviation between a measured and an ideal calculated RSSI curve with noise effects excluded:

$$\text{INL\_static} = rssi_{measured} - rssi_{calc}.$$

[16]

[0050]   CNR at the input of ADC 106 is defined as:

$$CNR = 20 \cdot log_{10}\left(\frac{veff_{post\_amp\_out(V_{in})}}{V_{noise\_rms_{post\_amp\_out(V_{in})}}}\right),$$

[17]

with effective AC voltage and over frequency bandwidth integrated noise voltage density at post-amplifier output.

[0051]   A typical curve for INL_static shows linearity error in RSSI steps <0.5 up to range 2 and <1 for range 3. A typical curve for CNR shows values ≥25dB for input levels >600μVpp.

[0052]   FIGS. 23-24 illustrate digital performance of AGC circuit 100, according to an embodiment. For a closed AGC loop in equilibrium RSSI values are simulated when CNR is varied at subranging ADC input and evaluated for median (INL_statistic) and variance (σ) with a spectral noise shape of the analog part and different numbers of averaging. Typical curves for INL_statistic do not show a dependency on the number of averages that have been used but there is a strong influence at low CNR values depending on the sampling method used. MHM mode shows a strong threshold effect for decreasing CNR starting from 15dB similar to that what is known for non-coherent detection. Maximum sample mode (MSM) shows a much weaker increase of INL_statistic that occurs due to nonlinear compression of logarithmic rssi curve when driven by strong noise fluctuations. Typical curves for σ show an improvement

with increasing CNR and increasing number of averages that have been used but there is nearly no influence by the sampling method used.

[0053]   FIGS. 25-26 illustrate measurement accuracy of AGC circuit 100, according to an embodiment. The overall accuracy is calculated by:

$$INL\_static + INL\_statistic + factor_{confidence} \cdot \sigma.$$

[18]

[0054]   With, e.g., $factor_{confidence}=2$ (a typical value for commercial measurement systems) 95% off all measurement results are within boundary as shown in FIG. 25. A typical curve shows for 256 averages accuracy <2 RSSI steps for all ranges and <1 RSSI step for a reduced input range of 200μVpp<Vin<1Vpp. With 1 RSSI step being B-1=2.345% accuracy can alternatively be expressed in %, as shown in FIG. 26. Measurement accuracy does not take variation of Vsens due to temperature or voltage supply condition into account, this is discussed somewhere else.

Example Process

[0055]   FIG. 27 is a flow diagram of an example process 2700 performed by the digital automatic gain control circuit (DAGC) of FIG. 1, according to an embodiment. Process 2700 can be performed by AGC circuit 100. In an embodiment, process 2700 begins by pre-dividing CW input signal(s) (2701), as described in reference to FIG. 2. Process 2700 continues by pre-amplifying the signal(s) (2702), as described in reference to FIG. 3. Process 2700 continues by post-dividing the signal(s) (2703), as described in reference to FIG. 4. Process 2700 continues by post-amplifying the signal(s) (2704), as described in reference to FIG. 5. Process 2700 continues by generating a digital data stream (e.g., quantized data stream) from the signal(s) (2705), as described in reference to FIG. 6. Process 2700 continues by sampling the digital data stream and setting the pre-divider and post-divider based at least on the sampled digital data stream and divider settings (2706). Process 2700 continues by generating RSSI values based on divider setting and pre-divider correction (2707).

[0056]   While this document contains many specific implementation details, these should not be construed as limitations on the scope of what may be claimed but rather as descriptions of features that may be specific to particular embodiments. Certain features that are described in this specification in the context of separate embodiments can also be

implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable sub combination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can, in some cases, be excised from the combination, and the claimed combination may be directed to a sub combination or variation of a sub combination.

What is claimed is:

CLAIMS

1.   An automatic gain control (AGC) circuit, comprising:

a pre-divider circuit operable to pre-divide an input analog signal according to a pre-divider circuit setting and output a pre-divided analog signal;

a pre-amplifier operable to pre-amplify the pre-divided analog signal and output a pre-amplified analog signal;

a post-divider circuit operable to post-divide the pre-amplified analog signal according to a post-divider circuit setting and output a post-divided analog signal;

an analog-to-digital converter (ADC) operable to convert the post-divided analog signal into a digital data stream; and

logic operable to:

sample the digital data stream;

determine a pre-divider circuit setting and a post-divider circuit setting based on the sampled data stream;

set the pre-divider circuit and the post-divider circuit based on the determined settings; and

generate a received signal strength value based on the pre-divider circuit setting and the post-divider circuit setting.

2.   The AGC circuit of claim 1, wherein the digital data stream represents an instantaneous amplitude of the input analog signal at the ADC input during a current period of the input analog signal.

3.   The AGC circuit of claim 1, wherein the post-divider circuit can be configured to have different resolutions.

4.   The AGC circuit of claim 1, further comprising:

a post-amplifier between the post-divider circuit and the ADC input, the post-amplifier circuit operable to post-amplify the post-divided analog signal.

5.   The AGC circuit of claim 1, further comprising:

a bandpass filter inserted between antenna input terminals and the input of the
ADC.

6.   The AGC circuit of claim 1, wherein at least one of the pre-divider circuit is
operable to bypass the input analog signal based on a strength of the input analog
signal and the post-divider circuit is operable to bypass the pre-amplified input analog
signal based on a strength of the pre-amplified analog signal.

7.   The AGC circuit of claim 1, wherein at least one of the pre-divider circuit and
the post-divider circuit are configured as logarithmic dividers.

8.   The AGC circuit of claim 1, wherein the ADC is a flash ADC.

9.   The AGC circuit of claim 8, wherein the flash ADC is an offset compensated
flash ADC.

10.   The AGC circuit of claim 1, wherein the logic is further operable to:
        sample the digital data stream over a period of the input analog signal;
        detect a peak value from the sample; and
        determine the pre-divider and post-divider circuit settings based on the
detected peak value.

11.   The AGC circuit of claim 1, wherein the logic is further operable to:
        sample the digital data stream ninety degrees after a zero crossing of the input
analog signal; and
        determine the pre-divider and post-divider circuit settings based on the
detected peak value.

12.   The AGC circuit of claim 1, wherein the pre-divider circuit is configured to
have input impedance that is substantially constant for all pre-divider circuit settings.

13.   The AGC circuit of claim 1, wherein the logic is further configured to send
feedback values to the pre-divider circuit and to the post-divider circuit every n

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period(s) of the input analog signal for use in setting the pre-divider circuit and the post-divider circuit, where n is a positive integer greater or equal to one.

14. The AGC circuit of claim 13, wherein the feedback values are averaged to reduce an amount of data.

15. The AGC circuit of claim 14, wherein the feedback values are averaged based on at least one of a number of feedback values that occurred during a time period.

16. The AGC circuit of claim 1, wherein the received signal strength values are determined by ADC samples in combination with values of the pre-divider circuit and post-divider circuit.

17. The AGC circuit of claim 1, wherein the AGC circuit is further configured to:
    store calibration data for individual pre-divider circuit attenuations to increase an accuracy over a complete range of received signal strength values.

18. The AGC circuit of claim 1, where the logic is further configured to:
    enforce the pre-divider to a range setting;
    measure one or more averaged post-divider values that result from a constant and continuous wave signal at the AGC circuit input after the AGC circuit has settled in a first calibration measurement;
    enforce the pre-divider to a next range setting and measure one or more averaged post-divider values that result from the constant and continuous wave signal at the AGC circuit input after the AGC circuit has settled and by maintaining an amplitude of the signal at a level related to a preceding measurement for a second calibration measurement;
    store a difference of post-divider values derived from the first and second calibration measurements as a calibration value;
    repeat the calibration measurement and store steps for other ranges; and
    calculate each received signal strength value from a current measured post-divider value and from a summation of stored pre-divider calibration values of ranges which are less than or equal to a current range setting.
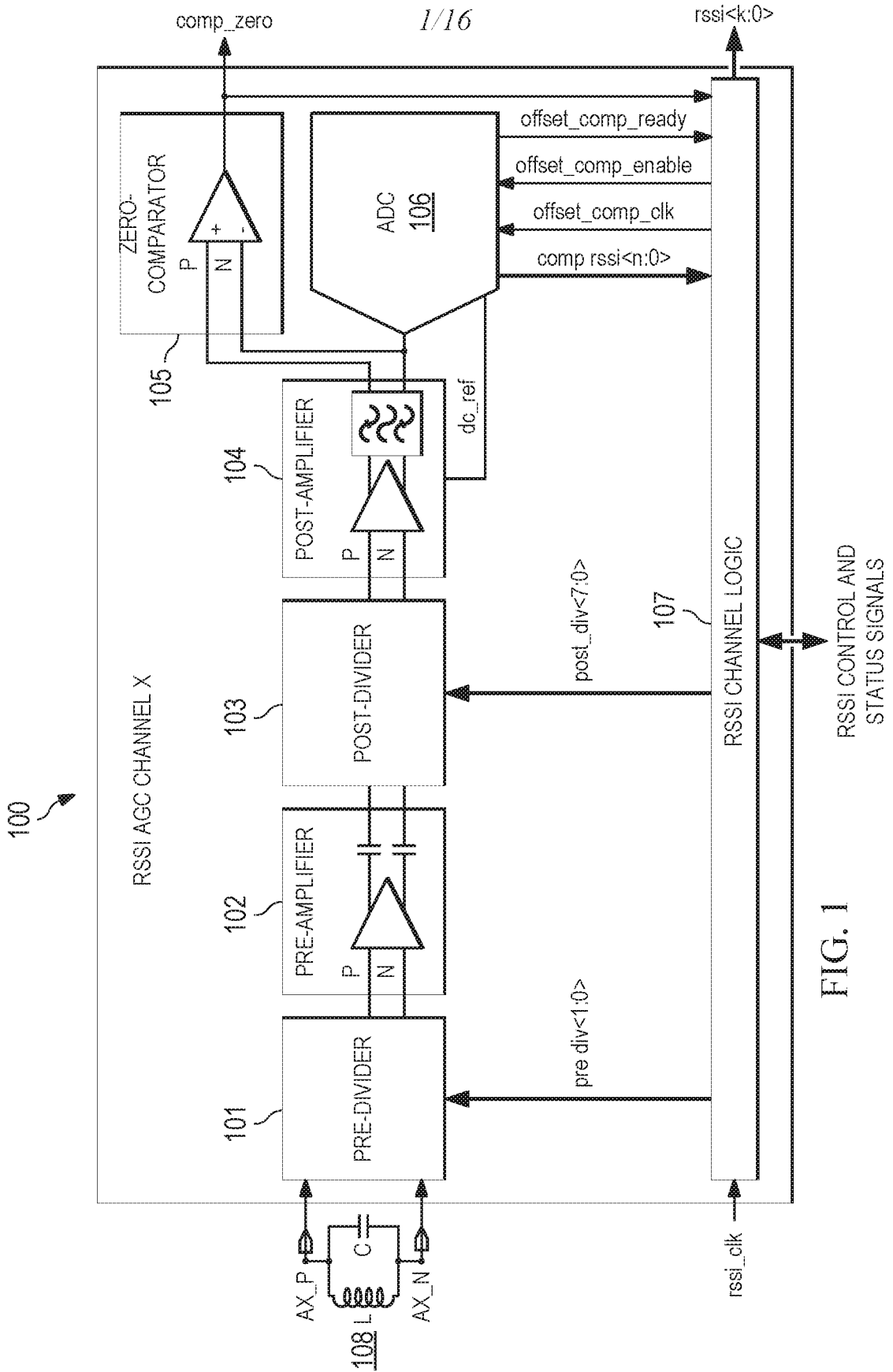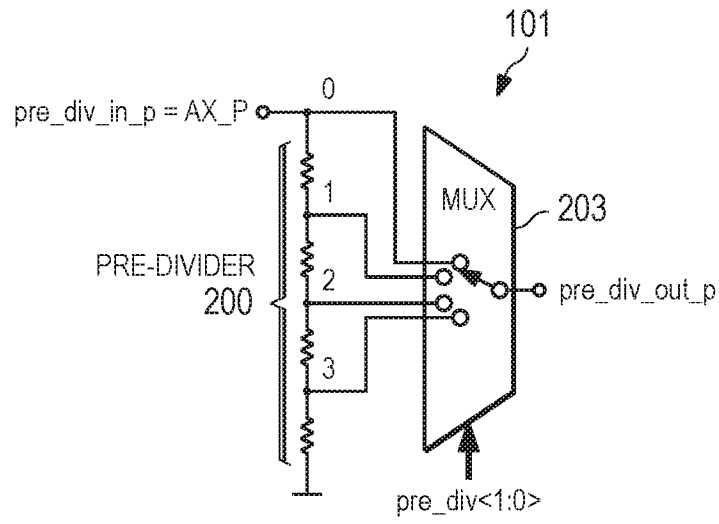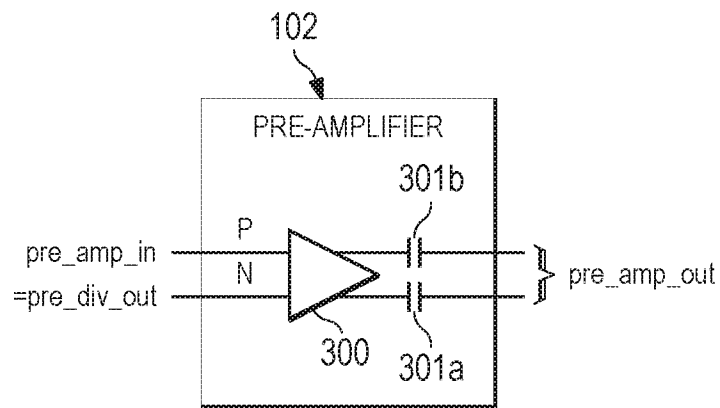
19.   A method of automatic gain control (AGC) performed by an AGC circuit,
comprising:

pre-dividing, by a pre-divider circuit, an input analog signal according to a
pre-divider circuit setting and outputting a pre-divided analog signal;

pre-amplifying, by a pre-amplifier, the pre-divided analog signal and
outputting a pre-amplified analog signal;

post-dividing, by a post-divider circuit, the pre-amplified analog signal
according to a post-divider circuit setting;

generating, by an analog-to-digital converter (ADC), a digital data stream
from the post-divided analog signal;

sampling the digital data stream;

determining a pre-divider circuit setting and a post-divider circuit setting
based on the sampled digital data stream;

setting the pre-divider circuit and the post-divider circuit based on the
determined settings; and

generating a received signal strength value based on the pre-divider circuit
setting and the post-divider circuit setting.

20.   The method of claim 19, wherein the digital data stream represents
instantaneous amplitude values of the input analog signal at the ADC for every signal
period.

21.   The method of claim 19, further comprising:

bypassing, by the pre-divider circuit, the input analog signal based on a
strength of the input analog signal; or

bypassing, by the post-divider circuit, the pre-amplified input analog signal
based on a strength of the pre-amplified analog signal.

22.   The method of claim 19, further comprising:

sampling the digital data stream over a period of the input analog signal;

detecting a peak value from the sample; and

determining the pre-divider and post-divider circuit settings based on the
detected peak value.

23.   The method of claim 19, further comprising:

sampling the digital data stream ninety degrees after a zero crossing of the input analog signal; and

determining the pre-divider and post-divider circuit settings based on the detected peak value.

24.   The method claim 19, further comprising:

sending feedback values to the pre-divider circuit and to the post-divider circuit every n period(s) of the input analog signal for use in setting the pre-divider circuit and the post-divider circuit, where n is a positive integer greater or equal to one.

25.   The method of claim 19, further comprising:

storing calibration data for individual pre-divider circuit attenuations to increase an accuracy over a complete range of received signal strength values.

26.   The method of claim 19, further comprising:

enforcing the pre-divider to a range setting;

measuring one or more averaged post-divider values that result from the input analog signal after the AGC circuit has settled in a first calibration measurement;

enforcing the pre-divider to a next range setting and measure one or more averaged post-divider values that result from the input analog signal after the AGC circuit has settled and by maintaining an amplitude of the input analog signal at a level related to a preceding measurement for a second calibration measurement;

storing a difference of post-divider values derived from the first and second calibration measurements as a calibration value;

repeating the calibration measurement and store steps for other ranges; and

calculating each received signal strength value from a current measured post-divider value and from a summation of stored pre-divider calibration values of ranges which are less than or equal to a current range setting.

FIG. 1

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FIG. 2

FIG. 3

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post_div_in_p =
pre_amp_out_p

POST-DIVIDER
400

post_div<7:0>

post_div_out_p

MUX   402

103

FIG. 4

104

POST-AMPLIFIER

post_amp_in

=post_div_out

P

N

500   501

post_amp_out

FIG. 5

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FIG. 6

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FIG. 7

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FIG. 8

FIG. 9

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ZERO-COMPARATOR

zero_comp_in ———— P +

=post_amp_out ———— N − ————————— comp_zero

FIG. 10

V_{dc_ref}

zero_comp_in_n

zero_comp_in_p

GND

comp_zero

0°   0°

FIG. 11

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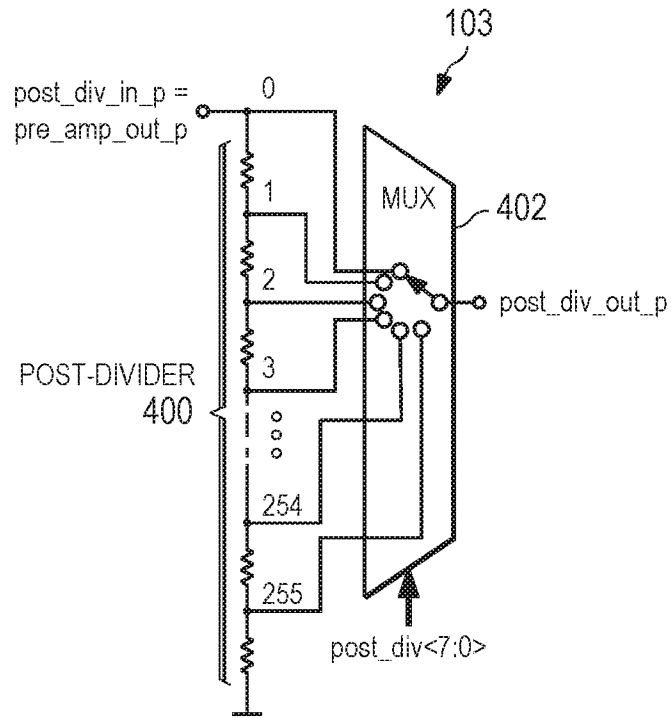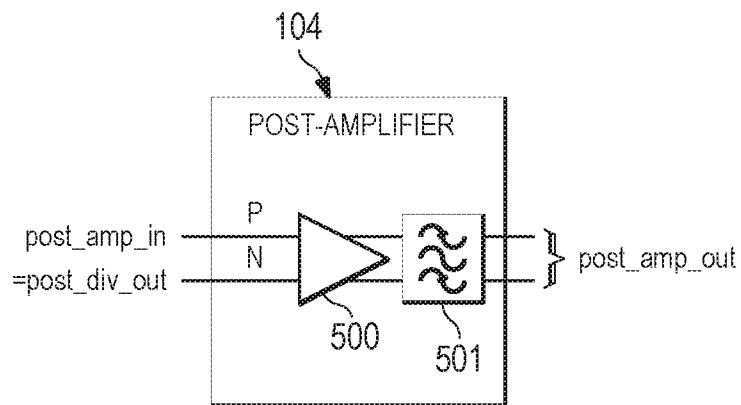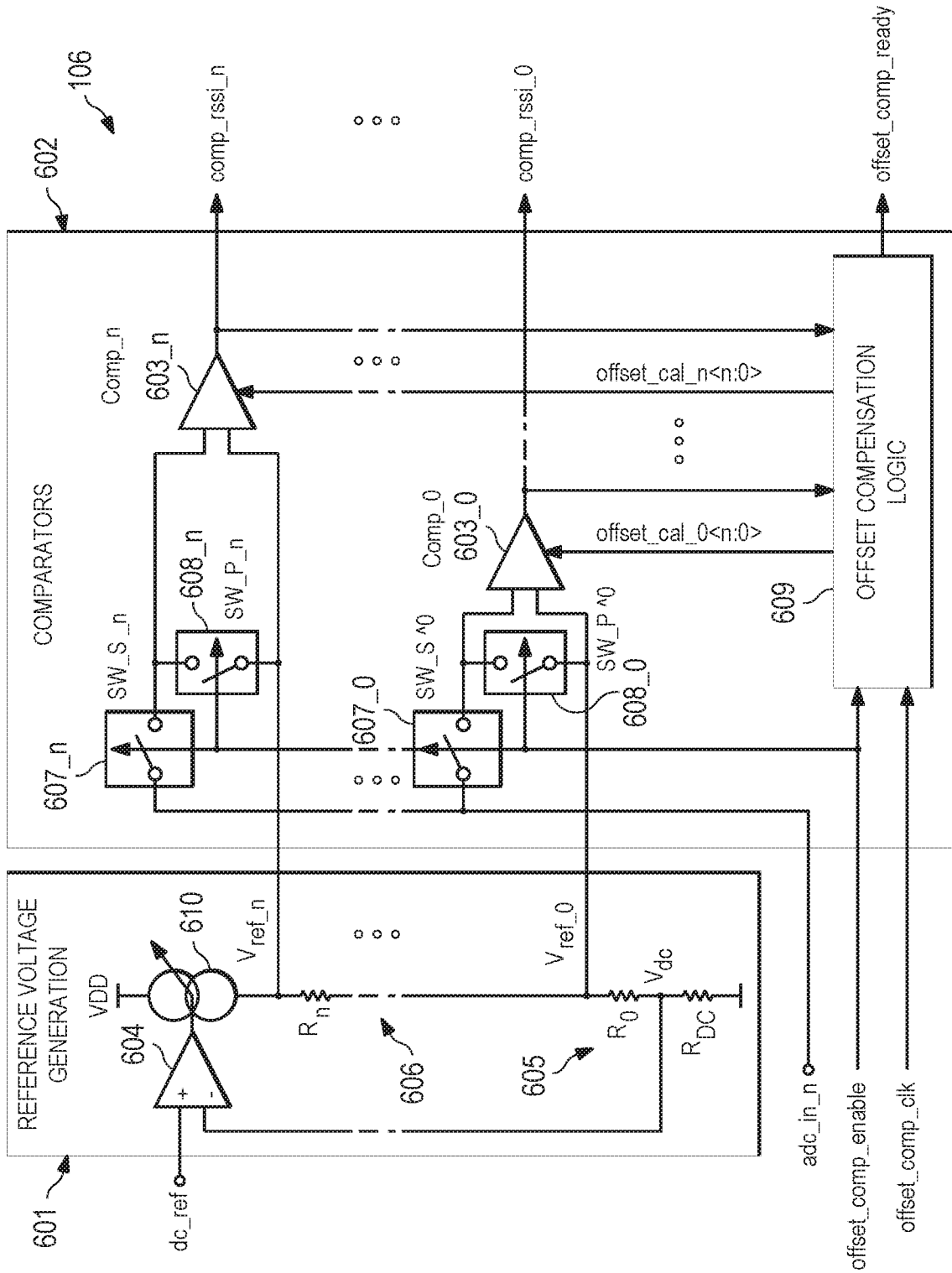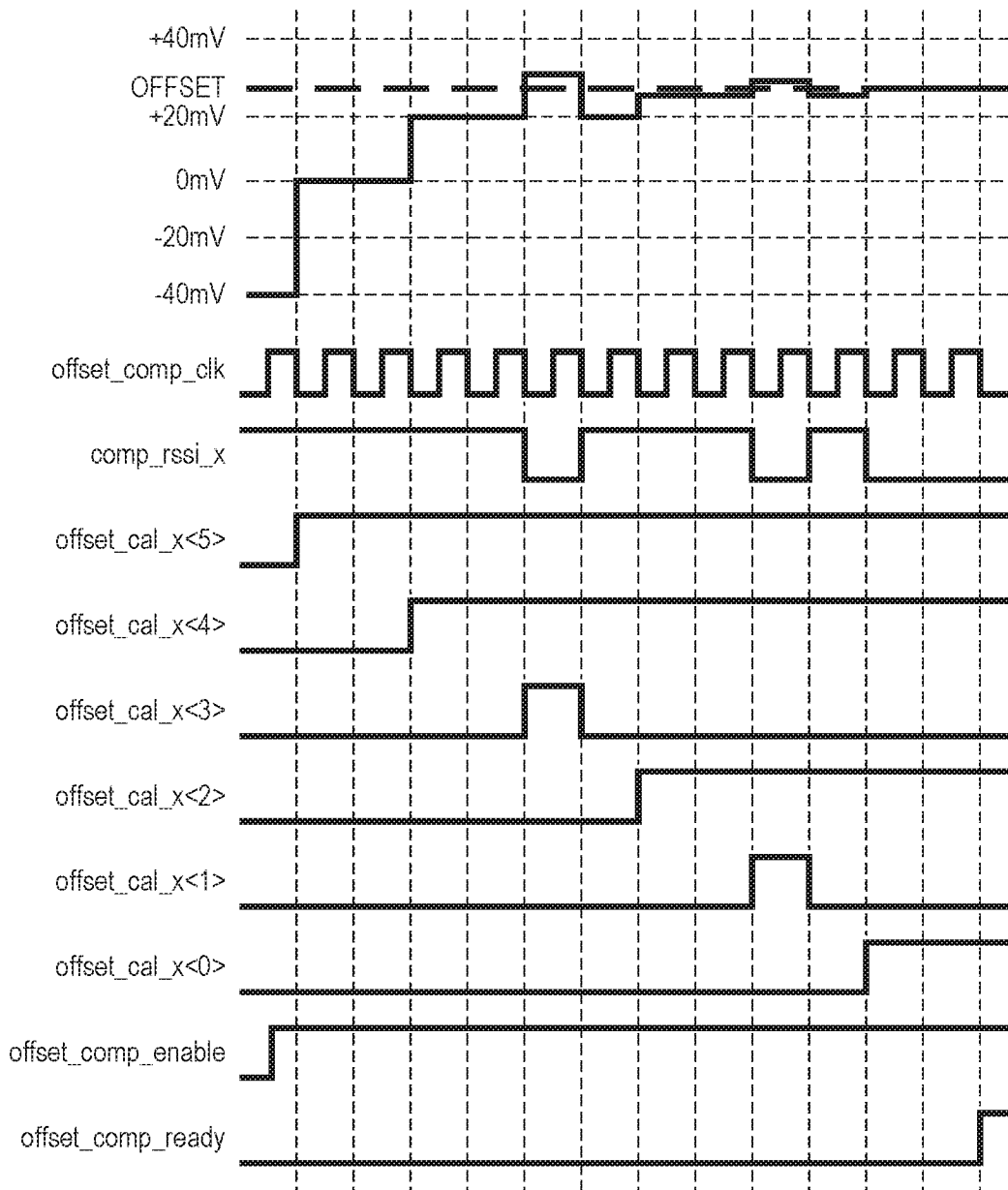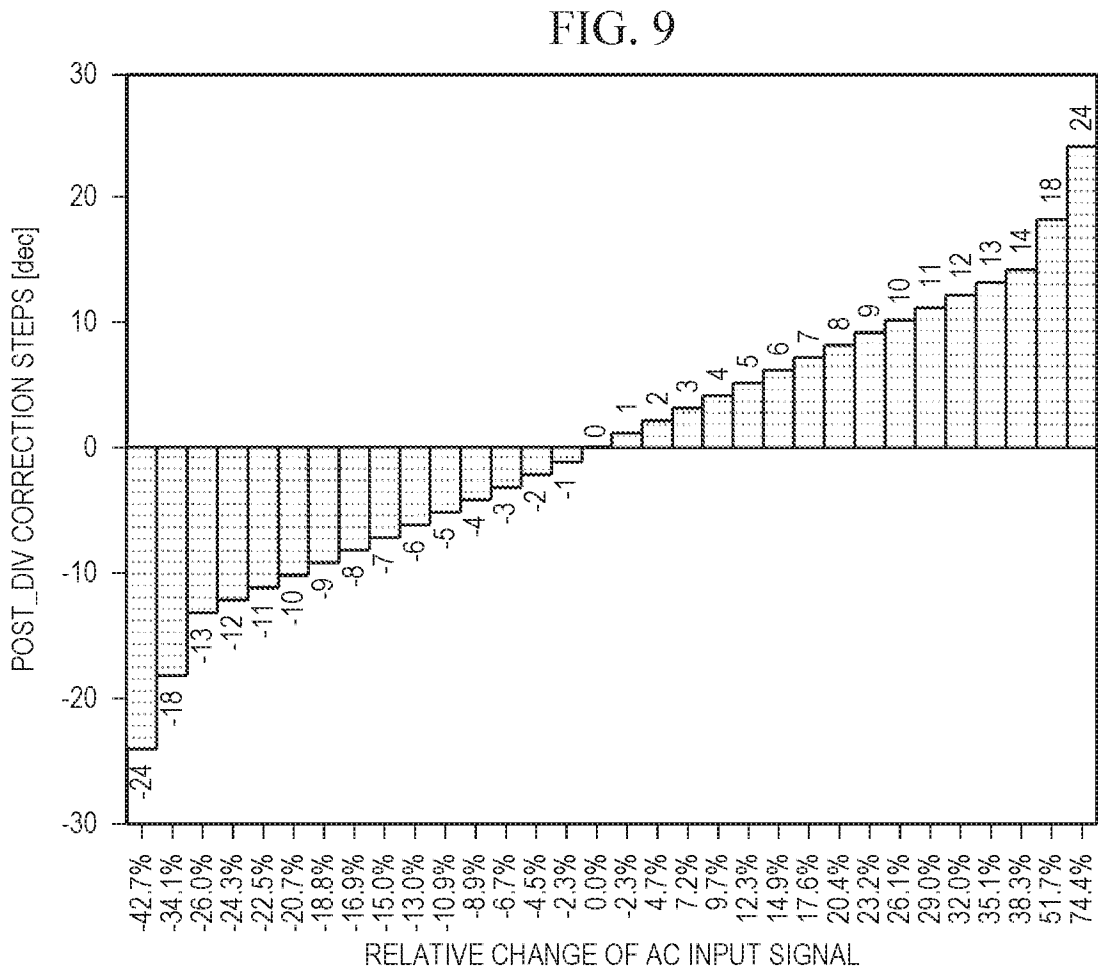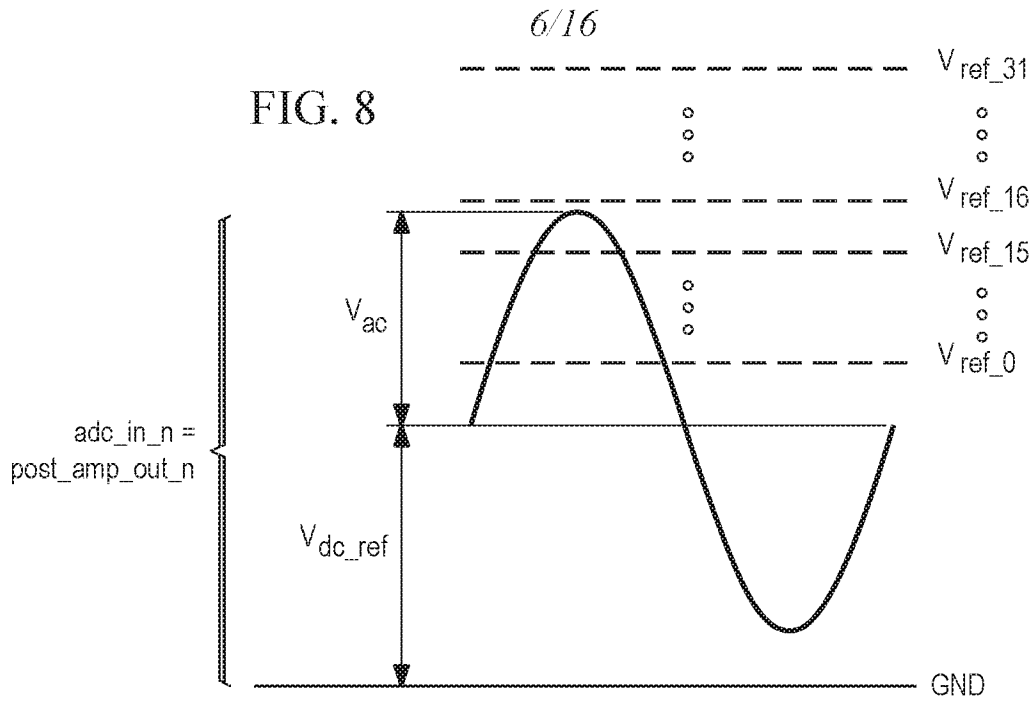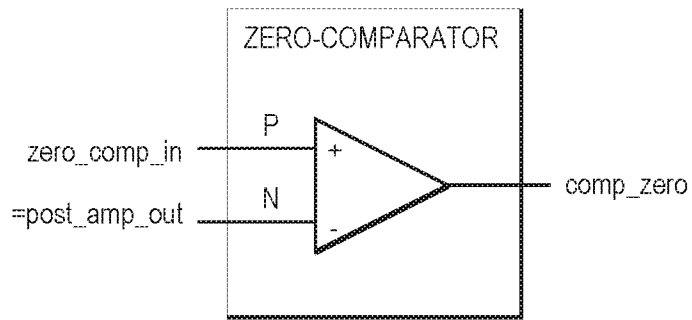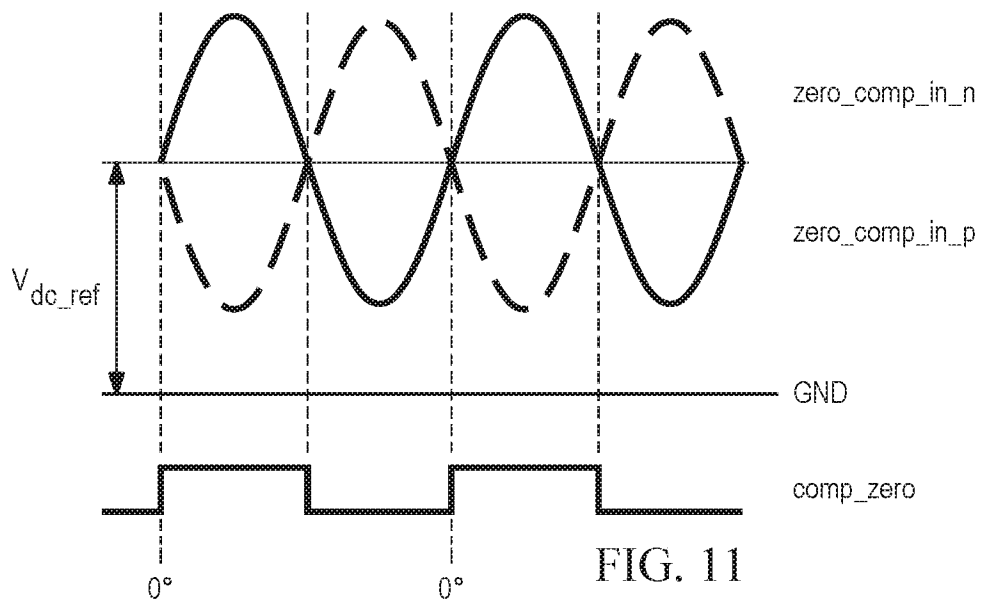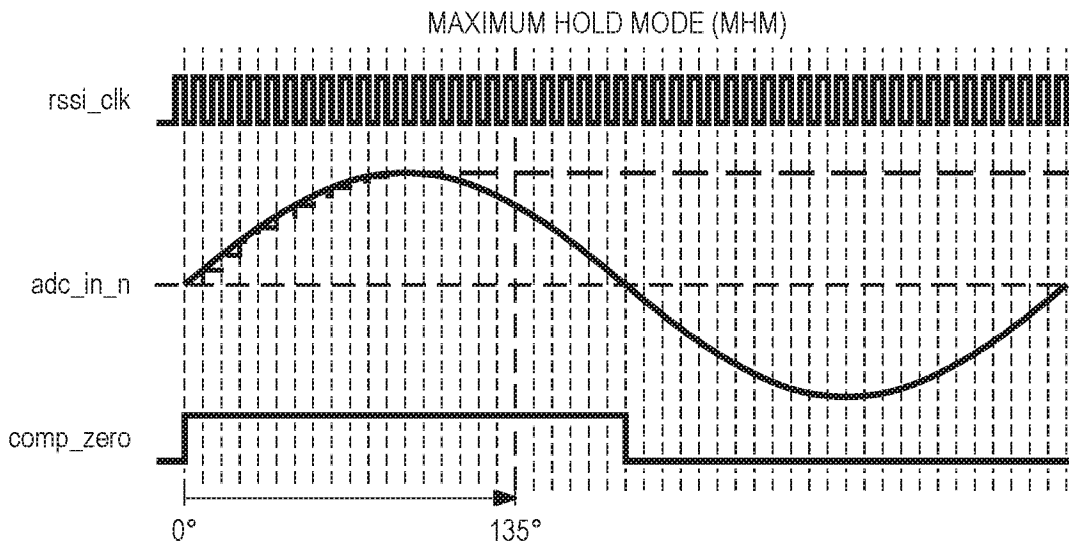
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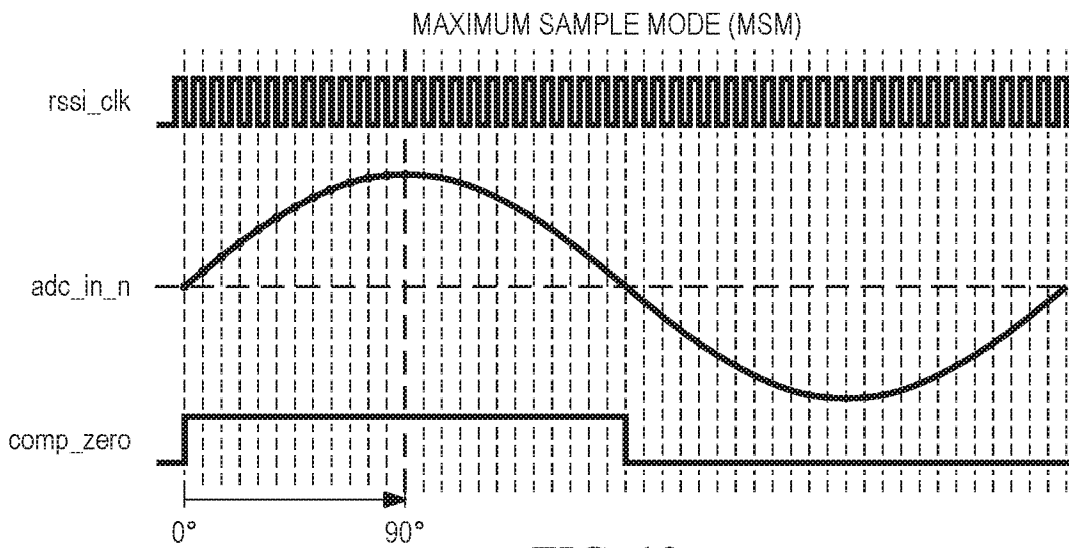
FIG. 13
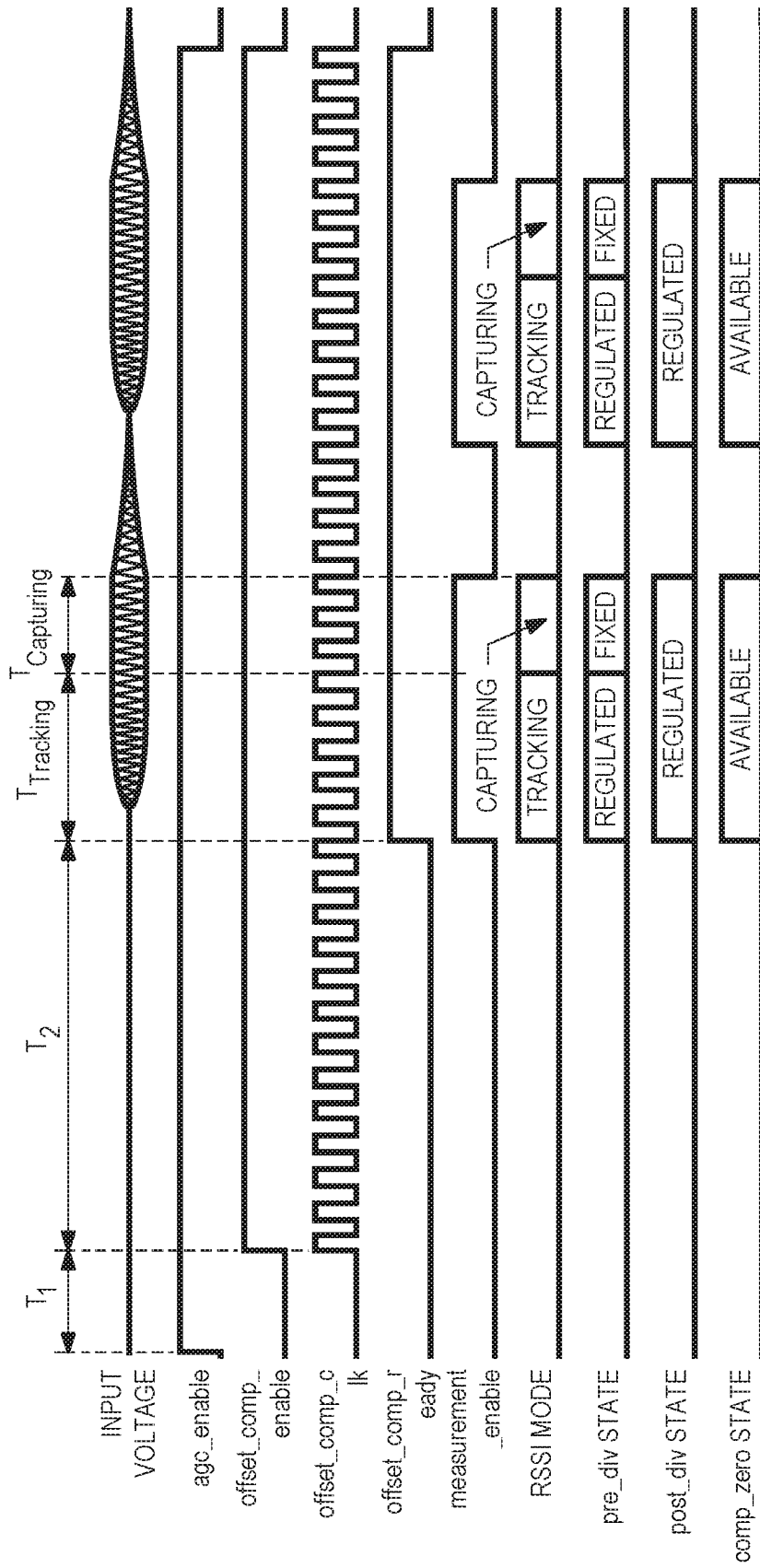
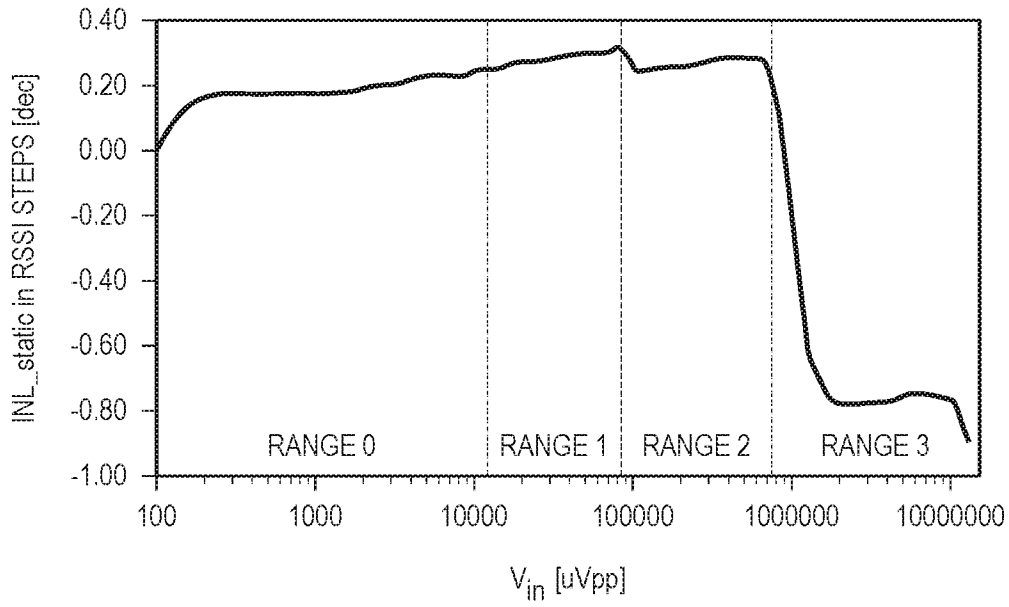# FIG. 14
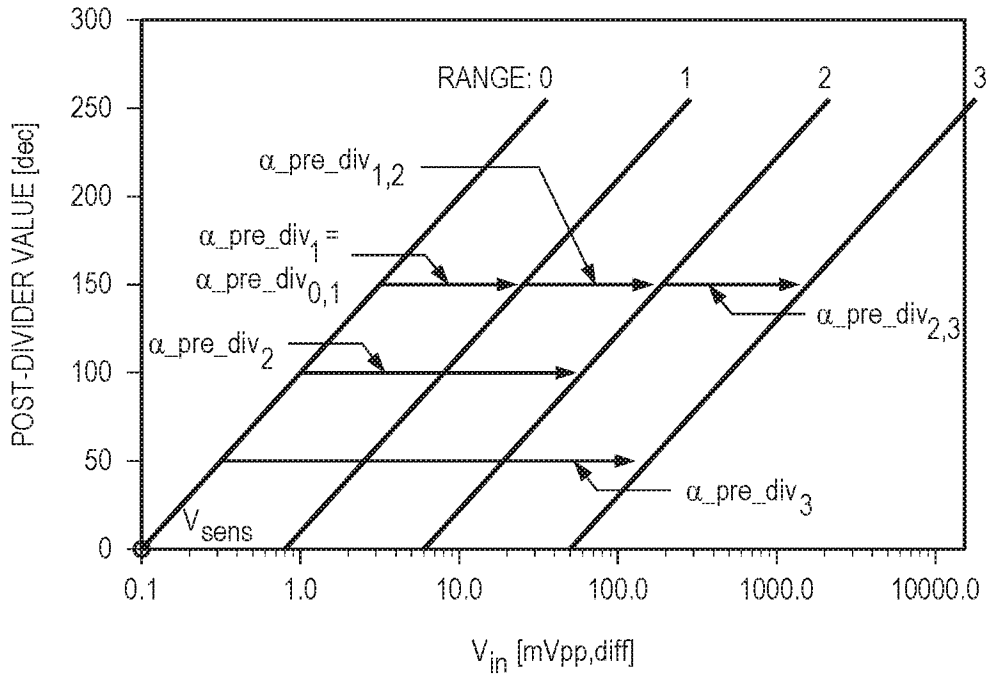
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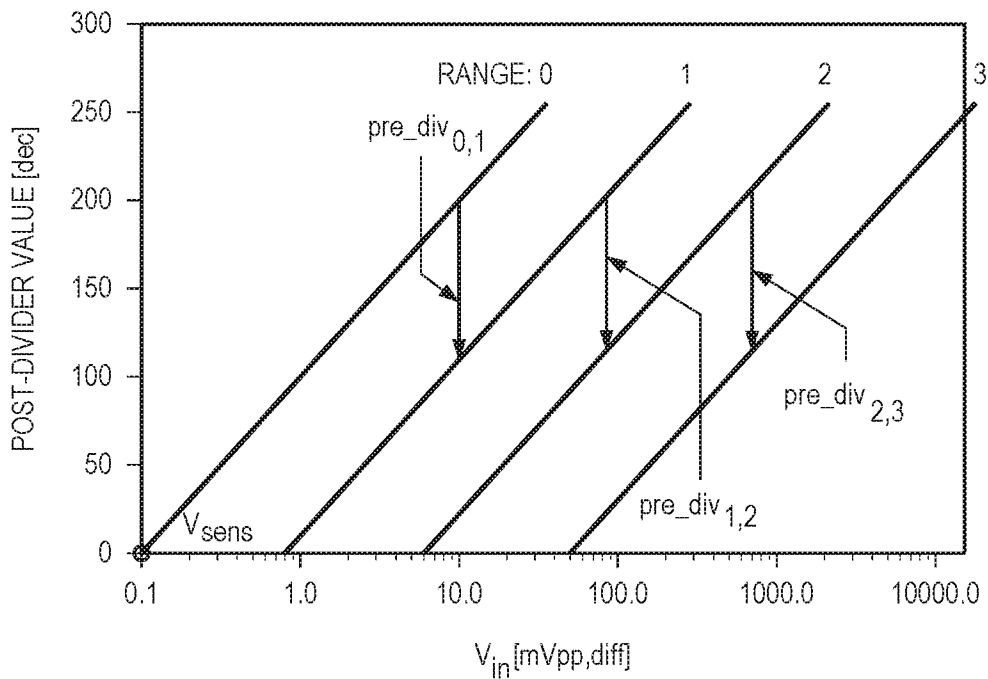
FIG. 16

FIG. 17

FIG. 18
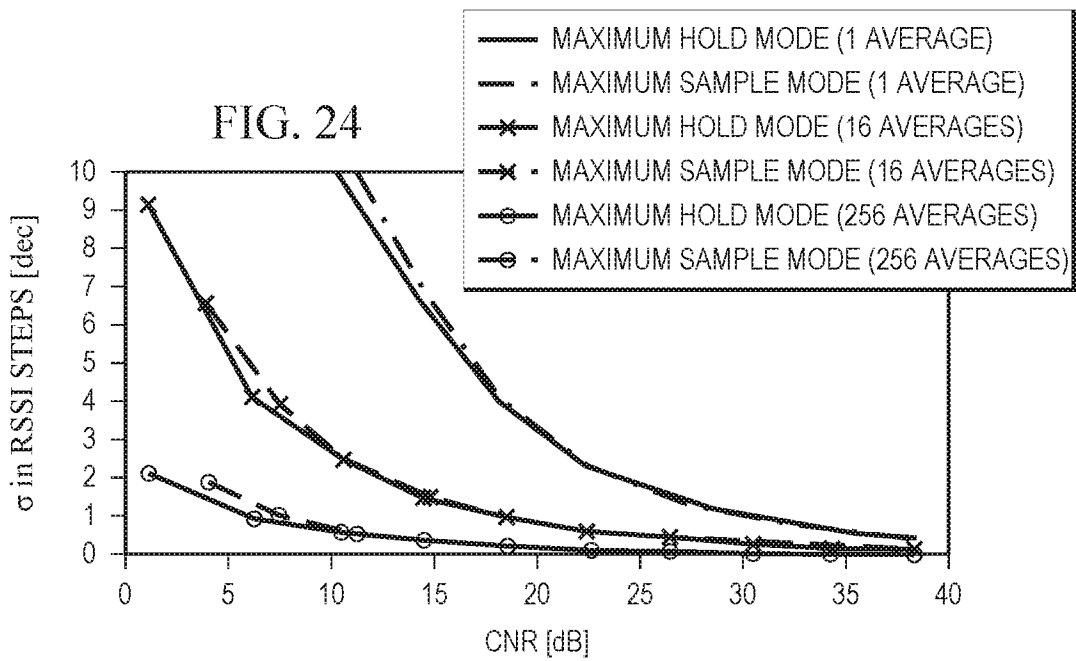

FIG. 19

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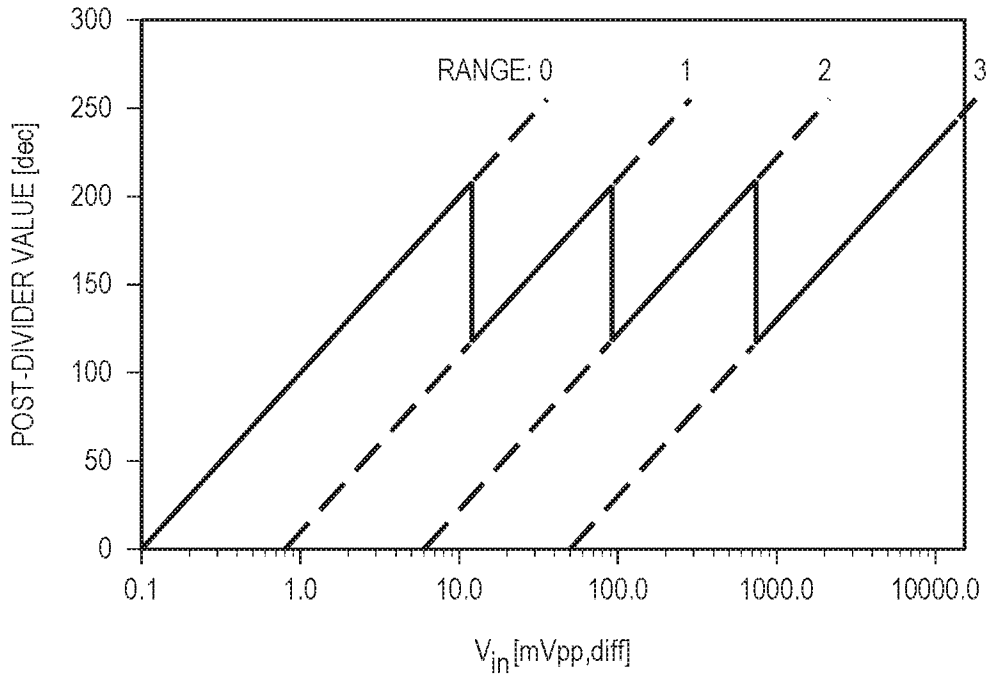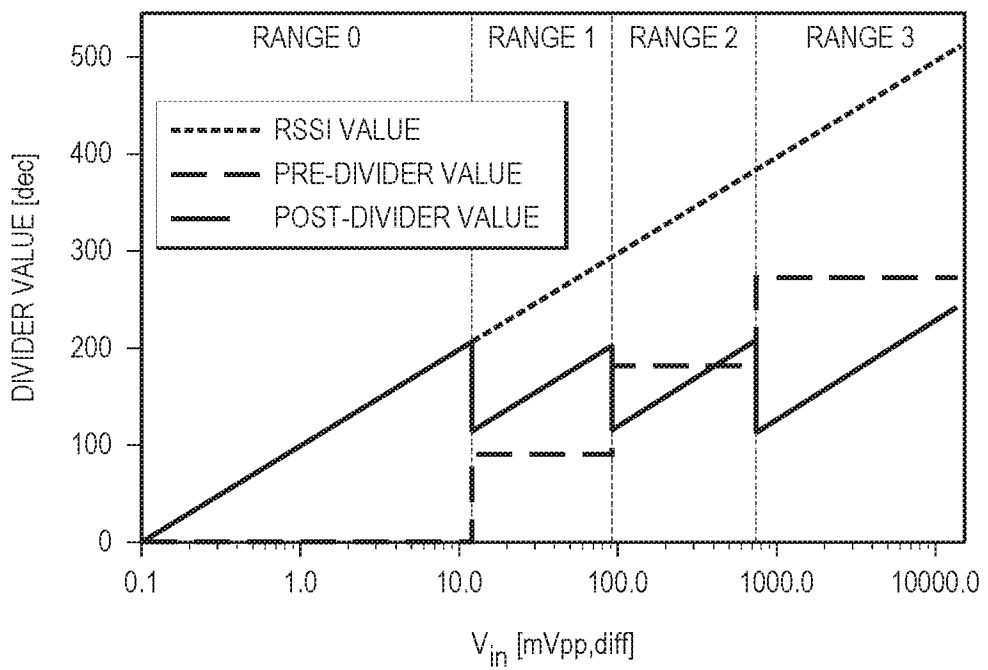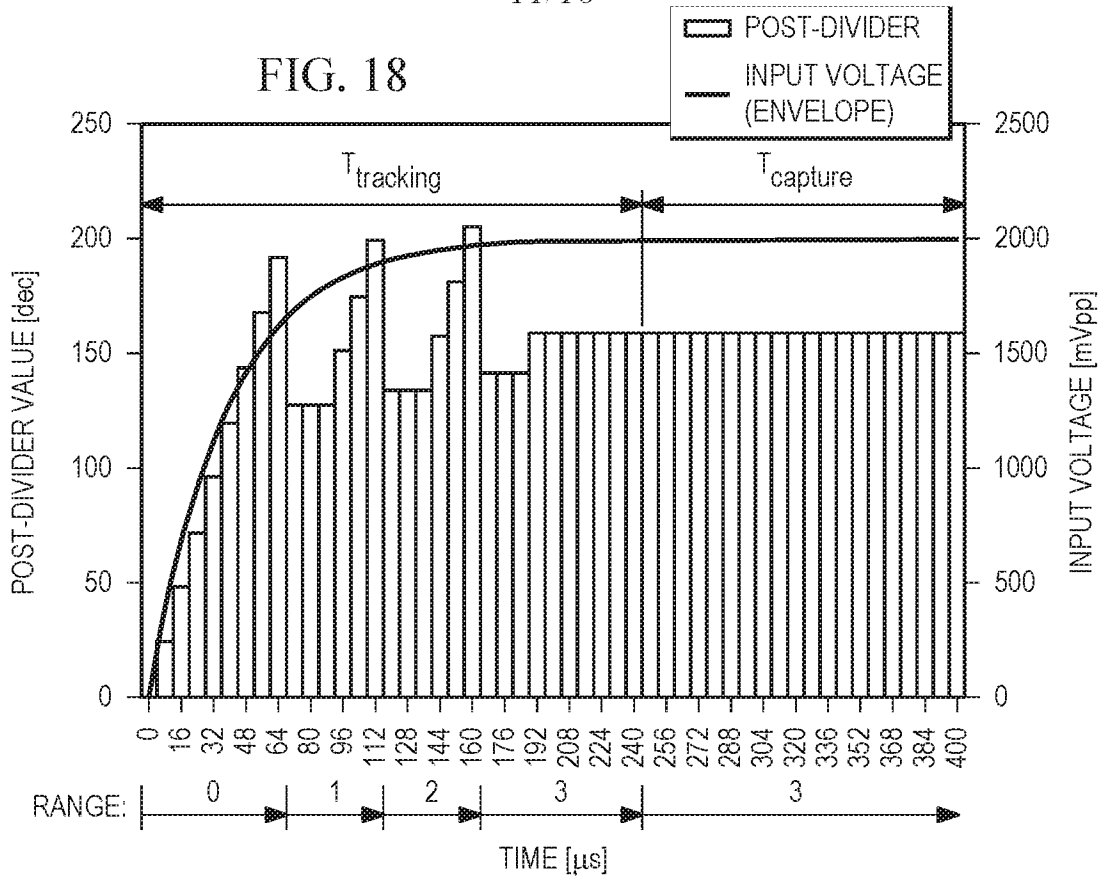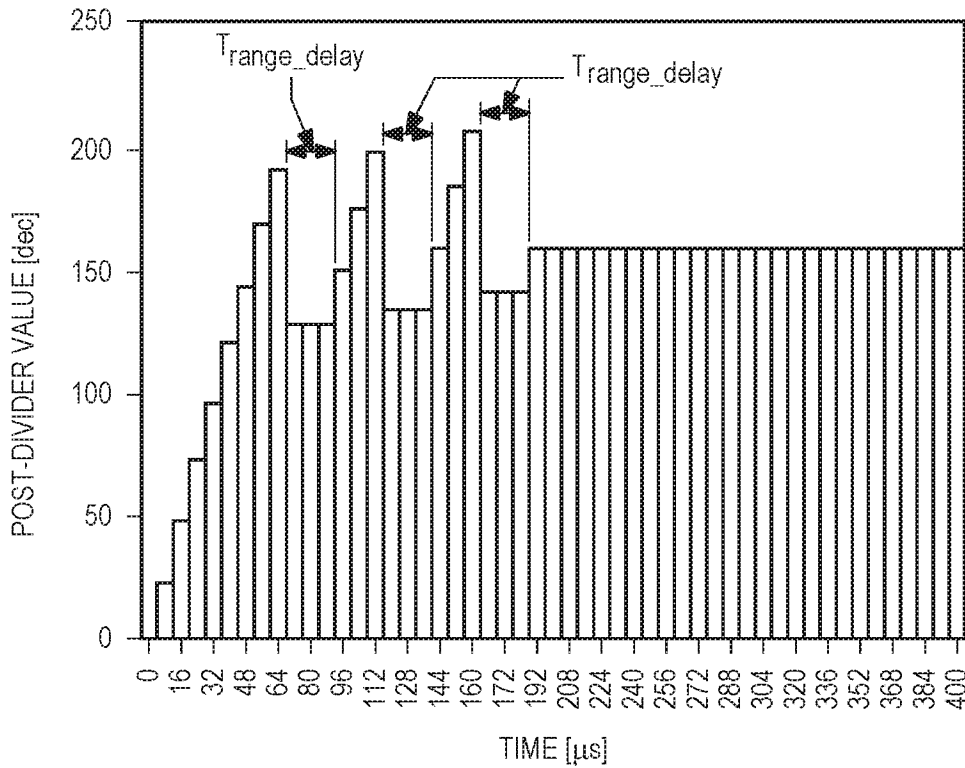
FIG. 20

FIG. 21

FIG. 22

FIG. 23
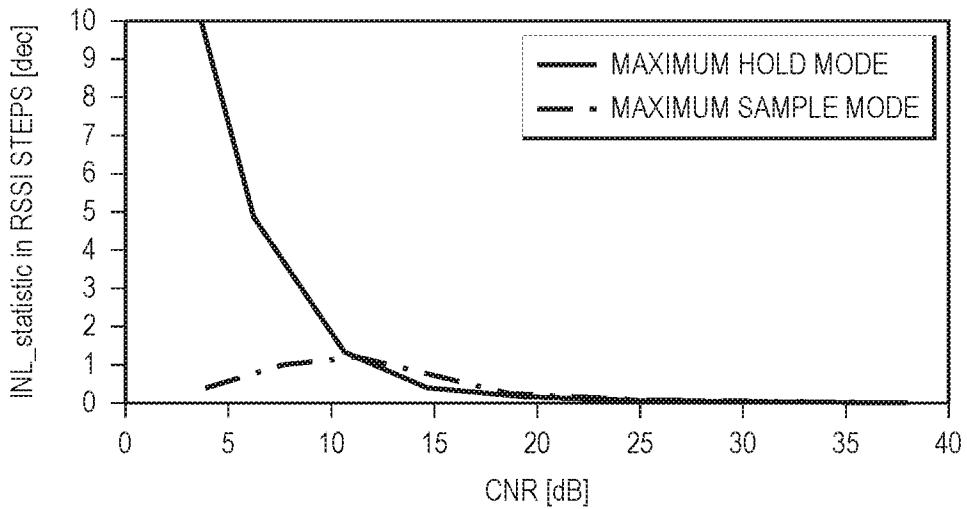
FIG. 24
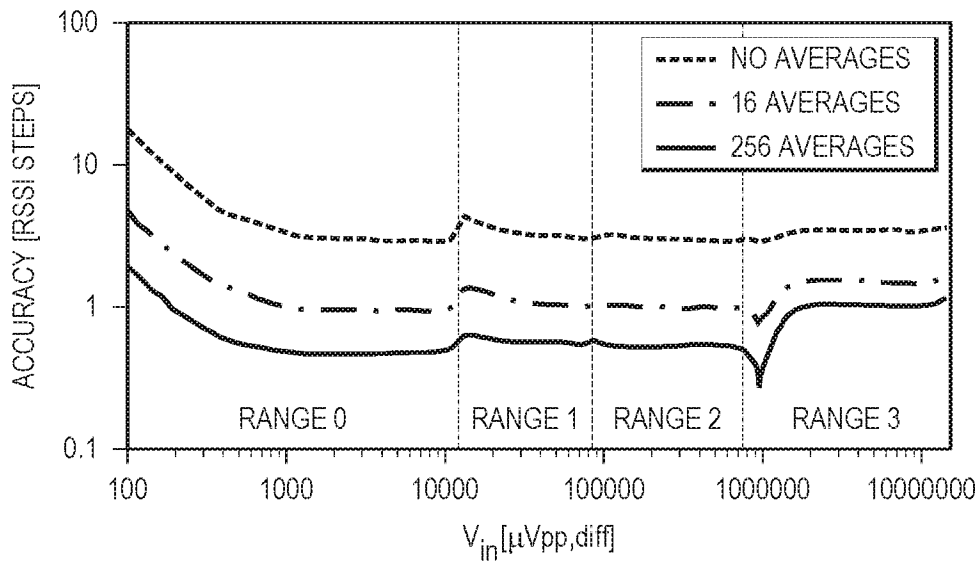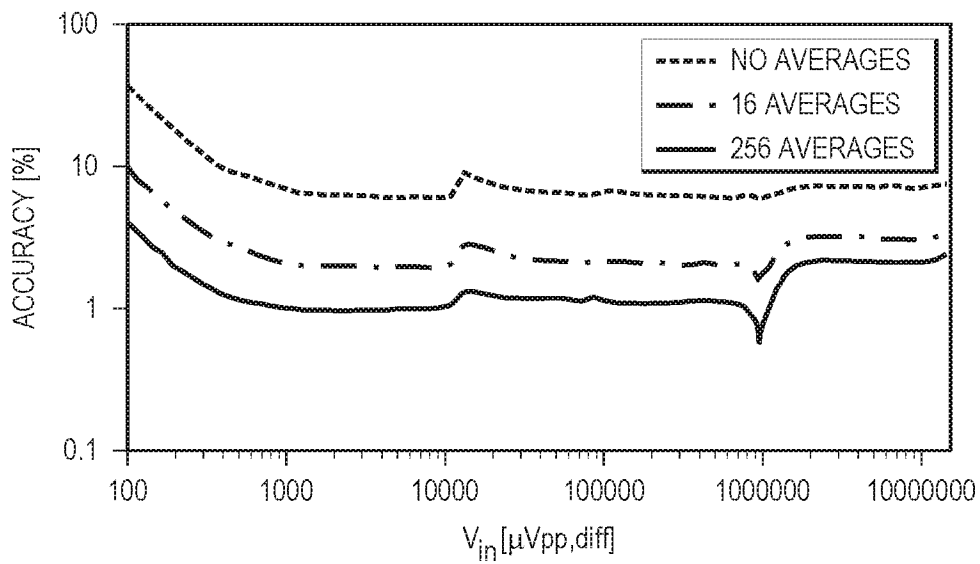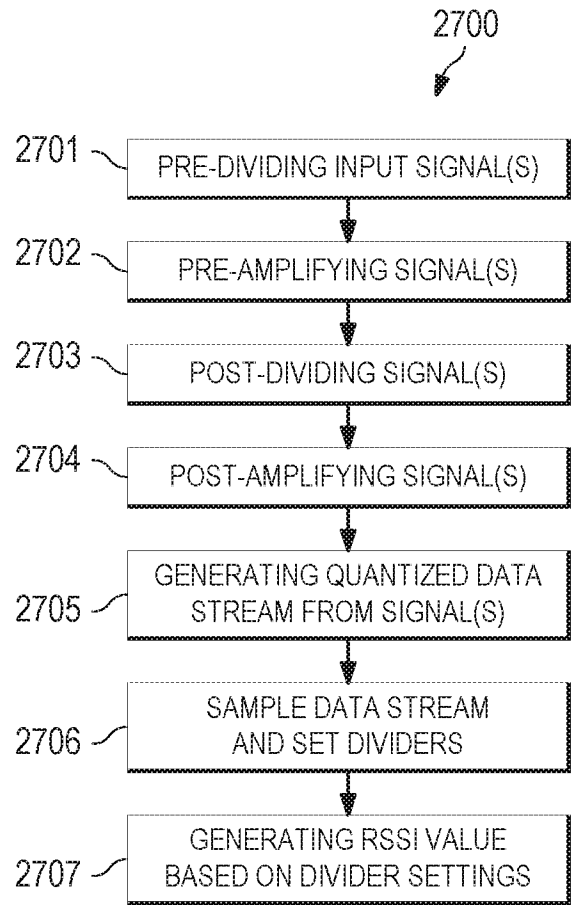
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FIG. 25

FIG. 26

2700

2701	PRE-DIVIDING INPUT SIGNAL(S)
2702	PRE-AMPLIFYING SIGNAL(S)
2703	POST-DIVIDING SIGNAL(S)
2704	POST-AMPLIFYING SIGNAL(S)
2705	GENERATING QUANTIZED DATA STREAM FROM SIGNAL(S)
2706	SAMPLE DATA STREAM AND SET DIVIDERS
2707	GENERATING RSSI VALUE BASED ON DIVIDER SETTINGS

FIG. 27

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03G3/30   H04B17/318
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03G H04B G01R G01D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 321 073 B1 (LUZ YUDA Y [US] ET AL) 20 November 2001 (2001-11-20) abstract; figures 1,3 column 2, lines 40-62 column 3, line 7 - column 6, line 22 -----	1-26
X	US 2012/274398 A1 (ALAVI REZA [US] ET AL) 1 November 2012 (2012-11-01) abstract; figures 1-6,9-12 paragraphs [0020], [0021], [0037], [0044] - [0047] -----	1-16
A	US 5 861 831 A (MURDEN FRANKLIN M [US] ET AL) 19 January 1999 (1999-01-19) abstract; figures 2-4,7-9 column 2, lines 30-54 column 3, line 48 - column 5, line 60 -----	1-26

-/--

| X | Further documents are listed in the continuation of Box C. | X | See patent family annex. |

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2017	09/06/2017

| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016 | Authorized officer Wichert, Beate |

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/216482 A1 (HOLLENBECK NEAL W [US] ET AL) 20 September 2007 (2007-09-20) abstract; figures 1-5 paragraphs [0015] - [0018] -----	1-26

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

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			KR	100436187 B1	16-06-2004
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