United States Patent [19]

Watson

[11] **3,743,755**

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[54] **METHOD AND APPARATUS FOR ADDRESSING A MEMORY AT SELECTIVELY CONTROLLED RATES**

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[73] Assignee: **North American Rockwell Corporation,** El Segundo, Calif.

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[21] Appl. No.: **170,992**

Related U.S. Application Data

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[52] **U.S. Cl.** **84/1.01,** 84/1.03

[51] **Int. Cl.** **G10h 5/00**

[58] **Field of Search** 84/1.01, 1.03; 340/172.5

[56] **References Cited**

UNITED STATES PATENTS

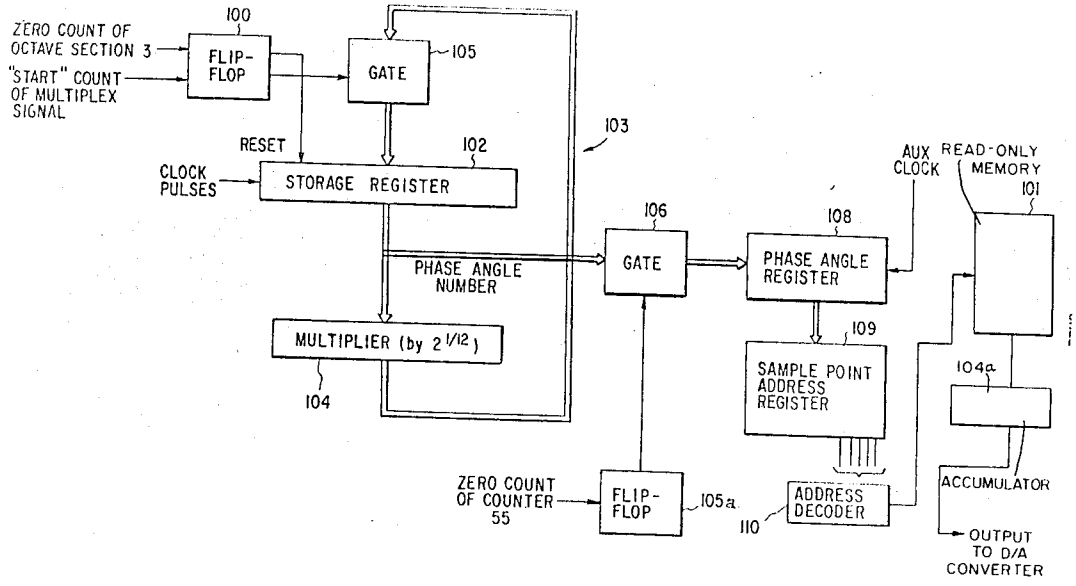
3,163,850	12/1964	Austin et al.	340/172.5
3,267,433	8/1966	Falkoff	340/172.5
3,328,770	6/1967	Silver	340/172.5
3,337,852	8/1967	Lee et al.	340/172.5
3,417,378	12/1968	Simonsen et al.	340/172.5
3,696,201	10/1972	Arsem et al.	84/1.01
3,697,661	10/1972	Deutsch	84/1.01
3,700,781	10/1972	Obayashi	84/1.01
3,515,792	6/1970	Deutsch	84/1.03
3,610,799	10/1971	Watson	84/1.01

Primary Examiner—Richard B. Wilkinson
Assistant Examiner—Stanley J. Witkowski
Attorney—L. Lee Humphries, H. Frederick Hamann et al.

[57] **ABSTRACT**

A memory contains digital data of related informational content in a plurality of discrete locations identified by respective addresses. The memory is addressed, or accessed, at a rate which depends upon the desired spacing between data from the various locations as it is sequentially read from the memory. In a specific embodiment, the data constitutes amplitude values of a complex waveform of the type produced by a musical instrument, at equally spaced points in time along an axis of the waveform. Apparatus for addressing the memory at any of a plurality of selectively controlled rates includes a calculator for continuously computing a set of numbers each defining a different spacing between the data during readout of the memory. When a desired rate of readout is selected, as by selecting a desired frequency of repetition of a complete cycle of the stored waveform, the number associated with that rate is sampled from the computed set and is periodically increased by its own value to identify appropriate data addresses in the memory, for accessing that data, at intervals of the periodic increase corresponding to the desired rate of readout.

6 Claims, 12 Drawing Figures



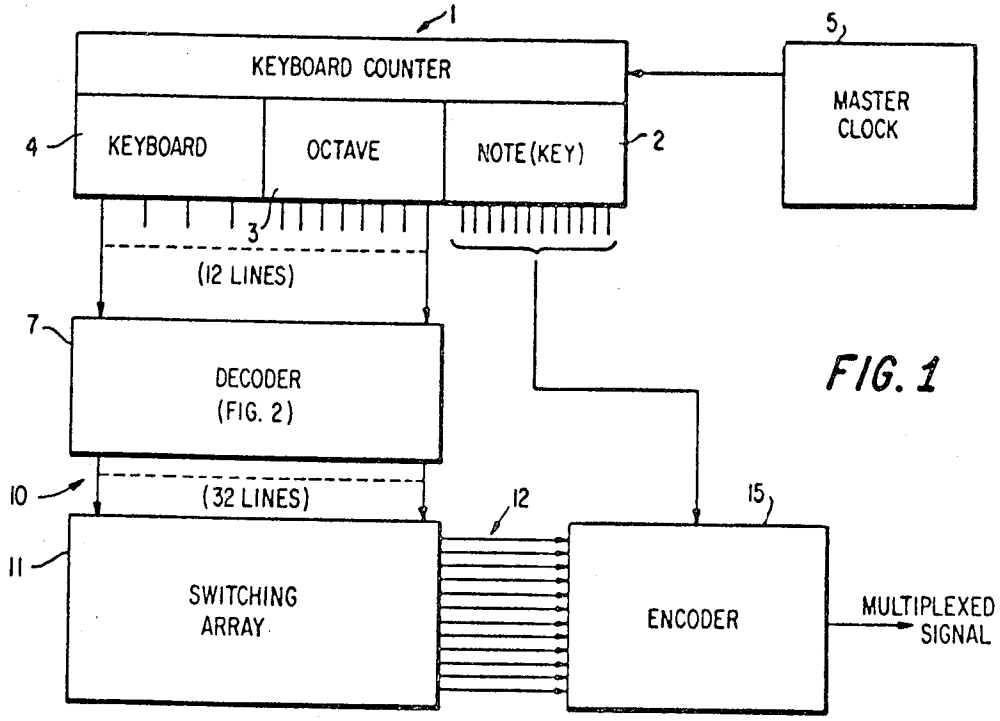

1
KEYBOARD COUNTER
5
MASTER CLOCK
4
KEYBOARD
OCTAVE
NOTE (KEY)
2
3
(12 LINES)
7
DECODER (FIG. 2)
10
(32 LINES)
12
15
11
SWITCHING ARRAY
ENCODER
MULTIPLEXED SIGNAL

FIG. 1

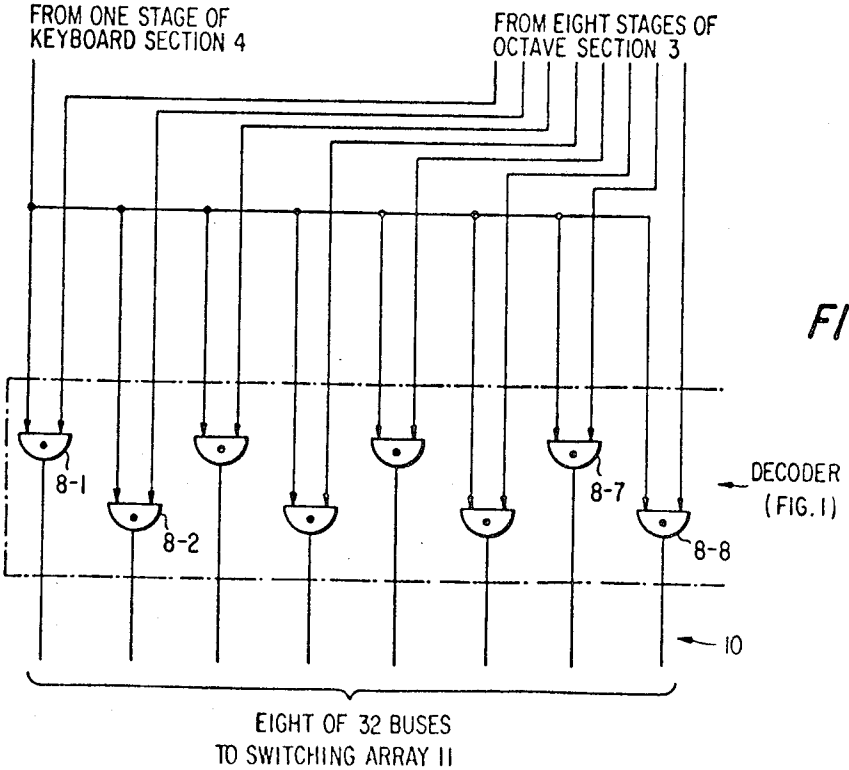

FROM ONE STAGE OF KEYBOARD SECTION 4
FROM EIGHT STAGES OF OCTAVE SECTION 3
8-1
8-2
8-7
8-8
DECODER (FIG. 1)
10
EIGHT OF 32 BUSES TO SWITCHING ARRAY 11

FIG. 2

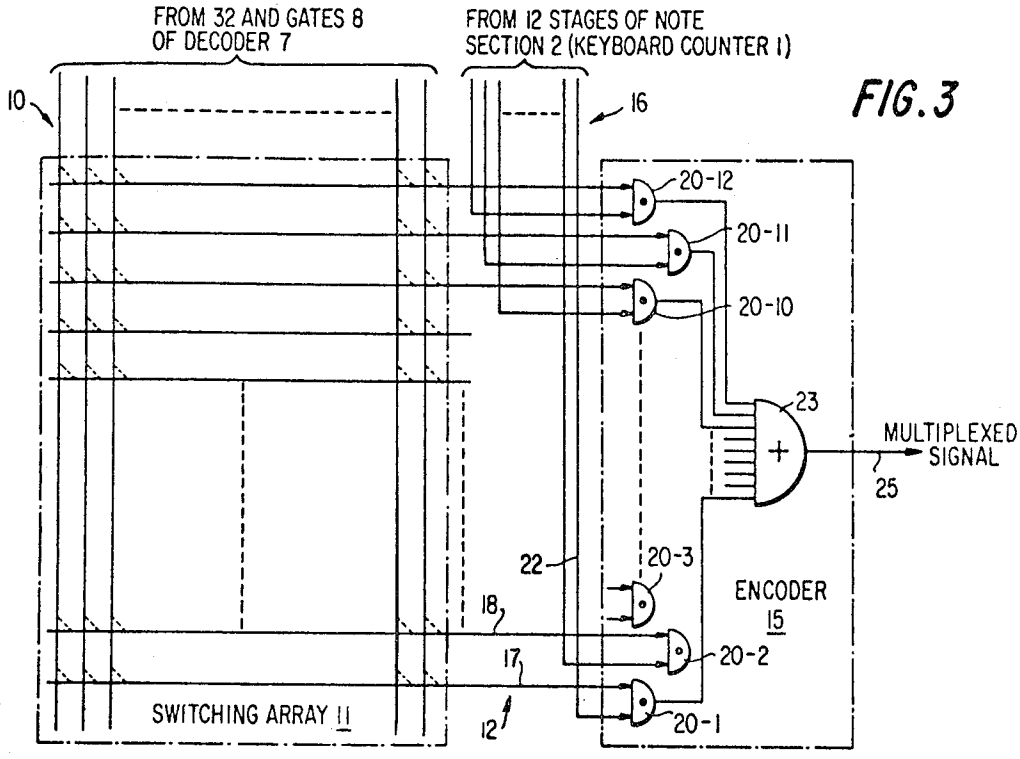

FROM 32 AND GATES 8 OF DECODER 7
FROM 12 STAGES OF NOTE SECTION 2 (KEYBOARD COUNTER 1)
10
16
20-12
20-11
20-10
23
MULTIPLEXED SIGNAL
25
22
20-3
ENCODER 15
18
20-2
17
12
20-1
SWITCHING ARRAY 11

FIG. 3

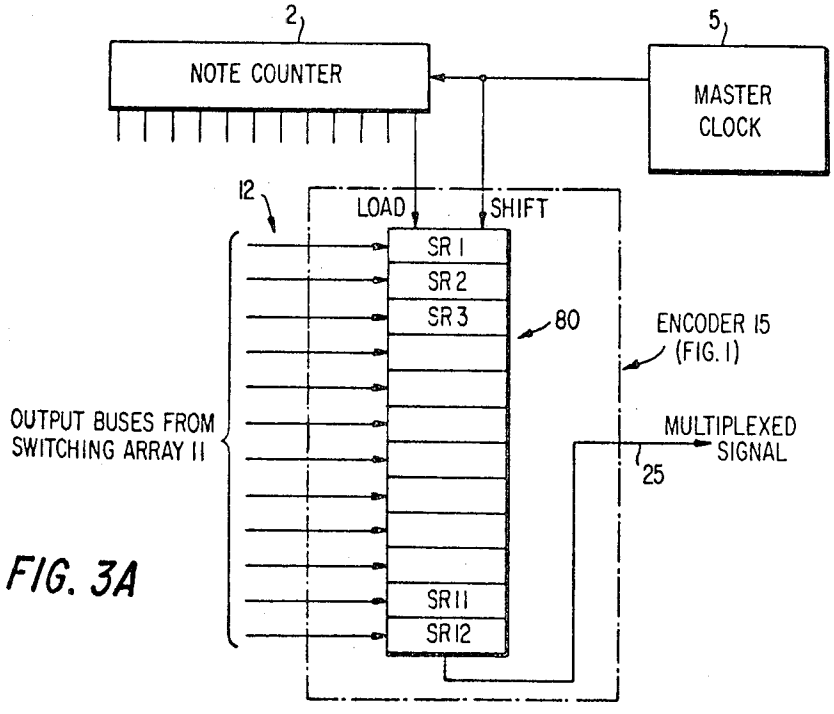

2
NOTE COUNTER
5
MASTER CLOCK
12
LOAD
SHIFT
SR 1
SR 2
SR 3
80
ENCODER 15 (FIG. 1)
OUTPUT BUSES FROM SWITCHING ARRAY 11
MULTIPLEXED SIGNAL
25
SR 11
SR 12

FIG. 3A

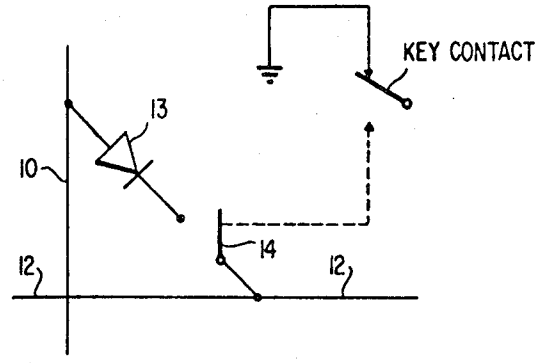
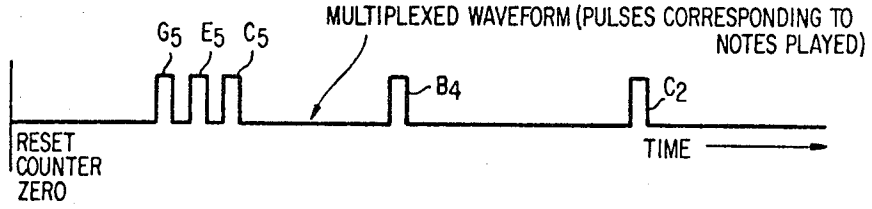


FIG. 4

FIG. 5



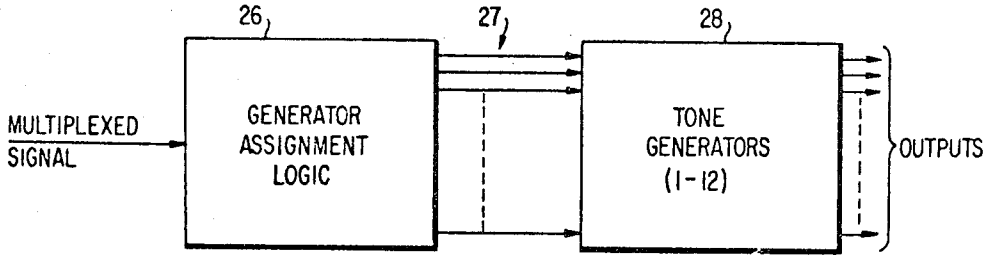


FIG. 6

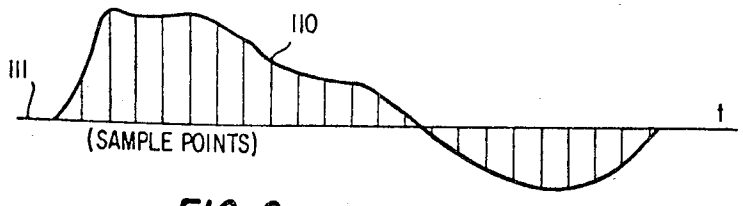


FIG. 9

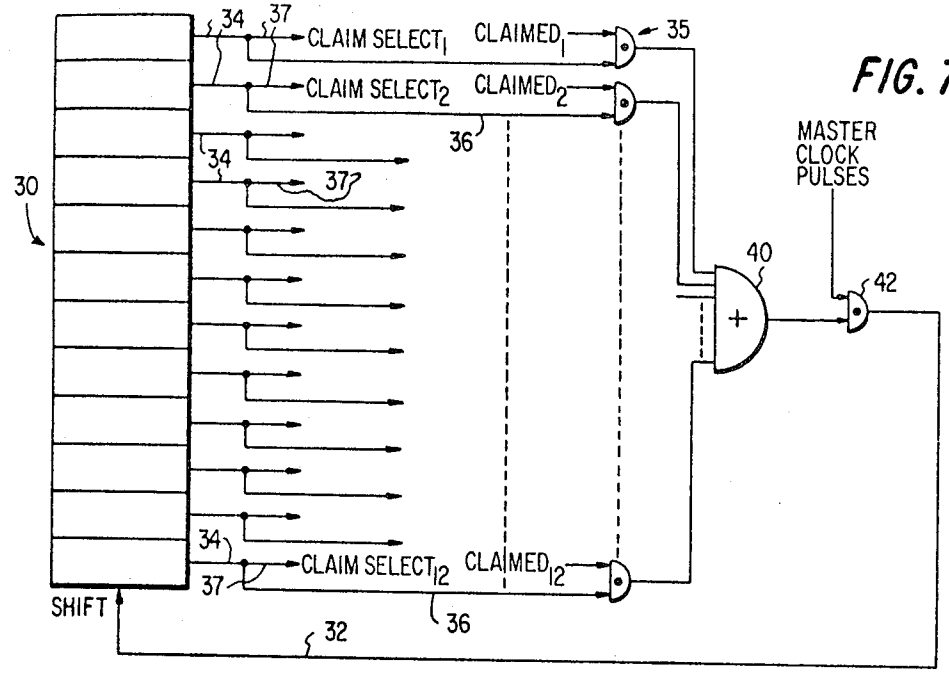

34
37
CLAIM SELECT1
CLAIMED1
35
CLAIM SELECT2
CLAIMED2
36
34
37
30
MASTER CLOCK PULSES
40
42
34
37
CLAIM SELECT12
CLAIMED12
SHIFT
36
32

FIG. 7A

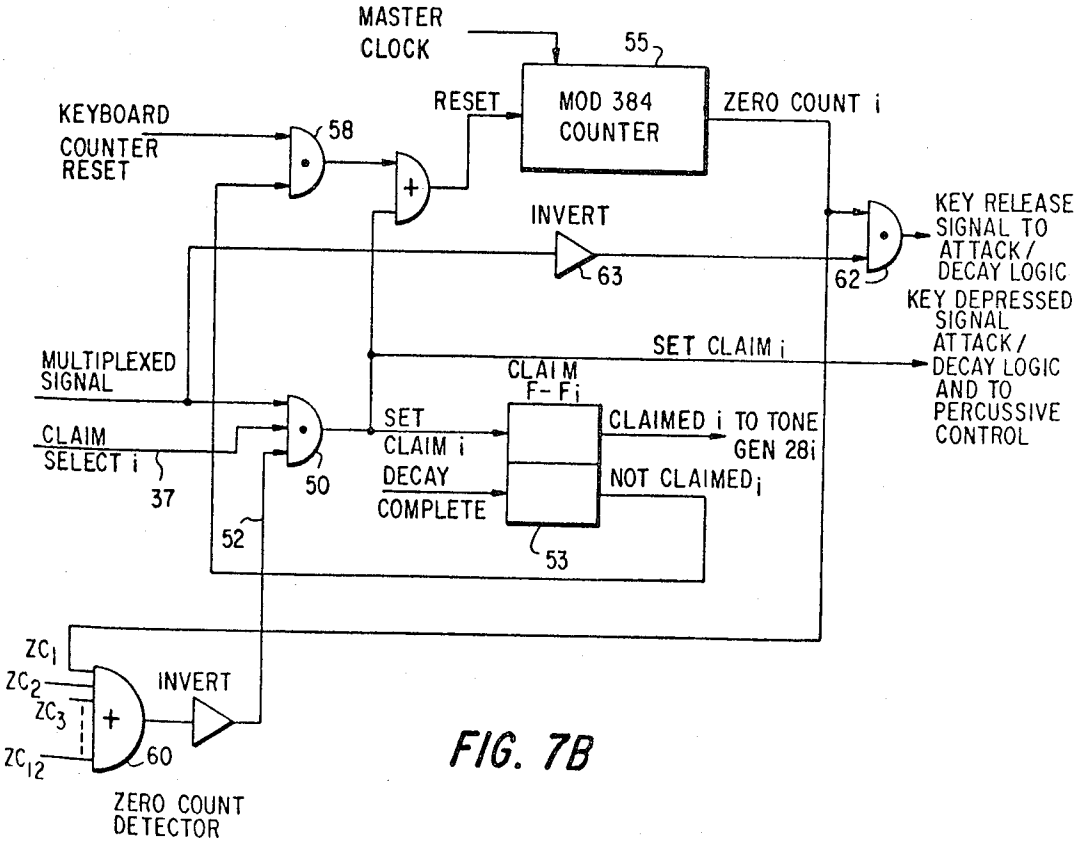
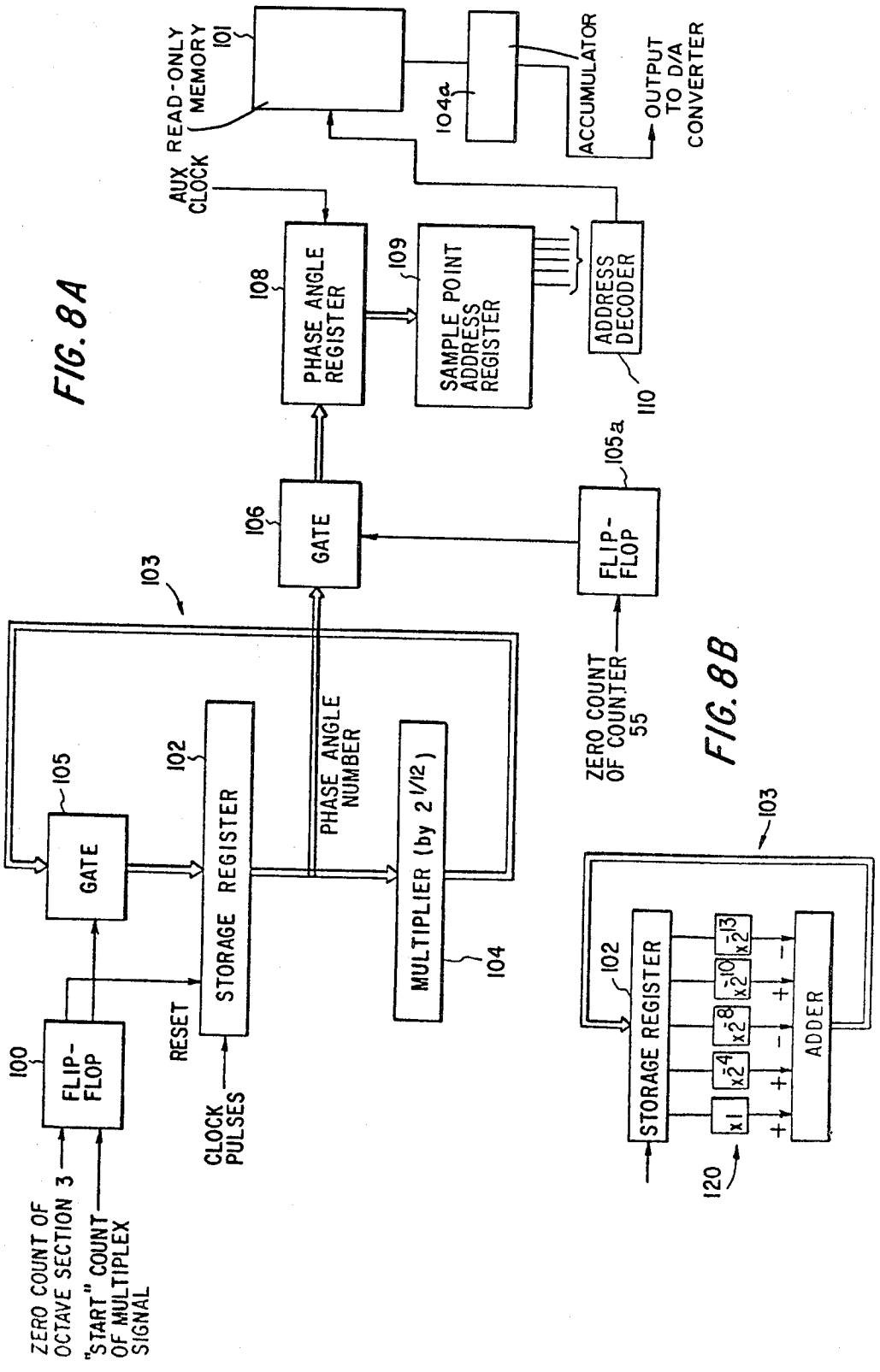

MASTER CLOCK
55
KEYBOARD COUNTER RESET
58
RESET
MOD 384 COUNTER
ZERO COUNT i
INVERT
63
62
KEY RELEASE SIGNAL TO ATTACK/ DECAY LOGIC
KEY DEPRESSED SIGNAL ATTACK/ DECAY LOGIC AND TO PERCUSSIVE CONTROL
SET CLAIM i
MULTIPLEXED SIGNAL
CLAIM F-Fi
CLAIM SELECT i
37
50
SET CLAIM i
DECAY COMPLETE
CLAIMED i TO TONE GEN 28i
NOT CLAIMED i
52
53
ZC1
ZC2
ZC3
ZC12
INVERT
60
ZERO COUNT DETECTOR

FIG. 7B


AUX READ-ONLY MEMORY
101
104a
ACCUMULATOR
OUTPUT TO D/A CONVERTER
AUX CLOCK
108
PHASE ANGLE REGISTER
109
SAMPLE POINT ADDRESS REGISTER
ADDRESS DECODER
110
105a
106
GATE
FLIP-FLOP
103
ZERO COUNT OF COUNTER 55
105
GATE
102
STORAGE REGISTER
PHASE ANGLE NUMBER
MULTIPLIER (by 2 1/12)
104
RESET
CLOCK PULSES
100
FLIP-FLOP
ZERO COUNT OF OCTAVE SECTION 3
"START" COUNT OF MULTIPLEX SIGNAL
FIG. 8A
FIG. 8B
103
102
STORAGE REGISTER
x1
x2^4
x2^8
x2^10
x2^13
ADDER
120

METHOD AND APPARATUS FOR ADDRESSING A MEMORY AT SELECTIVELY CONTROLLED RATES

This is a division of my copending application Ser. No. 875,178, filed Nov. 10, 1969, now U.S. Pat. No. 3,639,913.

BACKGROUND OF THE INVENTION

The present invention is directed generally toward the addressing of a memory containing digital data of related informational content in successive or sequential data locations, or addresses, therein. The data may, for example, consist of digital samples of the amplitude of a waveform at successive selected points, or may consist of a list of symbols identifying in a particular order the members of a class of prescribed characteristics, or may consist of a mathematical progression of numbers, or may consist of other information.

It is sometimes necessary or desirable to read data from a memory unit in which it is stored at a controllably variable rate. For example, in the case of stored amplitude samples of a waveform, the rate at which the samples are read from the memory can be used to determine the frequency of the output waveform, or the phase angle of the waveform relative to a fixed reference. Alternatively, if the rate at which samples are read from the memory is held constant, the frequency of the output waveform may be varied by changing the rate at which the address changes. In the latter case, the same data may be read from the memory several times in succession where the address is unchanged through several access commands, so that the same memory location is addressed each time. For certain types of stored data, no difficulty may be encountered with such a process. If the data in a specified memory location cannot be read out repetitively, without destroying the significance of the data, then special means must be devised to prevent supplying that data on a repeated basis to its ultimate processing circuitry to ensure that the same data is supplied only once, during a specific sequence, to subsequent processing circuitry.

SUMMARY OF THE INVENTION

Broadly, the invention includes means for performing a calculation to derive a number that determines the rate at which the memory shall be accessed, regardless of the consistency of the clock rate at which the overall system is operated. The calculating means continuously calculates a set of distinct and different numbers, and means are provided to select a desired number that will produce a predetermined rate of accessing of the memory based on the occurrence of a related one of a set of selected events. Thus, if an event occurs, the number with which that event is associated is selected and determines the rate at which the memory is accessed. Evey number is periodically calculated in cyclic sequence to ensure its availability when the event with which it is associated occurs.

In a specific embodiment demonstrating an exemplary application of the invention, a memory unit in a digital electronic musical instrument is addressed at a rate which is selectively controllable according to the frequency (or phase angle relative to a reference phase) of the note to be produced by the instrument. The memory unit contains digital data representing samples of the amplitude of a complex waveform at a plurality of uniformly spaced points in time (i.e., along the abscissa, or time axis, of the waveform). The complex waveform is identical for each note, but its rate of cyclic repetition is to be varied according to the frequency of the note to be played. The individual amplitude samples are stored in separate locations, preferably at sequential addresses although this is not absolutely necessary, of a read-only memory (ROM), and the memory is thereafter addressed, i.e., the stored data is accessed or read out, at a rate which depends upon the frequency of the note to be generated by the instrument.

In a digital electronic organ of the type specifically disclosed in the copending application of George A. Watson entitled "Multiplexing System for Selection of Notes and Voices in an Electronic Musical Instrument," filed Oct. 30, 1969 and issued Oct. 5, 1971 as U. S. Pat. No. 3,610,799 the instrument has a plurality of keyboards, including at least one manual and at least one pedal division. Each keyboard may cover several octaves. When a key is depressed on any keyboard of the digital electronic organ, a sound waveform is to be generated with a periodicity corresponding to the desired note frequency. The waveform is computed in digital format consisting of a series of digital words which represent the magnitude of the waveform at a series, or sequence, of uniformly spaced sample points. The digital sample point values thus generated are subsequently converted to analog form.

The sample points are preferably uniformly spaced because such a format permits the most direct analysis, and therefore the most direct synthesis, of the desired waveform. If desired, the uniform spacing of sample points may be such that there is provided an integral number of samples per cycle for each note frequency to be generated. Such a technique requires a sampling rate that varies directly with the frequency. Alternatively, the samples may be spaced uniformly in time, in which case the number of sample points differs according to frequency, and the phase angle between sample points varies with the frequency of the note to be generated. Although the synthesis of a multiplicity of note frequencies can be implemented for either technique, using a single clock frequency, the preferred frequency synthesis technique is that in which the phase angle between the sample points varies with frequency, i.e., in which the sampling rate is fixed for all note frequencies to be generated, and the various generated note frequencies are produced as a result of the different phase angles.

According to a specific application of the memory addressing technique of the present invention, then, there is provided a means for continuously calculating phase angles, to make available to a selection means any desired phase angle corresponding or related to a specific frequency, the selection means being governed by frequency criteria dependent on the note associated with the depressed key. The selection of a particular phase angle is translated into a sample point address in the memory unit within which the digital values representing amplitude samples of the waveform are stored.

As the phase angle changes, the rate at which the memory unit is addressed changes. This is accomplished by providing an address register to which the phase angle number is supplied, and which is incremented according to the value of the phase angle number. That is to say, once each clock time, the phase angle number is added to the sample point address reg-

ister. Only a relatively small number of bits of rather low significance in the latter register are used to designate the sample point addresses, and these bits are arranged to be incremented at a rate which depends upon the phase angle number, so that a new address may or may not be specified for several periodic increases in the address-identifying word. In the limit, an actual sample point address in the memory is identified and the memory is thereupon appropriately accessed for retrieval of the data contained at those addresses, for each increment dictated by the phase angle number. This limit is the uppermost note frequency that can be generated by the organ. For lower frequencies, the incrementing of the sample point address register is such that new addresses are identified only after a corresponding number of repetitions of the phase angle number, at the fixed clock frequency.

Accordingly, it is the principal object of this invention to provide a method and apparatus for addressing a memory at any one of several selectively controllable rates.

It is another object of this invention to provide methods and apparatus consistent with the object set forth immediately above, in which the memory unit contains digital data of related information content, so arranged or so located that sequential addresses of the memory are to be read out in sequence.

Still another object of this invention is to provide a method and apparatus as set forth above, specifically for use in the tone generating system of a digital electronic musical instrument.

BRIEF DESCRIPTION OF THE DRAWINGS

In describing the present invention, reference will be made to the accompanying figures of drawing, in which:

FIG. 1 is a simplified block diagram of a portion of a digital electronic organ system whose overall structure and function demonstrates a specific application of the controllable readout of a memory in accordance with the invention, in which portion a time division multiplexed signal is produced containing a recycling sequence of time slots each associated with a particular key of the organ, the contents of each time slot indicating whether the associated key has been actuated;

FIG. 2 is a circuit diagram of an exemplary decoder for use in the system of FIG. 1;

FIG. 3 is a more detailed circuit diagram of the switching array and encoder used in the system of FIG. 1;

FIG. 3A is a circuit diagram of an alternative encoder to that shown in FIG. 3, for use in the system of FIG, 1;

FIG. 4 is a circuit diagram of the input-output bus connecting means at each intersection in the switching array of FIG. 3;

FIG. 5 is illustrative of a multiplexed waveform developed by the system of FIG. 1 and responsive to actuation of selected keys;

FIG. 6 is a simplified block diagram of a generator assignment and tone generating apparatus for processing the multiplexed signal produced by the system of FIG. 1 to develop the desired tones as an audible output of the organ;

FIG. 7A and 7B together constitute a circuit diagram of one embodiment of the tone generator assignment logic for the system of FIG. 6;

FIG. 8A is a block diagram of a tone generator employing the principles of the present invention with regard to selective rate of addressing a memory, for use with assignment logic of FIGS. 7A and 7B in the system of FIG. 6;

FIG. 8B is a block diagram of an alternate embodiment of a portion of the tone generator of FIG. 8A; and

FIG. 9 is illustrative of a complex waveshape of the type produced by a pipe organ, and of the sample points at which amplitude values are taken for simulation at selected note frequencies.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, the keyboard multiplexing system or note selection system includes a keyboard counter 1 which is implemented to provide a specified count for each key of each keyboard (including manuals and pedal divisions) of the organ. If, for example, the electronic organ in which the multiplexing system is used has four keyboards, such as three manuals and a pedal board, each encompassing up to eight octaves, then keyboard counter 1 should have the capability of generating $4 \times 8 \times 12 = 384$ separate counts (digital words). It is essential that the counter be capable of developing a count representative of every key on every keyboard of the organ; however, it may be desirable to provide a counter that can produce a count greater than the number of available keys in order to have available certain redundant counts not associated with any keys. Such redundancy is readily provided by simply utilizing a counter of greater capacity than the minimum required count.

Keyboard counter 1 is divided into three separate sections (or separate counters) designated 2, 3 and 4. the first section (designated 2) is constructed to count modulo 12 so as to designate each of the twelve keys associated with the 12 notes in any octave. The second section (designated 3) is adapted to count modulo 8, to specify each of the eight octaves encompassed by any of the four keyboards. The last section (designated 4) is designed to count modulo 4 to specify each keyboard of the organ. Therefore, the overall keyboard counter is arranged to count modulo 384, in that at the conclusion of every 384 counts, the entire set of keyboards have been covered (scanned) and the count repeats itself. To that end, each counter section may be composed of a separate conventional ring counter, the three counters being connected in the typical cascaded configuration such that when section 2 reaches its maximum count it advances the court of counter section 3 by one, and will automatically initiate a repetition of its own count. Similarly, attainment of its maximum count by counter section 3 is accompanied by advancement of the count of section 4 by one.

Advancement of the count of counter 2 is accomplished by application of clock pulses thereto from a master clock source 5 which delivers clock pulses at a sufficiently rapid repetition rate (frequency) to ensure resolution of depression (actuation) and release (deactuation) of any key on any keyboard, i.e., to supply a pulse at the instant of either of these events. Scanning of all keyboards of the organ at a rate of 200 or more times a second is deemed quite adequate to obtain this desirable resolution. For the exemplary keyboard counter set forth above, this is equivalent to a minimum of $200 \times 384 = 76{,}800$ counts per second, so that a

master clock delivering clock pulses at a rate of 100 KC/s is quite suitable.

A total of four lines emanate from counter 4, one line connected to each ring counter stage, to permit sensing of the specific keyboard which is presently being scanned. Similarly, eight lines are connected to the eight ring counter stages, respectively, of octave counter 3 to detect the octave presently being scanned. Thus, a total of 12 lines extend from counters 3 and 4, and these twelve lines can carry signals indicative of 32 (8 × 4) possible states of the keyboard counter. The specific one of the 32 states, representative of a particular octave on a particular keyboard, which is presently being scanned is determined by use of a decoder circuit 7 composed of 32 AND gates designated 8–1, 8–2, 8–3, . . . , 8–32 (FIG. 2), each with two input terminals and an output terminal. The gates are arranged in four groups of eight each, with every gate of a particular group having one of its two input terminals (ports) connected to one of the four lines of counter 4. Distinct and different ones of the eight lines from counter 3 are connected to the other input terminal of respective ones of the eight AND gates of that group. A corresponding situation exists for each group of AND gates, with the only difference being that each group is associated with a different output line of counter section 4. Using this arrangement, the decoder logic designates every octave of keys in the organ by a respective driver pulse when a count corresponding to that octave is presently contained in the counter.

The output pulses derived from the AND gates (or drivers) of decoder circuit 7 are supplied on respective ones of 32 bus bars (or simply, buses), generally designated by reference numeral 10, to a keyboard switching array 11. From the preceding descripton, then, it will be clear that array 11 has one input bus 10 for every octave of keys in the organ (including every octave on every keyboard), and that a drive pulse will appear on each input bus approximately 200 times per second, the exemplary rate of scan of the keyboard, as noted above, for obtaining adequate resolution of operation of the keys. Switching array 11 also has twelve output buses, generally designated by reference number 12, each to be associated with a respective one of the twelve notes (and hence, the twelve keys) in any given octave.

Array 11 is basically a diode switching matrix, in which spaced input buses 10 and spaced output buses 12 are orthogonally arranged so that an intersection or crossing occurs between each input bus and each output bus (see FIG. 3), for a total of 384 intersections, one for each count of the keyboard counter 1. As is typical in this type of matrix, the crossed lines or buses are not directly interconnected. Instead, a "jump" diode, such as that designated by reference number 13 in FIG. 4, is connected between the input bus 10 and the output bus 12 at each intersection, the diode poled for forward conduction (anode-to-cathode) in the direction from an input bus 10 to an output bus 12. Wired in series circuit or series connection with each diode 13 is a respective switch 14 which is normally open circuited and is associated with a distinct respective one of the keys of the organ, such that depression of the associated key produces closure (close circuiting) of the switch 14 whereas release of the associated key results in return of the switch to its open state. Alternatively, each of switches 14 may itself constitute a respective key of the various keyboards of the organ.

While switch 14 is shown schematically as being of mechanical single pole, single throw (SPST) structure, it will be understood that any form of switch, electronic, electromechanical, electromagnetic, and so forth, may be utilized, the exact nature of the switch depending primarily upon the nature of the energization produced upon operation of the associated key. Switch 14, then, is adapted to respond to the particular form of enerization or actuation produced upon operation of a key on any keyboard (or, as observed above, may itself constitute the key), to complete the circuit connecting associated diode 13 between a respective input bus 10 and a respective output bus 12 at the intersection of those buses, when the key is depressed, and to open the circuit connecting the diode between respective input and output buses at that intersection when the key is released. Positive pulses occurring at the rate of approximately 200 per second, for example, according to the timing established by master clock 5, are transferred from input bus 10 to output bus 12 via the respective diode 13 and closed switch 14 when the associated key is depressed. While a switch alone (i.e., without the series connected diode) would serve the basic purpose of transferring a signal between the input and output lines of array 11, the diode provides a greater degree of isolation from sources of possible interference (noise) and acts to prevent feedback from output to input lines.

In FIG. 3, the output buses 12 from switching array 11 are connected to an encoder circuit 15 to which are also connected the twelve output lines, generally designated by reference number 16, from keyboard counter section 2. To produce an orderly arrangement in which each key of the organ is assigned a distinct and different time slot in a time-division multiplex waveform, the switches 14 associated with the respective keys are conveniently arranged in a specific sequence in the switching array 11. Assume, for example, that a specific output bus 17 of the switching array is to be associated with note A of any octave, a second output bus 18 is to be associated with note B of any octave, and so forth. Then switches 14 in the row corresponding to output bus 17 in array or matrix 11 are associated with the keys corresponding to the note A in each octave of keys in the organ. The column position of each switch 14 in matrix 11 corresponds to a specific octave of keys in the organ, and hence, to a specific octave encompassed by a specific keyboard of the organ.

Each of the output buses 12, including 17, 18, and so forth, is connected to one of the two input ports or terminals of a respective AND gate of the twelve AND gates 20–1, 20–2, 20–3, . . . , 20–12, of encoder circuit 15. An output lead 16 of counter section 2 associated with the ring counter stage designating the count for a particular note (key) in a given octave is connected to the remaining port of an encoder circuit AND gate having as its other input a pulse on the output bus 12 associated with that same note. A similar arrangement is provided for each of the remaining eleven output lines 16 of counter section 2 with respect to the AND gates 20 and the output buses 12. Thus, for example, if output bus 17 (associated with the row of switches 14 in matrix 11 for note A) is conected to one input terminal of AND gate 20–1, then output line 22 from the stage of counter 2 designating the count associated with note

A is connected to the remaining input terminal of gate **20–1.** The output terminal of each of AND gates **20** is connected to a respective input terminal of OR gate **23,** the output of the OR gate constituting the output signal of the encoder circuit. By virtue of its structure, encoder circuit **15** is effective to convert the parallel output of array **11** to a serial output signal in accordance with the scanning of output buses **12** as provided by the advancing and repeating count sensed in the form of pulses (at a rate of about 200 per second) appearing on output lines **16.** The end result of this circuitry is the production of a time-division multiplex (TDM) signal on a single conductor **25** emanating from encoder **15.**

As an alternative to the specific logic construction shown for encoder **15** in FIG. **3,** the encoder may have the circuit configuration exemplified by FIG. 3A. Referring to the latter Figure, the encoder includes a shift register **80** having twelve cascaded stages designated **SR1, SR2, SR3, . . . , SR12,** each connected to a respective output bus **12** of switching matrix **11** to receive a respective output pulse appearing thereon. The shift register stages are loaded in parallel with the data read from switching array **11** on output buses **12,** in response to each of the pulses appearing (i.e., each time a pulse appears) on one of the 12 output leads **16** of note counter **2.** That one output of the note counter which is to supply the load command for all twelve stages of shift register **80** is selected to permit the maximum amount of settling time to elapse between each advance of octave counter **3** and keyboard counter **4** and the loading of the shift register. In other words, it is extremely desirable that the data to be entered into the shift register from the switching array be stabilized to the greatest possible extent, and this is achieved by allowing the counters whose scanning develops this data, to settle at least immediately prior to loading. Thus, the first note counter stage, or one of the early stages, is selected to provide "load" pulses to shift register **80.**

"Shift" pulses are supplied to the shift register by master clock **5,** which also supplies note counter **2,** to shift the contents of each shift register stage to the next succeeding stage except during those bit times when the shift pulse is pre-empted by a load pulse from the note counter. Accordingly, shift register **80** is parallel loaded, and the data contents of the register are then shifted out of the register in serial format on encoder output line **25** until a one-bit pause occurs when another set of data is parallel loaded into the shift register, followed again by serial readout on line **25.** This serial pulse train constitutes the time division multiplexed output signal of encoder **15** just as in the embodiment of FIG. **3,** except that with the FIG. 3A configuration, decoder **7** (and the counters **3** and **4** supplying pulses thereto) undergo a greater amount of settling time.

It will be observed that this operation consitutes a parallel-to-serial conversion of the information on output buses **12** to a time-division multiplexed waveform on the output line **25** of encoder **15.**

In the TDM signal, each key has a designated time slot in the 384 time slots constituting one complete scan of every keyboard of the organ. In the specific example of the time base provided by master clock **5,** the TDM waveform (shown by way of example in FIG. **5**) is initiated about 200 times per second. This waveform contains all of the note selection information, in serial digital form on a single output line, that had heretofore required complex wiring arrangements. This waveform development will be more clearly understood from an example of the operation of the circuitry thus far discussed. It should be observed first, however, that all of the counter and logic circuitry described up to this point can be accommodated within a very small volume of space by fabrication in integrated circuit form using conventional microelectronic manufacturing techniques.

When the main power switch for the electronic organ is turned on, all components are energized to an operational state, the master clock delivering pulses to keyboard counter **1** at the aforementioned rate. Upon depression of a key on any keyboard of the organ, including the manuals and pedal divisions, a respective switch **14** associated in series connection with a diode **13** at the intersection between the appropriate input bus **10** and output bus **12** of the switching array **11** is closed, thereby connecting the two buses to supply pulses appearing on a given bus **10** from decoder **7,** to the appropriately connected output bus **12** for application to encoder **15.** If, for example, the key that was depressed is associated with note C in the second octave, C_2 appears in the appropriate time slot of the multiplexed signal emanating from encoder **15** and will repetitively appear in that time slot in each scan of the keyboards of the organ as long as that key is depressed. That is to say, a pulse appears on output line **10** of decoder **7** associated with the second octave in the manual being played, in accordance with the scan provided by master clock **5,** as the counter stage associated with that octave is energized in keyboard counter octave section **3** and the counter stage associated with that manual is energized in section **4** of the keyboard counter. The connection between the appropriate input bus **10** and output bus **12** of switching array **11** for the particular octave and keyboard under consideration is effected by the depression and continued operation of the key associated with the switch **14** for that intersection in the array. Since, as previously stated, each switch is associated with a particular note (key) and is positioned in a specific row of the switching array, a signal level is thereby supplied to the appropriate output bus **12** of the switching array arranged to be associated with that note. Each time the specified note, here the note C, is scanned in the sequence of count in the note section **2** of the keyboard counter, a second input is provided to the AND gate **20** receiving the signal level on output bus **12,** and a pulse is delivered to OR gate **23.** By virtue of this operation, the pulse which appears at the output of OR gate **23** always appears in the identical specified time slot in the multiplexed signal for a specific note associated with a particular key on a particular keyboard of the organ.

If more than one key is depressed, regardless of whether one or more keyboards is involved, operation corresponding to that described above for a single depressed key is effected for every operated key. Thus, for example, assume that the key associated with note C_2 is played on one manual, the note B_4 is played on a second manual, and the notes D_5, E_5, and G_5 are played on a third manual, the associated keys being depressed substantially simultaneously to produce desired simultaneous reproduction of all notes as the audio output of the organ. Under these conditions, the associated switches **14** in the switching array **11** are closed to provide through connections between the respective input

buses 10 and output buses 12 for the specific octaves and manuals involved. As the appropriate AND gates 20 in encoder 15 are supplied with gating signals from the sequentially energized counter stages of note section 2, during the scanning operation provided by that keyboard counter section, pulse levels appearing on output buses 12 for which switches 14 have been closed are gated in the appropriate time slots of the multiplex signal on the output lead 25 from OR gate 23 of encoder 15, for the specific notes involved.

An example of the multiplex signal waveform thus generated is shown in FIG. 5. While the pulses appearing in the time slots associated with the specific notes mentioned above are in a serial format or sequential order, their appearance is repetitive during the interval in which the respective keys are actuated. Hence, the effect is to produce a simultaneous reproduction of the notes as an audio output of the organ, as will be explained in more detail in connection with the description of operation of the tone generation section.

Referring now to FIG. 6, the multiplexed signal arriving from encoder 15 is supplied to generator assignment logic network 26 which functions to assign a tone generator 28 to a depressed key (and hence, to generate a particular note) when the associated pulse first appears in its respective time slot in the multiplexed signal supplied to the assignment logic. If only 12 tone generators 28 are available in the particular organ under consideration, for example, the assignments are to be effected in sequence (order of availability), and once particular pulses have been directed to all of the available generators (i.e., all available tone generators have been "captured" by respective note assignments), the organ is in a state of saturation. Therafter, no further assignments can be made until one or more of the tone generators 1s released. The availability of 12 (or more) tone generators, however, renders it extremely unlikely that the organ would ever reach a state of saturation since it is quite improbable that more than twelve keys would be depressed in any given instant of time during performance of a musical selection. The output waveforms from the captured tone generators at the proper frequencies for the notes being played, are supplied as outputs to appropriate waveshaping and amplification networks and thence to the acoustical output speakers of the organ. If the tone generators 28 supply a digital representation of the desired waveform, as is the case in one embodiment to be described, then the digital format is supplied to an appropriate digital-to-analog converter, which in turn supplies an output to the waveshaping network.

At any given instant of time, each tone generator 28 may be in only one of three possible states, although the concurrent states of the tone generators may differ from one tone generator to the next. These three states are as follows:

1. a particular note represented by a specific pulse in the multiplexed signal has captured (i.e., claimed) the tone generator;

2. the tone generator is presently uncaptured (i.e., unclaimed or available), but will be captured by the next incoming pulse in the multiplexed signal associated with a note which is not presently a tone generator captor; and

3. the tone generator is presently available, and will not be captured by the next incoming pulse.

It should be apparent from this delineation of possible states that any number of the tone generators provided (12, in this particular example) may be in one or the other of the states designated (1) and (3), above, but that only one of the tone generators can be in state (2) during a given instant of time. That is, one and only one generator is the next generator to be claimed. When the specific tone generator in state (2) is claimed by an incoming pulse, the next incoming pulse which is not presently claiming a tone generator is to be assigned to the generator that has now assumed state (2). For example, if the third tone generator (No. 3) of the 12 generators is captured by an incoming pulse (note representation) and the fourth generator (No. 4) was and still is captured by a previous note selection, then tone generator No. 4 is unavailable to the next incoming pulse, and the privilege of capture must pass to the next tone generator which is not presently in a state of capture. If all of the tone generators are captured, that is, all are in state (1as described above, then the organ is saturated and no further notes can be played until at least one of the tone generators is released. As previously observed, however, the saturation of an organ having 12 (or more) tone generators is highly unlikely. Generator assignment system 26 is utilized to implement the logic leading to the desired assignment of the tone generators 28, and thus to the three states of operation described above. An exemplary embodiment of the generator assignment logic is shown in FIGS. 7A and 7B. Referring to FIG. 7A, a ring counter 30, or a 12-bit recirculating shift register in which one and only one bit position is a logical "1" at any one time, is used to introduce a claim selection, i.e., to initiate the capture, of the next available tone generator in the set of tone generators 28 provided in the organ. A shift signal appearing on line 32 advances the "1" bit from one register or counter stage to the next, i.e., shifts the "1" to the next bit position. Each bit position is associated with and corresponds to a particular tone generator, so that the presence of the logical "1" in a particular bit position indicates selection of the tone generator to be claimed next, provided that it is not already claimed.

Each time the logical "1" appears in a stage of shift register 30, a "claim select" signal appears on the respective output line 34 associated with the stage. This "claim select" signal is supplied in parallel to one input of a respective one of AND gates 35, on line 36, and to further logic circuitry (to be described presently with reference to FIG. 7B), on line 37. The output line of each of AND gates 35 is connected to a separate and distinct input line of an OR gate 40 which, in turn, supplies an input to an AND gate 42 whose other input constitutes pulses from the master clock 5.

In operation of the portion of the generator assignment logic shown in FIG. 7A, assume that shift register stage No. 2 contains the logical "1". That stage therefore supplies "claim select 2" signal to the respectively associated AND gate 35 and, as well, to further logic circuitry on line 37. If this further logic circuitry determines that the associated note generator may be claimed, a "claimed" signal is applied as the second input to the respectively associated AND gate 35. Since both inputs of that AND gate are now "true" , an output pulse is furnished via OR gate 40 to the synchronization gate 42. The latter gate produces a "shift" pulse on line 32 upon simultaneous occurrence of the output pulse from OR gate 40 and a clock pulse from master

clock 5. Accordingly, the logical "1" is advanced one bit position, from stage No. 2 to stage No. 3 of shift register 30, in preparation for the claiming of the next tone generator.

Suppose, however, that the tone generator 28 corresponding to stage No. 3 is already claimed by a previous note pulse in the multiplexed signal. In that event a "claimed" signal appears as one input to the associated AND gate 35, and with the "claim select" signal appearing as the other input to that gate by virtue of stage No. 3 containing the single logical "1", another shift pulse is immediately generated on line 32 to advance the logical "1" to stage No. 4 of the shift register. Similar advancement of bit position of the "1" continues until an unclaimed tone generator is selected. If it should happen that no note is presently being selected on a keyboard of the organ at the time when an unclaimed tone generator is selected, the "1" bit remains in the shift register stage associated with the selected tone generator until such time as a "claimed" signal is concurrently applied to the respective AND gate 35, i.e., until the selected tone generator is claimed, because until that time no further shift signals can occur.

Referring now to FIG. 7B, each tone generator also has associated therewith a respective portion of the generator assignment logic as shown in that Figure. In other words, the circuitry of FIG. 7B, with minor exceptions to be noted in the ensuing description, is associated with the i'th tone generator (where $i = 1, 2, 3, \ldots, 12$), and since each of these portions of the assignment logic is identical, a single showing and description will suffice for all. An AND gate 50 has three inputs, one of which is the multiplexed signal deriving from encoder 15 (this being supplied in parallel to the AND gates 50 of the remaining identical portions of the assignment logic for the other tone generators, as well), a second of which is the "claim select" signal appearing on line 37 associated with the 11th stage of shift register 30 (FIG. 7A), and the third of which is a signal, on line 52, indicating that the pulse in the multiplexed signal has not captured any tone generator as yet. Of course, these signals are not present unless the respective events which produce them are actually occurring, but if all three signals are simultaneously presented as inputs to AND gate 50, a "set" signal is applied to a claim flip-flop 53 to switch that flip-flop to the "claimed" state and simultaneously therewith to supply a "claimed" signal to the AND gate 35 associated with the 11th stage of shift register 30 and to the respectively associated tone generator 28.

A modulo 384 counter 55 is employed to permit recognition by the respective portion of the generator assignment logic of the continued existence in the multiplexed signal of the pulse (time slot) which resulted in the capture of the associated tone generator. To that end, counter 55 is synchronized with keyboard counter 1 (also a modulo 384 counter) by simultaneous application thereto of clock pulses from master clock 5. The count of each counter 55 associated with an uncaptured tone generator is maintained in synchronism with the count of keyboard counter 1 by application of a reset signal to an AND gate 58 each time the keyboard counter assumes a zero count; i.e., each time the count of the keyboard counter repeats. However, that reset signal is effective to reset counter 55 only if the associated tone generator is uncaptured. The latter information is provided by the state of flip-flop 53, i.e., a "not claimed" signal is supplied as a second input to AND gate 58 whenever flip-flop 53 is in the "unclaimed" state.

When the flip-flop (and hence, the associated tone generator) is claimed, however, it is desirable to indicate the time slot occupied by the pulse which effected the capture, and for that reason a "reset" signal is applied to counter 55 at any time that an output signal is derived from AND gate 50. Thus, in the captured state, the zero count of counter 55 occurs with each repetition of the "capturing" pulse in the TDM waveform. Such information is valuable for a variety of reasons; for example, to prevent capture of an already captured tone generator when the zero count continues to appear simultaneously with a pulse in the TDM waveform, and to provide a "key released" indication when the zero count is no longer accompanied by a pulse in the TDM waveform. Capture prevention is effected by feeding a signal representative of zero count from counter 55 to the appropriate input terminal of an OR gate 60 associated with all of the tone generators and their respective generator assignment logic. The logical "1" supplied to OR gate 60 is inverted so that simultaneous identical logical inputs cannot be presented to AND gate 50. On the other hand, when the zero count is merely snychronized with the zero count of the keyboard counter and is not the result of capture of the associated tone generator it does not interfere with subsequent capture of that tone generator since it does not occur simultaneously with a pulse in the TDM signal. A "key release" indication is obtained by supplying the "zero count" signal to an AND gate 62 to which is also supplied any signal deriving from an inverter 63 connected to receive inputs from the TDM signal. If the zero count coincides with a pulse in the multiplexed signal, the inversion of the latter pulse prevents an output from AND gate 62, and this is proper because the coincidence of the zero count and the TDM pulse is indicative of continuing depression of the key which has captured the tone generator. Lack of coincidence is indicative that the key has been released, and results in the "key release" signal. Scanning of the keyboards is sufficiently rapid that any delay which might exist between actual key release and initiation of the "key release" signal is negligible, and in any event is undetectable by the human senses. Furthermore, the generation of a false "key release" signal when the tone generator is presently unclaimed, as a result of the occurrence of a zero count from counter 55 synchronized with the zero count of the keyboard counter and the simultaneous absence of a pulse in the TDM signal, can have no effect on the audio output of the organ since the associated tone generator is not captured and is therefore not generating any tone. In any case, the "key release" signal deriving from AND gate 62 is supplied to attack/delay logic of the tone generator to initiate the decay of the generated tone.

The "set claim" signal output of AND gate 50 that occurs with the simultaneous appearance of the three input signals to that gate is utilized to provide a "key depressed" indication to the attack/decay circuitry of the tone generator (and to percussive controls, if desired), as well as to provide its previously recited functions of "setting" flip-flop 53 and "resetting" counter 55.

The assignment logic embodiment of FIGS. 7A and 7B may be associated with only a small number of tone generators (twelve, in the example previously given), the exact number being selected in view of the cost limitations and the likely maximum number of keys that normally may be actuated simultaneously. In that case, each tone generator must supply every desired frequency corresponding to every note in every octave that may be played on the electronic organ.

FIG. 8A illustrates, in block diagrammatic form, an example of a suitable tone generator for generating the frequencies required for the notes selected on the organ keyboards. Appropriate frequencies are produced by properly addressing a memory unit containing amplitude samples of the desired waveform obtained at uniformly spaced points in time. Since the sample points are uniformly spaced in time, rather than uniformly spaced on the basis that an integral number of samples be present per cycle for each note frequency, the phase angle between sample points varies according to the frequency of the note to be generated. In a broader sense, the tone generator system of FIG. 8A demonstrates the teachings of the present invention with regard to addressing a memory unit at selectively controlled rates.

In implementing the memory addressing system of the present invention, the keyboard counter 1 is preferably provided with a note or key counter section 2 having at least one additional normally unused count that is to precede the initial count representing the sequence of keys and notes associated therewith. This redudant count, which is readily provided by merely employing a counter of greater capacity than is needed to handle the minimum count, is utilized to provide a "start" pulse which precedes the count that occurs each time the keyboard counter is reset to zero. Such a start pulse in the keyboard pulse train may, for example, be assigned to an imaginary key approximately two octaves below the lowest note in each manual. Thus, this start pulse is the first pulse in the scan, for the illustrative example of scanning from low frequencies to high frequencies on each keyboard, and occurs automatically with reset of the counter **1**. The start pulse is applied to a flip-flop **100** for a purpose which will be explained presently. In addition the zero count, or count designating the reset, of octave section **3** of keyboard counter **1** is supplied to the other input terminal of flip-flop **100**. A memory unit **101**, which is to be addressed at any of a number of selectively controlled rates, is preferably a read-only memory containing the digital amplitude values at predetermined sample points of a single cycle of the comlex periodic waveform to be produced for all note frequencies. That is to say, the same complex periodic waveform is to be reproduced for each note played, the only difference being that the phase angle between sample points stored in memory **101** will differ according to the frequency at which the complex waveform is reproduced.

Before proceeding with a description of the system of FIG. 8A and its operation, concurrent reference is made to FIG. **9** illustrating a typical complex waveshape of the type that might be produced by a pipe organ. The waveshape shown in FIG. **9** has been sampled at a multiplicity of points, shown as vertical lines in the Figure, to obtain the amplitude data to be stored in memory unit **101**. It is only these uniformly spaced samples of amplitude that are stored in the memory and these may be stored in absolute form or in incremental form. In the former case, the data accessed is the actual amplitude of the output waveform at the respective sample point (i.e., with respect to a "zero" level at the abscissa). In the case of incremental amplitude information, however, the amplitude at each sample point as stored in memory **101** is simply the difference in amplitude between the amplitude of the present sample and the amplitude of the immediately preceding sample. Each of the amplitude samples stored in the memory preferably comprises a digital word of approximately seven or eight bits.

Memory unit **101** may be a microminiature diode array of the type disclosed by R. M. Ashby et al. in U. S. Pat. No. 3,377,513, issued Apr. 9, 1968 and assigned to the same assignee as the present invention. The array may, for example, contain an amplitude representation of the desired waveform in the form of an eight bit binary word at each of 48 or more sample points. Such a capacity permits the storage of up to one hundred 28 amplitude levels in addition to a polarity (algebraic sign) bit. In any event, the capacity of memory **101** should be sufficient to allow faithful reproduction of each of the note frequencies.

The system for addressing memory **101** includes a storage register **102** which when reset contains a number representing the phase angle between sample points for the lowest note frequency to be produced by the tone generator. The storage register **102** is connected in a recirculating loop **103** which includes a multiplier **104** and a gate **105.** The purpose of the multiplier is to successively multiply the contents of the storage register by the twelfth root of two (i.e., $2^{1/12}$) for computation of the phase angles between sample points of the complex waveform stored in memory **101** for every note frequency in the entire range of frequencies capable of being generated by the organ. This follows from the fact that in the equal interval, or even temperament, musical scale the note frequencies differ from one another by $2^{1/12}$.

The required computation may be performed in either a serial or parallel arrangement. For example, the storage register may be 12-bits long, and for serial operation, may recirculate once each 12 bit times. In such a case, the multiplier **104** is specifically constructed and arranged for serial operation. The keyboard counter octave section **3** (FIG. **1**) advances once each twelve bit times, and hence, the storage register recirculates once each count of the octave section counter.

The computation of phase angle need not be performed in a serial format, however. Referring to FIG. **8B**, a parallel arrangement is shown in which the storage register **102** is connected to a scaling circuit **120** which, in turn, is coupled to an adder **121** in the recirculating loop **103.** The twelfth root of two is approximately equal to 1.0000111100111, base **2,** which is equivalent to $(1+2^{-4}-2^{-8}+2^{-10}-2^{-13})$. The scaling circuit **120** is simply a set of multipliers. The adder **121** is preferably a cascaded network of parallel two input adders adapted to receive the outputs of the scalers. The phase angle number constituting the result of the addition is then recirculated back to the storage register **102.**

Returning now to FIG. **8A**, flip-flop **100** is reset upon application of zero count of the octave section counter thereto, and the reset output of the flip-flop also serves to reset the storage register **102.** Upon application of

the "start" pulse of the multiplexed signal to the flip-flop, the latter is switched to remove the register reset and to open the gate **105a** in recirculating loop **103,** thereby allowing the register contents to be multiplied by $2^{1/12}$ and re-stored in the register.

The phase angle number which is thereby calculated with each advance of the keyboard count, and which represents a different phase angle between amplitude samples of the waveform stored in memory **101** for each different frequency, is always available when a note generator is captured and is assigned to generate a particular note frequency. When the modulo **384** counter **55** in the assignment logic associated with the captured note generator is reset to zero, the phase angle number available from the storage register **102,** which is the correct phase angle for the selected note, because of the synchronization between the phase angle calculation and the keyboard count, is read into a phase angle register **108,** and this occurs each time that modulo **384** counter **55** goes to zero. To that end, the zero count of counter **55** is applied to a flip-flop **105** (e.g., a one-shot) which is normally set to prevent passage of the phase angle number through an associated gate **106,** but which is reset to open the gate **106** to permit passage of the phase angle number therethrough to the phase angle register **108** when the flip-flop **105** is reset by the zero count of counter **55.**

Quite clearly, the overall phase angle calculator and the read-only memory **101** may be shared by all of the tone generator **28.** Each tone generator is addressed individually in the sequence of addressing all tone generators. For that reason, an auxiliary sampling clock (not shown) may be utilized which comprises a clock rate, provided by the master sampling clock, successive clock pulses of which are directed to the series of tone generators. The sampling clock addressed to a given tone generator is thus at a rate comprising the pulse repetition rate of the master sampling clock divided by the number of tone generators provided in the system. Furthermore, since the same read-only memory may be addressed by all of the tone generators, an accumulator **104a** associated with the memory may be a composite structure associated with appropriate gating circuitry related to each tone generator for accumulating the information read from memory **101** in response to accessing thereof by a given tone generator.

Once each sampling clock time, as determined by the auxiliary sampling clock source controlled by the master clock, the phase angle value stored in the respective phase angle register **108** is added to the previously stored value in a sample point address register **109.** An address decoder **110** decodes preselected bit positions of the count established in register **109** to effect addressing of memory unit **101.** It is important to note that during addressing of memory **101,** it is the rate at which the value of the sample point address register **109** increases, and not the absolute value of its contents, which is significant in the control of the rate of readout of the memory **101,** and thus in the control of the frequency of the note produced by the given tone generator.

In this manner, once each clock time the phase angle number, comprising a digital binary word, is added to the sample point address register value and correspondingly, for each such clock time, the amplitude data in the memory location corresponding to the sample point address then contained in register **109** (as decoded by decoder **110**) is accessed. As a practical manner, only a relatively small, finite set of amplitudes can be stored in memory **101** because of practical limitations on its capacity, and thus only a finite number of addresses is available. Furthermore, each register must be of a finite, practical length. In particular, the length of each register must be determined by the accuracy with which the frequency of the note is to be generated. The frequency actually produced is precisely the value of the phase angle multiplied by the clock rate at which the contents of the phase angle register are supplied to the address register **109.** Thus, as the phase angle corresponding to the specific frequency changes, when a different note is selected, the rate at which the memory unit **101** is addressed also changes. In particular, it will be observed that the sample point address register **109** is incremented by the value of the phase angle number at each auxiliary clock time. That is to say, once each clock time, the phase angle number is added to the sample point address register. Only a relatively small number of bits in the region of least significance of the address register contents are used to designate the sample point addressed in memory **101** and these bits are arranged to be incremented at a rate which depends upon the phase angle number. Accordingly, for small phase angle numbers, no new address may be specified for several increases in the address-identifying number. At the uppermost note frequency, on the other hand, a sample point address in the memory is identified, and the memory is addressed for retrieval of the data contained in the specified location, for each increment of the address register dictated by the phase angle number. For lower frequencies, the incrementing of the sample point address register is such that new addresses are identified only after a corresponding number of repetitions of the phase angle number at the fixed clock frequency. In the embodiment of FIG. **8A**, the same effect is achieved by use of an address decoder **110.** The digital words thus read from memory unit **101** are supplied to an accumulator **1042** which provides a digital representation of the waveform at selected sample points over a cycle of the waveform and at a frequency corresponding to the note to be reproduced. As above described, this digital waveform representation may itself be operated upon for waveshape control (for example, attack and decay) and is subsequently supplied to a digital-to-analog converter for producing an analog signal suiable for driving the acoustical output means, such as audio speakers, of the organ.

What is claimed is:

1. An electronic organ including a keyboard having a plurality of keys respectively associated with notes of the musical scale, said keys being operable, when actuated, to develop signals for calling forth respectively associated notes as audible tones of the desired note frequencies from said organ, and a tone generator said tone generator comprising:

a memory storing amplitude samples of a waveform to be reproduced at the desired note frequencies, said amplitude samples of the waveform being taken at points uniformly spaced in time over a cycle thereof,

clock means establishing a fixed rate of accessing amplitude samples of said waveform from said memory,

means for developing a succession of phase angle numbers respectively corresponding in value to the

frequencies of the notes of the musical scale available to be called forth selectively by actuation of corresponding ones of the keys, and 7

means responsive to a signal developed by the actuation of any one of said keys for selecting the corresponding phase angle number, and responsive to said clock means for addressing the sample points to be accessed from said memory at a rate in proportion to the corresponding, selected phase angle for the note frequency associated with each actuated key, to cyclically reproduce the stored waveform at a frequency corresponding to the note frequency associated with the respective, actuated key.

2. An electronic organ as recited in claim **1** wherein said number developing means includes:

means for establishing a first number corresponding to a lowest frequency note available to be reproduced, and

means for successively increasing the first and each successive number by a common factor to develop a set of numbers differing respectively in succession by the common factor, thereby to correspond to successive note frequencies of the musical scale, for all note frequencies to be synthesized.

3. An electronic organ as recited in claim **2** wherein said responsive means includes:

a note frequency number register for storing the numbers corresponding to the selected note, and an address register for adding the stored, corresponding number to the contents of said address register at the fixed frequency of said fixed frequency generator, the content of said address register thereby increasing at a rate corresponding to the fixed frequency and the selected number and establishing the rate of addressing said memory.

4. A tone generator for synthesizing frequencies of the notes of the musical scale in an electronic musical instrument, the instrument including means for selecting the notes to be synthesized, said generator comprising:

memory means for storing amplitude values of a waveform to be reproduced at the desired note frequencies, said amplitude values of the waveform being taken at uniformly spaced points in time over one cycle of the waveform,

a fixed frequency generator,

means for developing a succession of numbers respectively corresponding in value to the frequencies of the notes of the musical scale available for selection, and

means responsive to the selection of a particular note to be synthesized by said generator for responding to the number developed by said developing means for that note frequency and the fixed frequency of said fixed frequency generator, thereby to address said memory at a rate corresponding to the frequency of said generator and the number for the corresponding note frequency, thereby cyclically to read out the stored amplitude values from said memory for synthesizing the selected note frequency.

5. An electronic organ as recited in claim **4** wherein said number developing means includes:

means for establishing a first number corresponding to a lowest frequency note available to be reproduced, and

means for successively increasing the first and each successive number by a common factor to develop a set of numbers differing respectively in succession by the common factor, thereby to correspond to successive note frequencies of the musical scale, for all note frequencies to be synthesized.

6. An electronic organ as recited in claim **5** wherein said responsive means includes:

a note frequency number register for storing the numbers corresponding to the selected note, and an address register for adding the stored, corresponding number to the contents of said address register at the fixed frequency of said fixed frequency generator, the content of said address register thereby increasing at a rate corresponding to the fixed frequency and the selected number and establishing the rate of addressing said memory.

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