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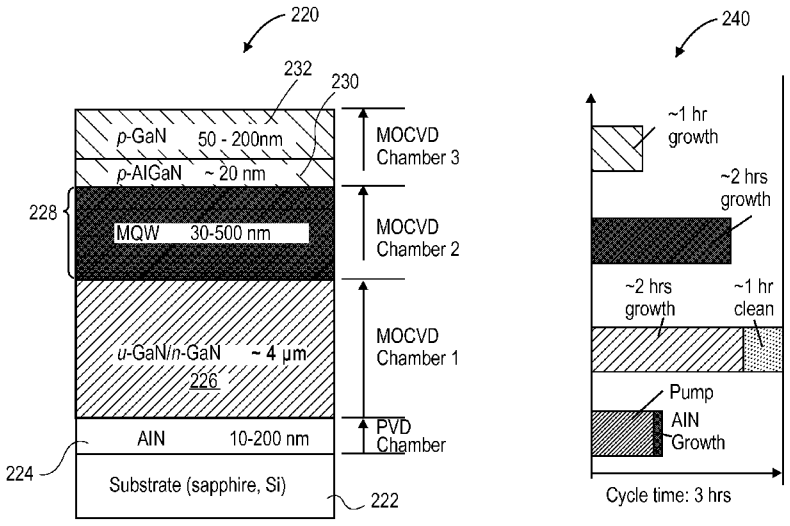

(57) Abstract: Oxygen controlled PVD AlN buffers for GaN-based optoelectronic and electronic devices is described. Methods of forming a PVD AlN buffer for GaN-based optoelectronic and electronic devices in an oxygen controlled manner are also described. In an example, a method of forming an aluminum nitride (AlN) buffer layer for GaN-based optoelectronic or electronic devices involves reactive sputtering an AlN layer above a substrate, the reactive sputtering involving reacting an aluminum-containing target housed in a physical vapor deposition (PVD) chamber with a nitrogen-containing gas or a plasma based on a nitrogen-containing gas. The method further involves incorporating oxygen into the AlN layer.

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OXYGEN CONTROLLED PVD ALN BUFFER FOR GAN-BASED OPTOELECTRONIC AND ELECTRONIC DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/785,128, filed March 14, 2013, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND

1) FIELD

[0002] Embodiments of the present invention pertain to the field of group III-nitride materials and, in particular, to the fabrication of gallium nitride-based optoelectronic or electronic devices with physical vapor deposition (PVD) formed aluminum nitride buffer layers.

2) DESCRIPTION OF RELATED ART

[0003] Group III-V materials are playing an ever increasing role in the semiconductor and related, e.g. light-emitting diode (LED), industries. Often, group III-V materials are difficult to grow or deposit on foreign substrates (known as heteroepitaxy) without the formation of defects or cracks. For example, high quality surface preservation of select films, e.g. a gallium nitride film, is not straightforward in many applications using stacks of material layers fabricated sequentially. The inclusion of one or more buffer layers between a substrate and a device layer has been one approach. However, group III-V materials are often sensitive to process conditions and care must be taken to avoid such conditions at particular periods of the fabrication process. Avoiding interaction of a sensitive group III-V film with potential damaging conditions, however, is also not straightforward in many applications.

SUMMARY

[0004] One or more embodiments of the present invention are directed to physical vapor deposition (PVD)-formed aluminum nitride buffer layers.

[0005] In an embodiment, a method of forming an aluminum nitride (AlN) buffer layer for GaN-based optoelectronic or electronic devices involves reactive sputtering an AlN layer above a substrate, the reactive sputtering involving reacting an aluminum-containing target housed in a physical vapor deposition (PVD) chamber with a nitrogen-containing gas or a plasma based on a nitrogen-containing gas. The method further involves incorporating oxygen into the AlN layer.

[0006] In another embodiment, a material stack for GaN-based optoelectronic or electronic devices includes a substrate, and an aluminum nitride (AlN) buffer layer disposed above the substrate. The AlN layer has a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

[0007] In another embodiment, a light-emitting diode (LED) device includes a substrate, and an aluminum nitride (AlN) buffer layer disposed above the substrate. The AlN layer has a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

[0008] In another embodiment, a GaN-based electronic device includes a substrate, and an aluminum nitride (AlN) buffer layer disposed above the substrate. The AlN layer includes a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

[0009] In another embodiment, a chamber for forming an aluminum nitride (AlN) buffer layer for GaN-based optoelectronic or electronic devices includes a pumping system and chamber cooling design that enables high base vacuum of 1E-7 torr or less and low rate-of-rise at high temperature. The chamber also includes a full face erosion magnetron cathode configured to enable consistent target erosion and uniform deposition of AlN film across carriers, within and between wafers. The chamber also includes a process kit and gas flow design configured to enable a uniform distribution of process gases, including O-containing gas, within the chamber for uniform AlN composition.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 illustrates a benchmark cluster tool schematic, a benchmark LED structure, and a benchmark time-to-deposition plot, in accordance with one or more embodiments of the present invention.

[0011] Figure 2A illustrates a cluster tool schematic and a corresponding temperature versus time plot for LED structure fabrication, in accordance with an embodiment of the present invention.

[0012] Figure 2B illustrates a light-emitting diode (LED) structure and a corresponding time-to-deposition plot, in accordance with an embodiment of the present invention.

[0013] Figures 3A-3C illustrate cross-sectional views of a process kit for a PVD chamber, in accordance with an embodiment of the present invention.

[0014] Figure 3D illustrates a cross-sectional view of a power delivery source for a PVD chamber, in accordance with an embodiment of the present invention.

[0015] Figure 4 is a schematic cross-sectional view of a MOCVD chamber suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0016] Figure 5 is a schematic cross-sectional view of a HVPE chamber suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0017] Figure 6 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0018] The fabrication of gallium nitride-based optoelectronic or electronic devices with physical vapor deposition (PVD) formed aluminum nitride (AlN) buffer layers is described. In the following description, numerous specific details are set forth, such as process chamber configurations and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as specific diode configurations, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. Additionally, other arrangements and configurations may not be explicitly disclosed in embodiments herein, but are still considered to be within the spirit and scope of the invention.

[0019] One or more embodiments are directed to oxygen controlled physical vapor deposition (PVD) based aluminum nitride (AlN) buffer layers for gallium nitride (GaN)-based optoelectronic and electronic devices. Embodiments may also include metal organic chemical vapor deposition (MOCVD) processes used to form layers on the PVD AlN film. Embodiments may be directed to lights emitting diodes (LEDs) or power devices. Features corresponding to one or more embodiments may include, or may implicate, sapphire substrates, patterned sapphire substrates, Si substrates, XRD, wafer bowing, film stress, and dislocations.

[0020] PVD AlN can be used as a buffer layer for GaN-based LEDs and power devices grown on a foreign substrate, such as a sapphire or silicon substrate. Use of a PVD AlN layer can improve the material quality of gallium nitride (GaN) layers grown on top of the AlN buffer. Improved GaN can be used to achieve improved device performance (e.g., brightness, IQE, device leakage and ESD in the case of LEDs, and higher breakdown voltage in the case of power devices) as well as reliability.

[0021] To provide context, in a typical MOCVD growth of GaN on a sapphire substrate, the use of PVD AlN buffer can eliminate operations of substrate pre-baking, low temperature GaN buffer and a big portion of temperature ramping, and enable fast growth and thinner device layers. Altogether, processing time can be reduced by saving cycle time by 1 to 3 hrs. For growth of GaN on silicon, where an AlN layer is necessary to protect a silicon substrate from gallium attack, PVD AlN can save about 3 to 6 hours of epitaxial process and chamber cleaning time combined. Such process time reduction can greatly enhance the system throughput. Thus, in accordance with embodiments of the present invention, the crystal quality of PVD AlN directly impacts the material quality of GaN grown on top of it.

[0022] As such, as described herein, one or more embodiments of the present invention provide process details, system, chamber and hardware configurations to achieve an AlN buffer layer that repeatedly leads to superior GaN properties.

[0023] More specifically, embodiments of the present invention described herein involve doping of an AlN layer with oxygen via introduction of an oxygen-containing gas prior to, during, or after AlN deposition to modify the properties, including chemical bonds, crystal structure, grain size and shape, and/or morphology of the AlN/substrate interface, AlN bulk film and AlN surface. In one such embodiment, not only the oxygen concentration but also the time and duration of

oxygen carrier introduction into a corresponding PVD chamber (e.g., for AlN formation) influence the quality of a subsequently formed GaN layer deposited thereon.

[0024] In an embodiment, applicable variables change depending on whether the starting substrate is planar or patterned (e.g., in the case of sapphire). When the oxygen concentration, flow rate, time of introduction, and other parameters (e.g., temperature, thickness, etc.) are optimized, growth of very high-quality AlN film is enabled. For example, in a specific embodiment, an AlN film with XRD (002) FWHM < 15 arcsec and surface roughness < 2 nm (root mean square) can be deposited. As a result, in a particular embodiment, GaN growth on foreign substrates with such buffer layers have much reduced dislocation density and narrower XRD FWHM (e.g., (002) < 100 arcsec, (102) < 150 arcsec). In a specific embodiment, the dislocation density is less than approximately 5E8 defects/cm^2. In an embodiment, XRD FWHM for (002) is approximately in the range of 50-250 arcsec. In an embodiment, XRD FWHM for (102) is approximately in the range of 70-250 arcsec. Embodiments of the invention are also directed to optimized hardware that enables high deposition rate, high precision control of temperature and gas composition that enables uniform modification of AlN interface, bulk and surface properties to ensure same high quality GaN achieved within the wafer and wafer to wafer.

[0025] An LED or power device method of fabrication can include the formation of a buffer layer of gallium nitride between a substrate and a device layer of un-doped and/or doped gallium nitride. In embodiments described herein, an aluminum nitride buffer layer is used in place of such a gallium nitride buffer layer, between the substrate and the device layer of un-doped and doped gallium nitride. The aluminum nitride layer may be formed by sputter deposition in a PVD process. This is different from traditional fabrication of group III-nitride buffer layers which is typically performed in a metal-organic vapor deposition (MOCVD) chamber, a molecular beam epitaxy (MBE) chamber, or a hydride vapor phase epitaxy (HVPE) chamber. The aluminum nitride layer may be formed by non-reactive sputtering from an aluminum nitride target housed in the PVD chamber or, alternatively, may be formed by reactive sputtering from an aluminum target housed in the PVD chamber and reacted with a nitrogen-containing gas or a plasma based on a nitrogen-containing gas.

[0026] In accordance with one or more embodiments, process conditions for PVD AlN buffer layers for GaN-based devices are described herein. One or more of the embodiments described herein may enable higher throughput in a multi-chamber fabrication tool used for LED or power device fabrication. Also, by including a PVD-formed aluminum nitride layer instead of a gallium nitride buffer layer, the device layer of un-doped and doped gallium nitride may be thinned overall. In a particular example, the un-doped portion may be thinned or eliminated altogether. Furthermore, preliminary sputter cleaning of a receiving substrate, such as a sapphire substrate, may be performed in the same PVD deposition chamber as is used to deposit the aluminum nitride layer. Additionally, the overall thermal budget of LED or power device fabrication may be reduced since the PVD aluminum nitride layer may be formed at temperatures below 300 degrees Celsius. By contrast, a typical gallium nitride or aluminum nitride MOCVD buffer layer is formed between 500-600 degrees Celsius. One or more of the embodiments described herein may enable faster deposition rates, e.g. two times the growth rate, for materials such as un-doped and/or n-type doped gallium nitride. Faster rates may be achieved since, in some embodiments, the un-doped and/or n-type doped gallium nitride layers are formed on an aluminum nitride (AlN) buffer layer which may provide an improved crystal orientation and morphological relationship for growing un-doped and/or n-type doped gallium nitride layers thereon. One or more of the embodiments described herein may enable an improvement of gallium nitride crystalline quality by forming the gallium nitride on a PVD-formed aluminum nitride buffer layer.

[0027] Embodiments of the present invention may provide improvements over a benchmark system or methodology developed during studies of the presently described systems and methodologies. For example, Figure 1 illustrates a benchmark cluster tool schematic, a benchmark LED structure, and a benchmark time-to-deposition plot, in accordance with one or more embodiments of the present invention.

[0028] Referring to Figure 1, a benchmark cluster tool 100 includes an un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 (MOCVD1: u-GaN/n-GaN), a multiple quantum well (MQW) MOCVD reaction chamber 104 (MOCVD2: MQW), and a p-type gallium nitride MOCVD reaction chamber 106 (MOCVD3: p-GaN). The benchmark cluster tool 100 may also include a load lock 108, a carrier cassette 110, and an optional additional un-doped and/or n-type gallium

nitride MOCVD reaction chamber 112 for high volume applications, all of which are depicted in Figure 1.

[0029] A benchmark LED structure 120 includes a stack of various material layers, many of which include III-V materials. For example, the benchmark LED structure 120 includes a silicon or sapphire substrate 122 (Substrate: sapphire, Si), a 20 nanometer thick buffer layer 124 (LT buffer), and an approximately 4 microns thick un-doped/n-type gallium nitride combination layer 126 (u-GaN/n-GaN). The buffer layer 124 may be a gallium nitride layer formed at relatively low processing temperatures. The buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 are formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 of benchmark cluster tool 100. The benchmark LED structure 120 also includes an MQW structure 128 with a thickness in the range of 30 – 500 nanometers. The MQW structure 128 is formed in MQW MOCVD reaction chamber 104 of benchmark cluster tool 100. The benchmark LED structure 120 also includes an approximately 20 nanometers thick p-type gallium aluminum nitride layer 130 (p-AlGaN) and a p-type gallium nitride layer 132 with a thickness in the range of 50 – 200 nanometers (p-GaN). The p-type gallium aluminum nitride layer 130 and the p-type gallium nitride layer 132 are formed in p-type gallium nitride MOCVD reaction chamber 106 of benchmark cluster tool 100.

[0030] A benchmark time-to-deposition plot 140 represents chamber usage in benchmark cluster tool 100. The formation of the MQW structure 128 in MQW MOCVD reaction chamber 104 has a growth time of approximately 2 hours. And, the formation of the p-type gallium aluminum nitride layer 130 and the p-type gallium nitride layer 132 in p-type gallium nitride MOCVD reaction chamber 106 has a growth time of approximately 1 hour. Meanwhile, the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 has a growth time of approximately 3.5 hours. An additional approximately 1 hour may be required for chamber cleaning of chamber 102. Thus, overall, the cycle time for fabricating benchmark LED structure 120 in benchmark cluster tool 100 is dictated by the cycle time of un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, which is approximately 4.5 hours. It is to be understood that cleaning time may, but need not, include time for shut-down, plus clean time, plus recovery time. It is also to be

understood that the above may represent an average since cleaning may not be performed between every chamber usage.

[0031] A benchmark timing sequence for LED material deposition specific to the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, as described in association with Figure 1, is provided below. For example, the growth time of approximately 3.5 hours is broken into a 10 minute high temperature treatment of a sapphire substrate, a 5 minute low temperature formation of a buffer layer, a 10 minute buffer annealing operation, a 30 minute growth recovery operation, a 2 hour un-doped/n-type gallium nitride combination layer formation operation, and a 30 minute temperature ramp and stabilization operation (e.g., temp ramp 2-3°C/s).

[0032] In reference to the benchmark systems and methodologies described in association with Figure 1, the benchmark approach may result in an unbalanced time flow for each functioning layer of the LED. For example, formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102 is 3.5 hrs, formation of the MQW structure 128 in MQW MOCVD reaction chamber 104 is 2 hours, and formation of the p-type gallium aluminum nitride layer 130 and the p-type gallium nitride layer 132 in p-type gallium nitride MOCVD reaction chamber 106 is 1 hour. Furthermore, as mentioned above, an additional approximately 1 hour of chamber cleaning (possibly including pump-down times) may be required between runs in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102. Such additional chamber cleaning may be required to avoid substrate contamination. As such, the progressive growth of the structure 120 with three MOCVD chambers results in significant idle time for the MQW MOCVD reaction chamber 104 and the p-type gallium nitride MOCVD reaction chamber 106, reducing the overall throughput of the system 100.

[0033] In an aspect of the present invention, the throughput of a cluster system for fabricating LED or power device structures may be improved by substituting one of or a portion of one of the above described MOCVD material growth capabilities or operations with a PVD sputtering deposition capability or operation. For example, Figure 2A illustrates a cluster tool schematic and a corresponding temperature versus time plot for LED structure fabrication, in accordance with an embodiment of the

present invention. Figure 2B illustrates an LED structure and a corresponding time-to-deposition plot, in accordance with an embodiment of the present invention.

[0034] Referring to Figure 2A, a cluster tool 200 includes a PVD aluminum nitride sputter chamber 202 (PVD AlN), an un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 (MOCVD1: u-GaN/n-GaN), a multiple quantum well (MQW) MOCVD reaction chamber 206 (MOCVD2: MQW), and a p-type gallium nitride MOCVD reaction chamber 208 (MOCVD3: p-GaN). The cluster tool 200 may also include a load lock 210, a carrier cassette 212, and a transfer chamber 214, all of which are depicted in Figure 2A.

[0035] Thus, in accordance with an embodiment of the present invention, a multi-chamber system includes a PVD chamber having a target of metallic or compound aluminum, and a chamber adapted to deposit un-doped and/or n-type gallium nitride, or both. In one embodiment, the target of the PVD chamber is composed of aluminum nitride. In such an embodiment, reactive sputtering need not be used since the target is composed of the same material desired for deposition. However, in an alternative embodiment, a target composed of aluminum is used, and aluminum nitride is reactively sputtered from the aluminum target by or in the presence of a nitrogen source. In one embodiment, the chamber adapted to deposit un-doped or n-type gallium nitride is a MOCVD chamber, as depicted in Figure 2A. However, in an alternative embodiment, the chamber adapted to deposit un-doped or n-type gallium nitride is a hydride vapor phase epitaxy (HVPE) chamber. In one embodiment, the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in a cluster tool arrangement, as depicted in Figure 2A. However, in an alternative embodiment, the PVD chamber and the chamber adapted to deposit un-doped or n-type gallium nitride are included in an in-line tool arrangement. Deposition processes based on PVD, as described herein, may be performed at temperatures approximating standard room temperature, or may be performed at higher temperatures.

[0036] Referring to Figure 2B, an LED structure 220 includes a stack of various material layers, many of which include III-V materials. For example, the LED structure 220 includes a silicon or sapphire substrate 222 (Substrate: sapphire, Si) and an aluminum nitride layer 224 (AlN) with a thickness approximately in the range of 10 – 200 nanometers. The aluminum nitride layer 224 is formed by sputter deposition in the PVD aluminum nitride sputter chamber 202 of cluster tool 200. The

LED structure 220 also includes an approximately 4 microns thick un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 (n-GaN). The un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 is formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 of cluster tool 200. The LED structure 220 also includes an MQW structure 228 with a thickness in the range of 30 – 500 nanometers. The MQW structure 228 is formed in MQW MOCVD reaction chamber 206 of cluster tool 200. In one embodiment, the MQW structure 228 is composed of one or a plurality of field pairs of InGaN well/GaN barrier material layers. The LED structure 220 also includes an approximately 20 nanometers thick p-type gallium aluminum nitride layer 230 (p-AlGaN) and a p-type gallium nitride layer 232 with a thickness in the range of 50 – 200 nanometers (p-GaN). The p-type gallium aluminum nitride layer 230 and the p-type gallium nitride layer 232 are formed in p-type gallium nitride MOCVD reaction chamber 208 of cluster tool 200. It is to be understood that the above thicknesses or thickness ranges are exemplary embodiments, and that other suitable thicknesses or thickness ranges are also considered within the spirit and scope of embodiments of the present invention.

[0037] A time-to-deposition plot 240 represents chamber usage in cluster tool 200. The formation of the MQW structure 228 in MQW MOCVD reaction chamber 206 has a growth time of approximately 2 hours. The formation of the p-type gallium aluminum nitride layer 230 and the p-type gallium nitride layer 232 in p-type gallium nitride MOCVD reaction chamber 208 has a growth time of approximately 1 hour. And, in accordance with an embodiment of the present invention, the formation of the un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204 has a growth time of only approximately 2 hours. An additional approximately 1 hour may be required for chamber cleaning of chamber 204. It is to be understood, however, that cleaning time may include time for shut-down, plus clean time, plus recovery time. It is also to be understood that the above may represent an average since cleaning may not be performed between every chamber usage.

[0038] Thus, instead of forming a buffer layer, such as buffer layer 124 of Figure 1, in the MOCVD chamber used to form gallium nitride layer 126, an aluminum nitride buffer layer 224 is instead included and is formed in another chamber, specifically in PVD aluminum nitride sputter chamber 202. Although the

AlN growth may be for a duration of approximately 5 minutes, excluding pump time (from approximately 400 torr to approximately 10^{-8} torr), the formation in a chamber separate from MOCVD chamber 1 increases throughput of cluster tool 200. For example, overall, the cycle time for fabricating LED structure 220 in cluster tool 200 is once again dictated by the cycle time of un-doped and/or n-type gallium nitride MOCVD reaction chamber 204, which is reduced to approximately 3 hours versus the benchmark system of 4.5 hours. As such, the progressive growth of the structure 220 with one PVD chamber in addition to three MOCVD chambers results in much less idle time for the MQW MOCVD reaction chamber 206 and the p-type gallium nitride MOCVD reaction chamber 208, improving the overall throughput of the system 200. For example, in one embodiment, tool throughput is improved from approximately 5.3 runs per day to approximately 8 runs per day, demonstrating an approximately 50% throughput improvement.

[0039] Referring again to Figure 2A, a representative temperature versus time plot 250 for LED structure fabrication in cluster tool 200 is provided. Region 252 of plot 250 is specific to the formation of un-doped/n-type gallium nitride combination or n-type gallium nitride-only layer 226 formed in un-doped and/or n-type gallium nitride MOCVD reaction chamber 204. In this region, only one temperature ramp (ramp down from approximately 1100 degrees Celsius to approximately 400 degrees Celsius) is needed. Such a single ramp event requirement is in stark contrast to the timing sequence for the formation of the buffer layer 124 and the un-doped/n-type gallium nitride combination layer 126 in un-doped and/or n-type gallium nitride MOCVD reaction chamber 102, as described above. In that case, the chamber starts at a high temperature for substrate treatment, ramps down in temperature for buffer layer fabrication, ramps back up in temperature for the gallium nitride deposition, and finally down again for stabilization. It is noted that in both cases, however, the region 254 and 256 of plot 250 specific to the formation of the MQW and the p-GaN, will be approximately the same. In an embodiment, referring to region 258 of plot 250, the temperature versus time plot for PVD-formed aluminum nitride could encompass either a high temperature (HT) or low temperature (LT) process, approximately in the range of 20 – 1200 degrees Celsius.

[0040] In addition to the throughput improvement for cluster tool 200, there may be additional benefits to a PVD chamber plus three MOCVD chamber tool arrangement. For example, cost savings may be achieved since less reaction gas may

need to be delivered to the first MOCVD chamber. PVD chamber engineering and design may be simpler compared with configuration time and complexity for an MOCVD chamber dedicated to both a buffer layer and a device layer, as is chamber 102 of benchmark cluster tool 100. In the case that the above process enables a reduced thickness for the un-doped gallium nitride portion of device layer 226, simpler down-the-line etch-back processes may be performed. This may also enable the saving of material and operation cost while reducing cycle time. Also, by using an aluminum nitride buffer layer in place of a gallium nitride buffer layer, reduced defectivity in the active layers of a device, such as an LED device or power device, may be achieved.

[0041] Thus, in accordance with an embodiment of the present invention, a multi-chamber system includes a PVD chamber having an aluminum nitride target, and a first MOCVD chamber to deposit un-doped or n-type gallium nitride. The multi-chamber system also includes a second MOCVD chamber to deposit a multiple quantum well (MQW) structure, and a third MOCVD chamber to deposit p-type aluminum gallium nitride or p-type gallium nitride, or both. In one embodiment, the PVD chamber having the aluminum nitride target is for non-reactive sputtering of aluminum nitride. In a specific such embodiment, the PVD chamber is for non-reactive sputtering of aluminum nitride at a low or slightly elevated temperature approximately in the range of 20 – 200 degrees Celsius. In another specific such embodiment, the PVD chamber is for non-reactive sputtering of aluminum nitride at a high temperature approximately in the range of 200 – 1200 degrees Celsius. In an alternative embodiment, the PVD chamber is for reactive sputtering of an aluminum target with a nitrogen-containing gas or a plasma derived from a nitrogen-containing gas.

[0042] It may be the case that regardless of deposition temperature, a PVD deposited aluminum nitride layer suitable for inclusion in LED structure 220 may need to be, at some point, exposed to a high temperature approximately in the range of 400 – 1400 degrees Celsius, e.g., about 900 degrees Celsius, in order to achieve requisite material properties (e.g., appropriate defect density, crystal grain size, crystal orientation, etc.). In accordance with an embodiment of the present invention, a rapid thermal processing (RTP) process is performed on the PVD deposited aluminum nitride layer prior to fabrication of additional layers on the aluminum nitride layer. An RTP chamber may, then, in some way be associated with the above described

fabrication process for LED structure 220. In one embodiment, a tool, such as a cluster tool or in-line tool including the PVD and three MOCVD chambers also includes a RTP chamber. In an alternative embodiment, however, an RTP process is performed in the PVD chamber. In another alternative embodiment, a laser annealing capability is associated with the above described fabrication process for LED structure 220.

[0043] In an aspect of the present invention, then, process conditions for forming a physical vapor deposition (PVD) aluminum nitride (AlN) buffer layer are described. Such a buffer layer may be included in, e.g., a GaN-based device. In an embodiment, a parametric process window is provided for the deposition of AlN with certain characteristic and properties.

[0044] In the case of light emitting diode (LED) fabrication, the process typically includes the formation of a low temperature buffer layer via metal organic chemical vapor deposition (MOCVD) on a substrate. Deposition of the buffer layer by MOCVD is typically followed by the formation of active device layers, e.g., un-doped, Si-doped n-type, MQW, and Mg-doped p-type GaN layers. Substrate pre-baking is normally performed at high temperatures (e.g., greater than approximately 1050 degrees Celsius). By contrast, deposition of the buffer layer is normally performed at low temperatures (e.g., approximately in the range of 500 – 600 degrees Celsius). The processes can account for approximately 10 - 30% of the total MOCVD process time. The MOCVD throughput may be enhanced by an ex-situ deposited buffer layer. Accordingly, in an embodiment, as described in greater detail below, an ex-situ deposited AlN buffer layer formed by PVD is described. In one embodiment, the PVD process is performed in a separate chamber.

[0045] In an embodiment, process conditions are provided for forming a substrate with an AlN buffer (template) suitable for use in GaN device fabrication. In one such embodiment, oxygen controlled deposition of the PVD AlN buffer is performed.

[0046] In an embodiment, an AlN buffer layer is formed by reactive sputtering from an aluminum-containing target housed in the PVD chamber and reacted with a nitrogen-containing gas or a plasma based on a nitrogen-containing gas. In one embodiment, oxygen incorporation is also performed. In an exemplary embodiment, one or more (or a combination thereof) of the following operations and conditions are used for the oxygen incorporation: (1) flow of an oxygen containing gas such as, but

not limited to, O_2, H_2O, CO, CO_2, NO, NO_2, O_3, or combinations thereof, into a PVD chamber; (2) the flow of oxygen containing gas prior to, during and/or after the plasma is turned on for deposition so that a chamber, process kit, and target can be pre-conditioned with absorbed oxygen, and/or have an optimal amount of oxygen incorporated at the AlN/substrate interface, in the AlN bulk film and at the AlN surface to render it suitable for high quality GaN growth; and (3) the oxygen containing gas flow amount, introduction time and duration are precisely controlled to ensure its uniform modification interface between the AlN and foreign substrate, in the AlN film and at the AlN surface. In a particular embodiment, the amount of oxygen (O) incorporated in the AlN film is approximately in the range of 1E18 to 1E23 atoms/cm^3. In an embodiment, the substrate having AlN deposition thereon is one such as, but not limited to, sapphire, Si, SiC, Si on diamond, ZnO, $LiAlO_2$, MgO, GaAs, copper, W, etc. The substrate may be flat or pre-patterned.

[0047] In an embodiment, hardware optimized for oxygen controlled deposition of a PVD AlN buffer layer includes one or more of the following configurations: (1) a pumping system, a chamber vacuum integrating design, and chamber cooling design that together enable a high base vacuum (e.g., 1E-7 torr or less) and a low vacuum leakage with a pressure rate-of-rise (e.g., 2,500 ntorr/min or less) at high temperature, e.g., 350 degrees Celsius or above; (2) a full face erosion magnetron cathode to ensure consistent target erosion and uniform deposition of an AlN film across sample carriers, within and between wafers; (3) a process kit and gas flow design that ensures a uniform distribution of process gases, including O-containing gas within the chamber so that optimal AlN composition can be achieved uniformly; (4) a high temperature biasable electro-static chuck that ensures fast and uniform heating up of wafers; and (5) inclusion of an Al target doped with oxygen so that optimal amount of oxygen can be uniformly incorporated into the deposited AlN film to ensure high quality GaN growth on top (e.g., in one embodiment, an aluminum target is doped with a concentration of oxygen approximately in the range of 1ppm – 10,000 ppm. In an embodiment, a chamber pasting process is utilized to ensure conditioning of a process kit and target uniformly and sufficiently and provide repeatable PVD AlN properties between pasting cycles. It is to be understood that, in one such embodiment, the number of pasting cycles can vary from one per run to one per target or process kit life. One or more of the above aspects is described below in association with Figures 3A-3D.

[0048] In one such embodiment, using the above conditions and hardware, deposition of high quality AlN is achieved repeatably from run to run, wafer to wafer and high uniformity within the wafer. On top of the AlN, high quality GaN with XRD (002) FWHM < 100 arcsec and/or XRD (102) FWHM < 150 arcsec can be grown, and the process has proven repeatability. In a specific embodiment, the GaN has a dislocation density less than approximately 5E8 defects/cm^2. In an embodiment, XRD FWHM for (002) is approximately in the range of 50-250 arcsec. In an embodiment, XRD FWHM for (102) is approximately in the range of 70-250 arcsec. In an embodiment, the above described unique hardware and process offer the exceptionally high AlN and GaN quality with high throughput and repeatability.

[0049] Exemplary embodiments of tool platforms suitable for housing a PVD chamber along with three MOCVD chambers include an Opus™ AdvantEdge™ system or a Centura™ system, both commercially available from Applied Materials, Inc. of Santa Clara, CA. Embodiments of the present invention further include an integrated metrology (IM) chamber as a component of the multi-chambered processing platform. The IM chamber may provide control signals to allow adaptive control of integrated deposition process, such as the multiple segmented sputter or epitaxial growth processes such as those described herein. The IM chamber may include a metrology apparatus suitable to measure various film properties, such as thickness, roughness, composition, and may further be capable of characterizing grating parameters such as critical dimensions (CD), sidewall angle (SWA), feature height (HT) under vacuum in an automated manner. Examples include, but are not limited to, optical techniques like reflectometry and scatterometry. In particularly advantageous embodiments, in-vacuo optical CD (OCD) techniques are employed where the attributes of a grating formed in a starting material are monitored as the sputter and/or epitaxial growth proceeds. In other embodiments, metrology operations are performed in a process chamber, e.g., in-situ in the process chamber, rather than in a separate IM chamber.

[0050] A multi-chambered processing platform, such as cluster tool 200 may further include an optional substrate aligner chamber, as well as load lock chambers holding cassettes, coupled to a transfer chamber including a robotic handler. In one embodiment of the present invention, adaptive control of the multi-chambered processing platform 200 is provided by a controller. The controller may be one of any form of general-purpose data processing system that can be used in an industrial

setting for controlling the various subprocessors and subcontrollers. Generally, the controller includes a central processing unit (CPU) in communication with a memory and an input/output (I/O) circuitry, among other common components. As an example, the controller may perform or otherwise initiate one or more of the operations of any of the methods/processes described herein. Any computer program code that performs and/or initiates such operations may be embodied as a computer program product. Each computer program product described herein may be carried by a medium readable by a computer (e.g., a floppy disc, a compact disc, a DVD, a hard drive, a random access memory, etc.).

[0051] Suitable PVD chambers for the processes and tool configurations contemplated herein may include the Applied Materials Endura® Impulse™ PVD system, commercially available from Applied Materials, Inc. of Santa Clara, CA. The Endura PVD system provides superior electromigration resistance and surface morphology as well as low cost of ownership and high system reliability. PVD processes performed therein may be done so at requisite pressures and suitable target-to-wafer distance which creates directional flux of deposited species in the process cavity. Chambers compatible with in-line systems such as the ARISTO chamber, also commercially available from Applied Materials, Inc. of Santa Clara, CA, provides automated loading and unloading capabilities, as well as a magnetic carrier transport system, permitting significantly reduced cycle times. The AKT-PiVot 55KV PVD system, also commercially available from Applied Materials, Inc. of Santa Clara, CA, has a vertical platform for sputtering deposition. The AKT-PiVot system's module architecture delivers significantly faster cycle time and enables a large variety of configurations to maximize production efficiency. Unlike traditional in-line systems, the AKT-PiVot's parallel processing capability eliminates bottlenecks caused by different process times for each film layer. The system's cluster-like arrangement also allows continuous operation during individual module maintenance. The included rotary cathode technology enables nearly 3x higher target utilization as compared with conventional systems. The PiVot system's deposition modules feature a pre-sputter unit that enables target conditioning using only one substrate, rather than up to 50 substrates that are needed with other systems to achieve the same results.

[0052] In an aspect of the present invention, designing a proper process kit may be important for Pulsed DC or RF chamber functionality in a PVD process chamber. As an example, Figures 3A-3C illustrate cross-sectional views of a process

kit for a PVD chamber, in accordance with an embodiment of the present invention. Figure 3D illustrates a cross-sectional view of a power delivery source for a PVD chamber, in accordance with an embodiment of the present invention.

[0053] Referring to Figures 3A-3C, a process kit 300 for a PVD chamber includes a first portion (Figure 3A) with an upper adapter 302, a lower adapter 304, a lower shield 306, and a DTESC 308. The process kit 300 for the PVD chamber also includes a second portion (Figure 3B) with a target 310, a dark space shield 312 and an Al spacer 314. The process kit 300 for the PVD chamber also includes a third portion (Figure 3C) with a cover ring 316 and a deposition ring 318.

[0054] Referring to Figure 3D, a power delivery source 350 for a PVD chamber includes an RF match 352 and an RF feed 354. A source distribution plate 356 (e.g., an aluminum source distribution plate) and a ground shield 358 (e.g., aluminum sheet metal) are also included, along with a metal housing 360 and a ring magnet 362. The power delivery source 350 also includes a DC filter box 364 and a DC feed 366. A top plate 368 and a distribution plate 370 are also included, along with an extension block 372, a shaft 374, and a target 376.

[0055] An example of an MOCVD deposition chamber which may be suitable for use as one or more of MOCVD chambers 204, 206, or 208, described above, is illustrated and described with respect to Figure 4. Figure 4 is a schematic cross-sectional view of an MOCVD chamber according to an embodiment of the invention.

[0056] The apparatus 4100 shown in Figure 4 includes a chamber 4102, a gas delivery system 4125, a remote plasma source 4126, and a vacuum system 4112. The chamber 4102 includes a chamber body 4103 that encloses a processing volume 4108. A showerhead assembly 4104 is disposed at one end of the processing volume 4108, and a substrate carrier 4114 is disposed at the other end of the processing volume 4108. A lower dome 4119 is disposed at one end of a lower volume 4110, and the substrate carrier 4114 is disposed at the other end of the lower volume 4110. The substrate carrier 4114 is shown in process position, but may be moved to a lower position where, for example, the substrates 4140 may be loaded or unloaded. An exhaust ring 420 may be disposed around the periphery of the substrate carrier 4114 to help prevent deposition from occurring in the lower volume 4110 and also help direct exhaust gases from the chamber 4102 to exhaust ports 4109. The lower dome 4119 may be made of transparent material, such as high-purity quartz, to allow light to pass through for radiant heating of the substrates 4140. The radiant heating may be

provided by a plurality of inner lamps 4121A and outer lamps 4121B disposed below the lower dome 4119, and reflectors 4166 may be used to help control chamber 4102 exposure to the radiant energy provided by inner and outer lamps 4121A, 4121B. Additional rings of lamps may also be used for finer temperature control of the substrate 4140.

[0057] The substrate carrier 4114 may include one or more recesses 4116 within which one or more substrates 4140 may be disposed during processing. The substrate carrier 4114 may carry six or more substrates 4140. In one embodiment, the substrate carrier 4114 carries eight substrates 4140. It is to be understood that more or less substrates 4140 may be carried on the substrate carrier 4114. Typical substrates 4140 may include sapphire, silicon carbide (SiC), silicon, or gallium nitride (GaN). It is to be understood that other types of substrates 4140, such as glass substrates 4140, may be processed. Substrate 4140 size may range from 50 mm-100 mm in diameter or larger. The substrate carrier 4114 size may range from 200 mm-750 mm. The substrate carrier 4114 may be formed from a variety of materials, including SiC or SiC-coated graphite. It is to be understood that substrates 4140 of other sizes may be processed within the chamber 4102 and according to the processes described herein. The showerhead assembly 4104 may allow for more uniform deposition across a greater number of substrates 4140 and/or larger substrates 4140 than in traditional MOCVD chambers, thereby increasing throughput and reducing processing cost per substrate 4140.

[0058] The substrate carrier 4114 may rotate about an axis during processing. In one embodiment, the substrate carrier 4114 may be rotated at about 2 RPM to about 100 RPM. In another embodiment, the substrate carrier 4114 may be rotated at about 30 RPM. Rotating the substrate carrier 4114 aids in providing uniform heating of the substrates 4140 and uniform exposure of the processing gases to each substrate 4140.

[0059] The plurality of inner and outer lamps 4121A, 4121B may be arranged in concentric circles or zones (not shown), and each lamp zone may be separately powered. In one embodiment, one or more temperature sensors, such as pyrometers (not shown), may be disposed within the showerhead assembly 4104 to measure substrate 4140 and substrate carrier 4114 temperatures, and the temperature data may be sent to a controller (not shown) which can adjust power to separate lamp zones to maintain a predetermined temperature profile across the substrate carrier 4114. In

another embodiment, the power to separate lamp zones may be adjusted to compensate for precursor flow or precursor concentration non-uniformity. For example, if the precursor concentration is lower in a substrate carrier 4114 region near an outer lamp zone, the power to the outer lamp zone may be adjusted to help compensate for the precursor depletion in this region.

[0060] The inner and outer lamps 4121A, 4121B may heat the substrates 4140 to a temperature of about 400 degrees Celsius to about 1200 degrees Celsius. It is to be understood that the invention is not restricted to the use of arrays of inner and outer lamps 4121A, 4121B. Any suitable heating source may be utilized to ensure that the proper temperature is adequately applied to the chamber 4102 and substrates 4140 therein. For example, in another embodiment, the heating source may include resistive heating elements (not shown) which are in thermal contact with the substrate carrier 4114.

[0061] A gas delivery system 4125 may include multiple gas sources, or, depending on the process being run, some of the sources may be liquid sources rather than gases, in which case the gas delivery system may include a liquid injection system or other means (e.g., a bubbler) to vaporize the liquid. The vapor may then be mixed with a carrier gas prior to delivery to the chamber 4102. Different gases, such as precursor gases, carrier gases, purge gases, cleaning/etching gases or others may be supplied from the gas delivery system 4125 to separate supply lines 4131, 4132, and 4133 to the showerhead assembly 4104. The supply lines 4131, 4132, and 4133 may include shut-off valves and mass flow controllers or other types of controllers to monitor and regulate or shut off the flow of gas in each line.

[0062] A conduit 4129 may receive cleaning/etching gases from a remote plasma source 4126. The remote plasma source 4126 may receive gases from the gas delivery system 4125 via supply line 4124, and a valve 4130 may be disposed between the showerhead assembly 4104 and remote plasma source 4126. The valve 4130 may be opened to allow a cleaning and/or etching gas or plasma to flow into the showerhead assembly 4104 via supply line 4133 which may be adapted to function as a conduit for a plasma. In another embodiment, apparatus 4100 may not include remote plasma source 4126 and cleaning/etching gases may be delivered from gas delivery system 4125 for non-plasma cleaning and/or etching using alternate supply line configurations to shower head assembly 4104.

[0063] The remote plasma source 4126 may be a radio frequency or microwave plasma source adapted for chamber 4102 cleaning and/or substrate 4140 etching. Cleaning and/or etching gas may be supplied to the remote plasma source 4126 via supply line 4124 to produce plasma species which may be sent via conduit 4129 and supply line 4133 for dispersion through showerhead assembly 4104 into chamber 4102. Gases for a cleaning application may include fluorine, chlorine or other reactive elements.

[0064] In another embodiment, the gas delivery system 4125 and remote plasma source 4126 may be suitably adapted so that precursor gases may be supplied to the remote plasma source 4126 to produce plasma species which may be sent through showerhead assembly 4104 to deposit CVD layers, such as Group III-V films, for example, on substrates 4140. In general, a plasma, which is a state of matter, is created by the delivery of electrical energy or electromagnetic waves (*e.g.*, radio frequency waves, microwaves) to a process gas (*e.g.*, precursor gases) to cause it to at least partially breakdown to form plasma species, such as ions, electrons and neutral particles (*e.g.*, radicals). In one example, a plasma is created in an internal region of the plasma source 4126 by the delivery electromagnetic energy at frequencies less than about 100 gigahertz (GHz). In another example, the plasma source 4126 is configured to deliver electromagnetic energy at a frequency between about 0.4 kilohertz (kHz) and about 200 megahertz (MHz), such as a frequency of about 162 megahertz (MHz), at a power level less than about 4 kilowatts (kW). It is believed that the formed plasma enhances the formation and activity of the precursor gas(es) so that the activated gases, which reach the surface of the substrate(s) during the deposition process can rapidly react to form a layer that has improved physical and electrical properties.

[0065] A purge gas (e.g., nitrogen) may be delivered into the chamber 4102 from the showerhead assembly 4104 and/or from inlet ports or tubes (not shown) disposed below the substrate carrier 4114 and near the bottom of the chamber body 4103. The purge gas enters the lower volume 4110 of the chamber 4102 and flows upwards past the substrate carrier 4114 and exhaust ring 420 and into multiple exhaust ports 4109 which are disposed around an annular exhaust channel 4105. An exhaust conduit 4106 connects the annular exhaust channel 4105 to a vacuum system 4112 which includes a vacuum pump (not shown). The chamber 4102 pressure may

be controlled using a valve system 4107 which controls the rate at which the exhaust gases are drawn from the annular exhaust channel 4105.

[0066] An example of a HVPE deposition chamber which may be suitable for use as the HVPE chamber 204 of alternative embodiments of chamber 204 (or of alternative embodiments for other chambers), described above, is illustrated and described with respect to Figure 5. Figure 5 is a schematic cross-sectional view of a HVPE chamber 500 suitable for the fabrication of group III-nitride materials, in accordance with an embodiment of the present invention.

[0067] The apparatus 500 includes a chamber 502 enclosed by a lid 504. Processing gas from a first gas source 510 is delivered to the chamber 502 through a gas distribution showerhead 506. In one embodiment, the gas source 510 includes a nitrogen containing compound. In another embodiment, the gas source 510 includes ammonia. In one embodiment, an inert gas such as helium or diatomic nitrogen is introduced as well either through the gas distribution showerhead 506 or through the walls 508 of the chamber 502. An energy source 512 may be disposed between the gas source 510 and the gas distribution showerhead 506. In one embodiment, the energy source 512 includes a heater. The energy source 512 may break up the gas from the gas source 510, such as ammonia, so that the nitrogen from the nitrogen containing gas is more reactive.

[0068] To react with the gas from the first source 510, precursor material may be delivered from one or more second sources 518. The precursor may be delivered to the chamber 502 by flowing a reactive gas over and/or through the precursor in the precursor source 518. In one embodiment, the reactive gas includes a chlorine containing gas such as diatomic chlorine. The chlorine containing gas may react with the precursor source to form a chloride. In order to increase the effectiveness of the chlorine containing gas to react with the precursor, the chlorine containing gas may snake through the boat area in the chamber 532 and be heated with the resistive heater 520. By increasing the residence time that the chlorine containing gas is snaked through the chamber 532, the temperature of the chlorine containing gas may be controlled. By increasing the temperature of the chlorine containing gas, the chlorine may react with the precursor faster. In other words, the temperature is a catalyst to the reaction between the chlorine and the precursor.

[0069] In order to increase the reactivity of the precursor, the precursor may be heated by a resistive heater 520 within the second chamber 532 in a boat. The

chloride reaction product may then be delivered to the chamber 502. The reactive chloride product first enters a tube 522 where it evenly distributes within the tube 522. The tube 522 is connected to another tube 524. The chloride reaction product enters the second tube 524 after it has been evenly distributed within the first tube 522. The chloride reaction product then enters into the chamber 502 where it mixes with the nitrogen containing gas to form a nitride layer on a substrate 516 that is disposed on a susceptor 514. In one embodiment, the susceptor 514 includes silicon carbide. The nitride layer may include n-type gallium nitride for example. The other reaction products, such as nitrogen and chlorine, are exhausted through an exhaust 526.

[0070] LEDs and related devices may be fabricated from layers of, e.g., group III-V films, especially group III-nitride films. Some embodiments of the present invention relate to forming gallium nitride (GaN) layers in a dedicated chamber of a fabrication tool, such as in a dedicated MOCVD chamber. In some embodiments of the present invention, GaN is a binary GaN film, but in other embodiments, GaN is a ternary film (e.g., InGaN, AlGaN) or is a quaternary film (e.g., InAlGaN). In at least some embodiments, the group III-nitride material layers are formed epitaxially. They may be formed directly on a substrate or on a buffers layer disposed on a substrate. Other contemplated embodiments include p-type doped gallium nitride layers deposited directly on PVD-formed buffer layers, e.g., PVD-formed aluminum nitride.

[0071] It is to be understood that embodiments of the present invention are not limited to formation of layers on the select substrates described above. Other embodiments may include the use of any suitable non-patterned or patterned single crystalline substrate upon which a high quality aluminum nitride layer may be sputter-deposited, e.g., in a non-reactive PVD approach. The substrate may be one such as, but not limited to, a sapphire (Al_2O_3) substrate, a silicon (Si) substrate, a silicon carbide (SiC) substrate, a silicon on diamond (SOD) substrate, a quartz (SiO_2) substrate, a glass substrate, a zinc oxide (ZnO) substrate, a magnesium oxide (MgO) substrate, and a lithium aluminum oxide ($LiAlO_2$) substrate. Any well know method, such as masking and etching may be utilized to form features, such as posts, from a planar substrate to create a patterned substrate. In a specific embodiment, however, a patterned sapphire substrate (PSS) is used with a (0001) orientation. Patterned sapphire substrates may be preferred for use in the manufacturing of certain types of LEDs because they increase the light extraction efficiency which is extremely useful in the fabrication of a new generation of solid state lighting devices. Substrate

selection criteria may include lattice matching to mitigate defect formation and coefficient of thermal expansion (CTE) matching to mitigate thermal stresses.

[0072] As described above, the group III-nitride films can be doped. The group III-nitride films can be p-typed doped using any p-type dopant such as but not limited Mg, Be, Ca, Sr, or any Group I or Group II element have two valence electrons. The group III-nitride films can be p-type doped to a conductivity level of between $1X10^{16}$ to $1X10^{20}$ atoms/cm^3. The group III-nitride films can be n-typed doped using any n-type dopant such as but not limited silicon or oxygen, or any suitable Group IV or Group VI element. The group III-nitride films can be n-type doped to a conductivity level of between $1X10^{16}$ to $1X10^{20}$ atoms/cm^3.

[0073] It is to be understood that the above processes may be performed in a dedicated chamber within a cluster tool, or other tool with more than one chamber, e.g. an in-line tool arranged to have a dedicated chamber for fabricating layers of an LED. It is also to be understood that embodiments of the present invention need not be limited to the fabrication of LEDs. For example, in another embodiment, devices other than LED devices may be fabricated by approaches described herein, such as but not limited to field-effect transistor (FET) devices, or power devices. In such embodiments, there may not be a need for a p-type material on top of a structure of layers. Instead, an n-type or un-doped material may be used in place of the p-type layer. It is also to be understood that multiple operations, such as various combinations of depositing and/or thermal annealing, may be performed in a single process chamber.

[0074] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to the present invention. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[0075] Figure 6 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 600 within which a set of instructions, for causing the machine to perform any one or more of the methodologies discussed herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein. In one embodiment, computer system 600 is suitable for use a computing device for an apparatus described in association with Figures 1, 2A, 3A, 3B, 4 or 5, described above.

[0076] The exemplary computer system 600 includes a processor 602, a main memory 604 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 606 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 618 (e.g., a data storage device), which communicate with each other via a bus 630.

[0077] Processor 602 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 602 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 602 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 602 is configured to execute the processing logic 626 for performing the operations discussed herein.

[0078] The computer system 600 may further include a network interface device 608. The computer system 600 also may include a video display unit 610 (e.g., a liquid crystal display (LCD) or a cathode ray tube (CRT)), an alphanumeric input device 612 (e.g., a keyboard), a cursor control device 614 (e.g., a mouse), and a signal generation device 616 (e.g., a speaker).

[0079] The secondary memory 618 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 631 on which is stored one or more sets of instructions (e.g., software 622) embodying any one or more of the methodologies or functions described herein. The software 622 may also reside, completely or at least partially, within the main memory 604 and/or within the processor 602 during execution thereof by the computer system 600, the main memory 604 and the processor 602 also constituting machine-readable storage media. The software 622 may further be transmitted or received over a network 620 via the network interface device 608.

[0080] While the machine-accessible storage medium 631 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0081] In accordance with an embodiment of the present invention, a non-transitory machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of forming a PVD AlN buffer for GaN-based optoelectronic and electronic devices in an oxygen controlled manner.

[0082] Thus, oxygen controlled PVD AlN buffer for GaN-based optoelectronic and electronic devices has been disclosed.

CLAIMS

What is claimed is:

1. A method of forming an aluminum nitride (AlN) buffer layer for GaN-based optoelectronic or electronic devices, the method comprising:

reactive sputtering an AlN layer above a substrate, the reactive sputtering comprising reacting an aluminum-containing target housed in a physical vapor deposition (PVD) chamber with a nitrogen-containing gas or a plasma based on a nitrogen-containing gas; and

incorporating oxygen into the AlN layer.

2. The method of claim 1, wherein incorporating the oxygen is performed by flowing of an oxygen-containing gas selected from the group consisting of O_2, H_2O, CO, CO_2, NO, NO_2, O_3, and combinations thereof, into the PVD chamber.

3. The method of claim 1, wherein incorporating the oxygen is performed by flowing of an oxygen-containing gas prior to reacting the aluminum-containing target with the nitrogen-containing gas or the plasma based on a nitrogen-containing gas.

4. The method of claim 1, wherein incorporating the oxygen is performed by flowing of an oxygen-containing gas while reacting the aluminum-containing target with the nitrogen-containing gas or the plasma based on a nitrogen-containing gas.

5. The method of claim 1, wherein incorporating the oxygen is performed by flowing of an oxygen-containing gas subsequent to reacting the aluminum-containing target with the nitrogen-containing gas or the plasma based on a nitrogen-containing gas.

6. The method of claim 1, where incorporating oxygen into the AlN layer comprises incorporating a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3} into the AlN layer.

7. A material stack for GaN-based optoelectronic or electronic devices, the material stack comprising:

a substrate; and

an aluminum nitride (AlN) buffer layer disposed above the substrate, the AlN layer comprising a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

8. The material stack of claim 7, wherein a portion of the oxygen is included at an AlN/substrate interface.

9. The material stack of claim 7, wherein a portion of the oxygen is included at an outermost surface of the AlN buffer layer.

10. The material stack of claim 7, further comprising

a high quality GaN layer disposed on the AlN buffer layer, the high quality GaN layer having XRD (002) FWHM < 100 arcsec and XRD (102) FWHM < 150 arcsec.

11. The material stack of claim 7, wherein the substrate is selected from the group consisting of sapphire, Si, SiC, Si on diamond, ZnO, LiAlO2, MgO, GaAs, Copper and W.

12. A light-emitting diode (LED) device, comprising:

a substrate; and

an aluminum nitride (AlN) buffer layer disposed above the substrate, the AlN layer comprising a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

13. The LED device of claim 12, wherein a portion of the oxygen is included at an AlN/substrate interface.

14. The LED device of claim 12, wherein a portion of the oxygen is included at an outermost surface of the AlN buffer layer.

15. The LED device of claim 12, further comprising

a high quality GaN layer disposed on the AlN buffer layer, the high quality GaN layer having XRD (002) FWHM < 100 arcsec and XRD (102) FWHM < 150 arcsec.

16. A GaN-based electronic device, comprising:

a substrate; and

an aluminum nitride (AlN) buffer layer disposed above the substrate, the AlN layer comprising a concentration of oxygen approximately in the range of 1E18 to 1E23 cm^{-3}.

17. The GaN-based electronic device of claim 16, wherein the device is one selected from the group consisting of a field effect transistor (FET) and a power device.

18. The GaN-based electronic device of claim 16, wherein a portion of the oxygen is included at an AlN/substrate interface.

19. The GaN-based electronic device of claim 16, wherein a portion of the oxygen is included at an outermost surface of the AlN buffer layer.

20. The GaN-based electronic device of claim 16, further comprising:

a high quality GaN layer disposed on the AlN buffer layer, the high quality GaN layer having XRD (002) FWHM < 100 arcsec and XRD (102) FWHM < 150 arcsec.

21. A chamber for forming an aluminum nitride (AlN) buffer layer for GaN-based optoelectronic or electronic devices, the chamber comprising:

a pumping system and chamber cooling design that enables high base vacuum of 1E-7 torr or less and low rate-of-rise at high temperature;

a full face erosion magnetron cathode configured to enable consistent target erosion and uniform deposition of AlN film across carriers, within and between wafers; and

a process kit and gas flow design configured to enable a uniform distribution of process gases, including O-containing gas, within the chamber for uniform AlN composition.

22. The chamber of claim 21, further comprising:
a high temperature biasable electro-static chuck configured to enable fast and uniform heating up of wafers.

23. The chamber of claim 21, further comprising:
an Al target doped with oxygen.

24. The chamber of claim 21, wherein the chamber vacuum rate-of-rise is 2,500 ntorr/min or lower.

25. The chamber of claim 21, wherein the high temperature is approximately or greater than 350 degrees Celsius.

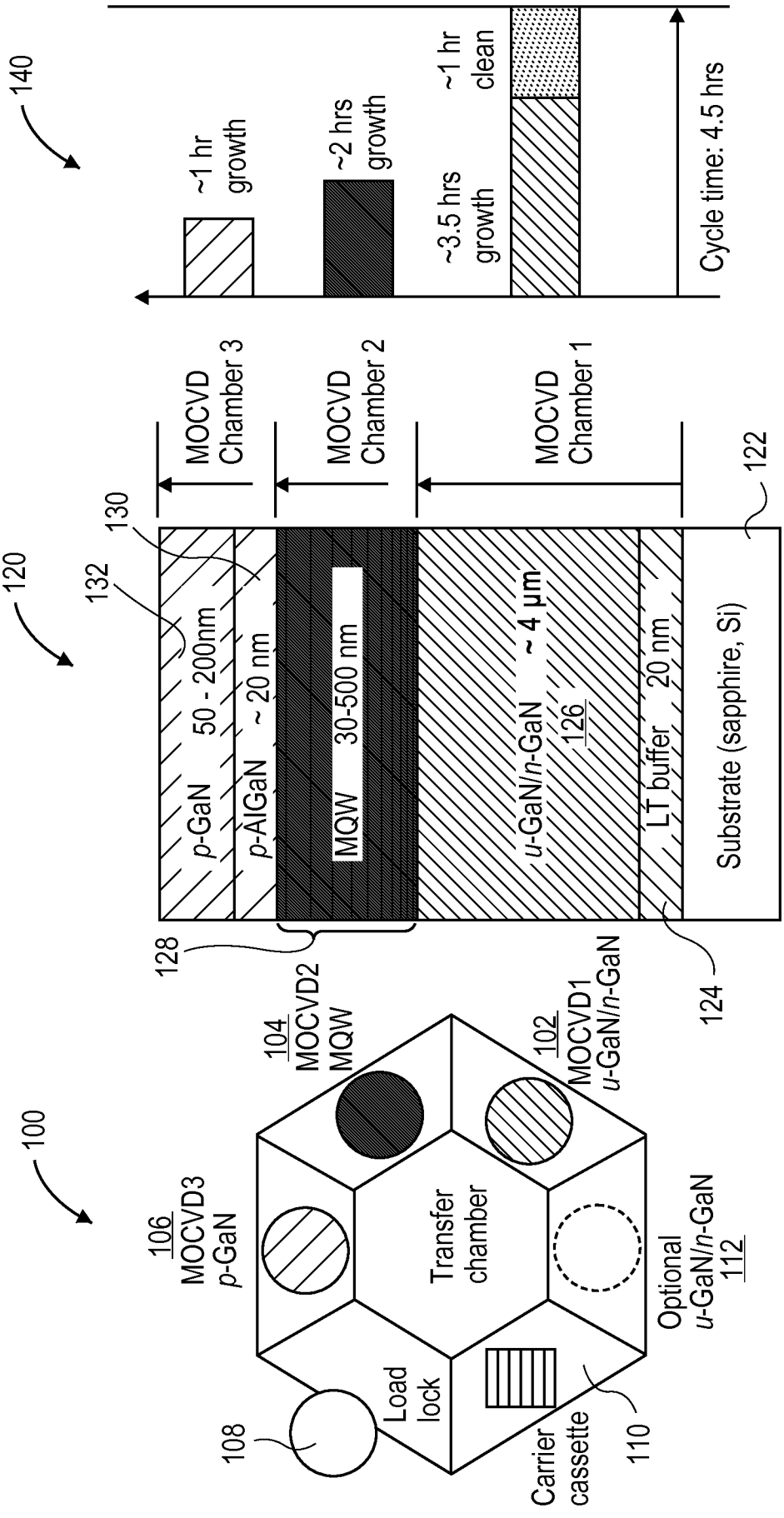
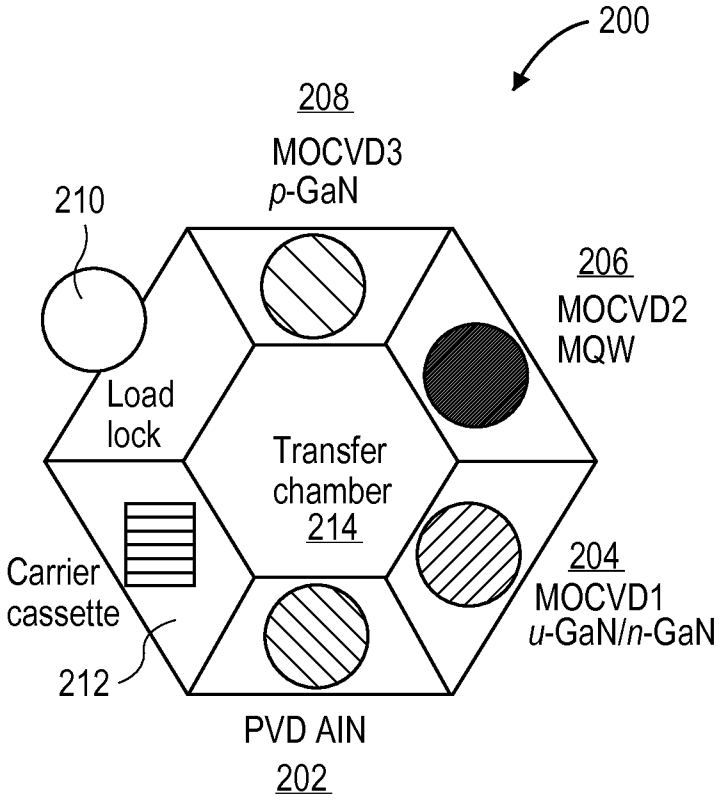

140
~1 hr growth
~2 hrs growth
~3.5 hrs growth
~1 hr clean
Cycle time: 4.5 hrs
120
130
132
MOCVD Chamber 3
MOCVD Chamber 2
MOCVD Chamber 1
122
p-GaN 50 - 200nm
p-AlGaN ~ 20 nm
MQW 30-500 nm
u-GaN/n-GaN ~ 4 µm
126
LT buffer 20 nm
Substrate (sapphire, Si)
128
124
100
104 MOCVD2 MQW
102 MOCVD1 u-GaN/n-GaN
106 MOCVD3 p-GaN
Transfer chamber
Optional u-GaN/n-GaN 112
Load lock
108
Carrier cassette
110

FIG. 1


200
208
MOCVD3
p-GaN
210
206
MOCVD2
MQW
Load
lock
Transfer
chamber
214
Carrier
cassette
212
204
MOCVD1
u-GaN/n-GaN
PVD AIN
202

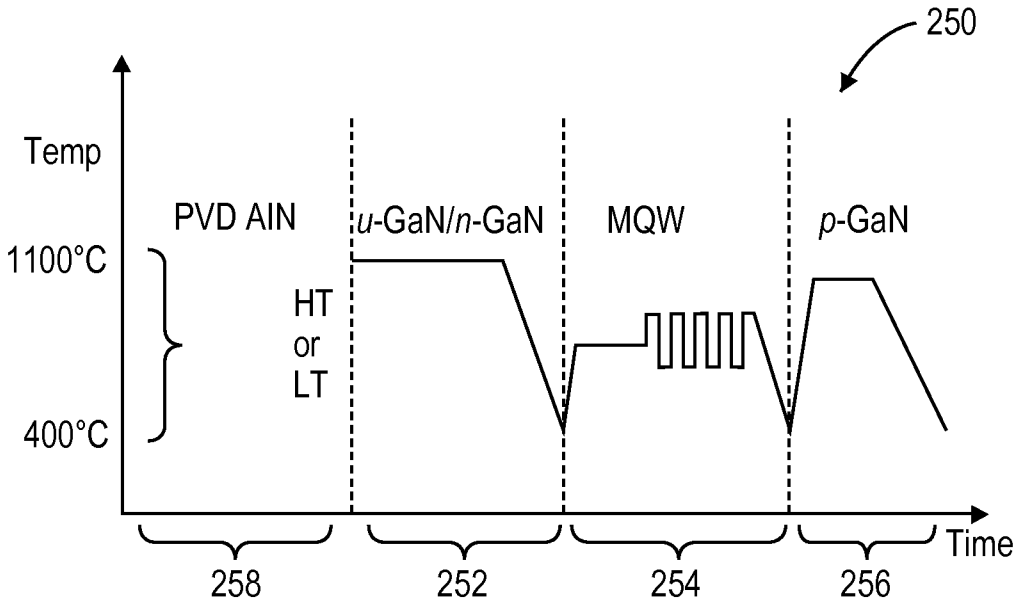

250
Temp
PVD AIN
u-GaN/n-GaN
MQW
p-GaN
1100°C
HT
or
LT
400°C
Time
258
252
254
256

FIG. 2A

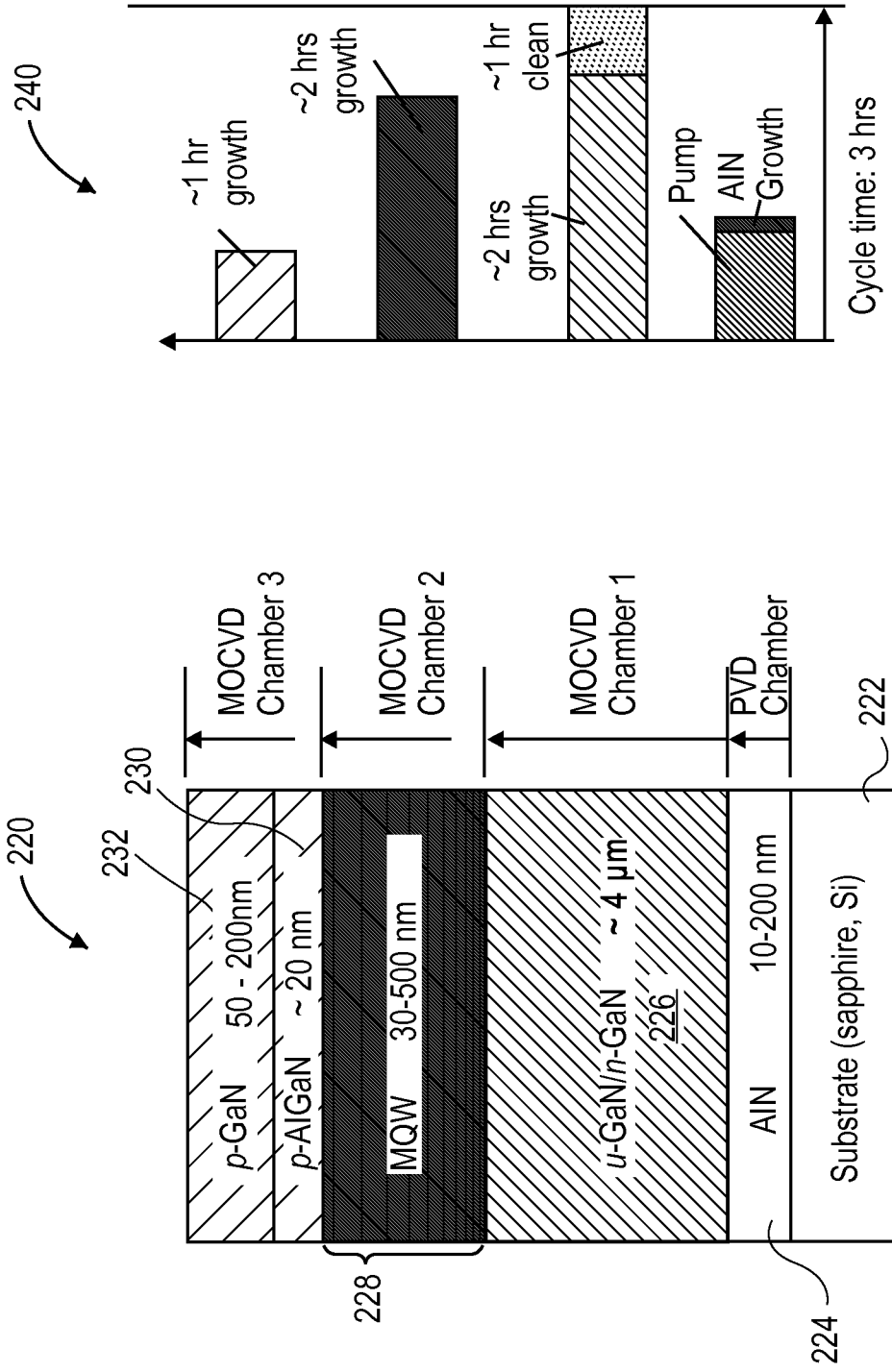

240
~1 hr growth
~2 hrs growth
~2 hrs growth
~1 hr clean
Pump
AlN Growth
Cycle time: 3 hrs
220
232
230
p-GaN 50 - 200nm
p-AlGaN ~ 20 nm
MQW 30-500 nm
u-GaN/n-GaN ~ 4 µm
226
AlN 10-200 nm
Substrate (sapphire, Si)
MOCVD Chamber 3
MOCVD Chamber 2
MOCVD Chamber 1
PVD Chamber
222
228
224

FIG. 2B

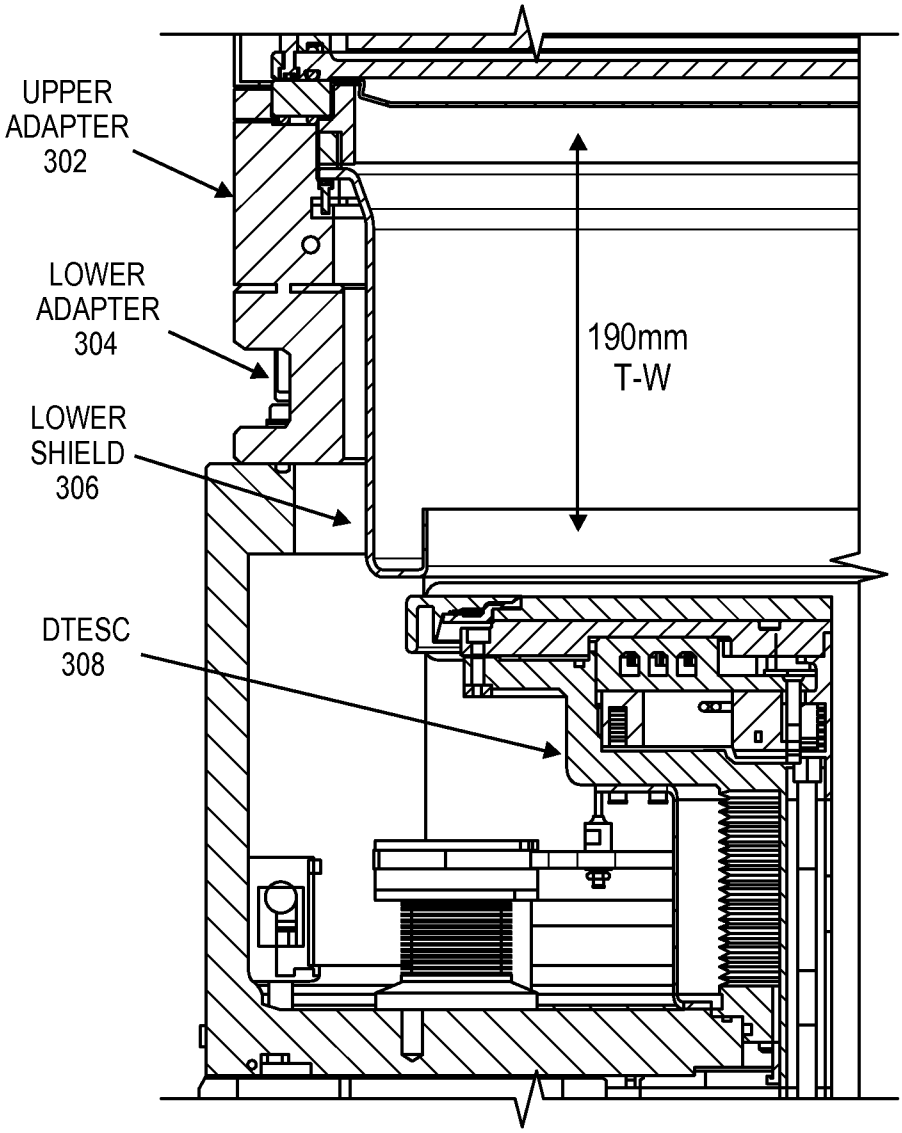

UPPER
ADAPTER
302
LOWER
ADAPTER
304
LOWER
SHIELD
306
DTESC
308
190mm
T-W

FIG. 3A

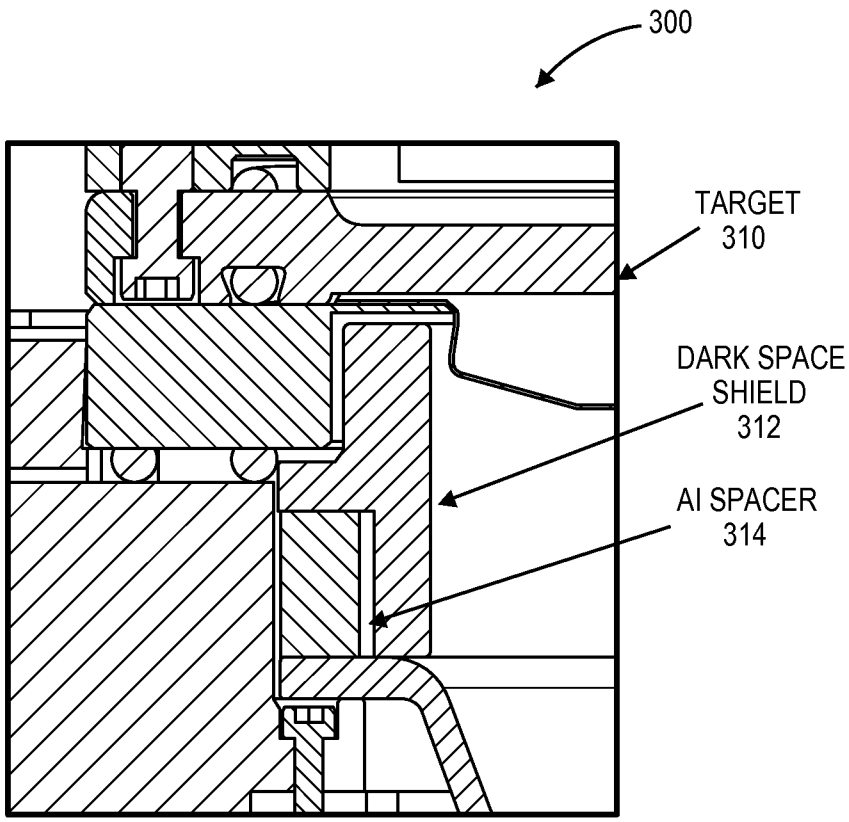

300
TARGET
310
DARK SPACE
SHIELD
312
Al SPACER
314

FIG. 3B

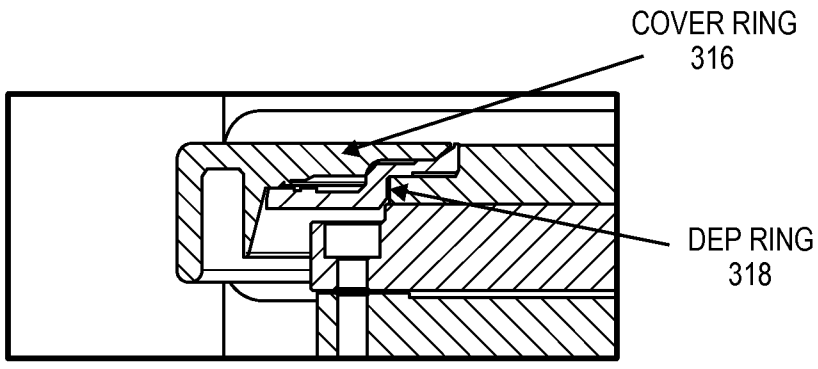

COVER RING
316
DEP RING
318

FIG. 3C

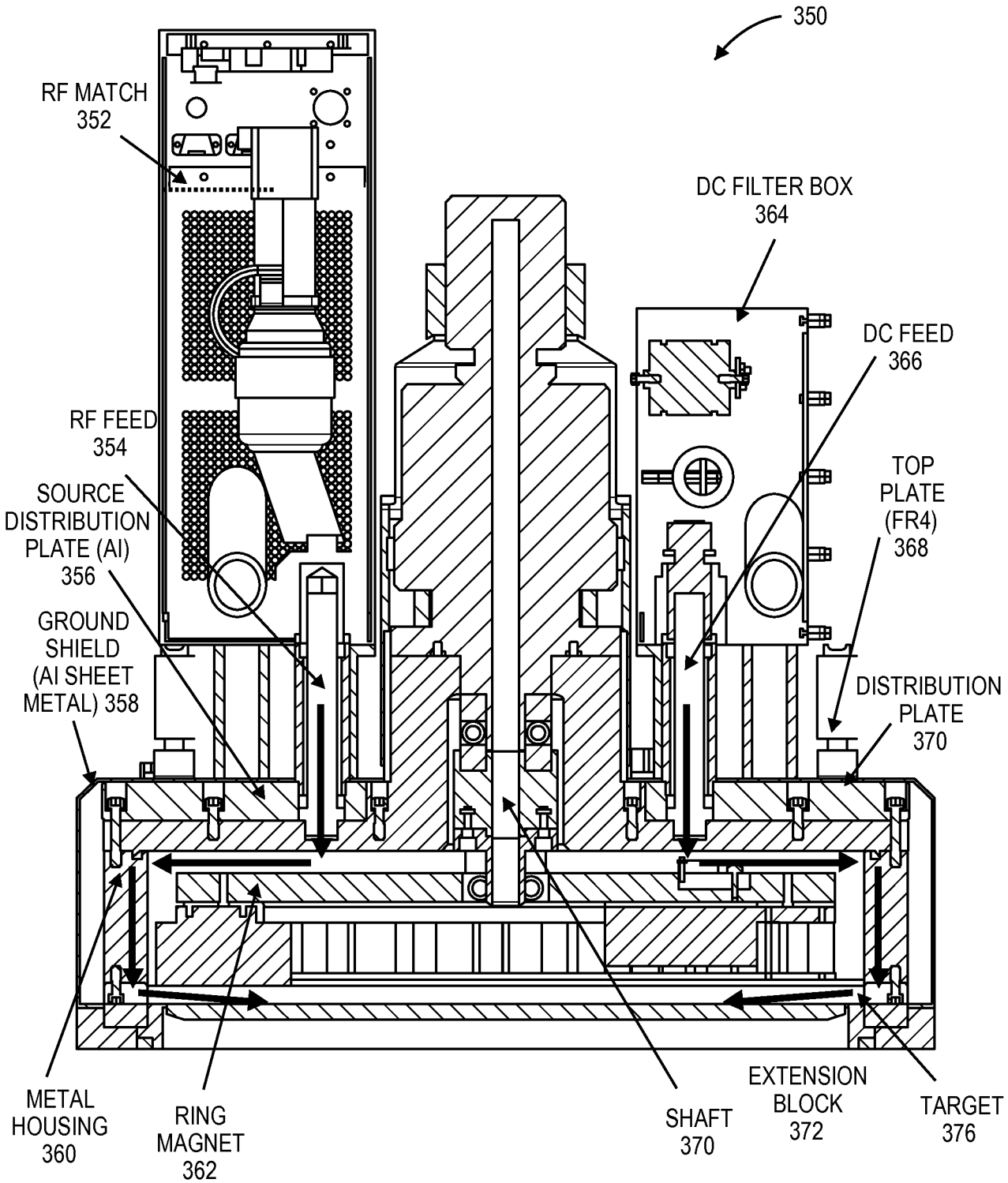

350
RF MATCH
352
DC FILTER BOX
364
DC FEED
366
RF FEED
354
SOURCE
DISTRIBUTION
PLATE (Al)
356
TOP
PLATE
(FR4)
368
GROUND
SHIELD
(Al SHEET
METAL) 358
DISTRIBUTION
PLATE
370
METAL
HOUSING
360
RING
MAGNET
362
SHAFT
370
EXTENSION
BLOCK
372
TARGET
376

FIG. 3D

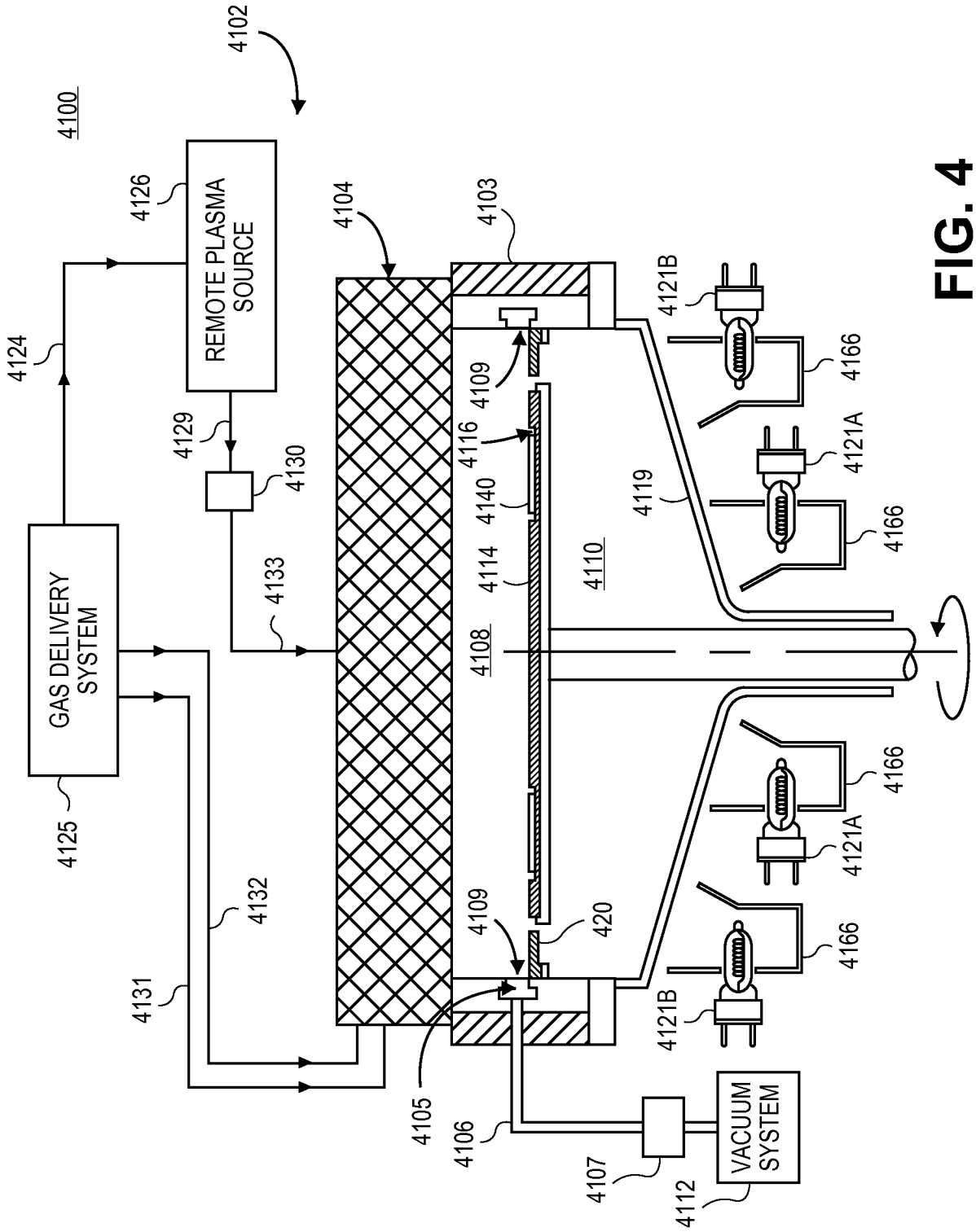

4100
4102
4103
4104
4105
4106
4107
4108
4109
4110
4112
4114
4116
4119
4121A
4121B
4124
4125
4126
4129
4130
4131
4132
4133
4140
4166
420
REMOTE PLASMA SOURCE
GAS DELIVERY SYSTEM
VACUUM SYSTEM

FIG. 4

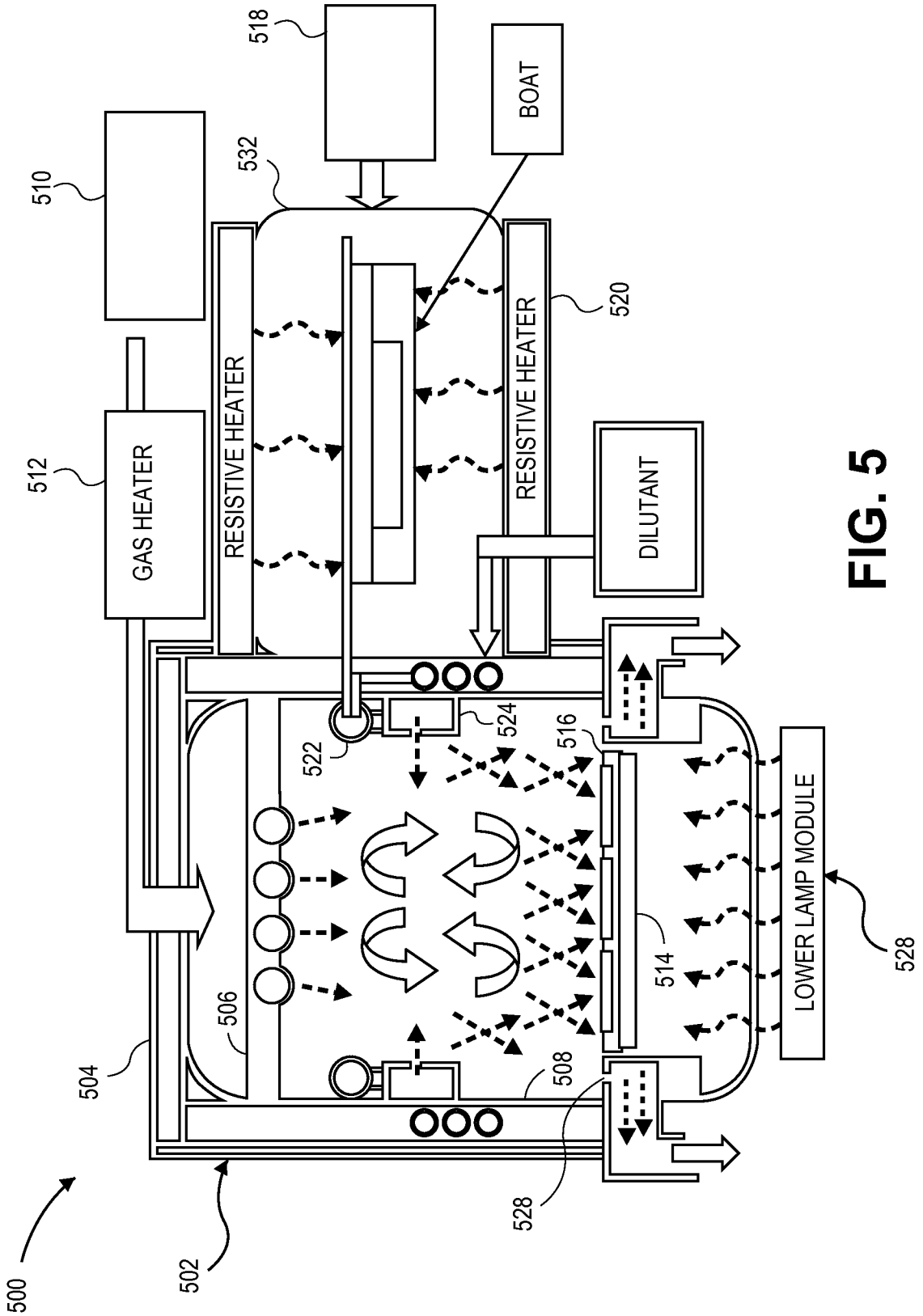

518
BOAT
532
510
520
RESISTIVE HEATER
RESISTIVE HEATER
512
GAS HEATER
DILUTANT
524
516
522
LOWER LAMP MODULE
514
528
506
504
508
528
502
500

FIG. 5

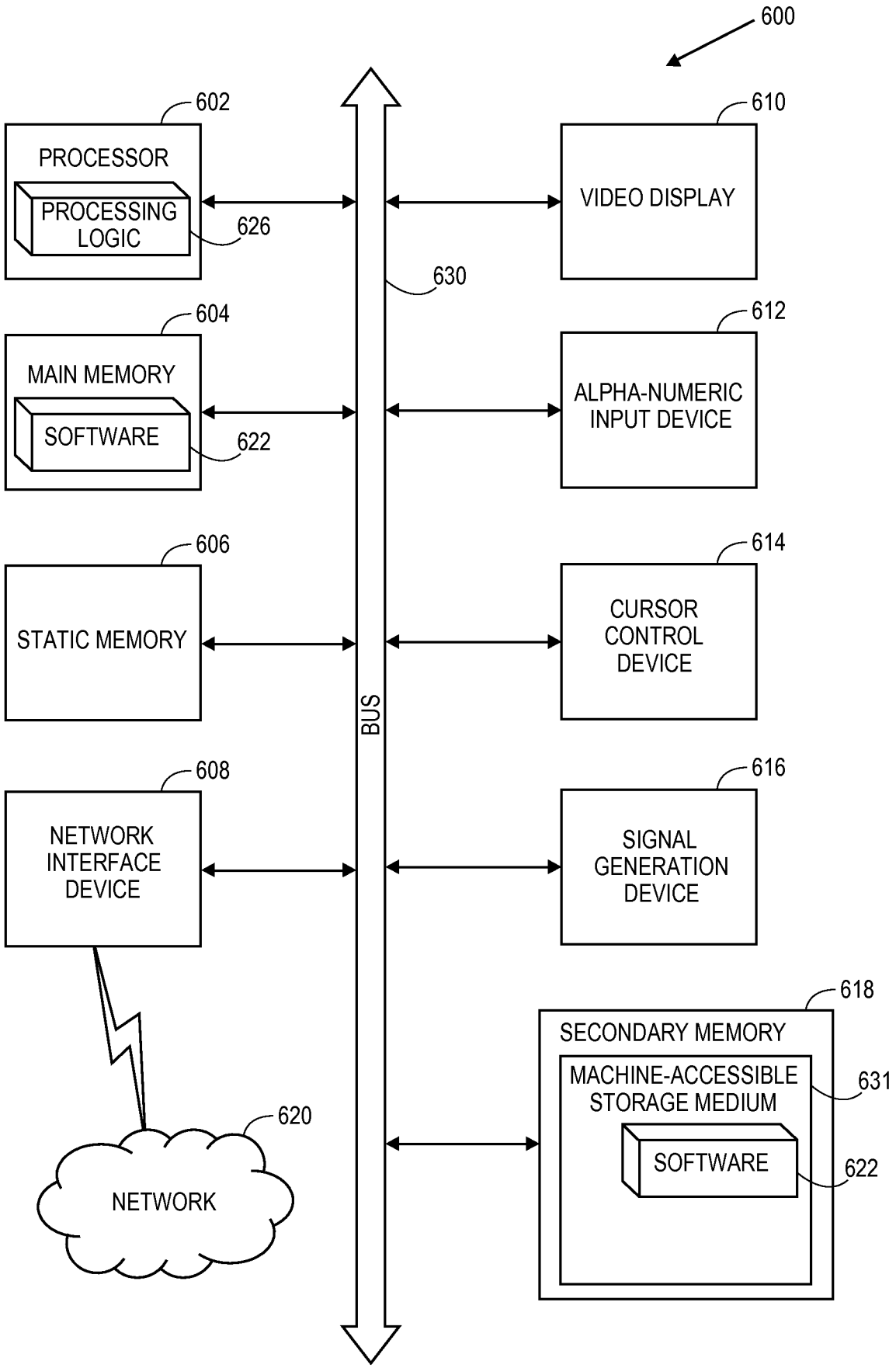

600
602
PROCESSOR
PROCESSING LOGIC
626
604
MAIN MEMORY
SOFTWARE
622
606
STATIC MEMORY
608
NETWORK INTERFACE DEVICE
620
NETWORK
630
BUS
610
VIDEO DISPLAY
612
ALPHA-NUMERIC INPUT DEVICE
614
CURSOR CONTROL DEVICE
616
SIGNAL GENERATION DEVICE
618
SECONDARY MEMORY
MACHINE-ACCESSIBLE STORAGE MEDIUM
631
SOFTWARE
622

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/053994

A. CLASSIFICATION OF SUBJECT MATTER

C23C 14/34(2006.01)i, C23C 14/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C23C 14/34; H01L 21/203; H01L 21/205; H01L 33/30; H01L 33/00; H01L 21/66; C30B 29/38; H01L 41/083; C23C 14/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: PVD, LED, gallium nitride, aluminum nitride, buffer, oxygen, and sputtering

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0219445 A1 (YOKOYAMA et al.) 02 September 2010 See abstract, paragraphs [0043],[0052]-[0068],[0110]-[0113],[0126],[0183] and claim 1.	1-25
A	JP 2010-518615 A (NANOGAN LTD.) 27 May 2010 See paragraphs [0048]-[0055] and figure 3.	1-25
A	US 7642693 B2 (AKIYAMA et al.) 05 January 2010 See column 3, line 58 - column 6, line 56 and claims 1-4.	1-25
A	US 7968361 B2 (OSAWA et al.) 28 June 2011 See abstract and column 2, line 45 - column 4, line 54.	1-25
A	JP 2008-135463 A (SHOWA DENKO K.K.) 12 June 2008 See abstract and paragraphs [0017]-[0024].	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2013 (25.11.2013)	**26 November 2013 (26.11.2013)**

Name and mailing address of the ISA/KR
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/053994

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		KR 10-2010-0049123 A	11/05/2010
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JP 2010-518615 A	27/05/2010	EP 2118921 A1	18/11/2009
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		KR 10-2009-0107403 A	13/10/2009
		TW 200901284 A	01/01/2009
		TW I395260 B	01/05/2013
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		KR 10-2008-0109835 A	17/12/2008
		TW 200805711 A	16/01/2008
		TW I377698B	21/11/2012
		US 2009-0114933 A1	07/05/2009
		WO 2007-119619 A1	25/10/2007
JP 2008-135463 A	12/06/2008	None	