A system and method comprising a master electrode arranged on substrate, said master electrode comprising a pattern layer, least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; said substrate comprising a top surface in contact with or arranged adjacent said first surface and having conducting material and/or structures of a conducting material arranged thereon, said substrate conducting material being electrically connected to at least one current supply contact; whereby a plurality of electrochemical cells are formed delimited by said cavities, said substrate conducting material and said electrode conducting material, said cells comprising an electrolyte; herein an electrode resistance between said electrode conducting material and said electrode current supply contact and a substrate resistance between said substrate conducting material and said substrate current supply contact are adapted for providing a predetermined current density in each electrochemical cell.
MASTER ELECTRODE AND METHOD OF FORMING IT

[0001] The present invention relates to a master electrode and a method of forming the master electrode. The master electrode is useable in an etching or plating method as described in a copending Swedish patent application No. 0502539-2 filed Nov. 28, 2005 and entitled “METHOD OF FORMING A MULTILAYER STRUCTURE”. The contents of this specification are incorporated herein by reference. The master electrode is similar to the master electrode described in a copending Swedish Patent Application No. 0502539-2 entitled “ELECTRODE AND METHOD OF FORMING THE ELECTRODE”. The contents of this specification are incorporated herein by reference. The master electrode is suitable for enabling production of applications involving micro and nano structures in single or multiple layers. The master electrode is useful for fabrication of PWB (printed wiring boards), PCB (printed circuit boards), MEMS (micro electro mechanical systems), IC (integrated circuit) interconnects, above IC interconnects, sensors, flat panel displays, magnetic and optical storage devices, solar cells and other electronic devices. Different types of structures in conductive polymers, structures in semiconductors, structures in metals, and others are possible to produce using this master electrode.

BACKGROUND ART

[0002] WO 02/103085 relates to an electrochemical pattern replication method, ECPR, and a construction of a conductive master electrode for production of applications involving micro and nano structures. An etching or plating pattern, which is defined by a master electrode, is replicated on an electrically conductive material, a substrate. The master electrode is put in close contact with the substrate and the etching/plating pattern is directly transferred onto the substrate by using a contact etching/plating process. The contact etching/plating process is performed in local electrochemical cells, that are formed in closed or open cavities between the master electrode and the substrate.

[0003] The master electrode is used for cooperation with a substrate, onto which a structure is to be built. The master electrode forms at least one, normally a plurality of electrochemical cells in which etching or plating takes place. The master electrode may be made of a durable material, since the master electrode should be used for a plurality of processes of etching or plating.

[0004] A problem is that the etching rate or plating rate may be higher in the electrochemical cells located closer to the contact area of the seed layer, such as in the perimeter, than in other areas.

[0005] This problem is encountered when etching and/or plating is performed on a substrate provided with a seed layer which conducts the current at the substrate. If the seed layer is so thin that a substantial potential difference occurs across the seed layer, the current density in the electrochemical cells will vary over the surface of the substrate resulting in varying etching depths or plating heights. This problem is exacerbated by the fact that the current density is exponentially dependent on the cell voltage.

SUMMARY OF THE INVENTION

[0006] An object of the present invention is to provide a master electrode in which the above-mentioned problem is at least partly eliminated or alleviated.

[0007] According to an aspect of the invention, there is provided a system comprising a master electrode arranged on a substrate, said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; said substrate comprising a top surface in contact with or arranged adjacent said first surface and having conducting material and/or structures of a conducting material arranged thereon, said substrate conducting material being electrically connected to at least one current supply contact; whereby a plurality of electrochemical cells are formed delimited by said cavities, said substrate conducting material and said electrode conducting material, said cells comprising an electrolyte; wherein an electrode resistance between said electrode conducting material and said electrode current supply contact and a substrate resistance between said substrate conducting material and said substrate current supply contact are adapted for providing a predetermined current density in each electrochemical cell.

[0008] In an embodiment, the electrode resistance and said substrate resistance each may be formed by at least one electrically conducting material, having a predetermined specific conductivity defined as the thickness of the material divided by the resistivity of the material. The specific conductivity may be arranged varying over the surface of the master electrode. The specific conductivity may be arranged varying by changing the thickness of the material. The specific conductivity may also be arranged varying by changing the resistivity of the material. The material may be a doped semiconductor material having a doping which is arranged varying for providing said resistivity.

[0009] In an embodiment, the electrode conducting material may comprise a disc having substantially the same extent as said first surface. The disc may be made of a conducting and/or semi-conducting material. The electrode conducting material may comprise cavity conducting material arranged in the bottom of each cavity. The cavity conducting material may be a material arranged in the bottom of said cavity and being of an inert material. The cavity conducting material may be a further material which is deposited in said cavity and at least partly consumed during a plating process. The cavity conducting material may be in electric contact with said disc.

[0010] In an embodiment, the disc may have a substantially constant thickness. The disc may comprise a plurality of disc members having different specific conductivities, said disc members being arranged on top of each other.

[0011] In an embodiment, the electrode supply contact may be arranged in the middle of said disc. The electrode supply contact may comprise several discrete contacts. The discrete contacts may comprise at least one ring contact or ring segment contact arranged at a radius from a centrum of the disc. Each discrete contact may be provided with a specific potential during a plating or etching process.

[0012] In an embodiment, the disc may be substantially circular. The thicknesses of at least one of said disc members may change with the distance to the center of the disc.

[0013] In an embodiment, the substrate resistance may be at least partly provided by a seed layer arranged on at least a part of the substrate top surface. The substrate electrode contact may be arranged at least a part of a perimeter of said substrate seed layer. The substrate electrode contact may be arranged...
along a perimeter of said substrate seed layer. The substrate electrode contact may comprise several discrete contacts. Each discrete contact may be supplied with a specific potential during a plating or etching process. The master electrode may comprise at least one contact area for contact with said seed layer for providing current to said seed layer.

[0014] In an embodiment, the pattern layer may comprise at least one area of conducting material arranged in said first surface in portions between said cavities for being in contact with said substrate conducting material during a plating or etching process for increasing the specific conductivity of said substrate conducting material over said areas.

[0015] In an embodiment, the adaptation may be performed if the potential difference over the surface of said electrode conducting material and/or over the surface of said substrate conducting material is significant, so that the current density difference in said electrochemical cells between said surfaces is more than 1%, such as more than 2%. The adaptation may result in that the specific conductivity of the electrode conducting material in average is between 0.1 to 100 times, such as between 0.5 to 20 times, for example 1 to 10 times, such as about 1 to 7 times the specific conductivity of said substrate conducting material. Each cavity may be provided with a material having a thickness which is specific for each cavity.

[0016] In another aspect, there is provided a master electrode intended to be arranged on a substrate, said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; whereby a plurality of electrochemical cells are intended to be formed delimited by said cavities, said electrode conducting material and a substrate; wherein an electrode resistance between said electrode conducting material and said electrode current supply contact is adapted in relation to an intended substrate conducting material for providing a predetermined current in each electrochemical cell to be formed.

[0017] In an embodiment, the electrode resistance and said substrate resistance may each be formed by at least one electrically conducting material, having a predetermined specific conductivity defined as the thickness of the material divided by the resistivity of the material. The specific conductivity may be arranged varying over the surface of the master electrode. The specific conductivity may be arranged varying by changing the thickness of the material. The specific conductivity may be arranged varying by changing the resistivity of the material. The material may be a doped semiconductor material having a doping which is arranged varying for providing said varying resistivity.

[0018] In an embodiment, the electrode conducting material may comprise a disc having substantially the same extent as said first surface. The disc may be arranged in a conducting and/or semi-conducting material. The electrode conducting material may comprise cavity conducting material arranged in the bottom of each cavity. The cavity conducting material may be a material arranged in the bottom of said cavity and being of an inert material. The cavity conducting material may be a further material which is predeposited in said cavity and at least partly consumed during a plating process. The cavity conducting material may be in electric contact with said disc.

[0019] In an embodiment, the disc has substantially constant thickness. The disc may comprise a plurality of disc members having different specific conductivities, said disc members being arranged on top of each other. The electrode supply contact may be arranged in the center of said disc. The electrode supply contact may comprise several discrete contacts. The discrete contacts may comprise at least one ring contact or ring segment contact arranged at a radius from a center of the disc. The discrete contact may be provided with a specific potential during a plating or etching process.

[0020] In an embodiment, the disc may be substantially circular. The thicknesses of at least one of said disc members may change with the distance to the center of the disc. Each cavity may be provided with a material having a thickness which is specific for each cavity.

[0021] In a further aspect, there is provided a method of predeposition of material in cavities of a master electrode having a pattern layer comprising an insulating material, in which said cavities are formed, and a conducting electrode layer forming a bottom of said cavities, said conducting electrode layer having contact portions for external connection to an electric power source, the method comprising: arranging a contact member at a support; arranging said master electrode on said contact member for obtaining electrical contact between the contact member and said conducting electrode layer in at least two contact portions; arranging an electroplating anode of a material to be deposited in said cavities on said master electrode, whereby electrochemical cells are formed delimited by said cavities, said substrate conducting electrode layer and said electroplating anode, whereby said cells comprise an electrolyte; connecting an electric power source to said contact member and said electroplating anode for passing a current through said electrochemical cells for transferring material from said anode to said conducting electrode layer, which is cathode, in order to deposit said material in the cavities on top of said conducting electrode layer.

[0022] In a still further aspect, there is provided a method of performing etching or plating of a substrate by means of a master electrode, said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; the method comprising: arranging said master electrode on a support; supplying an electrolyte to the cavities; arranging a substrate on said master electrode, said substrate comprising a top surface having conducting material and/or structures of a conducting material arranged thereon, said substrate conducting material being electrically connected to at least one current supply contact, whereby electrochemical cells are formed delimited by said cavities, said substrate conducting electrode layer and said electrode conducting material, whereby said cells comprise an electrolyte; connecting an electric power source to said electrode current supply contact and said substrate current supply contact for passing a current through said electrochemical cells for transferring material between said master electrode and said substrate; whereby the method further comprises selection of a master electrode, the specific resistivity of which is adapted to the substrate conducting material.

BRIEF DESCRIPTION OF DRAWINGS

[0023] Further objects, features and advantages of the invention will appear from the following detailed description of several embodiments with reference to the drawings, in which:
FIGS. 1(a) to 1(d) are schematic cross-sectional views of several method steps in forming a master electrode from a conducting or semiconductor carrier.

FIGS. 2(a) to 2(d) are schematic cross-sectional views of several method steps in forming a master electrode from a non-conducting carrier.

FIGS. 3(a) to 3(e) are schematic cross-sectional views of several method steps in forming a master electrode from a conducting carrier with added conducting layer in a pattern.

FIGS. 4(a) to 4(e) are schematic cross-sectional views of several method steps in forming a master electrode with pattern arranged in the carrier.

FIG. 5 is a schematic cross-sectional view of a master electrode in which cells of the pattern are deep.

FIGS. 6(a) to 6(c) are schematic cross-sectional views of several method steps in forming a master electrode with an adhesion layer bonded insulating pattern layer.

FIG. 7(a) is a schematic cross-sectional view and FIG. 7(b) is a top view of a master electrode applied on a large substrate.

FIG. 7(c) is a schematic cross-sectional view and FIGS. 7(d) to 7(e) are top views of a master electrode provided with one or several recesses.

FIGS. 7(f) to 7(i) are schematic cross-sectional views of a master electrode provided with contact areas to a substrate.

FIGS. 8(a) and 8(b) are diagrams showing the potential distribution at the master electrode and seed layer, and FIG. 8(c) is a diagram showing the current distribution, in one embodiment.

FIGS. 9(a) and 9(b) are diagrams showing the potential distribution at the master electrode and seed layer, and FIG. 9(c) is a diagram showing the current distribution in another embodiment.

FIGS. 10(a) and 10(b) are diagrams showing the potential distribution at the seed layer and the current distribution in a yet another embodiment.

FIGS. 11(a) and 11(b) are diagrams showing the potential distribution at the master electrode and seed layer, and FIG. 11(c) is a diagram showing the current distribution in another embodiment.

FIG. 12 is an enlarged cross-sectional view of conductive paths in several electrochemical cells.

FIGS. 13(a) and 13(b) are cross-sectional views in which the substrate is concave from the start.

FIGS. 14(a) and 14(b) are cross-sectional views similar to FIGS. 13(a) and 13(b) in which the substrate is convex from the start.

FIGS. 15(a) to 15(e) are schematic cross-sectional views of an embodiment of a master electrode provided with three-dimensional cavities in a pattern layer.

FIGS. 16(a) to 16(c) are schematic cross-sectional views of another embodiment of a master electrode provided with three-dimensional cavities in a pattern layer.

FIGS. 17(a) to 17(b) are schematic cross-sectional views showing an embodiment of the master electrode having cavities of different depths with an uneven distribution of predeposited material.

FIGS. 18(a) to 18(b) are schematic cross-sectional views showing another embodiment of the master electrode having cavities with an uneven distribution of predeposited material.

FIG. 19(a) is a schematic cross-sectional views showing a master electrode with several contact portions. FIG. 19(b) is a plan view of the master electrode of FIG. 19(a).

FIGS. 20(a) to 20(b) and 21(a) to 21(b) are schematic cross-sectional views respectively showing the electrochemical cell and the current distribution in a polar and a linear model.

DETAILED DESCRIPTION OF EMBODIMENTS

Below, several embodiments of the invention will be described with references to the drawings. These embodiments are described in illustrating purpose in order to enable a skilled person to carry out the invention and to disclose the best mode. However, such embodiments do not limit the invention, but other combinations of the different features are possible within the scope of the invention.

When etching and/or plating is performed on a substrate provided with a seed layer, which conducts the current at the substrate, it occurs that a substantial potential difference occurs across the seed layer. This being especially true in thin seed layers and at high etching/plating currents. If a potential difference of more than about 1% is present over the electrochemical cells as a result of a potential difference over the surface of the seed layer, the current densities in the electrochemical cells will vary in such an extent that a height difference is observable in the etched/plated structures formed. This problem is amplified by the fact that the current density in the electrochemical cells is exponentially dependent on the cell voltage. A 1% variation of the cell voltage results in a larger variation of the heights of the structures.

This problem is larger with thin seed layers on the substrate. In this specification we will use the concept of specific conductance, which is the thickness (h) of the conducting layer divided by the resistivity (ρ) thereof. For a copper layer of a thickness of less than 1 μm, this problem may be present. Such a thin layer has a specific conductivity of about 58Ω⁻¹.

We have observed this phenomena when the specific conductivity is lower than about 1000Ω⁻¹, such as lower than about 100Ω⁻¹, for example lower than about 20Ω⁻¹.

Such observations have been made at current densities of between 0.1 A/dm² and about 100 A/dm².

The problems also differ for different contact geometries. In a substrate, the seed layer can often only be contacted at the perimeter of the substrate. If the substrate can be contacted at other places, for example through vias, the potential difference may be eliminated or reduced.

Sometimes, conducting structures at the substrate aids in increasing the specific conductivity, thereby reducing this problem.

Below some embodiments are presented for reducing this problem. Thus, the master electrode used for forming the electrochemical cells is designed so that the master electrode to some extent mimics the potential difference over the electrochemical cells.

This can be done by different means in the master electrode.

The specific conductivity of the master electrode can be adapted to that of the conducting layer of the substrate. Thus, the specific conductivity of the master electrode should be from about 0.1 to 100 times, such as between 0.5 to 20, such as between 1 to 10 times the specific conductivity of the conductive layer of the substrate.
In a polar geometry in which a thin seed layer of a substrate is contacted over the perimeter of the seed layer and the master electrode is contacted in the centerum, the specific conductivity of the master electrode should be from about 1 to 10 times, such as about 3 to 8 times, for example about 5 to 7 times the specific conductivity of the conductive layer of the substrate.

In a linear geometry in which a thin seed layer of a substrate is contacted over one side of the seed layer and the master electrode is contacted over the other side, the specific conductivity of the master electrode should be from about 0.2 to 10 times, such as about 0.5 to 5 times, for example from about 0.8 to 1.2 of the specific conductivity of the conductive layer of the substrate.

The specific conductivity of the master electrode may vary over the surface, which could be obtained by varying the thickness of the conducting material or varying the resistivity of the material. The resistivity can be varied, for example by having a semiconducting material, such as silicon, doped at a varying degree over the surface. The doping rate determines the resistivity.

In a substantially centric or polar layout, in which the master electrode is contacted in the centerum, the specific conductivity could be high in the middle and reduced towards the perimeter.

Another means to solve the problem is to provide the master electrode with several contact points over the surface and feed the contact portions with voltages at different potentials, which mimics the current density distribution at the substrate. In this way, the potential difference over the electrochemical cell can be made with less fluctuation over the surface of the substrate.

By combining the use of several contact portions and varying specific conductivity of the master electrode, the current density in each cell can be controlled.

In some embodiments it is desirable to have a varying current density over the surface of the substrate. In this situation, the use of several contact portions and varying or adapted specific conductivity of the master electrode conducting material, can be combined to obtain a desired current distribution.

The master electrode is adapted to the expected substrate conditions. However, during plating with predeposited anode material in the cavities, the predeposition may take place by electrochemical deposition from an electroplating anode, such as an anode plate, an anode disc or anode balls. If the electrode conducting material has a low conductivity, there is a risk that the predeposition will be less in cavities at a distance from a central contact portion of the master electrode, specifically if the anode is thick and highly conducting. In order to counteract this phenomenon, the master electrode can be provided with several contact portions or be contactable over a large area, thereby reducing the difference in predeposition rate. Thus, specific contact portions may be used for predeposition and other contact portions for the plating process.

The current density in each electrochemical cell is dependent on the distance between the anode and cathode. This being especially true if the conductivity in the electrolyte used for the electrochemical cell is low or if the current density used is high, such as close to the limiting current. Thus, the current density distribution between the electrochemical cells can be controlled by the thickness of the material in each cell.

The above-mentioned principles may be embodied in a master electrode as mentioned above. Below, some general remarks are given with regard to the master electrode and methods of forming the master electrode. Several methods are described for forming a master electrode that can be used for producing one or multiple layers of structures of one or multiple materials including using an electrochemical pattern replication (ECPR) technology described below. The methods generally include forming a master electrode that comprises a carrier which is conducting/semiconducting in at least some parts; forming a conducting electrode layer which functions as anode in ECPR plating and cathode in ECPR etching; and forming an insulating pattern layer that defines the cavities in which ECPR etching or plating can occur in the ECPR process; in a way that makes possible electrical contact from an external power supply to the conducting parts of the carrier and/or to the conducting electrode layer.

The master electrode comprises at least one cavity for forming an electrochemical cell. Although there may exist a single cell, normally a large plurality of cells are used. Thus, the surface of the master electrode may be regarded as having a cell density of for example 1% to 50% meaning that the cavities occupy 1% to 50% of the total surface of the master electrode. The master electrode may have a lateral dimension of several tenths or hundreds of millimeters, up to thousands of millimeters, and the cavities may be in the micrometer or nanometer size.

The master electrode is to be used for producing one or multiple layers of structures using the electrochemical pattern replication (ECPR) technology including the following steps, namely:

- a) putting a master electrode in contact with the substrate, such as a seed layer of the substrate, to form multiple electrochemical cells;
- b) forming structures in said seed layer by etching or forming structures on said seed layer by plating; and
- c) separating said master electrode from said substrate.

In a first step (a) a master electrode comprising an electrically conducting electrode layer, at least one material, which normally is inert such as platinum or gold and which may have been provided with a predeposited anode material, such as copper or nickel, and an insulating pattern layer, is put in close physical contact with a conducting top layer or seed layer of a substrate in the presence of an electrolyte. In this way, there is formed electrochemical cells, filled with electrolyte. The cells are defined by the cavities of the insulating structures on the master electrode, the conducting electrode layer or predeposited anode material of the master electrode and the conducting top layer of the substrate.

Said seed layer can comprise one or several layers of metals such as Ru, Os, Hf, Re, Rh, Cr, Au, Ag, Cu, Pd, Pt, Sn, Ta, Ti, Ni, Al, alloys of these materials, Si, other materials such as W, TiN, TiW, NiB, NiP, NiCoNiB, NiM-P, W, TaN, Wo, Co, CoReP, CoP, CORWP, CoWB, CoWB, conducting polymers such as polyoxline, solder materials such as SnPb, SnAg, SnAgCu, SnCu alloys such as monel, permalloy and/or combinations thereof. The seed layer of the substrate can be cleaned and activated before usage in the ECPR process. The cleaning method can include the use of organic solvents e.g. acetone or alcohols; and/or inorganic solvents e.g. nitric acid, sulfuric acid, phosphoric acid, hydrochloric acid, acetic acid, hydrofluoric acid, strong oxidizing agents, e.g. peroxydis, persulfates, ferric-chloride, and/or de-ionized water.
Cleaning can also be performed by applying oxygen plasma, argon plasma and/or hydrogen plasma or by mechanically removing impurities. Activation of the seed layer can be performed with solutions removing oxides, e.g. sulfuric acid, nitric acid, hydrochloric acid, hydrofluoric acid, phosphoric acid and etchants, e.g. sodium-per sulfate, ammonium-per sulfate, hydrogen-peroxide, ferric-chloride and/or other solutions comprising oxidizing agents.

[0073] Putting the master electrode in close contact with the top layer on the substrate includes aligning the master electrode insulating pattern to the patterned master electrode on the substrate. This step can include the use of alignment marks on the front side or backside of the master electrode that can be aligned to the corresponding alignment mark on the substrate. The alignment procedure can be performed before or after applying the electrolyte. Predeposited anode material may previously be arranged onto said conducting electrode layer in the cavities of the insulating pattern layer prior to putting the master in contact with a substrate. Predeposited anode material in the master electrode cavities can be cleaned and activated in advance, in the same manner as described for the substrate seed layer, before putting the master into contact with the substrate.

[0074] Said electrolyte comprises a solution of cations and anions appropriate for electrochemical etching and/or plating, such as conventional electroplating baths. For instance, when the ECPR etched or plated structures are copper, a copper sulphate bath can be used, such as an acidic copper sulphate bath. Acidic may include a pH=1-4, such as between pH=2 and pH=4. In some embodiments, additives can be used, such as suppressors, levellers and/or accelerators, for instance PEG (poly-ethylene glycol) and chloride ions and/or SPS (bis(3-sulpropyl)disulphide). In another example, when the ECPR etched or plated structures are Ni, a Watt’s bath can be used. Appropriate electrolyte systems for different materials of ECPR etched or plated structures are described in: Lawrence J. Dumey, et al., Electroplating Engineering Handbook, 4th ed., (1984).

[0075] In a second step (b) structures of conducting material are formed using ECPR etching or plating by applying a voltage, using an external power source, to the master electrode and to the seed layer on the substrate for creating an electrochemical process simultaneously inside each of the conducting material cavities of the master electrode layer. The conducting material cavities of the master electrode and the top layer on the substrate.

[0076] When the voltage is applied in such a manner that the seed layer on the substrate is anode and the conducting electrode layer in the master electrode is cathode, the seed layer material is dissolved and at the same time material is deposited inside the cavities of the master electrode. The grooves created by dissolving the seed layer separate the remaining structures of the seed layer. The structures formed from the remaining seed layer is a negative image of the cavities of the insulating pattern layer of the master electrode; and these structures are referred to as “ECPR etched structures” below in this specification.

[0077] When the voltage is applied in such a manner that the conducting electrode layer in the master electrode is anode and the seed layer of the substrate is cathode, the predeposited anode material inside the cavities of the master electrode is dissolved and at the same time material is deposited on the conducting layer on the substrate in the cavities that are filled with electrolyte. The deposited material on the conducting layer on the substrate forms structures that are a positive image of the cavities of the insulating pattern layer of the master electrode; and these structures are referred to as “ECPR plated structures” below in this description.

[0078] Said ECPR etched or ECPR plated structures can be comprised of conducting materials, such as metals or alloys, for instance Au, Ag, Ni, Cu, Sn, Pb and/or SnAg, SnAgCu, AgCu and/or combinations thereof, for example Cu.

[0079] In one embodiment, said anode material is predeposited in the cavities of the master electrode by using ECPR etching of a material, which is anode, and depositing said material onto the conducting electrode, which is cathode, in the cavities of the insulating pattern layer of the master electrode. In other embodiments, said anode material is predeposited by regular electroplating, electroless plating, immersion plating, CVD, MO-CVD, (charged) powder-coating, chemical grafting and/or electrografting said material selectively onto the conducting electrode layer in the cavities of the insulating pattern layer of the master electrode.

[0080] The voltage can be applied in a manner that improves the uniformity and/or properties of the etched and/or plated structures. The applied voltage can be a DC voltage, a pulsed voltage, a square pulsed voltage, a pulse reverse voltage and/or a combination thereof.

[0081] The uniformity of the etched and/or plated structures can be improved by choosing an optimized combination of applied voltage waveform, amplitude and frequency. The etch depth or plating height can be controlled by monitoring the time and the current passing through the master electrode. If the total electrode area is known, the current density can be predicted from the current passing through the electrode area. The current density corresponds to an etching or plating rate and hence the etching depth or plating height can be predicted from the etching or plating rate and time.

[0082] In some embodiments, the etching or plating process is stopped by disconnecting the applied voltage before reaching the underlying surface of the dissolving anode material. For the etching process, this means that the process is stopped when a layer is still remaining in the bottom of the etched grooves in the seed layer, covering the underlying substrate layer. Otherwise, there is a risk that the electric connection to certain portions of the seed layer may be broken. For the plating process, this means that the process is stopped when a layer of predeposited anode material still remains, such as 5% to 50%, covering the conducting electrode layer. Otherwise, uneven current distribution may occur in the respective electrochemical cells.

[0083] In some embodiments, the desired height of the plated structures are significantly less than the thickness of the predeposited anode material. This implies that several layers of structures can be plated onto one or several substrates before having to predeposit new anode material. In some examples the height of the predeposited material can be at least twice as thick as the height of the plated structures.

[0084] In some embodiments, multiple layers of ECPR plated structures are applied directly onto each other.

[0085] In a third step (c) after the ECPR etched or plated structures are formed, the master is separated from the substrate in a manner that minimizes damages on the master or on the ECPR etched or plated structures on the substrate. The method can be performed by holding the substrate in a fixed position and moving the master electrode in a direction perpendicular to the substrate surface or by holding the master electrode in a fixed position and moving the substrate in a direction perpendicular to the master electrode surface. In
other embodiments, the separation can be performed in a less parallel manner in order to ease the separation. After the ECPR etching or plating step, remaining material deposited inside the cavities of the master electrode can be removed using removal methods that include applying wet etching chemicals suitable for dissolving the remaining materials. An anisotropic etching method can also be used for instance with dry-etching methods such as ion-sputtering, reactive-ion-etching (RIE), plasma-assisted-etching, laser-ablation, ion-milling. In still another embodiment, said removal methods include a combination of dry-etching and wet-etching methods. The remaining material can in some embodiments also be removed by regular plating and/or ECPR plating onto any cathode and/or dummy substrate respectively. In some embodiments this is done prior to using the master electrode in another ECPR etching step or prior to predepositing new material inside the cavities of the master used for the ECPR plating step. Alternatively, during plating, only a portion of the predeposited material may be used in a single procedure and another portion of the predeposited material may be used in the next procedure, for a number of procedures. Alternatively, during etching, the material deposited on the cathode, i.e. the master electrode, may not need to be removed between each procedure, but may be removed between each second, third etc procedure.

Three embodiments of methods for forming a master electrode generally comprises the following steps:

1. supplying an insulating or conducting/semiconducting carrier
2. applying a conducting electrode layer onto at least some parts of said carrier
3. applying an insulating pattern layer onto at least some parts of said conducting electrode layer

or

1. supplying an insulating or conducting/semiconducting carrier
2. applying an insulating pattern layer onto at least some parts of said carrier
3. applying a conducting electrode layer onto selected parts of said carrier which are not covered by said insulating pattern layer

or

1. supplying and patterning a conducting/semiconducting carrier
2. applying an insulating pattern layer onto at least some parts of said patterned carrier
3. applying a conducting electrode layer into selected parts of said patterned carrier that is not covered by said insulating pattern layer.

The materials used for the portions of the master electrode that are exposed to the chemical and/or electrochemical environment during ECPR etching, ECPR plating, predeposition, cleaning and/or removal methods, are generally resistant to dissolution and oxidation in said chemical and/or electrochemical environment.

In one embodiment, said conducting electrode layer is applied onto said carrier and said insulating pattern layer is applied onto the conducting electrode layer.

In another embodiment, said insulating pattern layer is applied onto said carrier and said conducting electrode layer is applied onto at least some parts of the carrier inside the cavities of the insulating pattern layer.

In still another embodiment, recesses are created in said carrier and said insulating pattern layer is applied in areas of the carrier, which are not provided with the recesses, while said conducting electrode layer is applied onto the carrier in the bottom of and onto the walls of the recesses that are not covered by the insulating pattern layer.

Said carrier may comprise one or several layers of:

- at least one conducting/semiconducting material;
- at least one insulating/conducting material and at least one layer of insulating material.

Said layers of said carrier can be flexible and/or rigid and/or a combination of flexible and rigid layers. In some embodiments, said carrier is rigid enough to avoid bending down significantly into the cavities of said insulating pattern when applying the force needed to put the master electrode in contact with a substrate, thereby avoiding a short circuit contact between the carrier and the substrate during ECPR etching and/or ECPR plating. For instance, the distance that the carrier bends down when applying required pressure should be less than 50% of the height of the cavities, such as less than 25%, for example less than 10%, for instance less than about 1%. In one embodiment, said carrier is flexible enough to compensate for waviness and/or unevenness of the substrate when a force is applied to put the master into contact with the substrate during ECPR etching and/or ECPR plating. In some cases, the carrier is at least as flexible as the substrate. For instance, the substrate can be a glass, quartz or silicon wafer. In this example, the master electrode carrier can have the same or higher flexibility as a glass, quartz or silicon wafer, respectively.

The conducting/semiconducting material can be made of materials such as conducting polymers, conducting paste, metals, Fe, Cu, Au, Ag, Pt, Si, SIC, Sn, Pd, Pt, Co, Ti, Ni, Cr, Al, Indium-Tin-Oxide (ITO), SiGe, GaAs, InP, Ru, Ir, Re, Hf, Os, Rh, alloys, phosphorous-alkoxies, SnAg, PbAg, SnAgCu, NiP, AuCu, silicides, stainless steel, brass, conducting polymers, solder materials and/or combinations thereof. The insulating layer can be comprised of oxides such as SiO₂, Al₂O₃, TiO₂, quartz, glass, nitrides such as SiN, polymers, polyimide, polyurethane, epoxy polymers, acrylate polymers, PDMS, (natural) rubber, silicones, lacquers, elastomers, nitrile rubber, EPDM, neoprene, PFTE, parylene and/or other materials used for said insulating pattern layer mentioned below.

In one embodiment, the carrier comprises a conducting/semiconducting disc that is covered by an insulating material coating over at least some parts. The insulating material coating may be applied so that it covers all parts of said conducting/semiconducting disc except for the center parts on the front- and back-side. The insulating material coating can be applied by methods such as thermo-oxidation, Plasma-Enhanced-Chemical-Vapor Deposition (PECVD), Physical Vapor Deposition (PVD), Chemical-Vapor-Deposition (CVD), Flame Hydrolysis Deposition (FHD), electrical anodization, Atomic-Layer-Deposition (ALD), spin-coating, spray-coating, roller-coating, powder-coating, adhesive taping, pyrolysis, bonding by other suitable coating techniques and/or combinations thereof. The insulating material coating can be applied selectively to the intended parts of said conducting/semiconducting disc or by applying it to the entire conducting/semiconducting disc followed by removing parts of the insulating material coating in selected areas. For instance, the insulating material coating can be removed by etching methods, such as by using an etch-mask to protect the areas where the insulating material coating should be intact and/or by using mechanical removing methods.
Said etching methods can be wet-etching and/or dry-etching methods. Wet-etching is performed by applying liquid chemicals that dissolve the material intended to be etched, said chemicals often including strong oxidizing chemicals such as strong acids and the like. For instance, buffered, diluted or concentrated hydrofluoric acid can be used to etch SiO$_2$. Said dry-etching methods can include methods such as ion-sputtering, reactive-ion-etching (RIE), plasma-assisted-etching, laser-ablation, ion-milling. The pattern of the etch-mask can be produced with lithographical methods such as photolithography, laser lithography, E-beam lithography, nanoimprinting and/or other lithographic processes suitable for patterning the etch-mask. Said etch-mask can be a polymer material, for instance a resist used in said lithographical methods such as a thinfilm photoresist, polyimide, BCB and/or a thick film resist. The etch-mask can also be a hard-mask comprising material such as SiN, SiC, SiO$_2$, Pt, Ti, TiW, TiN, Al, Cr, Au, Ni, other hard materials and/or combinations thereof. The hard-mask is patterned by said lithographical methods followed by etching the hard-mask selectively in the areas not covered by the patterned lithography mask. Said mechanical removing methods can include polishing, grinding, drilling, ablation, (sand or fluid) blasting and/or combinations thereof.

In another embodiment, the carrier comprises an insulating disc with at least some parts being of conducting/semiconducting material. In this case, the conducting/semiconducting part may be applied in the center of the insulating disc. In one embodiment, the carrier is formed by creating cavities in the insulating material disc in selected area and applying conducting/semiconducting material in the cavities. The cavities in the insulating disc can be formed by said wet-etching methods, said dry-etching methods and/or by said mechanical removing methods. Said etch-mask can be used in the method for creating the cavities and the etch-mask can be patterned with said lithographic methods. Methods for applying said conducting/semiconducting material in the cavities can be PVD, CVD, sputtering, electroless deposition, immersion deposition, electrodeposition, mechanical placement, soldering, gluing, by other suitable deposition methods and/or by combinations thereof. In some embodiments, a planarization step can be performed on the carrier in order to increase its planarity and to reduce surface roughness.

Said conducting electrode layer can be comprised of one or several layers of a conducting/semiconducting material. For instance, the conducting electrode layer can be comprised of Fe, Cu, Sn, Ag, Au, Pd, Co, Ti, Ni, Pt, Cr, Al, W, ITO, Si, Ru, Rh, Re, Os, Hf, other metals, alloys, phosphorous alloys, SnAg, SnAgCu, CuN, CuW, CcoW, NiP, AnC, silicides, graphite, stainless steel, conducting polymers, solder materials and/or combinations thereof. The conducting electrode layer can be applied to the carrier by methods such as ALD, Metallorganic-Chemical-Vapor-Deposition (MOCVD), PVD, CVD, sputtering, electroless deposition, immersion deposition, electrodeposition, electro-graffing, other suitable deposition methods and/or combinations thereof. In some embodiments, said conducting electrode layer can be deposited selectively onto conducting/semiconducting surfaces using methods such as electroless deposition, electrodeposition, immersion deposition, electro-graffing, chemical-graffing, selective CVD and/or selective MOCVD.

In some embodiments, the conducting electrode layer is treated by thermal methods. Said thermal methods may be performed in high vacuum, forming gas, hydrogen gas, nitrogen gas, gas environments with low oxygen content and/or by combinations thereof. Said thermal methods can be annealing (e.g. rapid-thermo-annealing (RTA)), furnace treatment, hot-plate treatment and/or combinations thereof. Said thermal methods can in some embodiments improve the adhesion between the conducting electrode layer and the carrier and/or improve the electrical and/or mechanical properties of the master electrode (such as hardness and/or wear resistance), by reducing internal stress and/or contact resistance to said carrier. In some embodiments, the conducting electrode layer is formed by applying several layers of at least one material and by treating at least one layer by said thermal methods before applying a next layer.

In one embodiment, an adhesion layer is applied onto at least some parts of the carrier prior to applying said conducting electrode layer. Said adhesion layer can be comprised of a material or several materials that increase the adhesion of the conducting electrode layer to the carrier. The adhesion layer may be comprised of a conducting material such as Pt, Al, Ni, Pd, Cr, Ti, TiW or an insulating material such as AP-3000 (Dow Chemicals), AP-100 (Silicon Resources), AP-200 (Silicon Resources), AP-300 (Silicon Resources), silanes such as HMDS and/or combinations thereof. If necessary, the adhesion layer is not covering all areas of said carrier in order to enable an electrical connection to said carrier, such as when the adhesion layer is insulating. Alternatively the adhesion layer is applied covering the entire carrier and then some parts are removed in areas where electrical connection is required between the conducting electrode layer and the carrier, for instance in the center of the front-side. The adhesion layer can in some embodiments also function as a catalytic layer facilitating or improving the deposition of the conducting electrode layer. The adhesion layer can be applied by using deposition methods such as electrodeposition, spin-coating, spray-coating, dip-coating, Molecular-Vapor-Deposition (MVD), ALD, MOCVD, CVD, PVD, sputtering, electroless deposition, immersion deposition, electrografting, chemical grafting and/or other deposition methods suitable for the adhesion material.

Said insulating pattern layer can be comprised of one or several layers of patterned electrically insulating material. The insulating pattern layer may be applied with methods giving low surface roughness and high thickness uniformity of the layer. In some embodiments, the insulating pattern layer can be applied using methods such as thermal oxidation, thermal nitridation, PECVD, PVD, CVD, Flame Hydrolysis Deposition (FHD), MOCVD, electrochemical anodization, ALD, spin-coating, spray-coating, dip-coating, curtain-coating, roller-coating, powder-coating, pyrolysis, adhesive taping, bonding, by other deposition techniques and/or by combinations thereof.

In one embodiment, an adhesion layer is applied prior to applying the insulating pattern layer onto said carrier. Said adhesion layer may comprise at least one layer of at least one material that improves the adhesion properties between the insulating pattern layer and the surface of said carrier. Said adhesion layer may be comprised of an insulating or conducting material. Said adhesion layer can for instance be comprised of Pt, Ni, Al, Cr, Ti, TiW, AP-3000 (Dow Chemicals), AP-100 (Silicon Resources), AP-200 (Silicon Resources), AP-300 (Silicon Resources), silanes such as HMDS, Bottom-Anti-Reflective-Coating (BARC) materials and/or combinations thereof. The adhesion layer can be
applied using methods such as PECVD, PVD, CVD, MOCVD, ALD, spin-coating, spray-coating, roller-coating, powder-coating and/or by combinations thereof.

[0115] In some embodiments, a planarization step can be performed on the applied insulating pattern layer in order to achieve a more planar surface. Said planarization step can be done prior to patterning the insulating pattern layer. Said planarization methods can include etching and/or polishing methods such as chemical-mechanical-polishing (CMP), lapping, contact planarization (CP) and/or dry etching methods such as ion-sputtering, reactive-ion-etching (RIE), plasma-assisted-etching, laser-ablation, ion-milling and/or by other planarization methods and/or by combinations thereof.

[0116] The insulating pattern layer can be comprised of organic compounds, such as polymers, as well as insulating in-organic compounds such as oxides and/or nitrides. Used polymer materials can for instance be: polyimide, siloxane modified polyimide, BCB, SU-8, polytetrafluoroethylene (PTFE), silicones, elastomeric polymers, E-beam resists (such as ZEP (Sumitomo)), photoresists, thinfilm resists, thickfilm resists, polycyclic olefins, polynorbornene, polyethylene, polycarbonate, PMMA, BARC materials, Lift-Off Layer (LOL) materials, PDMS, polyurethane, epoxy polymers, fluoro elastomers, acrylate polymers, (natural) rubber, silicones, lacquers, nitride rubber, EPDM, neoprene, PTFE, parylene, fluoromethylcyano ester, inorganic-organic hybrid polymers, (fluorinated and/or hydrofluorinated) amorphous carbon, by other polymers and/or by combinations thereof. Used in-organic compounds can for instance be organic doped silicon glass (OSG), fluorine doped silicon glass (FGS), PCTFTESilicon compound, tetrathyl orthosilicate (TEOS), SiO, SiON, SiOC, SiCN-H, SiOCH materials, SiCH materials, silicones, silicon based materials, silsesquioxane (SSQ) based material, methyl-silsesquioxane (MSQ), hydrogen-silsesquioxane (HSQ), TiO, AlO, TiN and/or combinations thereof. The insulating pattern layers may have properties that ease the patterning process (lithography and/or etching), have good adhesion to the underlying layer, have good mechanical durability and/or are inert during the ECPR process and/or intermediate cleaning and/or removal steps.

[0117] In some embodiments, the pattern (cavities) of the insulating pattern layer is fabricated using methods such as lithography and/or etching. Said lithography methods can include photolithography, UV-lithography, laser-lithography, electron-beam (E-beam) lithography, nanoimprint, other lithographic methods and/or combinations thereof.

[0118] Said insulating patterning layer can have different heights depending on the desired shape and size of the ECPR etched or plated structures. In some embodiments, said insulating pattern layer can have a thickness up to a few hundred microns. In other embodiments, the insulating pattern layer can be thin, such as down to 20 nm. In some embodiments, the height/width ratio of a cavity (called aspect ratio) is less than 10, such as less than about 5, for instance less than about 2, for example less than about 1. In some embodiments, such as for above-IC applications, the insulating pattern layer is less than about 50 μm, for instance less than about 15 μm, such as less than about 5 μm, with an aspect ratio of less than about 5, for instance less than about 2, such as less than about 1. In some embodiments, such as for IC interconnect applications, the insulating pattern layer is less than about 2 μm such as for IC interconnect global wiring, such as less than 500 nm such as for IC interconnect intermediate wiring, for example less than 200 nm such as for IC interconnect intermediate wiring, such as less than about 100 nm such as for IC interconnect “Metal 1” wiring, for instance less than about 50 nm such as for IC interconnect “Metal 1” wiring. Since there is no forced convection inside said electrochemical cells, the limiting maximum current and hence the maximum plating/etching rate is determined by the properties of the electrolyte and distance between the electrodes, i.e. the height of the insulating pattern layer. A higher limiting current is achieved using electrolytes comprising higher concentration of ions of the material being electrochemically etched or deposited. Furthermore, less distance between the conducting electrode layer and the seed layer of the substrate results in higher limiting current. However, short distance, i.e. thin insulating pattern layer, increases the risk of getting short circuits. The thickness of the structure layer to be formed can be less than about 90% of the insulating layer thickness, such as less than about 50%, for example less than about 10%.

[0119] Said etching methods include using an etch-mask to protect the areas where the insulating pattern layer should be intact and/or by using mechanical removing methods. Etching methods can include wet-etching and/or dry etching methods such as ion-sputtering, reactive-ion-etching (RIE), plasma-assisted-etching, laser-ablation, ion-milling. The pattern of the etch-mask can be produced with said lithographical methods. The etch-mask can be a polymer resist used in said lithographical methods such as a thinfilm photoresist, polyimide, BCB, a thick film resist and/or other polymers and the like. The etch-mask can also be a hard-mask comprising material such as SiN, SiO, SiC, Pt, Ti, TiW, TiN, Al, Cr, Au, Cu, Ni, Ag, NiP, other hard materials, alloys thereof and/or combinations thereof. Said hard-mask can be applied with methods such as PVD, CVD, MOCVD, sputtering, electroless deposition, immersion deposition, electroless deposition, PECVD, ALD, other suitable deposition methods and/or combinations thereof. The hard-mask is in some embodiments patterned by said lithographical methods followed by etching the hard-mask, selectively in the areas not covered by the patterned lithography mask, using wet- and/or dry-etching methods.

[0120] In some embodiments, said hard-mask can comprise at least one layer of ECPR etched or plated structures, for instance when the materials used for the hard-mask are Cu, Ni, NiFe, NiP Au, Ag, Sn, Pb, SnAg, SnAgCu, SnPb and/or combinations thereof. In this case, the insulating pattern layer of a master electrode can be patterned by using another master electrode, in combination with said etching methods, and other lithographical methods may not be required.

[0121] In some embodiments, an etch-stop layer is applied prior to applying said insulating pattern layer. Said etch-stop layer comprises at least one layer of one or several materials that are less affected by the etching process than the insulating pattern layer, thereby stopping or slowing down the etching process thus protecting the underlying layer when the etching has gone through the insulating pattern layer. Said etch-stop layer can comprise materials such as: Ti, Pt, Au, Ag, Cr, TiW, SiN, Ni, Si, SiC, SiO, Al, InGaP, Co, COWP, NiP, NiPco, AuCo, Xerox (Applied Materials) or other materials less affected by said etching methods and/or combinations thereof.

[0122] In one embodiment, the said patterning methods can be modified in order to affect the angle of inclination of the pattern cavity sidewalls in the insulating pattern layer. The
angle of inclination depends on the application of the ECPR etched or plated structures. In some embodiments, close to vertical sidewalls (close to 90 degree angle of inclination between the sidewalls of the insulating pattern layer and the carrier surface, vertical means in relation to a normal position of the structure in which it is horizontal) are used in order to achieve certain electrical properties. This means that the sidewalls have an angle to the normal of the electrode surface (angle of inclination) of less than about 1°, such as less than about 0.1°. In other embodiments, a larger angle of inclination is used in order to improve the separation method of the master electrode from the ECPR plated structures without causing damages either on the insulating pattern layer or on the ECPR plated structures. Such an angle may be up to about 45°, such as up to 20°, for example up to about 5°. Said separation method can be improved by modifying said angle of inclination so that it is more than zero degrees, which means that the cavities of the insulating pattern layer have an open area at the top which is larger than at the bottom (generally called "positive angle of inclination"). The angle should not be substantially negative.

In some embodiments, photoresists used for creating the insulating pattern layer, by using said lithographic methods may have chemical and physical properties that give vertical side walls or a positive angle of inclination. For instance, negative photoresists such as SU-8 (Microchem), THB (JSR Micro) or E-beam resists such as ZEP (Sumitomo) can be used in order to achieve an angle of inclination which is close to zero. Other positive photoresists such as AZ® AX™, AZ® P9200, AZ® P4000 (AZ Electronic Materials), ARF resists (JSR Micro), SPR resists (Rohm & Haas Electronic Materials) and/or other positive photoresists can be used for creating an insulating pattern layer with a positive angle of inclination. The angle of inclination can also be adjusted by modifying parameters of the photolithographic methods. For instance, the angle of inclination of the side walls can be varied by modifying the depth of focus when exposing the photoresist through a projection lens. Also, the angle of inclination can be optimized by varying parameters in a photolithographic patterning method, for instance: using wave-length filters, using anti-reflective coatings, modifying the exposure dose, modifying the development time, using thermal treatment and/or combinations thereof.

In another embodiment, said etching methods used for patterning said insulating pattern layer can be modified in order to achieve a vertical side wall or positive angle of inclination. For instance, a certain angle of inclination can be obtained by optimizing the gas composition, platen power (RF power) and/or plasma power (also called coil power) for dry-etching methods such Reactive-Ion-Etching (RIE). Said gas composition can for instance comprise fluorocarbon, oxygen, hydrogen, chlorine and/or argon. The angle of inclination can be controlled by modifying the level of polymerization of passivating substances on the sidewalls. For instance, by increasing or decreasing the level of fluorocarbon in the gas composition, the level of polymerization increases or decreases respectively which in turn results in an increased (less vertical) or decreased (more vertical) angle of inclination, respectively. Further, the degree of polymerization can be controlled by: modifying the oxygen and/or hydrogen content by increasing the oxygen level which reduces polymerization and give a smaller angle of inclination (more vertical) and vice versa, and/or by increasing the hydrogen level which increases polymerization and give a larger angle of inclination (less vertical) and vice versa. In some embodiments, said angle of inclination is decreased (made more vertical) by decreasing said coil power while holding said platen power constant. This increases the sputtering effect and thereby results in more vertical side walls when etching said insulating pattern layer. By instead increasing said coil power the opposite effect can be achieved thereby resulting in a larger angle of inclination (less vertical). In another embodiment, said angle of inclination is decreased (more vertical) by increasing said platen power while said coil power is held constant. A larger angle of inclination (less vertical) when etching said insulating pattern layer can be achieved by decreasing said platen power while said coil power is held constant.

In yet another embodiment, a damascene process can be used to create the cavities (pattern) of said insulating pattern layer: said damascene process involving firstly applying a sacrificial pattern layer onto a carrier, secondly applying an insulating material so that it cover said sacrificial pattern layer as well as fills up the cavities of the sacrificial pattern, by using said application methods mentioned above for the insulating pattern layer, planarizing said insulating material, using planarization methods mentioned above, until the sacrificial pattern layer is uncovered; and removing said sacrificial pattern layer whereby an insulating pattern layer is formed. Said sacrificial pattern layer can for instance be formed by ECPR etching or plating a structure layer or by using known lithographical and/or etching/plating methods. This alternative patterning method can for instance be used for embodiments including an insulating pattern layer material which is difficult to pattern directly with lithography and/or etching methods.

In an embodiment, said insulating pattern layer surface can be treated in order to improve better separation from the ECPR plated structures. For instance, the insulating pattern layer surface can be treated with methods that give an anti-sticking effect between the side-walls of said cavities and the side-walls of ECPR plated structures. This can include coating said insulating pattern layer surface with a release layer that decreases the mechanical and chemical bonds to ECPR plated structures. Such a release layer can be applied using spin-coating, spray-coating, CVD, MOCVD, MVD, PVD and/or by combinations thereof. Said release layer can comprise: silanes such as methoxy-silanes, chloro-silanes, fluoro-silanes, siloxanes such as poly-di-methyl-siloxane, poly-ethylane-glycol-siloxanes, dimethyl-siloxane oligomer (DMS) and/or other polymers such as amorphous fluoro-polymers, fluoro-carbons poly-tetra-fluoro-ethylen (PTFE), Cyto-fluoro-polymers and/or combinations thereof.

In one embodiment, the materials used for the insulating pattern layer have properties and/or are treated with methods that improve the ability of getting said electrolyte to wet and to fill up the cavities of the insulating pattern. In one embodiment, at least some parts of the insulating pattern layer materials have low surface energy properties and are hydrophilic, i.e. have a low contact angle with aqueous solutions. Furthermore, some parts of the insulating pattern layer material can be treated with methods that lower the surface energy and create hydrophilic surfaces. Such surface treatment methods can for instance be thermal treatment, oxygen/nitrogen/argon plasma treatment, surface conversion for anti-sticking (SURCAS) and/or treating the surface with strong oxidizing agents such as peroxides, persulfates, concentrated acids/bases and/or combinations thereof. In other embodiments, at
least some parts of the insulating pattern layer have high surface energy or can be treated with methods in order to increase the surface energy making the surface hydrophobic. Such methods can include treatment with hydrogen plasma. In an embodiment, the insulating pattern layer comprises one or several layers of at least one material having properties such that the side-walls of the cavities of the insulating pattern layer become hydrophilic and the top of the insulating pattern layer becomes hydrophobic. Said hydrophobic material can be for instance be SiN, SiO₂, polymers (such as photoresists and/or elastomers) that have been treated with oxygen plasma and/or other materials with polar functional molecule groups at the surface and/or combinations thereof. Said hydrophobic material can be materials with non-polar functional molecule groups such as hydrogen terminated polymers, Teflon, fluoro- and chloro-silanes, siloxanes, fluoro-elastomers and/or combinations thereof.

[0128] In another embodiment, the insulating pattern layer can have one or several layers of at least one material which improve the mechanical contact between the top of the insulating pattern layer surface and the seed layer surface of the substrate when the master electrode is pressed against said seed layer. As mentioned above, the insulating pattern layer can be comprised of at least one layer of flexible materials such as elastomers. In one embodiment, the insulating pattern layer comprises at least one layer of rigid material and at least one layer of said elastomer material. Said layers of elastomer material may be applied on top of said layers of rigid material. Said elastomer layer can have high compressibility and/or elastic properties; be electrically insulating and/or have low dielectric properties; have good chemical resistance against the environment used in the ECPR process and/or intermediate cleaning and/or removal steps, for instance against said electrolytes; be applied by methods such as PECVD, PVD, CVD, MOCVD, ALD, spin-coating, spray-coating, roller-coating, powder-coating, pyrolysis and/or combinations thereof; have strong adhesion to underlying layers such as metals, silicon, glass, oxides, nitrides and/or polymers; have high resistance against shrinking or swelling over time and/or in the environment used in the ECPR process, for instance in said electrolytes; be non-bleeding, i.e., are not releasing contaminating organic compounds; be sensitive to UV-light; be patterned with said lithography methods; be transparent; and/or be patterned by using said etching methods, for instance by said dry-etching methods. In some embodiments, said elastomers can be comprised of Poly-Di-Methyl-Siloxane (PDMS), silicones, epoxy-silicones, fluoro-silicones, fluoro-elastomers, (natural) rubber, neoprene, EPDM, nitrile, acrylate elastomers, polystyrene and/or combinations thereof. In some embodiments, said elastomer layer can have a tensile elastic modulus (Young's modulus) less than 0.1 GPa, such as less than 1 MPa, for example less than about 0.05 MPa. In some embodiments, said elastomer layer can have a hardness of less than 90 Shore-A, such as less than 30 Shore-A, for example less than about 5 Shore-A.

[0129] In other embodiments, an insulating layer is applied onto at least some parts of an already patterned surface, for instance a patterned carrier. In an embodiment, the insulating pattern layer is applied with a method in which the applied materials conformally follow the structures of underlying patterned carrier for instance by using methods such as thermal oxidation, thermal nitridation, sputtering, PECVD and/or ALD. Said insulating layer can be patterned in order to uncover at least some parts of said underlying patterned carrier. Said patterning method may uncover at least some parts of the cavities of said underlying patterned carrier from the insulating pattern layer. A usable patterning method includes that the insulating pattern layer is covering the side-walls and/or the top of the structures of said patterned carrier while the bottoms of the cavities of said patterned carrier are uncovered in at least some areas. Said patterning methods can be methods such as said lithography and/or etching methods described above. In some embodiments, said patterned carrier has at least one layer of insulating material on top of the patterned structures prior to applying said insulating pattern layer. For instance, the carrier is patterned by using said etching methods where the etch-mask comprise at least one layer of insulating material and the etch-mask is not stripped prior to applying said insulating pattern layer. This results in a thicker layer of insulating material on top of the structures, compared to the bottom, of said patterned carrier. In this embodiment, using etching methods, such as said dry-etching methods, can uncover the bottom of the cavities of the patterned carrier before uncovering the top. Said dry-etching method may have a higher etching speed in the direction perpendicular do the plane of said patterned carrier than in lateral direction, known as anisotropic etching, which allows for uncovering the insulating pattern material in the bottom of the cavities of the patterned carrier while leaving the side-walls still covered by the insulating material. In other embodiments, the insulating pattern layer is patterned in order to uncover at least some parts that can be used for electrical connection to said carrier and/or said conducting electrode layer.

[0130] Several embodiments of the master electrode will be described below with reference to the Figures on the drawings.

[0131] An embodiment includes supplying a carrier 1 comprising a conducting/semiconducting disc 2 and an insulating coating layer 3. Said insulating coating layer 3 may cover all areas of the conducting/semiconducting disc 2 except for an area in the center on the back-side and front-side, as shown in FIG. 1(a). A conducting electrode layer 4 can be applied onto the front-side of the carrier 1, covering and being in electrical contact with at least some parts of the conducting/semiconducting disc 2. In one embodiment, said conducting electrode layer 4 is also covering at least some parts of said insulating coating layer 3. In some embodiments, a connection layer 5 is applied onto at least some parts of said conducting/semiconducting disc on the back-side of the carrier in order to enable a good electrical connection to the master electrode from an external electrical source. A cross section of one embodiment of a carrier 1, comprising a conducting/semiconducting disc 2 and an insulating coating layer 3, with a conducting electrode layer 4 and connection layer 5 is illustrated in FIG. 1(b). In an embodiment, an insulating material 6 is applied onto the carrier 1 and the conducting electrode layer 4 as shown in FIG. 1(c). The insulating material can be patterned using said lithographical and/or etching methods, forming an insulating pattern layer 7. A cross section of an embodiment of a master electrode 8 comprising a carrier 1, conducting electrode layer 4, connection layer 5, and insulating pattern layer 7 is illustrated in FIG. 1(d).

[0132] In an embodiment, a carrier 1 comprises an insulating disc 9 with a conducting via 11 in the center at least partly filled with conducting/semiconducting material 10, as illustrated in FIG. 2(a). The insulating disc 9 may be transparent in order to enable alignment capabilities between the master
electrode and a substrate. In one embodiment, a conducting electrode layer 4 is applied onto the front-side of the carrier 1. In addition, a connection layer 5 can be applied on the back-side in order to enable a good electrical connection from an external electrical source to the master electrode. Electric connection between the conducting electrode layer 4 and the connection layer 5 is enabled by the via 11. A cross section of one embodiment of a carrier 1, which comprises an insulating disc 9 and a conducting via 11, a conducting electrode layer 4 and a connection layer 5 is illustrated in FIG. 2(b). An insulating material 6 can be applied onto the carrier 1 and the conducting electrode layer 4 as shown in FIG. 2(c). The insulating material can be patterned using said lithographical and/or etching methods, forming an insulating pattern layer 7.

FIG. 2(d) illustrates a cross section of one embodiment of a master electrode comprising a carrier 1, which comprise an insulating disc 9 and a connecting via 11, a conducting electrode layer 4, a connection layer 5 and an insulating pattern layer 7.

[0133] Another embodiment includes supplying a carrier 1 comprising a conducting/semiconducting disc 2 which is covered by an insulating coating layer 3 on at least some parts, such as on the front-side, of said carrier. In some embodiments, the insulating coating layer is firstly applied so that it completely covers said conducting/semiconducting disc, as illustrated in FIG. 3(a). In an embodiment, the insulating coating layer is patterned using said lithographical and/or etching methods creating an insulating pattern layer 7. In the cavities thus formed, at least some of the conducting/semiconducting disc 2 are uncovered, as illustrated in FIG. 3(b). The conducting electrode layer 4 can be applied selectively onto the conducting/semiconducting disc in the bottom of the cavities in the insulating pattern layer as shown in FIG. 3(c). Some parts, such as the center of the back-side of the insulating pattern layer 7 can be removed, thereby uncovering the conducting/semiconducting disc 2, in order to enable an electrical connection to the master electrode. A connection layer 5 can be applied on the uncovered area of the conducting/semiconducting disc, such as on the back-side, of the master electrode in order to enable a good electrical connection from an external electrical source to the master electrode. In some embodiments, some parts of the insulating pattern layer 7 at the backside are removed prior to applying the conducting electrode layer 4. The connection layer 5 can then be applied in the same step and with the same method as applying the conducting electrode layer. However, in some embodiments the connection layer 5 can be comprised of at least one layer, applied in the same step as applying the conducting electrode layer 4, and at least another conducting layer applied in a subsequent step. FIG. 3(d) illustrates a cross section of a master electrode 8 comprising a conducting/semiconducting disc 2, an insulating pattern layer 7, a conducting electrode layer 4 and a connection layer 5. FIG. 3(e) illustrates a cross section of another embodiment of a master electrode 8 comprising a conducting/semiconducting disc 2, an insulating pattern layer 7, a conducting electrode layer 4 and a connection layer 5 where the connection layer comprises several layers where at least one is also covering some parts of the insulating pattern layer 7 at the backside.

[0134] A further embodiment includes supplying a conducting/semiconducting carrier 1. The carrier is patterned on at least the front-side using said lithographical and/or etching methods. In one embodiment, an etch-mask 12 which is used for patterning the carrier comprises an insulating material. A cross section of the patterned conducting/semiconducting carrier 1, with an insulating material as etch-mask 12, is illustrated in FIG. 4(a). An insulating pattern layer 7 can be applied onto said patterned carrier and onto said etch-mask 12. In some embodiments, the insulating pattern layer 7 is applied with a method so that it conformally follows the structures of the underlying pattern layer, as shown in FIG. 4(b). This results in a thicker insulating layer on top of said pattern than in the bottom of the cavities because of the combination with layer 12.

[0136] Said etching methods can be used to uncover the carrier 1 from the insulating pattern layer 7 in the bottom of the pattern while leaving the insulating pattern layer 7 on the side walls and on the top. Dry-etching methods can be used that are characterized by having a higher etch-rate in the bottom of the cavities than on the side walls. In some embodiments, the same amount of insulating material is removed from the bottom of the cavities as on the top, leaving an insulating material thickness on the top corresponding to the thickness of said etch-mask 12 used for patterning the carrier. FIG. 4(c) illustrates a master electrode 8 comprising a patterned carrier 1, an etch-mask 12 and an insulating pattern layer 7 that has been etched in order to uncover the bottom of the cavities of the patterned carrier.

[0137] In some embodiments, a conducting electrode layer is applied selectively in the areas on the patterned carrier 1 that is not covered by an etch-mask 12 or an insulating pattern layer 7, and a second etch-mask 12 can be applied in the back-side in order to remove the insulating pattern layer and thereby uncovering some parts of the carrier 1 in a subsequent step, as shown in FIG. 4(d).

[0138] Removing parts of the insulating pattern layer 7 at the backside can be done by using said lithographical, and/or etching methods. A connection layer 5 can be applied on the uncovered parts of the carrier in order to enable a good electrical connection from an external electrical source to the master electrode. In some embodiments, the electrical connection in the master electrode is fabricated in the center of the back-side of the master electrode. In some embodiments, the connection layer 5 is applied in the same step as applying the conducting electrode layer 4. In this case, the uncovering of the carrier 1 in the connection area, is done prior to applying the conducting electrode layer 4. In some embodiments, the connection layer 5 is only applied in the uncovered parts of the carrier 1. In other embodiments, the connection layer is applied on the uncovered parts of the carrier and onto some parts of the insulating pattern layer 7.

[0139] FIG. 4(e) illustrates a cross section of one embodiment of a master electrode comprising a patterned conducting/semiconducting carrier 1 with an insulating etch-mask 12 on top of the carrier structures, an insulating pattern layer 7, a conducting electrode layer 4 applied in the cavities of the patterned carrier and a connection layer 5 applied on the back-side onto some parts of the insulating pattern layer and onto the uncovered parts of the carrier.

[0140] In some embodiments, the cavities of the master electrode (8) can be made deeper, prior to applying the conducting electrode layer 4, by removing material from the carrier 1 in the bottom of the cavities of the insulating pattern layer 7, for instance by using said etching methods. In some embodiments, dry-etching methods can be used. For some embodiments, said insulating pattern layer 7 can be used as an etch-mask. Creating deeper cavities results in that the master electrode cavities can be filled with a larger amount of pre-
deposited material used for ECPR plating and/or by etched material during ECPR etching.

[0141] FIG. 5 illustrates a cross section of a master electrode 8 where the cavities of the insulating pattern layer 7 have been etched deeper into the carrier 1 which thereafter has been covered by a selectively deposited conducting electrode layer 4.

[0142] One embodiment includes forming said insulating pattern layer 7 onto said carrier 1 by bonding and patterning an insulating bond-layer 13. In some embodiments, the carrier 1 comprises a conducting/semiconducting disc 2 covered with an insulating coating layer 3 except for in the center of the front- and back-side of the carrier. In other embodiments, the carrier comprises an insulating disc 9 with a conducting via 11 in the center of the carrier 1.

[0143] In some embodiments a conducting electrode layer 4 has been applied onto the carrier prior to applying the insulating bond-layer 13. In some embodiments, the insulating bond-layer is adhered to a bond-carrier 14 that can be removed after the insulating bond-layer 13 has been applied onto the carrier 1. For instance, the insulating bond-layer 13 can be SiO₂ on a Si bond-carrier 14 or the insulating bond-layer 13 can be glass, such as quartz, or a polymer film on any removable bond-carrier 14. In some embodiments, an adhesive bond-layer 15 can be applied onto the insulating bond-layer 13 prior to bonding it to the carrier 1 in order to improve bonding properties such as adhesive strength. The adhesive bond-layer 15 can be of a material that gives good bond properties together with the carrier and/or with the conducting electrode layer 4 on the carrier 1 and should be of a conducting material. Alternatively, the adhesive bond-layer 15 can be of a non-conducting material and be selectively removed by etching. For instance, the adhesive bond-layer 15 may comprise a metal and/or an alloy that bobs well with the conducting electrode layer 4. The adhesive bond-layer can comprise materials such as mentioned for said conducting electrode layer 4.

[0144] A cross section of a carrier 1 with a conducting electrode layer 4 and a bond-carrier 14 with an insulating bond-layer 13 and an adhesive bond-layer 15 prior to bonding is illustrated in FIG. 6(a).

[0145] FIG. 6(b) illustrates how an insulating bond-layer 13 on a bond-carrier 14 is bonded to a carrier 1 with a conducting electrode layer 4 and an adhesive bond-layer 15 in-between. In some embodiments, the layers in-between the insulating bond-layer 13 and the carrier 1 are altered (e.g., mixed) during the bonding process and a bond-intermediate layer 16 is formed. The bond-carrier 14 can be removed mechanically and/or by using said etching methods, such as dry-etching or wet-etching. After the bond-carrier 14 has been removed, the insulating bond-layer 13 can be patterned using said lithographical and/or etching methods. FIG. 6(c) illustrates a cross section of one embodiment of a master electrode 8 comprising a patterned insulating bond-layer 13 that has been bonded to a carrier 1 with a bond-intermediate layer 16 in between which is comprising a conducting electrode layer 4 and an adhesive bond-layer 15. In some embodiments, a conducting electrode layer 4 can be applied selectively into the cavities of the patterned insulating bond-layer 13 onto said bond-intermediate layer 16 or onto said carrier 1 if no bond-intermediate layer 16 exists (i.e. when the insulating bond-layer 13 is applied directly onto the carrier 1).

[0146] In an embodiment, the master electrode enables an electrical connection from an external electrical source to at least some parts of said conducting electrode layer.

[0147] In some embodiments, the electrical connection is made from an external electrical source to said conducting/semiconducting material of said carrier which is connected to at least some parts of the conducting electrode layer.

[0148] In an embodiment, the electrical connection is made from an external electrical source to a connection layer which is connected to at least some parts of the conducting/semiconducting parts of the carrier which in turn is connected to the conducting electrode layer.

[0149] The electrical connection can for instance be located on the back-side of said carrier, i.e. the opposite side of the insulating structures of the master electrode. In some embodiments, the electrical connection can be used in the center of the back-side of said carrier. In another embodiment, the electrical connection is made from front-side, such as in the perimeter of said carrier.

[0150] In some embodiments, the insulating parts of said carrier and/or the insulating pattern layer have been applied in a way that there will be no significant electrical connection and/or no short circuit between the electrical connection to the conducting electrode layer and the electrical connection to the substrate, either directly and/or through the electrolyte, except for in the electrolyte filled cavities defined by the insulating pattern layer and the substrate during ECPR etching or ECPR plating. For instance, insulating material is covering all conducting/semiconducting parts of the carrier except for in the cavities of the insulating pattern layer and in an electrical connection area.

[0151] In some embodiments, the master electrode is characterized by allowing for creating an electrical connection from an external electrical source to a substrate seed layer when the master electrode is put in contact with the substrate during ECPR etching or plating.

[0152] In some embodiments, at least some areas of said seed layer, which can be used for electrical contact, is not covered by the master electrode during physical contact with the substrate.

[0153] In some embodiments, an electrical contact to the substrate seed layer can be supplied by having a master electrode with an area that enters into physical contact with a larger substrate seed layer area.

[0154] FIG. 7(a) illustrates a cross section of a master electrode 8 with smaller area that enters into contact with a large substrate 17 seed layer 18 area.

[0155] FIG. 7(b) illustrates a top view of one embodiment of a master electrode with smaller area that enters into contact with a larger substrate seed layer 18 area.

[0156] In some embodiments, the master electrode and the substrate have the same dimensions and material has been removed from the master electrode in at least some areas in order to give place for an electrical connection to the seed layer on the substrate. In one embodiment, a recess is arranged in the perimeter of the master electrode which allows for a connection to the seed layer of the substrate.

[0157] FIG. 7(c) illustrates a cross section of a master electrode 8 with a recess 19 that allows for electrical connection to the substrate seed layer. Said recess can be present all around the circumference of the master electrode or in a few specific connection sites.

[0158] In some embodiments, connection holes 20 can be made through the master electrode 8 allowing for electrical...
connection to the seed layer 17 of the substrate 17. In one embodiment, the connection holes 20 are made adjacent the perimeter of the master electrode 8.

[0159] FIG. 7(d) illustrates a top view of the front-side of a master electrode 8 comprising an insulating pattern layer 7 and a conducting electrode layer 4, with connection holes 20 in the perimeter. In one embodiment, the connection holes 20 are made inside the master electrode 8 area, as illustrated in a top view in FIG. 7(e). Said recess and/or connection sites can be created by methods such as said lithographical and/or etching methods and/or with mechanical methods such as polishing, grinding, drilling, ablation, CNC-machining, ultra-sonic machining, diamond machining, waterjet machining, laser machining, (sand or fluid) blasting, and/or by combinations thereof. The recess and/or connection sites may be dimensioned to fit electrical contacts. An electrical contact can for instance be a thin foil, springs and/or other suitable electrical contacts and/or by a combination thereof. The electrical contact can comprise at least one layer of material that does not erode or oxidize during the ECPR etching and/or plating process and/or the electrolytes used therefore, for instance: stainless steel, Au, Ag, Cu, Pd, Pt, platinum titanium and/or by combinations thereof.

[0160] In some embodiments, the connection sites to the seed layer, provided by the master electrode design, are located in a way that it enables a uniform current distribution in the seed layer during ECPR etching and/or plating. For instance, a recess can be located along the perimeter of the master electrode which allows for a continuous electrical connection to the seed layer perimeter. In another embodiment, a number of (such as at least three) connection holes can be distributed evenly along the perimeter of the master electrode, which enables that a well distributed electrical connection can be achieved to the seed layer of the substrate.

[0161] In some embodiments, the parts of the master electrode that are conducting and connected to the conducting electrode layer and are located in contact with and/or in close proximity of the electrical connection to the seed layer, are coated with and insulating material in order to prevent a short circuit from the conducting electrode layer of the master electrode to the substrate seed layer during ECPR etching and/or ECPR plating.

[0162] In some embodiments, an electrical seed layer connection is an integrated part of the master electrode. In this case, the seed layer connection on the master electrode must be isolated from the conducting parts of the master electrode that are connected to the conducting electrode layer. Otherwise there could be a short circuit between the two electrodes when the master electrode is used for ECPR etching or plating. In some embodiments, the electrical connection to the conducting electrode layer of the master electrode is made in the center of the back-side of said carrier where the insulating coating of the carrier has been removed. In this case, the seed layer connection can be a conducting layer from the back-side perimeter to the front-side, separated from the conducting parts of the carrier by an insulating material. Said seed layer connection can comprise the same materials and can be applied with the same methods as used for said conducting electrode layer described above.

[0163] FIG. 7(f) illustrates a master electrode 8 comprising a conducting carrier, an insulating pattern layer 7 and a conducting electrode layer 4. Said insulating pattern layer is covering all areas of the conducting carrier except for in the cavities on the front side and in the center of the back-side, in which an electrical connection is enabled through a connection layer 5. Said seed layer connection 31 is provided on the perimeter on the back-side, the edge, and the perimeter on the front side of the master electrode. The seed layer connection 31 is isolated from the other conducting parts of the master electrode by the insulating pattern layer. An insulating layer may be arranged at the lateral sides of the seed layer connection.

[0164] FIG. 7(g) illustrates how the master electrode 8 comprising an insulating pattern layer 7, a conducting carrier 1, a conducting electrode layer 4, a connection layer 5 and a seed layer connection 31 is put in contact with a substrate 17 with a seed layer 18. An electrolyte 29 is enclosed in the electrochemical cells defined by the cavities between the insulating patter layer and the seed layer. An external electrical voltage source is connected to the connection layer 5 (said connection layer being electrically connected to said conducting electrode layer 4 through said carrier 1) and to the seed layer connection 31 (said seed layer connection being electrically connected to said seed layer) whereby an anode material, which is predeposited on said conducting electrode layer, which is anode, in the cavities of the insulating pattern layer, is dissolved and transported through said electrolyte and plated structures 24 are formed onto the seed layer, which is cathode, inside said electrochemical cells. By reversing the polarity of the electric voltage source, electrochemical etching of the seed layer takes place.

[0165] FIG. 7(h) illustrates how the seed layer connection 31 is arranged over a large surface of the pattern layer 7 and substantially over the entire surface, except adjacent the edges to the cavities of the pattern layer. The separate seed layer connection portions 31 shown in FIG. 7(h) are interconnected at other positions not shown in FIG. 7(h) because the surface of the pattern layer may form a continuous surface.

[0166] If the surface of the pattern layer does not form a continuous surface, the different portions 31 of the connection can be connected with connection areas at the backside of the carrier through the carrier as shown in FIG. 7(i). Otherwise, the seed layer contacted by the separate connection portions 31 may form a connection between the separate connection portions 31. The separate connection portions 31 can contribute to decreasing the resistance of the seed layer, especially at thin seed layers. Less resistance may have advantages as described further below.

[0167] In one embodiment of the invention, a master electrode comprising an at least partly conducting/semiconducting carrier, a conducting electrode layer, an insulating pattern layer and/or a predeposited anode material form at least one electrochemical cell together with a substrate which comprises a conducting seed layer. Said electrochemical cell comprises an electrolyte which is enclosed in the cavities of said insulating pattern layer and is in contact with said conducting electrode layer or predeposited anode material and said seed layer. The thickness and resistivity of said conducting parts of the carrier, said conducting electrode layer, said seed layer and/or said predeposited anode material are arranged so as to give a minimum current density difference between said electrochemical cells. For instance, said thicknesses and resistances can be arranged so as to give a difference in current density which is less than 50%, such as less than 20%, for instance less than 10%, such as less than 5%, for example less than about 1%.

[0168] For instance, due to the resistance in a thin seed layer there can be a resistive voltage drop, i.e. a potential
difference, between any points located on said seed layer. The conducting materials in the master electrode can be arranged so as to give a similar or comparable resistive voltage drop, i.e., potential difference, between corresponding points located on said master electrode.

In some embodiments, said conducting/semiconducting parts of the master electrode can comprise at least one layer of conducting/semiconducting material, where said at least one layer can have different thickness and/or resistivity in different areas. In one example, the thickness of said at least one conducting/semiconducting layer is greater in a point located at a shorter radial distance from the center of the master electrode compared to a point located at a longer radial distance from the center. In another example, the resistivity of said at least one layer is lower in a point located at a shorter radial distance from the center of the master electrode compared to a point located at a longer radial distance from the center. In yet another example, the specific conductivity of said at least one layer is greater in a point located at a shorter radial distance from the center of the master electrode compared to a point located at a longer radial distance from the center.

In some embodiments, the master electrode can comprise several points and/or areas that can be individually contacted with different external potentials. Different external potentials can be applied to points on said master electrode where said difference in applied external potential is equal to or similar to the potential difference in said seed layer between corresponding points, due to the resistive voltage drop in said seed layer.

In some embodiments, the potential difference and/or current density difference between electrochemical cells, can be calculated using mathematical modeling and/or can be measured in experiments.

In some embodiments, the specific conductivity of the conducting/semiconducting parts of said master electrode is equal to or greater than the specific conductivity of said seed layer. For instance, the sum of the specific conductivity of said conducting/semiconducting carrier, said conducting electrode layer and/or said predeposited anode material is equal to or greater than the specific conductivity of said seed layer, such as greater than 2 times, for example greater than 5 times, such as greater than 7 times, for instance greater than about 10 times.

In some embodiments, said master electrode has a circular geometry. For instance, the master electrode can have substantially the same dimensions as silicon wafers, for instance according to SEMITM-standards. For example, said master electrode can have the dimensions of a standard 100 mm, 150 mm, 200 mm, 300 mm or 450 mm diameter silicon wafer. Said substrate can have substantially the same circular shape and/or thickness as the master electrode.

In some embodiments, said master electrode is arranged so as to allow for electrical connection from an external power supply to the conducting electrode layer. The electrical connection area 33, see FIG. 19, can be located on the backside of the master electrode 8, for instance in contact with said carrier 1 which in turn can be in contact with said conducting electrode layer 4. There can be several electrical connection areas 33 located on the master electrode 8 and they can be separated from each other by an insulating material 32. The electrical connection areas 33 can for instance have the shapes of circulars, squares, rectangles, arcs, rings and/or segments thereof. In one embodiment, the master electrode 8 is arranged with a circular connection area 33 in the center of the back side and/or with at least one ring/arc shaped connection area 33 located on the back side at a distance between the center ring and the perimeter separated by an insulating material 32, as illustrated in FIGS. 19(a) and (b). In some embodiments, at least two ring- and/or arc-shaped connection areas are located between the center and the perimeter of the master electrode. The at least two ring- and/or arc-shaped connection areas can be uniformly spread out over the distance between the center and the perimeter. In other embodiments, the radial space between different contact areas can be less at a higher distance from the center. In some embodiments, the number of rings and/or arcs located between the center and the perimeter is at least 3, for instance at least 4, such as at least 5, for instance more than at least 8.

The connection areas can be arranged independently from each other and different external potentials can be applied separately to each connection area. In some embodiments, different external potentials are applied in different positions within at least one connection area. The connection from an external power supply can be supplied onto several positions within one connection area, for instance in order to allow for a uniform spreading of the current/potential.

In other embodiments, the same external potential can be applied to at least some of the different connection areas on the master. In one embodiment, all or substantially all connection areas, e.g., on the back side of the master electrode, are contacted with an external power supply with the same or substantially the same potential when predepositing an anode material onto said master, such as when the predeposition is done with electroluting methods. Said electroluting methods can be done with said ECPR etching methods from a seed layer and/or by standard electroluting methods.

In one example, a master electrode forms at least one electrochemical cell with a substrate; wherein said electrochemical cell for simplicity is assumed to cover all areas between said master electrode and substrate; and wherein said seed layer comprise a thin conducting layer with uniform thickness on a circular substrate with a 200 mm radius, wherein the specific conductivity of said seed layer is 5Ω⁻¹; said master electrode comprises a carrier, a conducting electrode layer and an insulating pattern layer; said master electrode having a the shape of disc with a 200 mm radius; wherein the sum of the specific conductivities of said carrier and conducting electrode layer is 25Ω⁻¹; an external voltage is applied to a point at the center of the back-side of said master electrode and to the entire perimeter of said seed layer; wherein at least one point in the electrochemical cell is located in the radial center of the master electrode and seed layer; and at least one point in the electrochemical cell is located in the radial perimeter of the master electrode and seed layer; wherein the electrical potential over the conducting electrode layer is as illustrated in FIG. 8(a), having a maximal potential difference of 6 mV; and wherein the electrical potential difference over the seed layer is as illustrated in FIG. 8(b) with a maximal potential difference of 5 mV; which results in that the current density in the center is 13.7 mA/mm² and the current density in the perimeter is 13.5 A/dm², as illustrated in FIG. 8(c). This particular example illustrates how the specific conductivity of the conducting parts of the master electrode has been matched to the seed layer so as to give the substantially the same current density in different points.
In a further example; wherein said specific conductivity of said seed layer is $5 \Omega^{-1}$ and the sum of the specific conductivity of said carrier and conducting electrode layer is $30 \Omega^{-1}$; wherein the electrical potential difference over the conducting electrode layer is as illustrated in FIG. 9(a); and wherein the electrical potential difference over the seed layer is as illustrated in FIG. 9(b); whereby the current density in the center is $13.7 \text{ A/dm}^2$ and the current density in the perimeter is $13.7 \text{ A/dm}^2$, as illustrated in FIG. 9(c). This particular example illustrates how the specific conductivity of the conducting parts of the master electrode has been matched to the seed layer so as to give the same current density in different points.

In a further example, said specific conductivity of said seed layer is $5 \Omega^{-1}$ and the specific conductivity of said carrier and conducting electrode layer is $100 \Omega^{-1}$; wherein the electrical potential difference over the seed layer is as shown in FIG. 10(a); whereby the current density in the center is about $13.7 \text{ A/dm}^2$ and the current density in the perimeter is about $14.4 \text{ A/dm}^2$, as illustrated in FIG. 10(b). This particular example illustrates when the specific conductivity of the conducting parts of the master electrode is more un-matched to the seed layer, which results in substantial differences in current densities in different points.

In the examples, the electrochemical cell has been assumed to be one cell covering the entire surface between said seed layer and master electrode, while in many embodiments there are several electrochemical cells which are separated by said insulating patter layer. For instance, the cell area may cover between 5 and 50% of the total seed layer and master electrode area, and they can be uniformly spread out over said master and seed layer surface. Furthermore, the results described in above examples can be similar to the results with multiple electrochemical cells.

As illustrated in the examples, the geometry and resistivity of the conducting layers of the master, which are being in electrical connection to said at least one electrochemical cell, can be chosen in relation to the geometry and specific conductivity of said seed layer so as to give the same or substantially the same potential drop over the conducting layers of the master electrode as over the seed layer; whereby the current densities in said electrochemical cells are the same or substantially the same.

Said potential drop and current density distribution can be described for any body (such as the master electrode and/or the seed layer) which can be described with x, y and z coordinates and any contacting points for applying an external voltage. The electrical potential distribution in the said body can be determined by a partial differential equation:

$$-\sigma (\nabla^2 \phi + V \nabla \phi) + V \phi = 0$$

wherein $\sigma$ is the electrical conductivity and $V$ is the electrical potential; and the boundary conditions are set either as a potential $V$ or as a current density $J$, for instance:

1. At the said contacting areas: a fixed electrical potential $V$; or a fixed current density $J$

2. At the surfaces which are interfacing said electrochemical cell: Current density $J$

wherein $J$ at any point in said electrochemical cell can be described by the Butler-Volmer equation $J = i_0 \exp(C^* (\eta))$, wherein $i_0$ is the exchange current density, $C$ is a constant which is depending on the electrochemical properties of said electrochemical cell and $\eta$ is the over-potential at a point located on said anode or cathode surface.

1. At electrically insulating surfaces: Current density $J = 0$.

In some embodiments, said differential equation can be solved by using calculations comprising numerical methods, such as methods for solving Ordinary-Differential-Equations (ODE), for instance Euler’s method, Taylor Series method or Runge-Kutta method; or methods for solving partial differential equations, such as Finite-Difference Method, Crank-Nicolson method or Elliptic PDE’s. In some embodiments, such numerical methods can be performed for a 2-dimensional system, for instance by using spherical coordinates. In other embodiments, such numerical methods can be performed for a 3-dimensional system. In yet further embodiments, such numerical methods can comprise the use of finite-element-methods.

In one embodiment, choosing geometry and specific conductivity of the conducting layers of the master electrode so as to match the geometry and resistance of the seed layer, can comprise measuring the potential distribution of said conducting layers and/or of said seed layer. Furthermore, one embodiment can comprise measuring the current density (i.e. plating/etching speed) distribution in said at least one electrochemical cell. For instance, measuring said current distribution can comprise measuring the thickness distribution of the structure layer formed in said at least one electrochemical cell, since the plating/etching speed has a linear dependence to the current density. In yet a further embodiment, an iterative method is used wherein the geometry and thickness of said conducting layers of the master electrode is modified after measuring the current density distribution in said at least one electrochemical cell; where after subsequent modifications and measurements of current density distribution are performed until the difference in current density between any points in said least one electrochemical cell are minimized.

As shown in FIGS. 20(a) and (b), the electrochemical cells have a polar distribution with a first contact portion of the master electrode in the center and a second contact portion of the seed layer along the perimeter, which may be circular. In this case, the resistance of the conducting layers will have an exponential relationship to the specific conductivity. Thus, the potential distribution over the seed layer will be exponential as shown in FIG. 8(b). In order to obtain a relatively uniform current density, the specific conductivity of the master electrode should be about 5 to 7 times the specific conductivity of the seed layer.

In another embodiment, the electrochemical cells may have a linear distribution with a first contact portion at one side of a rectangular master electrode and a second contact portion at an opposite side of a rectangular seed layer. In this case the potential distribution will be linear. In one embodiment, the specific conductivity of the master electrode may be substantially equal to the specific conductivity of the seed layer in order to obtain a substantially uniform current density in the electrochemical cells.

The specific conductivity of the master electrode is influenced by a number of factors, as appears from FIG. 7(b). The master electrode may comprise a disc 1 of a conducting semiconducting material. The disc may be made from several disc members of different materials. These materials together
form the specific conductivity of the disc. For example, the disc may be made of a semiconducting material such as silicon, doped at a predetermined rate, which determines the resistivity. The doping may be uniform or varying over the surface. The semiconducting material may be provided with a further layer of a conducting material, such as platinum or gold for further adapting the specific conductivity. The disc may have a constant thickness or varying thickness.

[0192] The conducting and/or semiconducting disc may be provided with a conducting electrode layer 4, which is only positioned at the bottom of the cavities, as illustrated in FIG. 7(h). Since this material often is thin in comparison to the disc, it will only contribute to the specific conductivity to a small extent. Finally, predeposited anode material may be arranged on to of the conducting electrode layer 4. Also this anode material will contribute to the specific conductivity to some extent depending on the thickness and the cell density. The specific conductivity being higher with thick anode material and higher cell density. In one embodiment, these materials can be tailored to provide different lengths of the electrochemical cells, in order to induce different current densities. For example, if the cavity is 25 µm in height, the material 4 can have a height of 1 µm in one cavity and 20 µm in another cavity, thereby influencing upon the current passing through the electrochemical cell. This being significant if the conductivity of the electrolyte in the electrochemical cells is low or if the current density is high so that the electrochemical etching/plating process is mass transport limited, such as when being close to the limiting current.

[0193] As appears from FIG. 7(h), the material 31, which will enter into contact with the seed layer during an etching/plating process, will aid in increasing the specific conductivity of the seed layer, thereby making the current distribution more uniform.

[0194] All these factors can be used in combination to provide the desired end result. In addition, different potentials can be added to different portions of the master electrode and to the substrate as mentioned above.

[0195] In some embodiments, during the fabrication of the master electrode 8, the electrical specific conductivity of the conducting/semitcconducting parts of the carrier 1 and the conducting electrode layer 4 may be matched to the specific conductivity of the seed layer 17 on a substrate 17, which is only the resistance and thickness of the conducting electrode layer 4 that needs to be matched with the seed layer 18.

[0201] In some embodiments, the carrier 1 and the conducting electrode layer 4 of the master electrode 8 are characterized in that a current supplied during ECPR etching and/or plating will experience the same total resistance when passing through the carrier 1, conducting electrode layer 4 and the seed layer 18, independently on in which area it passes the electrochemical cells 23. In some embodiments, this is done by supplying an electrical contact from an external power supply only to the center of the back-side of the carrier 1 and to the perimeter of the seed layer 18 on the substrate 17. In this case, if the total electrical resistance for a current passing from the center of the back-side of the carrier 1, through the said carrier, conducting electrode layer 4 and the seed layer 18 to the electrical contacts at the perimeter is the same independent on in which area it passes through the electrochemical cells 23, the current density that passes during ECPR etching and/or plating will be the same independent on the location of the electrochemical cells with respect to the seed layer electrical contacts. Thereby, the etching and/or plating rate, which is linearly proportional to the current density, will be the same in all electrochemical cells 23, independent on the location. The described master electrode/seed layer resistance matching reduces a problem of radial dependent non-uniform etching/plating rates, resulting in non-uniform radial height distribution, inherently associated with conventional electrodeposition/electrochemical etching methods, said problems being described as the terminal effect.

[0202] In some embodiments, such as at thin seed layer, the total resistance of the carrier 1 and conducting electrode layer 4 is lower than the resistance of the seed layer 18, causing the current density to become higher in the electrochemical cells 23 that are located closer to the perimeter than in the center of the substrate and master electrode when performing ECPR etching and/or plating. In other embodiments, such as at thick seed layer, the total resistance of the carrier 1 and conducting electrode layer 4 is higher than the seed layer 18, causing the current density to become lower in the electrochemical cells 23 that are located closer to the perimeter than in the center of the substrate 17 and master electrode 8 when performing ECPR etching and/or ECPR plating.

[0203] For instance, a resistance R of the path to and from the electrochemical cells 23 in the center can be matched to the resistance R of the path to and from the electrochemical cells in the perimeter, illustrated in FIG. 12, so that:

1. if R = 1/(R + R) + R, then j = j; or
2. if R > 1/(R + R) + R, then j > j; or
3. if R < 1/(R + R) + R, then j < j.

where j is the current density in the electrochemical cells in the center and j is the current density in the electrochemical cells in the perimeter.

[0208] By matching the resistances Rₕ and Rₜ to Rₜ in different ways, a specific height distribution of ECPR etched or plated structures along a radial direction from the center to the perimeter of the master electrode can be achieved.

[0209] In some embodiments, the conducting parts (for instance a conducting/semitcconducting disc) of the carrier 1 is only connected to the conducting electrode layer 4 in the center on the front-side due to an insulating material coating 3 as illustrated in FIG. 1(a). In this case, it is only the resistivity and thickness of the conducting electrode layer 4 that needs to be matched with a seed layer 18.
In some embodiments, a radial depending height distribution of ECPR etched or plated structures can be used to compensate a different height distribution that comes from a previous or subsequent process step. In one embodiment, the resistance in the master is matched to a seed layer 18, which is applied with a uniform thickness (for instance by PVD) onto a substrate 17 with a concave layer 25 illustrated in FIG. 13(a), so that 1/R = 1/R = 1/R, and ECPR etched or plated structures 24 is fabricated with a convex radial height distribution that compensates for the concave layer so that the top of said ECPR etched or plated structures 24 end up at the same height h from the substrate, as illustrated on FIG. 13(b).

In another embodiment, the resistance in the master is matched to a seed layer 18, which is applied with a uniform thickness (for instance by PVD) onto a substrate 17 with a convex layer 26 illustrated in FIG. 14(a), so that 1/R = 1/R = 1/R, and ECPR etched or plated structures 24 is fabricated with a concave radial height distribution that compensates for the convex layer so that the top of said ECPR etched or plated structures 24 end up at the same height h from the substrate, as illustrated on FIG. 14(b).

In order to achieve certain plating or etching effects, the master electrode may be arranged with a disc and electrode layer having different thicknesses from the central and/or having different materials from the central; said different materials having different specific conductivity. For example, the thickness may be halved or alternatively the resistivity may be doubled at half the radial distance from the center.

In some embodiments, the master electrode is arranged using methods that result in very uniform height distribution of ECPR etched or plated structure layers. However, in some other embodiment, at least some portion of the carrier and/or conducting electrode layer can be altered in the cavities of an insulating pattern layer in order to give a non-uniform pattern in a portion of said structure layer. In one embodiment, the carrier 1 of a master electrode 8 can have a recess in at least one cavity of an insulating pattern layer 7; said recess being coated on the walls with a conducting electrode layer 4, and a predesposited anode material 28 is arranged onto said conducting electrode layer, as illustrated in FIG. 21(a). During ECPR plating on a substrate 17 inside said cavities with said recesses, the areas located closer to the walls of the insulating pattern layer 7 will achieve a higher current density (plating rate) resulting in a larger height of the ECPR plated structures 24, as illustrated in FIG. 21(b).

In another embodiment, the carrier 1 and the conducting electrode layer 4 exert a protruding structure in at least one cavity of an insulating pattern layer 7; and a predesposited anode material 28 is arranged onto said conducting electrode layer, as illustrated in FIG. 22(a). During ECPR plating on a substrate 17 inside said cavities with protruding structures, the areas on the substrate located closer to the protruding structure will achieve a higher current density (plating rate) resulting in a larger height of the ECPR plated structures 24, as illustrated in FIG. 22(b). In some case, the embodiments for creating structure layers with a non-uniform height such as in FIG. 21(b) and FIG. 22(b) can be used for applications such as interlocking bump structures, solder ball placement foundations or mechanical alignment structures/fiducials.

Herein above, several features and method steps have been described in different combinations and constellations. However, it is emphasized that other combinations may be performed as occur to a skilled person reading this specification, and such combinations are within the scope of the present invention. Moreover, the different steps can be modified or altered still within the scope of the invention. The invention is only limited by the appended patent claims.

1-57. (canceled)

58. A system comprising a master electrode arranged on a substrate, said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; said substrate comprising a top surface in contact with or arranged adjacent said first surface and having conducting material and/or structures of a conducting material arranged thereon, said substrate conducting material being electrically connected to at least one current supply contact; whereby a plurality of electrochemical cells are formed delimited by said cavities, said substrate conducting material and said electrode conducting material, said cells comprising an electrolyte; characterized in that an electrode resistance between said electrode conducting material and said electrode current supply contact and a substrate resistance between said substrate conducting material and said substrate current supply contact are adapted, such that a specific conductivity of the electrode conducting material in average is from 0.1 to 100 times a specific conductivity of the substrate conducting material.

59. The system of claim 58, wherein the specific conductivity of the electrode conducting material in average is from 0.5 to 20 times the specific conductivity of the substrate conducting material.

60. The system of claim 58, wherein the specific conductivity of the electrode conducting material in average is from 1 to 10 times the specific conductivity of the substrate conducting material.

61. The system of claim 58, wherein the specific conductivity of the electrode conducting material in average is 1 to 7 times the specific conductivity of the substrate conducting material.

62. The system of claim 58, wherein said specific conductivity is arranged varying over the surface of the master electrode.

63. The system of claim 62, wherein the specific conductivity is arranged by changing the thickness of the material.

64. The system of any one of claims 62 and 63, wherein said specific conductivity is arranged by changing the resistivity of the material.

65. The system of claim 64, wherein said material is a doped semiconductor material having a doping which is arranged varying for providing said resistivity.

66. The system of claim 58, wherein said electrode conducting material comprises a disc having substantially the same extent as said first surface.

67. The system of claim 66, wherein said disc is made of a conducting and/or semi-conducting material.
68. The system of claim 58, wherein said electrode conducting material comprises cavity conducting material arranged in the bottom of each cavity.

69. The system of claim 68, wherein said cavity conducting material is a material arranged in the bottom of said cavity and being of an inert material.

70. The system of claim 69, wherein said cavity conducting material is a further material which is predeposited in said cavity and at least partly consumed during a plating process.

71. The system of any one of claims 68, 69, and 70, wherein said cavity conducting material is in electric contact with said disc.

72. The system of any one of claims 68, 69, and 70, wherein said disc has substantially constant thickness.

73. The system of claim 66, wherein said disc comprises a plurality of disc members having different specific conductivities, said disc members being arranged on top of each other.

74. The system of claim 66, wherein said electrode supply contact is arranged in the middle of said disc.

75. The system of claim 66, wherein said electrode supply contact comprises several discrete contacts.

76. The system of claim 75, wherein said discrete contacts comprise at least one ring contact or ring segment contact arranged at a radius from a center of the disc.

77. The system of claim 75, wherein each discrete contact is provided with a specific potential during a plating or etching process.

78. The system of claim 66, wherein said disc is substantially circular.

79. The system of claim 73, wherein the thicknesses of at least one of said disc members change with the distance to the center of the disc.

80. The system of claim 58, wherein said substrate resistance is at least partly provided by a seed layer arranged on at least a part of the substrate top surface.

81. The system of claim 80, wherein said substrate electrode contact is arranged at least a part of a perimeter of said substrate seed layer.

82. The system of claim 80, wherein said substrate electrode contact is arranged along a perimeter of said substrate seed layer.

83. The system of any one of claims 80, 81, and 82, wherein said substrate electrode contact comprises several discrete contacts.

84. The system of claim 83, wherein each discrete contact is supplied with a specific potential during a plating or etching process.

85. The system of claim 80, wherein said master electrode comprises at least one contact area for contact with said seed layer for providing current to said seed layer.

86. The system of claim 80, wherein said pattern layer comprises at least one area of conducting material arranged in said first surface in portions between said cavities for being in contact with said substrate conducting material during a plating or etching process for increasing the specific conductivity of said substrate conducting material over said areas.

87. The system of claim 58, wherein said adaptation is performed if the potential difference over the surface of said electrode conducting material and/or over the surface of said substrate conducting material is significant, so that the current density difference in said electrochemical cells between said surfaces is more than 1%, such as more than 2%.

88. The system of claim 87, wherein said adaptation results in that the specific conductivity of the electrode conducting material in average is between 0.1 to 100 times, such as between 0.5 to 20 times, for example 1 to 10 times, such as about 1 to 7 times the specific conductivity of said substrate conducting material.

89. The system of claim 58, wherein each cavity is provided with a material having a thickness which is specific for each cavity.

90. A master electrode intended to be arranged on a substrate,

said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact;

whereby a plurality of electrochemical cells are intended to be formed delimiting said cavities, said electrode conducting material and a substrate;

characterized in that

an electrode resistance between said electrode conducting material and said electrode current supply contact is adapted in relation to an intended substrate conducting material, such that a specific conductivity of the electrode conducting material in average is from 0.1 to 100 times a specific conductivity of the substrate conducting material.

91. The master electrode of claim 90, wherein the specific conductivity of the electrode conducting material in average is from 0.5 to 20 times the specific conductivity of the substrate conducting material.

92. The master electrode of claim 90, wherein the specific conductivity of the electrode conducting material is from 1 to 10 times the specific conductivity of the substrate conducting material.

93. The master electrode of claim 90, wherein the specific conductivity of the electrode conducting material is from 1 to 7 times the specific conductivity of the substrate conducting material.

94. The master electrode of any one of claims 90 and 91, wherein said specific conductivity is arranged varying over the surface of the master electrode.

95. The master electrode of claim 94, wherein the specific conductivity is arranged varying by changing the thickness of the material.

96. The master electrode of claim 94, wherein said specific conductivity is arranged varying by changing the resistivity of the material.

97. The master electrode of claim 94, wherein said material is a doped semiconductor material having a doping which is arranged varying for providing said varying resistivity.

98. The master electrode of claim 90, wherein said electrode conducting material comprises a disc having substantially the same extent as said first surface.

99. The master electrode of claim 98, wherein said disc is made of a conducting and/or semi-conducting material.

100. The master electrode of claim 80, wherein said electrode conducting material comprises cavity conducting material arranged in the bottom of each cavity.

101. The master electrode of claim 100, wherein said cavity conducting material is a material arranged in the bottom of said cavity and being of an inert material.
102. The master electrode of any one of claims 100 and 101, wherein said cavity conducting material is a further material which is predeposited in said cavity and at least partly consumed during a plating process.

103. The master electrode of claim 100, wherein said cavity conducting material is in electric contact with said disc.

104. The master electrode of claim 98, wherein said disc has substantially constant thickness.

105. The master electrode of claim 98, wherein said disc comprises a plurality of disc members having different specific conductivities, said disc members being arranged on top of each other.

106. The master electrode of claim 98, wherein said electrode supply contact is arranged in the center of said disc.

107. The master electrode of claim 98, wherein said electrode supply contact comprises several discrete contacts.

108. The master electrode of any one of claims 107 and 108, wherein each discrete contact is provided with a specific potential during a plating or etching process.

109. The master electrode of claim 98, wherein said disc is substantially circular.

110. The master electrode of claim 105, wherein the thicknesses of at least one of said disc members changes with the distance to the center of the disc.

111. The master electrode of claim 93, wherein each cavity is provided with a material having a thickness which is specific for each cavity.

112. A method of predeposition of material in cavities of a master electrode having a pattern layer comprising an insulating material, in which said cavities are formed, and a conducting electrode layer formed on a bottom of said cavities, said conducting electrode layer having contact portions for external connection to an electric power source, the method comprising:

arranging a contact member at a support;
arranging said master electrode on said contact member for obtaining electrical contact between the contact member and said conducting electrode layer in at least two contact portions;
arranging an electroplating anode of a material to be deposited in said cavities on said master electrode, whereby electrochemical cells are formed delimited by said cavities, said substrate conducting electrode layer and said electroplating anode, whereby said cells comprise an electrolyte;
connecting an electric power source to said contact member and said electroplating anode for passing a current through said electrochemical cells for transferring material from said anode to said conducting electrode layer, which is cathode, in order to deposit said material in the cavities on top of said conducting electrode layer.

114. A method of performing etching or plating of a substrate by means of a master electrode, said master electrode comprising a pattern layer, at least partly of an insulating material and having a first surface provided with a plurality of cavities in which a conducting material is arranged, said electrode conducting material being electrically connected to at least one electrode current supply contact; the method comprising:

arranging said master electrode on a support;
supplying an electrolyte to the cavities;
arranging a substrate on said master electrode, said substrate comprising a top surface having conducting material and/or structures of a conducting material arranged thereon, said substrate conducting material being electrically connected to at least one current supply contact, whereby electrochemical cells are formed delimited by said cavities, said substrate conducting electrode layer and said electrode conducting material, whereby said cells comprise an electrolyte;
connecting an electric power source to said electrode current supply contact and said substrate current supply contact for passing a current through said electrochemical cells for transferring material between said master electrode and said substrate;
characterized by adapting an electrode resistance between said electrode conducting material and said electrode current supply contact and a substrate resistance between said substrate conducting material and said substrate current supply contact.

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