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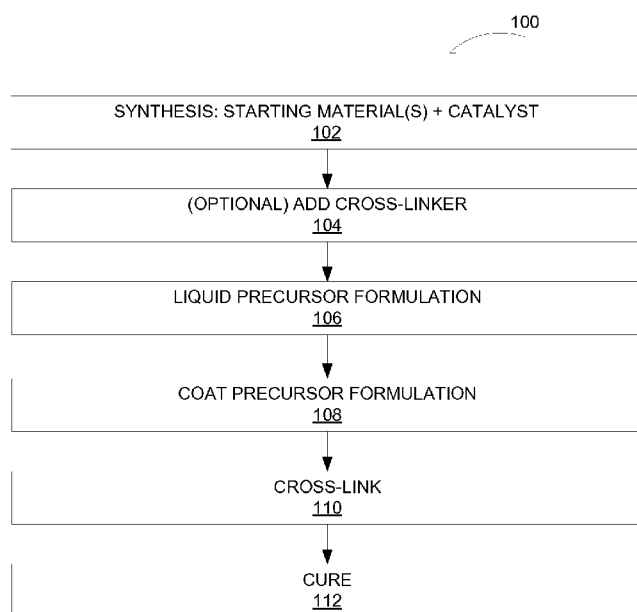
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- (54) **Title:** LIQUID PRECURSOR BASED DIELECTRICS WITH CONTROL OF CARBON, OXYGEN AND SILICON COMPOSITION

**FIG. 1**

(57) **Abstract:** Several classes of dielectric materials formed by coating techniques involving cross-linking of liquid precursors into solid dielectric materials are disclosed. Various liquid precursors are made by similar processing involving action of a tris(pentafluorophenyl)borane catalyst with a compound containing multiple Si-H bonds and either the same or a different compound containing multiple Si-X bonds, e.g. Si-O-SiR, Si-OCH₂CH₃, Si-OCH₃ and other alkoxysilanes; or Si-allyl, Si-vinyl, Si-alkynyl and other silanes with unsaturated C-C bonds. Controlling the amount and the nature of cross-linking agents being used, the ratio of Si-H to Si-X bonds, conditions of preparing the liquid precursors, and/or cross-linking process following coating of liquid precursors onto substrates allows controlling carbon (C), oxygen (O), and silicon (Si) composition of the resulting solid dielectric materials, thereby fine-tuning the properties of such materials. Dielectric materials spanning compositions from carbosilanes and carbosiloxanes to silicon dioxides may be formed in this manner.

LIQUID PRECURSOR BASED DIELECTRICS WITH CONTROL OF CARBON, OXYGEN AND SILICON COMPOSITION

Technical Field

[0001] This disclosure relates generally to the field of integrated circuits and semiconductor manufacturing, and more specifically, to fabricating dielectric materials spanning compositions from carbosilanes and carbosiloxanes to silicon dioxide using coating of liquid precursors.

Background

[0002] For the past several decades, the scaling of features in integrated circuits (ICs) has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor IC chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity.

[0003] IC chips are used in a variety of devices including automobiles, computers, appliances, mobile phones and consumer electronics. A plurality of IC chips can typically be formed on a single silicon wafer, i.e. a silicon disk having a diameter of, for example, 300 millimeters (mm), which is then diced apart to create individual chips. IC chips can include features sizes on the nanometer scale and can comprise hundreds of millions of components. Improved materials and manufacturing techniques have reduced features sizes to, for example, less than 45 nanometers (nm).

[0004] The drive for the ever-increasing capacity, however, is not without issue. The desire to make smaller IC chips continuously places demands on the methods and materials used to manufacture these devices. In particular, there is a need for fabricating structures with dielectric materials that can be fine-tuned to possess various complex properties that could be required in using advanced patterning schemes. Some properties may include smooth film formation, low shrinkage and outgassing, good dielectric properties (such as e.g. low electrical leakage, suitable value of a dielectric constant, and thermal stability), and etching

characteristics sufficiently distinct from commonly used dielectrics such as e.g. silicon nitride (Si_3N_4). Still further properties include ability to fabricate the materials using coating techniques and ability to fill the materials in high aspect ratio features.

Brief Description of the Drawings

[0005] FIG. 1 provides a schematic flow chart illustrating a process of forming a dielectric material from a liquid precursor formulation made using a BCF catalyst, according to some embodiments of the present disclosure.

[0006] FIG. 2 provides chemical structures illustrating precursor synthesis via hydrosilation using tetraallylsilane cross-linker, according to some embodiments of the present disclosure.

[0007] FIG. 3 provides chemical structures illustrating precursor synthesis via hydrosilation using single-source precursor, according to some embodiments of the present disclosure.

[0008] FIGs. 4a-4h provides chemical structures illustrating various cross-linking agents and single-source precursors, according to various embodiments of the present disclosure.

[0009] FIG. 5 provides chemical structures illustrating precursor synthesis for forming SiO_2 -rich dielectric materials, according to some embodiments of the present disclosure.

[0010] FIGs. 6a and 6b provide chemical structures illustrating precursor synthesis via dehalocoupling of a trisilacyclohexane precursor, without and with the use of a comonomer to tune SiC content, according to some embodiments of the present disclosure.

[0011] FIG. 7 illustrates an exemplary structure comprising openings filled with one or more dielectric materials as described herein, according to some embodiments of the present disclosure.

[0012] FIG. 8 provides a schematic illustration of an interposer, according to some embodiments of the present disclosure.

[0013] FIG. 9 provides a schematic illustration of a computing device built in accordance with some embodiments of the present disclosure.

Detailed Description

[0014] Several classes of dielectric materials formed by coating techniques involving cross-linking of liquid precursors into solid dielectric materials are disclosed. Various liquid precursors are made by similar processing involving action of a tris(pentafluorophenyl)borane catalyst with a compound containing multiple Si-H bonds and either the same or a different compound containing multiple Si-X bonds, e.g. Si-O-SiR, Si-OCH₂CH₃, Si-OCH₃ and other alkoxy silanes; or Si-allyl, Si-vinyl, Si-alkynyl and other silanes with unsaturated C-C bonds. Controlling the amount and the nature of cross-linking agents being used, the ratio of Si-H to Si-X bonds, conditions of preparing the liquid precursors, and/or cross-linking process following coating of liquid precursors onto substrates allows controlling carbon (C), oxygen (O), and silicon (Si) composition of the resulting solid dielectric materials, thereby fine-tuning the properties of such materials. Dielectric materials spanning compositions from carbosilanes and carbosiloxanes to silicon dioxides may be formed in this manner.

[0015] In some embodiments, the dielectric material may comprise cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly via Si-Si bonding or via a C-containing link.

[0016] In some embodiments, the dielectric material may comprise cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units via a C-containing link in the form of -CH₂CH₂CH₂-.

[0017] In some embodiments, the dielectric material may comprise a mixture of cyclic carbosilane units having a ring structure including C and Si and tetrahedral (SiO₄) units connected to at least some of the cyclic carbosilane units or/and other tetrahedral units, the dielectric material further comprising a plurality of non-linked vacancies occupied by one or more of H, OH, CH₃, CH₂CH₃, or tBu (where "Bu" indicates butyl (CH₃CH₂CH₂CH₂), and "tBu" indicates tertiary, or tert-, butyl). As used herein, "non-linked vacancy" refers to a functional group which does not directly participate in cross-links.

[0018] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0019] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0020] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0021] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of

group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0022] In various embodiments, the interconnects as described herein may be used to connect various components associated with an integrated circuit. Components include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an integrated circuit may include those that are mounted on an integrated circuit or those connected to an integrated circuit. The integrated circuit may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a computer.

[0023] In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0024] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc.

Examples of high-k materials that may be used in the gate interconnect support layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0025] The gate electrode layer is formed on the gate interconnect support layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0026] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0027] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and

does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0028] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0029] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0030] One or more interlayer dielectrics may be deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0031] In general, a low-k dielectric material is a dielectric material that has a lower dielectric constant (k) than silicon dioxide (SiO_2). Silicon dioxide has a dielectric constant of 3.9. The use of dielectric materials in integrated circuit devices has enabled continued device size reduction. Although a variety of materials have lower dielectric constants than SiO_2 not all materials are suitable for integration into integrated circuits and integrated circuit manufacturing processes. Embodiments of the present disclosure are particularly suitable for forming low-k dielectric materials with k being less than 3.9. However, teachings provided herein are also applicable to dielectric materials with k higher than that of SiO_2 , e.g. to carbosilane-based dielectric materials having k that is in the range of 3.9-4.1. Materials with a k-value higher than 3.9 are useful for a number of applications, specifically ones where the higher k material would also bring unusual properties such as e.g. different etch rate relative to SiO_2 , allowing the material to be uniquely etched in a given etch chemistry/condition.

[0032] In general, an interlayer dielectric (ILD) or inter metal dielectric (IMD) film is the insulating material used between metal conductors and devices (such as transistors) in integrated circuit devices.

[0033] To provide context, conventionally, fabrication techniques used for integrating advanced interconnects require dielectric materials with unique compositions. Preferably, such dielectric materials can be formed from liquid precursors using coating techniques, such as e.g. spin-coating, chemical vapor deposition (CVD), or similar techniques. After a liquid precursor formulation is coated on a substrate, precursor cross-links to form a solid dielectric material.

[0034] As used herein, the term “spin-on dielectric material” and variations thereof is used to describe dielectric materials formed using liquid precursors applied to a substrate using any one of known coating techniques including, but not limited to e.g. spin-coating, CVD, or other similar coating techniques.

[0035] Precursor formulations currently available from different vendors are limited and do not satisfy all of the requirements which may be placed on dielectric materials to be used in a particular manufacturing setting. Furthermore, these precursor formulations do not readily allow for compositional tuning, e.g. with respect to control of carbon, oxygen and silicon composition of the final dielectric materials.

[0036] To improve on one or more of these issues, some embodiments of the present disclosure provide improved fabrication techniques for forming different classes of dielectric materials with careful control of carbon, oxygen and silicon composition. Improved fabrication techniques described herein allow creating a spectrum of spin-on dielectric materials spanning different carbon, oxygen, and silicon compositions from carbosilanes and carbosilaxanes to silicon dioxides where synthetic and processing methods can be rationally controlled to ensure desired final properties of the dielectric materials. In some embodiments, simplicity of the synthetic method where minimal byproducts are created allows for precursor formulations to be created “at-the-tool” immediately prior to coating, leading to improved stability, reduced waste (and, hence, lower cost), and maximum tenability.

[0037] Various liquid precursors disclosed herein are made by similar processing involving action of a catalyst such as e.g. tris(pentafluorophenyl)borane ($B(C_6F_5)_3$, commonly referred to as “BCF”) with a molecule containing multiple Si-H bonds and another or the same molecule containing multiple Si-OEt, Si-allyl, or other functionalities, depending on the desired cross-linking that fine-tunes final properties of the dielectric materials. Based on the ratio of Si-H to Si-X and other factors described herein, the molecular weight and remaining reactive functionality of the resulting dielectric material may be controlled. Similar coating and processing steps may then be utilized to create final solid dielectric films where unreacted Si-H and/or Si-X bonds are utilized for increased cross-linking and setting of the film.

[0038] FIG. 1 provides a schematic flow chart 100 illustrating a process of forming a dielectric material from a liquid precursor formulation made using a BCF catalyst, according to some embodiments of the present disclosure. First, the process is described in general terms, with reference to boxes 102-112 shown in FIG. 1, followed by descriptions of various examples illustrating various exemplary precursor synthesis approaches (boxes 102 and 104) leading to creation of dielectric materials with various C, O, and Si compositions.

[0039] As shown with box 102 in FIG. 1, precursor synthesis starts with one or more starting materials containing multiple Si-H bonds combined with a BCF catalyst. Presence of the catalyst initiates or/and assists cross-linking of the starting materials to create higher molecular weight oligomers and/or polymers of the precursor. As shown with box 104 in FIG. 1, in some embodiments, precursor synthesis may optionally include adding one or more cross-linkers, i.e. compounds that ensure cross-linking of the starting materials via predefined functional groups. Cross-linkers can contain various types of cross-linking groups depending on the properties required for the resulting dielectric material. For example, for introduction of oxygen crosslinks, ethoxysilanes, ethers and alcohols can be used; for introduction of carbon crosslinks, multifunctional allyl, vinyl, alkynyl and other unsaturated derivatives can be used. The ratio of Si-H and coreactant (ie Si-OEt, Si-allyl etc) can be fine-tuned to achieve desired properties of the solid dielectric film.

[0040] Next, precursor oligomers/polymers that were created in box 102, with the optional involvement of box 104, are dissolved in one or more solvents, thus forming a chemical formulation that can be used as a liquid precursor for forming solid dielectric materials (box 106 in FIG. 1). In some embodiments, solvents such as toluene, cyclohexanone, 2-heptanone, or propyleneglycol monomethyl ether acetate may be used. In general, any common solvents used for spin-coating or CVD may be used.

[0041] Properties such as the average molecular weight of the precursor oligomers/polymers can be pre-determined by controlling reaction conditions such as concentration of components (including starting materials and the catalyst), time of addition, solvent or co-solvents, and temperature. Molecular weights may be selected to improve the applicability of the precursor when spun onto a structure with a plurality of openings, e.g. on a substrate/wafer. In some embodiments, two, three, four or more

different precursor oligomers/polymers may be physically mixed together to form desired liquid precursor formulation. These precursor oligomers/polymers may differ, for example, with regard to their molecule structure, average molecular weight, molecular weight distribution, atomic percent C, atomic percent O, atomic percent Si, atomic percent H, any ratios between C, O, Si, and H, amount of branching, capping species, porogen content, etc.

[0042] In some embodiments, the organic solvent, any unreacted starting molecules, and low molecular weight precursor oligomers/polymers can be removed in a rotary evaporator or a similar apparatus. Remaining high molecular weight oligomers/polymers can be re-dissolved into new solvents, e.g. 2-heptanone. At this point, a new solvent than the one used in the precursor oligomer/polymer synthesis of boxes 102 and 104 may be used. However, use of new solvents other than that used for reaction synthesis could have manufacturing, environmental health and safety (EHS), and fillability implications. Whether the rotary evaporator is used for solvent exchange or not, in box 106 the precursor oligomers/polymers may then be diluted to target concentrations for coating. The dilution tunes the thickness of the film that results after coating. For example, in case of filling the dielectric material into nanostructures of a substrate, the dilution can be tuned for incomplete fill, nearly complete fill, or complete fill with various amounts of overburden (i.e. when not only all of the openings are filled, but also there is a layer of thin film over the structure). The dilution may depend on the aspect ratio of the features that need to be filled.

[0043] Turning back to FIG. 1, as shown with box 108, liquid precursor formulation of box 106 may then be coated onto a substrate, with could comprise either a substantially planar substrate on which dielectric film in bulk/blanket form will be formed or a patterned wafer or any structure with openings that need to be filled with the dielectric material. Precursor coating can happen by e.g. dispensing and spin coating of the precursor formulation described above using industry standard spin tracks. For example, in some embodiments, spin coating the precursor onto the substrate may include spin coating for 1-60 seconds, including all values and ranges therein, at 500-6000 rotations per minute (rpm), including all values and ranges therein.

[0044] In other embodiments, precursor may be provided on the substrate in box 108 by means other than spin coating, such as e.g. dipcoating, dropcasting, solution immersion, and flowable chemical vapor deposition (CVD) methods.

[0045] Concepts described herein are applicable to both providing dielectric materials on a substrate in a bulk or blanket form (i.e. where the dielectric material is provided as a layer, e.g. as a thin film, over a surface) as well as for filling patterned features of a substrate. Expression “on/in a substrate” in context of providing a precursor formulation and/or the dielectric material on/in a substrate is indicative of this fact. In this context, providing a precursor formulation or the dielectric material “on” a substrate refers to dielectric material being in a bulk or blanket form, while providing a precursor formulation or the dielectric material “in” a substrate refers to dielectric material being provided within patterned features of a substrate. In the following, “dielectric film” may refer to both dielectric material disposed in a bulk/blanket form and dielectric material filling patterned features.

[0046] In the embodiments where patterned features of a substrate are filled with dielectric materials as described herein, a substrate may include a plurality of openings, and a dielectric material is disposed within the plurality of openings. The plurality of openings may include openings, holes, or gaps (referred to herein as simply “openings”) of various aspect ratios, where, as used herein, “aspect ratio” refers to a ratio between a height or a depth of an opening to a width of an opening. In various embodiments, openings referred to herein may have aspect ratios between 1 and 20, including all values and ranges therein, e.g. between 1 and 15, between 5 and 10, etc. Preferably, dimensions of the openings are on the nanometer scale, e.g. with a width of an opening being about 20 nm and a depth of an opening being about 100 nm, i.e. aspect ratio of 5. Therefore, such structures with openings are sometimes described as nanostructures or nanopatterned structures.

[0047] In various embodiments, nanostructures with dielectric materials as described herein could be a part of a semiconductor device or an IP package, e.g. a part of an interconnect, e.g. a backend interconnect, used for providing electrical conductivity in the semiconductor device or the IC package. As used herein, the term “backend interconnect” is used to describe a region of an IC chip containing wiring between transistors and other elements, while the term “frontend interconnect” is used to describe a region of an IC chip

containing the rest of the wiring. Nanostructures described herein may be used in any devices or assemblies where one electrically conductive element of the wiring needs to be separated from another electrically conductive element, which could be done both in backend and frontend interconnects. Such devices or assemblies would typically provide an electronic component, such as e.g. a transistor, a die, a sensor, a processing device, or a memory device, and an interconnect for providing electrical connectivity to the component. The interconnect includes a plurality of conductive regions, e.g. trenches and vias filled with electrically conductive materials as known in the art. The plurality of openings filled with dielectric materials as described herein could be used to electrically isolate at least some of the conductive regions from one another. For example, the structure in which the openings are made could be made of a conductive material.

[0048] As a result of coating the precursor formulation on/in a substrate in box 108, an unreacted precursor material is provided on the substrate. In this context, “unreacted” refers to the fact that the precursor oligomers/polymers are not yet cross-linked into a solid dielectric material. Next, excitation, such as e.g. thermal or/and optical excitation, is applied to cross-link the precursor coated on the substrate into a solid dielectric material (box 110). After that, optionally but preferably, a curing step is applied (box 112) to further cross-link, harden, and/or outgas the solid dielectric material. For the cross-linking of box 110, typically a low temperature bake or photochemical activation is used, while for the curing of box 112, typically high temperature bake or ultraviolet (UV) cure is used.

[0049] In various embodiments, the cross-linking of box 110 can be facilitated, for example, by heat, radiation, a chemical catalyst, or any other excitation means that activate cross-linking, or a combination of various means. Furthermore, cross-linking may be preceded by baking the substrate with coated precursor at 303 to 673 degrees Celsius for 30 seconds to 30 minutes (a process sometimes referred to as “soft-baking”), in order to get rid of solvents and low molecular weight components.

[0050] In case of heat-assisted cross-linking in box 110, in some embodiments, the substrate with coated precursor may be baked at higher temperatures, e.g. at 573 to 773 degrees Celsius (a process sometimes referred to as “hard-baking”). Hard-baking may be

carried out under nitrogen or under a reactive gas such as e.g. ammonia, hydrogen, oxygen, diborane, or disilane.

[0051] The crosslinking of box 110 brings mechanical stability such as stiffness (high Young's modulus), reduced swelling in organic solvent, and reduced material shrinkage after exposure to UV photons, free electrons, or electron beams.

[0052] In case of radiation-assisted cross-linking in box 110, UV activation may be used, with UV radiation comprising a broad range of wavelengths. In some embodiments, any wavelength below 300 nm can be effective. Intensity of UV radiation should be selected to be adequate to fully cross-link the precursor oligomers/polymers. In some embodiments an intensity of from 0.01 to 1.0 W/cm² has been found effective. Exposure time can be adjusted for specific precursor formulations as well as specific wavelengths and radiation intensity. To achieve complete crosslinking, times from 5 seconds to 20 minutes have been used in many embodiments.

[0053] Once the solid dielectric material is set into a cross-linked network, the substrate/wafer could, optionally, be subjected to higher temperature outgassing bakes (not shown in FIG. 1) at 400-450 degrees Celsius, including all values and ranges therein, for 1-30 minutes, including all values and ranges therein, in order to remove any thermally labile species. Preferably, the outgassing bake is carried out under nitrogen gas. As used herein, the term "outgassing" is used to describe release of zero or more gases that may have been dissolved, trapped, absorbed, or otherwise included within the cross-linked carbosilane material.

[0054] The material may also be subsequently cured (box 112 of FIG. 1), e.g. by using heat, UV photons or/and electron beams, in order to mechanically harden and/or change or fine-tune the etch properties of the final dielectric material. In some embodiments, curing may involve heating the solid dielectric material of box 110 between 200-450 degrees Celsius, including all values and ranges therein, while simultaneously exposing to optical radiation of 170-254 nm wavelengths (i.e., deep ultraviolet light), including all values and ranges therein. In other embodiments, curing may involve heating the solid dielectric material of box 110

between 200-450 degrees Celsius, including all values and ranges therein, and exposing the solid material to electrons.

[0055] It should be noted that concepts described above are applicable to most spin-on dielectric materials where a catalyst would assist cross-linking of a spin-on resin, with or without added cross-linking material. However, for illustrative purposes and for the sake of clarity, the descriptions below focus on extreme cases of SiC and SiO₂-based dielectric materials. Following sections describe three examples illustrating various precursor synthesis approaches based on BCF catalyst (boxes 102 and 104 of FIG. 1) leading to creation of dielectric materials with various C, O, and Si compositions.

Example 1: SiC-rich dielectric materials formed using cross-linkers

[0056] In the embodiments of Example 1, a starting material of box 102 may include trisilacyclohexane, such as e.g. 1,3,5-trisilacyclohexane and a cross-linker of box 104 may include a silane containing multiple C=C bonds, such as e.g. tetraallylsilane. To that end, as shown in FIG. 2, a starting material such as e.g. 1,3,5-trisilacyclohexane may be reacted in excess (between 2-4 molar equivalents) with a cross-linker such as e.g. tetraallylsilane in presence of a small amount of BCF catalyst, e.g. between 0.01 and 5.0 mol% relative to the reactants. BCF mediates the hydrosilation of C=C bonds creating oligomeric mixture with multitude of unreacted Si-H bonds and Si-allyl bonds remaining. Upon coating thin films onto the substrate, these Si-H groups may be utilized for forming more cross-links within the film. If bakes of boxes 110 and 112 are completed in air, oxygen may be incorporated into film through Si-O-Si linkages. However, if air is excluded, oxygen can be excluded and other reactions will take place.

[0057] In particular, in one embodiment of Example 1, box 102 of FIG. 1 may include dissolving 1,3,5-trisilacyclohexane and BCF catalyst in a compatible solvent such as e.g. toluene. In other embodiments, other aromatic solvents, alkanes and chlorinated solvents may also be used, in place of toluene. Box 104 of FIG. 1 may then include dissolving a cross-linker such as tetraallylsilane (TAS), in desired molar ratio between 0.25-0.50 relative to 1,3,5-trisilacyclohexane, in the same solvent as that used in box 102. In other embodiments, in place of TAS, other multifunctional silanes such as tetravinylsilane,

diallyldimethylsilane may also be used. The solution of 1,3,5-trisilacyclohexane and BCF is then added gradually, e.g. over a time period between 1 and 120 minutes, to the cross-linker solution. After a time period of, preferably, at least 24 hours, the reaction solution may be diluted to desired concentration and filtered (box 106), to be used for coating of box 108.

[0058] In some embodiments, the resulting precursor solution may be concentrated following the reaction and re-dissolved in a new solvent prior to coating.

[0059] In some embodiments, optionally, after synthesis of boxes 102 and 104 but before the coating of box 108, the cross-linker such as tetraallylsilane and BCF catalyst can be re-added to the liquid precursor formulation, providing enhanced cross-linking through more hydrosilation reactions. Si-C content as well as, if desired, O content, can be controlled through control of ratio of Si-H bonds to Si-allyl bonds and through control of the bake conditions such as temperature and environment (e.g. air vs. nitrogen).

[0060] As a result, a dielectric material may be formed either as a thin film or within a plurality of openings in a patterned substrate, or both, the dielectric material comprising cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly via Si-Si bonding or via a C-containing link. In an embodiment, the Si-C rings may be connected based on non-cyclic Si-C groups with minimal, if at all, oxygen content. Such materials may be advantageously used for bulk/blanket films but are also suitable as gapfill materials (i.e. materials able to fill plurality of openings in a substrate, in particular high aspect ratio openings).

Example 2: SiC-rich dielectric materials formed using single-source precursors

[0061] Similar to Example 1 described above, embodiments of Example 2 are also based on synthesizing a precursor through reactions of Si-H and Si-allyl or other Si-olefin functionality. However, instead of using a silane compound as a cross-linker of box 104, a single-source precursor starting material that contains both Si-H and Si-allyl bonds may be used. An example of such starting material is 1,3-diallyl-1,3,5-trisilacyclohexane which contains both Si-H and Si-allyl bonds. As illustrated in FIG. 3, upon addition of BCF to such a starting

material, hydrosilation reactions ensue, leading to complex mixture containing both Si-H and Si-allyl bonds. This material, when coated, thus has both Si-H and C=C functionalities required for further cross-linking in film.

[0062] In particular, in one embodiment of Example 2, box 102 of FIG. 1 may include dissolving 1,3-diallyl-1,3,5-trisilacyclohexane and BCF catalyst in a compatible solvent such as e.g. toluene. In other embodiments, other aromatic solvents, alkanes and chlorinated solvents may also be used, in place of toluene. Following box 102, liquid precursor formulation is formed according to box 106 (i.e. cross-linker of box 104 is not added in this Example).

[0063] In some embodiments, the resulting precursor solution may be concentrated following the cross-linking of box 102 and re-dissolved in a new solvent prior to coating.

[0064] Similar to Example 1, in this case, Si-C content as well as, if desired, O content, can be controlled through control of ratio of Si-H bonds to Si-allyl bonds and through control of the bake conditions such as temperature and environment (e.g. air vs. nitrogen).

[0065] As a result, a dielectric material similar to that of Example 1 may be formed either as a thin film or within a plurality of openings in a patterned substrate, or both. In this case, the dielectric material may include cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units via a C-containing link in the form of -CH₂CH₂CH₂-.

[0066] In still further embodiments, Examples 1 and 2 may be mixed in that a single-source precursor starting material that contains both Si-H and Si-allyl bonds may be used, in combination with a cross-linker containing multiple C=C bonds. Applicable to such embodiments, as well as to embodiments of Example 1 and Example 2 individually, a wide variety of cross-linking agents or/and starting materials can be used, as illustrated in FIGs. 4a-4h, providing additional control of final SiC content. FIGs. 4a-4f illustrate tetravinylsilane (FIG.s 4a), dimethyldivinylsilane (FIG. 4b), trivinylbenzene (FIG. 4c), tetraallylsilane (FIG. 4d), dimethyldiallylsilane (FIG. 4e), and cyclohexadiene (FIG. 4f) as exemplary cross-linking

agents. FIGs. 4g and 4h illustrate 1,3-divinyl-1,3-5-trisilacyclohexane and 1,3,5-trivinyl-1,3-5-trisilacyclohexane as exemplary single-source starting materials.

Example 3: SiO₂-rich dielectric materials

[0067] In order to create spin-on SiO₂-rich dielectric materials with control of Si-O content, in embodiments of Example 3 materials with minimal C content may be chosen as the starting materials of box 102, where any C present can be removed via thermolysis (i.e., chemical decomposition caused by heat) or photolysis (i.e., chemical decomposition caused by photons) during processing. To that end, similar chemistry as that of Examples 1 and 2 may be used, but without the use of trisilacyclohexane starting materials. In some embodiments of Example 3, new oligomeric and polymeric materials may be synthesized by catalytic reaction using BCF catalyst and molecule containing multiple SiH bonds with another molecule containing multiple Si-OEt, or other alkoxy, groups. For example, starting materials such as e.g. n-butyldisilane (n-BuSiH₃), tert-butyldisilane (tBuSiH₃) or methyltrisilane (MeSiH₃), when reacted in fourfold excess with tetraethoxysilane (TEOS) in presence of BCF, lead to formation of oligomeric mixture as shown in FIG. 5. As illustrated in FIG. 5, in addition to Si-O-Si network which has been created, there are multiple SiH bonds available for further reactions with water or oxygen during film coating and baking process in air. Depending on thermal and photochemical stability of Si-C bonds present (e.g. nBu-Si, tBu-Si, Me-Si), additional reactive sites can be created in film via thermolysis or photolysis leading to Si radical centers from homolysis of Si-C bond.

[0068] In particular, in one embodiment of Example 3, box 102 of FIG. 1 may include dissolving an alkylsilane RSiH₃ (where R is nBu, tBu, Me etc) and BCF catalyst in a compatible solvent such as e.g. toluene. In other embodiments, other aromatic solvents, alkanes and chlorinated solvents may also be used, in place of toluene. Box 104 of FIG. 1 may then include dissolving a cross-linker such as tetraethoxysilane (TEOS), in desired molar ratio between 0.25-0.50 relative to RSiH₃, in the same solvent as that used in box 102. In other embodiments, in place of TEOS, other alkoxysilanes such as (MeO)₄Si or/and MeSi(OEt)₃ may also be used in place of TEOS. The solution of RSiH₃ and BCF is then added, e.g. over a time period between 1 minute and 120 minutes, to the TEOS solution. After a time period

of, preferably, at least 24 hours, the reaction solution may be diluted to desired concentration and filtered (box 106), to be used for coating of box 108. Alternatively, the TEOS solution can be added to RSiH_3 and BCF.

[0069] As a result, a dielectric material may be formed either as a thin film or within a plurality of openings in a patterned substrate, or both, the dielectric material comprising interconnected $[\text{SiO}_4]$ tetrahedral (i.e. tetrahedral SiO_4 units) interspersed with random H- SiO_3 units and SiO_3 pairs joined through Si-Si bonds. In some embodiments, the resulting dielectric material may include tetrahedral SiO_4 units connected to 3 or 4 other tetrahedral SiO_4 units where non-linked vacancies are occupied by any of the following functions: H, OH, CH_3 , CH_2CH_3 , tBu, etc.

[0070] The generality of the BCF-catalyzed reactions allows for mixing multiple starting materials to produce materials with diverse properties. Thus, in further embodiments, Examples 1, 2, and 3 may be mixed in various combinations.

[0071] In particular, when Examples 1 or 2 are mixed with Example 3, precursor formulation comprising both Si-C rings as described above in association with Examples 1 and 2, and tetrahedral SiO_4 units as described above in association with Example 3 may be obtained. As a result, a dielectric material may be formed within a plurality of openings and/or as thin film, where the dielectric material includes a mixture of cyclic carbosilane units having a ring structure including C and Si and tetrahedral SiO_4 units connected to other carbosilane units or other tetrahedral units where non-linked vacancies are occupied by any of the following functions: H, OH, CH_3 , CH_2CH_3 , tBu, etc

[0072] As the foregoing illustrates, through control of starting materials and processing conditions, use of BCF catalyst to synthesize precursor materials enables exquisite control of the ultimate Si:C:O content in dielectric films, allowing tuning of properties such as etch and thermal stability.

[0073] Yet another class of SiC-rich materials such as the ones described in Example 1 and 2 may be formed via reaction different from that based on the use of BCF catalyst, namely via dehalocoupling described in the following section.

Dehalocoupling

[0074] In another aspect of the present disclosure, dehalocoupling (i.e. metal-mediated removal of halogen from two Si atoms with formation of new Si-Si bond and metal halide) may be used to generate precursor polymers from trisilacyclohexane starting materials (homopolymers or copolymers). For example, as shown in FIG. 6a, when 1,3-dibromo-1,3,5-trisilacyclohexane or 1,3-dichloro-1,3,5-trisilacyclohexane is mixed with lithium (Li), sodium (Na), potassium (K), magnesium (Mg) or other metals in a solvent such as tetrahydrofuran (THF) or dioxane, dehalocoupling of two Si-X bonds, where X is either bromine (Br) or chlorine (Cl), occurs, leading to formation of new Si-Si bonds and MX byproduct, such as e.g. LiCl or NaBr. As shown in FIG. 6b, in order to tune SiC content, a comonomer such as dimethyldibromosilane (Me_2SiBr_2) or vinylmethyldibromosilane (vinyl- MeSiBr_2) can be used during the synthesis prior to addition of Na, leading to random copolymer. In other embodiments, other alkyl groups and hydrido groups can be used. In general, “comonomer” is used to describe a group of monomers that, when polymerized, form a copolymer, in this case the precursor polymer. After that, liquid precursor formulation may be made as described above in box 106, and dielectric material may be formed from the liquid precursor formulation as described above in boxes 108-112.

[0075] As a result, a dielectric material similar to that of Examples 1 and 2 may be formed either as a thin film or within a plurality of openings in a patterned substrate, or both. In this case, the dielectric material may include cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly (i.e. no intermediate links) or via relatively short $-(\text{SiR}_2)_n-$ links, where R is an alkyl group and n is 1, 2, 3..., through use of R_2SiBr_2 or R_2SiCl_2 , reactants in the polymerization reaction.

[0076] In this example, cross-linking agents such as the ones shown in FIGs. 4a-4h may be used, in order to provide mechanical stiffening and tune Si:C content in final films.

Exemplary Structure

[0077] FIG. 7 provides a schematic illustration of a cross-section of a structure 71 comprising a plurality of openings 72 filled with a dielectric material 73 formed according to

any embodiment of the present disclosure. As can be seen, FIG. 7 is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. The structure 71 can be disposed on a substrate 74, and an etch-stop layer 75 may be provided to ensure that when the openings 72 are made by etching the structure 71, etching does not extend into the substrate 74. Height H and width W of the openings 72 are also indicated in FIG. 7.

[0078] In a particular example shown in FIG. 7, the dielectric material 73 is shown to fill the features 72 to a large extent, but not completely – the upper parts of the openings 72 are not filled with the material 73. However, in other embodiments, the dielectric material may fill the features completely and may even form a thin film covering the entire structure 72.

[0079] In various embodiments, each one of the structure 71 and the substrate 74 may be comprised of one or more of silicon, silicon dioxide, germanium, indium, antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide and gallium antimonide. In some embodiments, the structure 71 may be an interlayer dielectric (ILD). Two or more layers of the interlayer dielectric may be stacked to form an integrated circuit. In some embodiments, the ILD may include one or more sacrificial layers deposited over a dielectric substrate. The ILD may include one or more dielectric materials, which are understood to be materials that are insulators but are polarized upon application of an electric field. In some embodiments, the structure 71 may have a thickness in the range of 50 nm to 300 nm, including all values and ranges therein, such as 100 nm to 300 nm, 100 nm to 200 nm, etc.

[0080] In other embodiments, the dielectric material according to any embodiments of the present disclosure may be provided as a layer, e.g. a thin film, on a substrate (not shown in FIG. 7).

Implementation in an interposer

[0081] In accordance with embodiments of the disclosure, dielectric materials disclosed herein may be used in the fabrication of an interposer, such as e.g. the one shown in FIG. 8. In particular, the dielectric materials described herein may be used in the fabrication of various interconnects of the interposer shown in FIG. 8. For example, the materials described herein may be used in forming dielectric regions within the interposer 800, e.g.

regions between at least some of the trenches 808 and vias 810, which could be done instead of or in addition to a conventional dual damascene process.

[0082] FIG. 8 illustrates an interposer 800 that includes one or more embodiments of the disclosure. The interposer 800 is an intervening substrate used to bridge a first substrate 802 to a second substrate 804. The first substrate 802 may be, for instance, an integrated circuit die. The second substrate 804 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 800 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 800 may couple an integrated circuit die to a ball grid array (BGA) 806 that can subsequently be coupled to the second substrate 804. In some embodiments, the first and second substrates 802/804 may be attached to opposing sides of the interposer 800. In other embodiments, the first and second substrates 802/804 may be attached to the same side of the interposer 800. In further embodiments, three or more substrates may be interconnected by way of the interposer 800.

[0083] The interposer 800 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0084] The interposer may include metal interconnect trenches 808 and vias 810, including but not limited to through-silicon vias (TSVs) 812. The vias 810 may be enclosed by first and second diffusion barrier layers as described herein. The interposer 800 may further include embedded devices 814, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 800.

Implementation in a computing device

[0085] In accordance with embodiments of the disclosure, dielectric materials disclosed herein may be used in the fabrication of a computing device, such as e.g. the one shown in FIG. 9. In particular, the dielectric materials described herein may be used in the fabrication of various interconnects of the computing device shown in FIG. 9.

[0086] Figure 9 illustrates a computing device 900 in accordance with one embodiment of the disclosure. The computing device 900 may include a number of components. In one embodiment, these components may be attached to one or more motherboards. In an alternate embodiment, some or all of these components may be fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 900 include, but are not limited to, an integrated circuit die 902 and at least one communications logic unit 908. In some implementations the communications logic unit 908 may be fabricated within the integrated circuit die 902 while in other implementations the communications logic unit 908 may be fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that may be shared with or electronically coupled to the integrated circuit die 902. The integrated circuit die 902 may include a CPU 904 as well as on-die memory 906, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0087] Computing device 900 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 910 (e.g., DRAM), non-volatile memory 912 (e.g., ROM or flash memory), a graphics processing unit 914 (GPU), a digital signal processor 916, a crypto processor 942 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 920, an antenna 922, a display or a touchscreen display 924, a touchscreen controller 926, a battery 928 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 928, a compass 930, a motion coprocessor or sensors 932 (that may include an accelerometer, a gyroscope, and a compass), a speaker 934, a camera 936, user input devices 938 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 940 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0088] The communications logic unit 908 enables wireless communications for the transfer of data to and from the computing device 900. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 908 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 900 may include a plurality of communications logic units 908. For instance, a first communications logic unit 908 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 908 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0089] The processor 904 of the computing device 900 may include one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0090] The communications logic unit 908 may also include one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0091] In further embodiments, another component housed within the computing device 900 may contain one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0092] In various embodiments, the computing device 900 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

[0093] Some Examples in accordance with various embodiments of the present disclosure are now described.

[0094] Example 1 provides a method of preparing a liquid precursor formulation for forming a dielectric material with a predefined composition of silicon, carbon, and/or oxygen. The method includes selecting, based on the predefined composition of silicon, carbon, and/or oxygen, one or more starting materials; selecting, based on the predefined composition of silicon, carbon, and/or oxygen, zero or more cross-linking agents for cross-linking the one or more starting materials; reacting the one or more selected starting materials and the zero or more selected cross-linking agents in presence of a catalyst to produce precursor oligomers or/and polymers of the one or more selected starting materials; and dissolving the precursor oligomers or/and polymers in one or more solvents to form the liquid precursor formulation.

[0095] Example 2 provides the method according to Example 1, where the one or more starting materials and the zero or more cross-linking agents include compounds with multiple Si-H bonds and compounds with multiple Si-X bonds, where X is a functional group selected from OEt, allyl, vinyl, or OSiR₃.

[0096] Example 3 provides the method according to Example 2, where the one or more starting materials and the zero or more cross-linking agents are selected to achieve a predefined ratio between Si-H bonds and Si-X bonds, the ratio depending on the predefined composition of silicon, carbon, and/or oxygen.

[0097] Example 4 provides the method according to any one or Examples 1-3, where the one or more starting materials include trisilacyclohexane and the zero or more cross-linking agents include one or more silanes containing multiple C=C bonds.

[0098] Example 5 provides the method according to Example 4, where the trisilacyclohexane includes 1,3,5-trisilacyclohexane and/or where the one or more silanes include a tetraallylsilane.

[0099] Example 6 provides the method according to Example 5, where a molar ratio between the tetraallylsilane and the 1,3,5-trisilacyclohexane is between 0.25 and 0.50.

[00100] Example 7 provides the method according to Example 4, where the trisilacyclohexane includes 1,3,5-trisilacyclohexane and/or where the one or more silanes include a tetravinylsilane or a diallyldimethylsilane.

[00101] Example 8 provides the method according to any one or Examples 1-3, where the one or more starting materials include a material including both Si-H bonds and Si-allyl bonds.

[00102] Example 9 provides the method according to Example 8, where the material including both Si-H bonds and Si-allyl bonds includes 1,3-diallyl-1,3,5-trisilacyclohexane.

[00103] Example 10 provides the method according to any one of the preceding Examples, where the one or more solvents include an aromatic solvent, alkane or a chlorinated solvent.

[00104] Example 11 provides the method according to any one of the preceding Examples, where the catalyst includes a Lewis acid of comparable (equal) or greater Lewis acidity than BH_3 .

[00105] Example 12 provides the method of Example 11, where the Lewis acid includes tris(pentafluorophenyl)borane ($\text{B}(\text{C}_6\text{F}_5)_3$).

[00106] Example 13 provides a liquid precursor formulation for forming a dielectric material with a predefined composition of silicon, carbon, and/or oxygen. The precursor formulation includes precursor oligomers or/and polymers of one or more starting materials and zero or more cross-linking agents including unreacted Si-H bonds and/or Si-X bonds, where a ratio between Si-H bonds and Si-X bonds is defined by the predefined composition of silicon, carbon, and/or oxygen.

[00107] Example 14 provides the precursor formulation according to Example 13, where the precursor oligomers or/and polymers are dissolved in one or more solvents.

[00108] Example 15 provides the precursor formulation according to Example 14, where the one or more solvents include an aromatic solvent, alkane or a chlorinated solvent.

[00109] Example 16 provides the precursor formulation according to any one of Examples 13-15, where X is a functional group selected from OEt, allyl, vinyl, or OSiR₃.

[00110] Example 17 provides the precursor formulation according to any one or Examples 13-16, where the one or more starting materials include trisilacyclohexane and the zero or more cross-linking agents include one or more silanes containing multiple C=C bonds.

[00111] Example 18 provides the precursor formulation according to Example 17, where the trisilacyclohexane includes 1,3,5-trisilacyclohexane and/or where the one or more silanes include a tetraallylsilane.

[00112] Example 19 provides the precursor formulation according to Example 18, where a molar ratio between the tetraallylsilane and the 1,3,5-trisilacyclohexane is between 0.25 and 0.50.

[00113] Example 20 provides the precursor formulation according to Example 17, where the trisilacyclohexane includes 1,3,5-trisilacyclohexane and/or where the one or more silanes include a tetravinylsilane or a diallyldimethylsilane.

[00114] Example 21 provides the precursor formulation according to any one or Examples 13-16, where the one or more starting materials include a material including both Si-H bonds and Si-allyl bonds.

[00115] Example 22 provides the precursor formulation according to Example 21, where the material including both Si-H bonds and Si-allyl bonds includes 1,3-diallyl-1,3,5-trisilacyclohexane.

[00116] Example 23 provides a semiconductor device that includes a dielectric material disposed as a film on a substrate or/and within a plurality of openings of the substrate, the dielectric material including cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly via Si-Si bonding or via a C-containing link.

[00117] Example 24 provides the semiconductor device according to Example 23, where the C-containing link is essentially free of oxygen (O).

[00118] Example 25 provides a semiconductor device that includes a dielectric material disposed as a film on a substrate or/and within a plurality of openings of the substrate, the dielectric material including cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units via a C-containing link in the form of -CH₂CH₂CH₂-.

[00119] Example 26 provides the semiconductor device according to Example 25, where the dielectric material is essentially free of oxygen (O).

[00120] Example 27 provides a semiconductor device that includes a dielectric material disposed as a film on a substrate or/and within a plurality of openings of the substrate, the dielectric material including a mixture of cyclic carbosilane units having a ring structure including C and Si and tetrahedral (SiO₄) units connected to at least some of the cyclic carbosilane units or/and other tetrahedral units, the dielectric material further including a plurality of non-linked vacancies occupied by one or more of H, OH, CH₃, CH₂CH₃, or tBu.

[00121] Example 28 provides the semiconductor device according to Example 27, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly via Si-Si bonding or via a C-containing link.

[00122] Examples 29 provides the semiconductor device according to Example 27, where each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units via a C-containing link in the form of $-\text{CH}_2\text{CH}_2\text{CH}_2-$.

[00123] Example 30 provides a method of preparing a liquid precursor formulation for forming a dielectric material. The method includes generating a precursor polymer from a starting material including trisilacyclohexane molecules, each molecule including a plurality of Si-X bonds, by dehalocoupling two Si-X bonds from the plurality of Si-X bonds from at least some of the molecules.

[00124] Example 31 provides the method according to Example 30, where the trisilacyclohexane molecules include 1,3-dibromo-1,3,5-trisilacyclohexane molecules and X is Br.

[00125] Example 32 provides the method according to Example 30, where the trisilacyclohexane molecules include 1,3-dichloro-1,3,5-trisilacyclohexane molecules and X is Cl.

[00126] Example 33 provides the method according to any one of Examples 30-32, where dehalocoupling occurs by mixing the trisilacyclohexane molecules with lithium (Li), sodium (Na), potassium (K), or magnesium (Mg) in a solvent including tetrahydrofuran or dioxane.

[00127] Example 34 provides the method according to any one of Examples 30-33, further including adding a comonomer of the precursor polymer prior to dehalocoupling.

[00128] Example 35 provides the method according to Example 34, where the comonomer includes Me_2SiBr_2 , vinyl- MeSiBr_2 or other dibromo- or tribromosilanes when the trisilacyclohexane molecules include 1,3-dibromo-1,3,5-trisilacyclohexane molecules.

[00129] Example 36 provides the method according to Example 34, where the comonomer includes Me_2SiCl_2 or vinyl- MeSiCl_2 or other dichloro- or trichlorosilanes when the trisilacyclohexane molecules include 1,3-dichloro-1,3,5-trisilacyclohexane molecules.

[00130] Example 37 provides the method according to any one of Examples 30-36, further including dissolving the precursor polymer in one or more solvents to form the liquid precursor formulation.

[00131] Example 38 provides the method according to Example 37, where the one or more solvents include toluene, cyclohexanone, or 2-heptanone, or any other common solvents.

[00132] Example 39 provides a liquid precursor formulation for forming a dielectric material. The precursor formulation includes an oligomer or polymer including direct bonds between Si atoms of multiple trisilacyclohexane rings.

[00133] Example 40 provides the precursor formulation according to Example 39, where the multiple trisilacyclohexane rings are connected by zero or more dialkylsilyl (R_2Si) linkers, where R is an alkyl, an aryl, or hydrogen (H).

[00134] Example 41 provides the precursor formulation according to Examples 39 or 40, further including a catalyst with cross-linking molecules including one or more of tetraallylsilane, tetravinylsilane, and 1,3-diallyl-1,3,5-trisilacyclohexane.

[00135] Example 42 provides the precursor formulation according to Examples 39 or 40, further including a catalyst in absence of cross-linking molecules.

[00136] Example 43 provides the precursor formulation according to Examples 41 or 42, where the catalyst includes tris-pentafluorophenylborane ($B(C_6F_5)_3$).

[00137] Example 44 provides a semiconductor device that includes a dielectric material disposed as a film on a substrate or/and within a plurality of openings of the substrate, the dielectric material including cross-linked cyclic carbosilane units having a ring structure including C and Si, where each unit of at least some cyclic carbosilane units is linked to each of at least two other cyclic carbosilane units either directly or via a $-(SiR_2)_n-$ link, where R is an alkyl group or a hydrido group, and n is a positive integer.

[00138] Example 45 provides the semiconductor device according to Example 44, where the alkyl group includes a methyl, a vinyl.

[00139] Example 46 provides the semiconductor device according to Example 44, where the dielectric material has composition with ratio of Si:C substantially equal to that of stoichiometric silicon carbide.

[00140] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[00141] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A method of preparing a liquid precursor formulation for forming a dielectric material with a predefined composition of silicon, carbon, and/or oxygen, the method comprising:

selecting, based on the predefined composition of silicon, carbon, and/or oxygen, one or more starting materials;

selecting, based on the predefined composition of silicon, carbon, and/or oxygen, zero or more cross-linking agents for cross-linking the one or more starting materials;

reacting the one or more selected starting materials and the zero or more selected cross-linking agents in presence of a catalyst to produce precursor oligomers or/and polymers of the one or more selected starting materials; and

dissolving the precursor oligomers or/and polymers in one or more solvents to form the liquid precursor formulation.

2. The method according to claim 1, wherein the one or more starting materials and the zero or more cross-linking agents comprise compounds with multiple Si-H bonds and compounds with multiple Si-X bonds, where X is a functional group selected from OEt, allyl, vinyl, or OSiR₃.

3. The method according to claim 2, wherein the one or more starting materials and the zero or more cross-linking agents are selected to achieve a predefined ratio between Si-H bonds and Si-X bonds, the ratio depending on the predefined composition of silicon, carbon, and/or oxygen.

4. The method according to any one of claims 1-3, wherein the one or more starting materials comprise trisilacyclohexane and the zero or more cross-linking agents comprise one or more silanes containing multiple C=C bonds.

5. The method according to claim 4, wherein the trisilacyclohexane comprises 1,3,5-trisilacyclohexane and/or wherein the one or more silanes comprise a tetraallylsilane.

6. The method according to claim 5, wherein a molar ratio between the tetraallylsilane and the 1,3,5-trisilacyclohexane is between 0.25 and 0.50.
7. The method according to claim 4, wherein the trisilacyclohexane comprises 1,3,5-trisilacyclohexane and/or wherein the one or more silanes comprise a tetravinylsilane or a diallyldimethylsilane.
8. The method according to any one of claims 1-3, wherein the one or more starting materials comprise a material comprising both Si-H bonds and Si-allyl bonds.
9. The method according to claim 8, wherein the material comprising both Si-H bonds and Si-allyl bonds comprises 1,3-diallyl-1,3,5-trisilacyclohexane.
10. The method according to any one of claims 1-3, wherein the catalyst comprises tris(pentafluorophenyl)borane ($B(C_6F_5)_3$).
11. A liquid precursor formulation for forming a dielectric material with a predefined composition of silicon, carbon, and/or oxygen, the precursor formulation comprising:

precursor oligomers or/and polymers of one or more starting materials and zero or more cross-linking agents comprising unreacted Si-H bonds and/or Si-X bonds, where a ratio between Si-H bonds and Si-X bonds is defined by the predefined composition of silicon, carbon, and/or oxygen.
12. The precursor formulation according to claim 11, wherein X is a functional group selected from OEt, allyl, vinyl, or OSiR₃.
13. The precursor formulation according to claims 11 or 12, wherein the one or more starting materials comprise trisilacyclohexane and the zero or more cross-linking agents comprise one or more silanes containing multiple C=C bonds.
14. The precursor formulation according to claims 11 or 12, wherein the one or more starting materials comprise a material comprising both Si-H bonds and Si-allyl bonds.

15. The precursor formulation according to claim 14, wherein the material comprising both Si-H bonds and Si-allyl bonds comprises 1,3-diallyl-1,3,5-trisilacyclohexane.

16. A semiconductor device comprising:

a dielectric material disposed as a film on a substrate or/and within a plurality of openings of the substrate, the dielectric material comprising a mixture of cyclic carbosilane units having a ring structure including C and Si and tetrahedral (SiO₄) units connected to at least some of the cyclic carbosilane units or/and other tetrahedral units, the dielectric material further comprising a plurality of non-linked vacancies occupied by one or more of H, OH, CH₃, CH₂CH₃, or tBu.

17. The semiconductor device according to claim 16, wherein each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units either directly via Si-Si bonding or via a C-containing link.

18. The semiconductor device according to claim 16, wherein each unit of at least some cyclic carbosilane units is linked to at least two other cyclic carbosilane units via a C-containing link in the form of -CH₂CH₂CH₂-.

19. A method of preparing a liquid precursor formulation for forming a dielectric material, the method comprising:

generating a precursor polymer from a starting material comprising trisilacyclohexane molecules, each molecule comprising a plurality of Si-X bonds, by dehalocoupling two Si-X bonds from the plurality of Si-X bonds from at least some of the molecules.

20. The method according to claim 19, wherein the trisilacyclohexane molecules comprise 1,3-dibromo-1,3,5-trisilacyclohexane molecules and X is Br.

21. The method according to claims 19 or 20, wherein dehalocoupling occurs by mixing the trisilacyclohexane molecules with lithium (Li), sodium (Na), potassium (K), or magnesium (Mg) in a solvent comprising tetrahydrofuran or dioxane.

22. The method according to claims 19 or 20, further comprising:

adding a comonomer of the precursor polymer prior to dehalocoupling.

23. The method according to claim 22, wherein the comonomer comprises Me_2SiBr_2 , vinyl- MeSiBr_2 or other dibromo- or tribromosilanes.

24. The method according to claims 19 or 20, further comprising:

dissolving the precursor polymer in one or more solvents to form the liquid precursor formulation.

25. The method according to claim 24, wherein the one or more solvents comprise toluene, cyclohexanone, or 2-heptanone.

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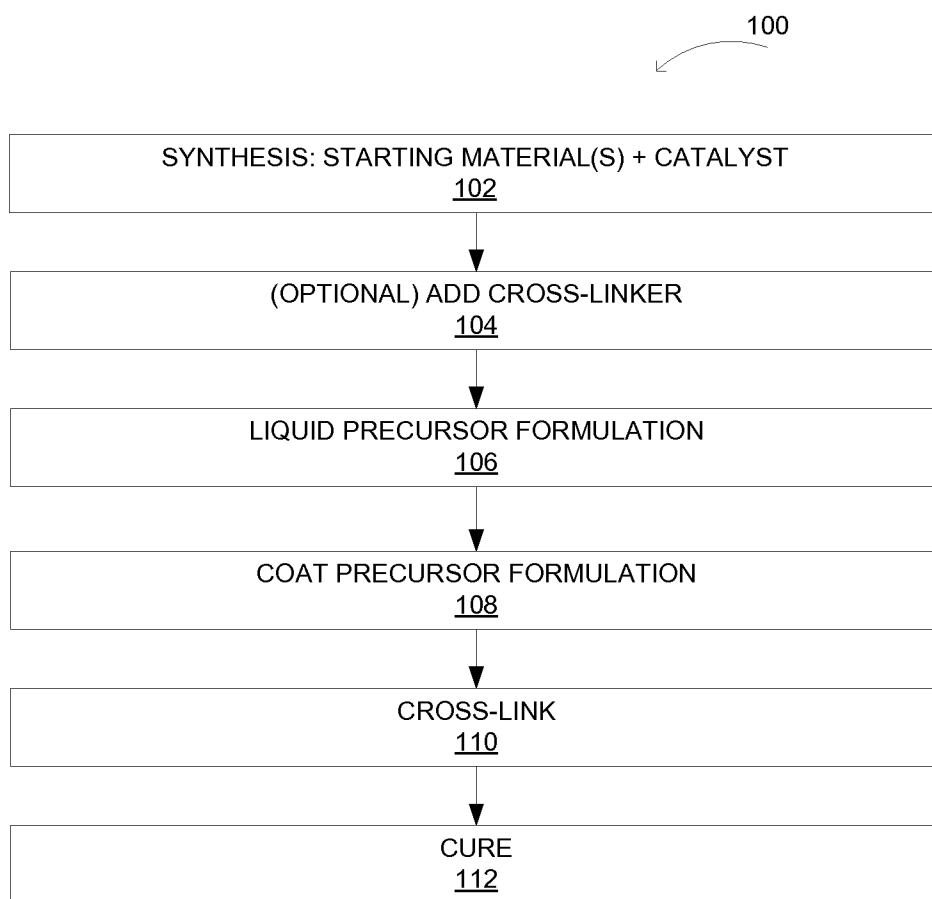


FIG. 1

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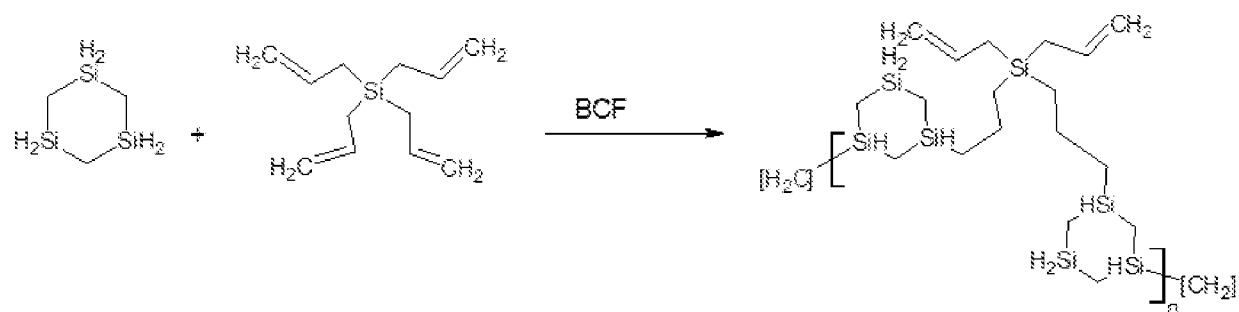


FIG. 2

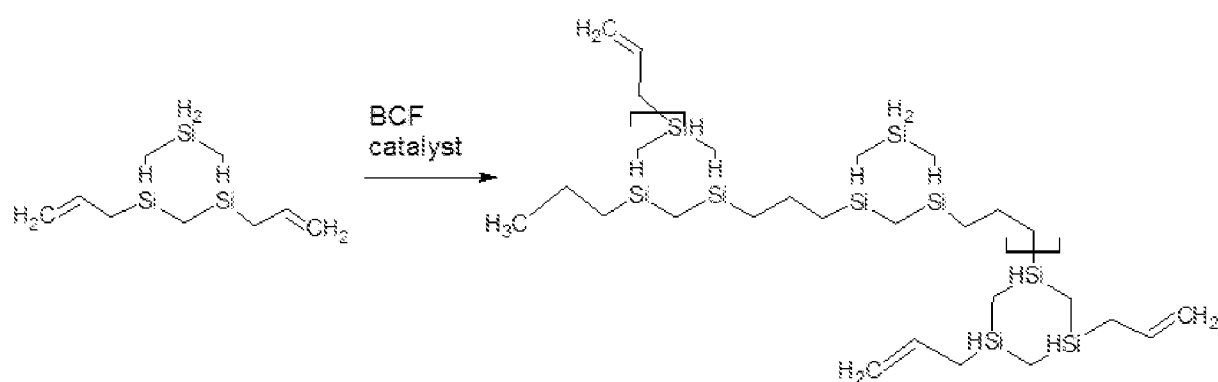
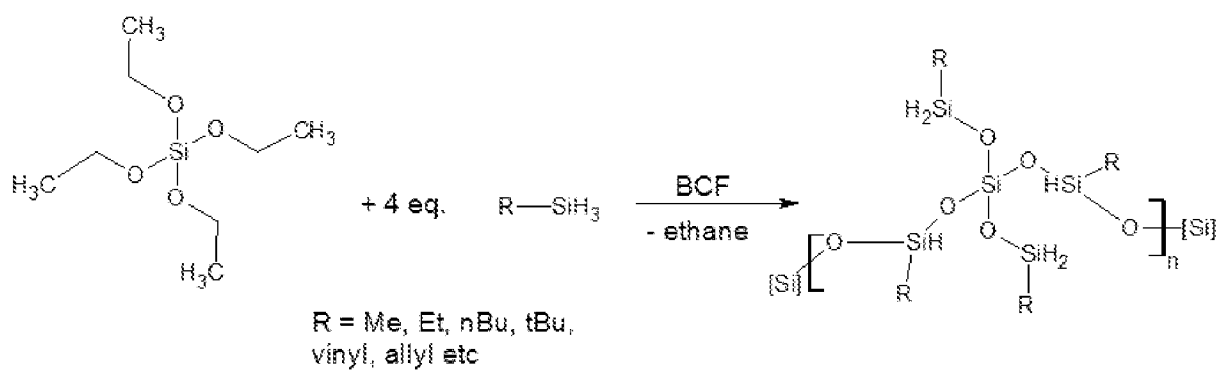
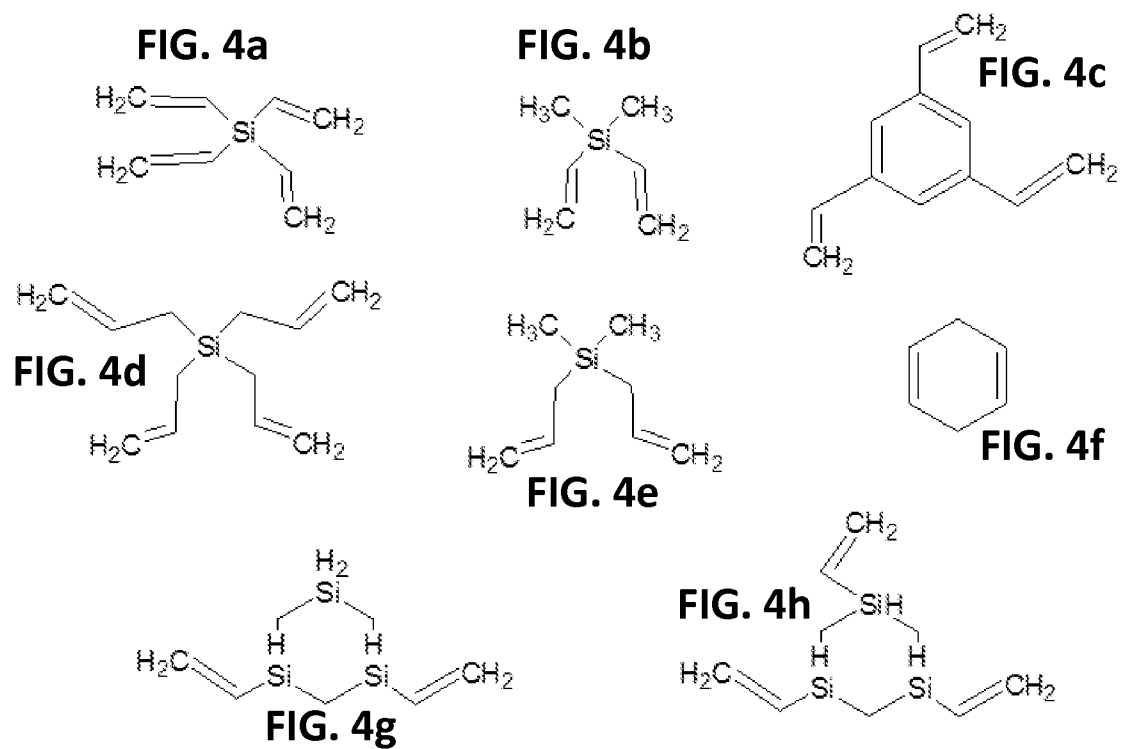


FIG. 3

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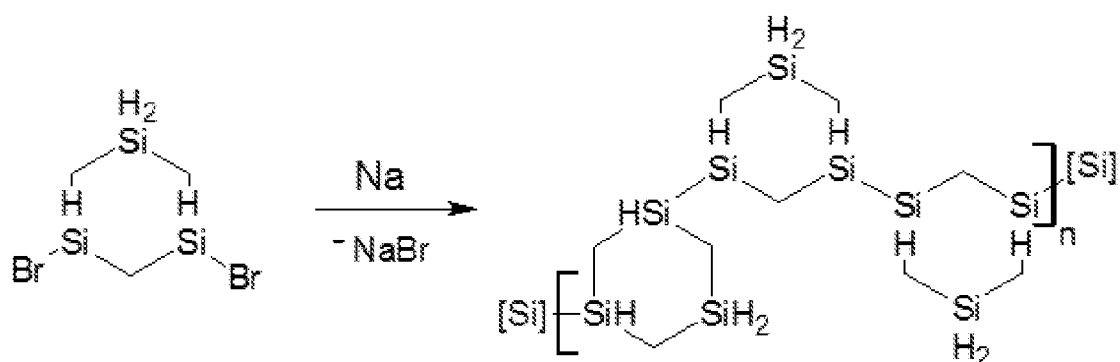


FIG. 6a

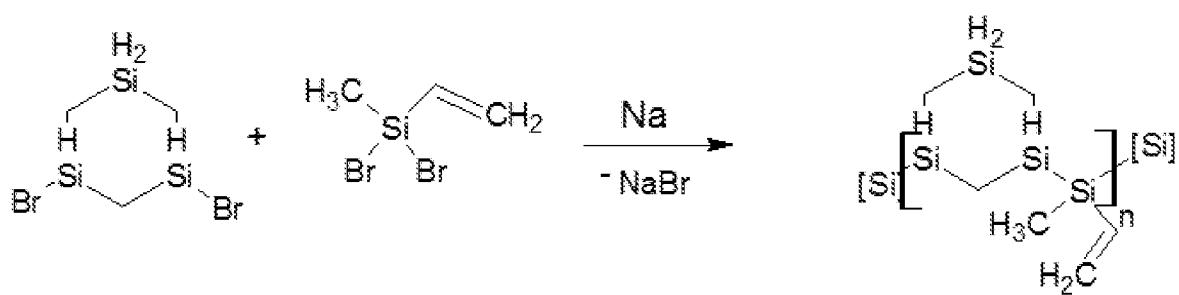


FIG. 6b

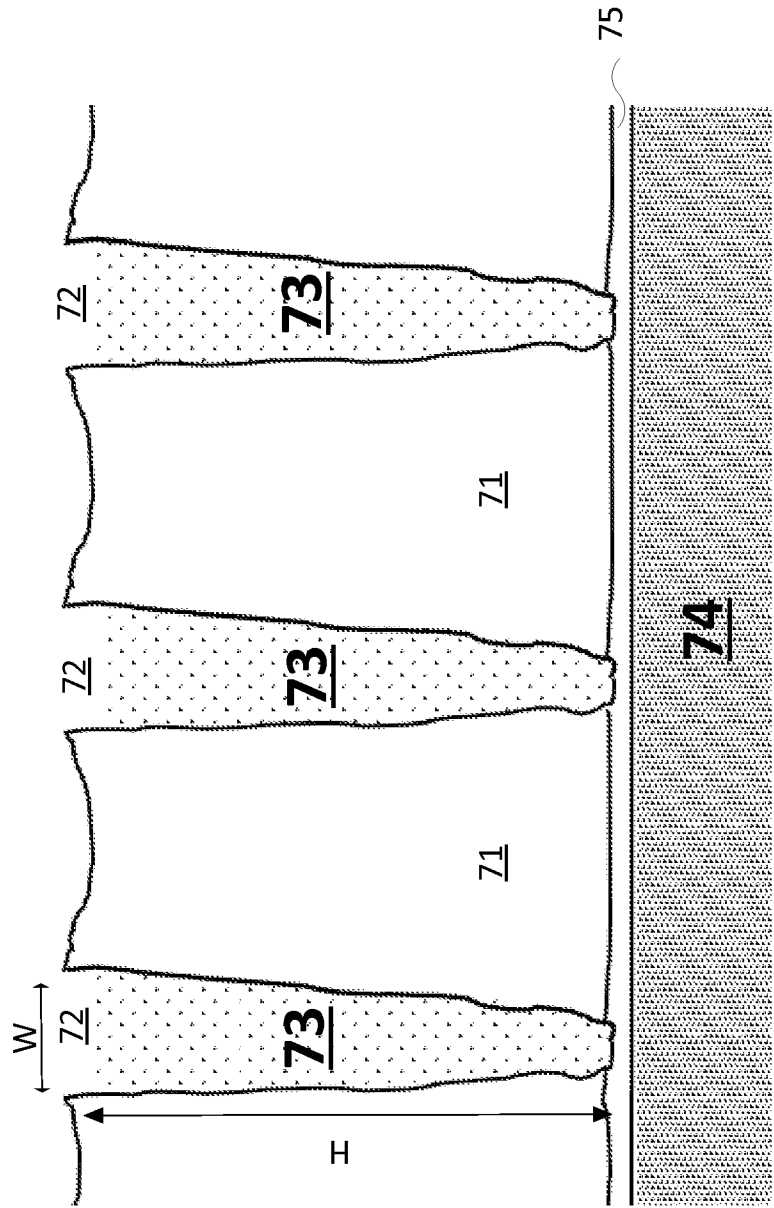


FIG. 7

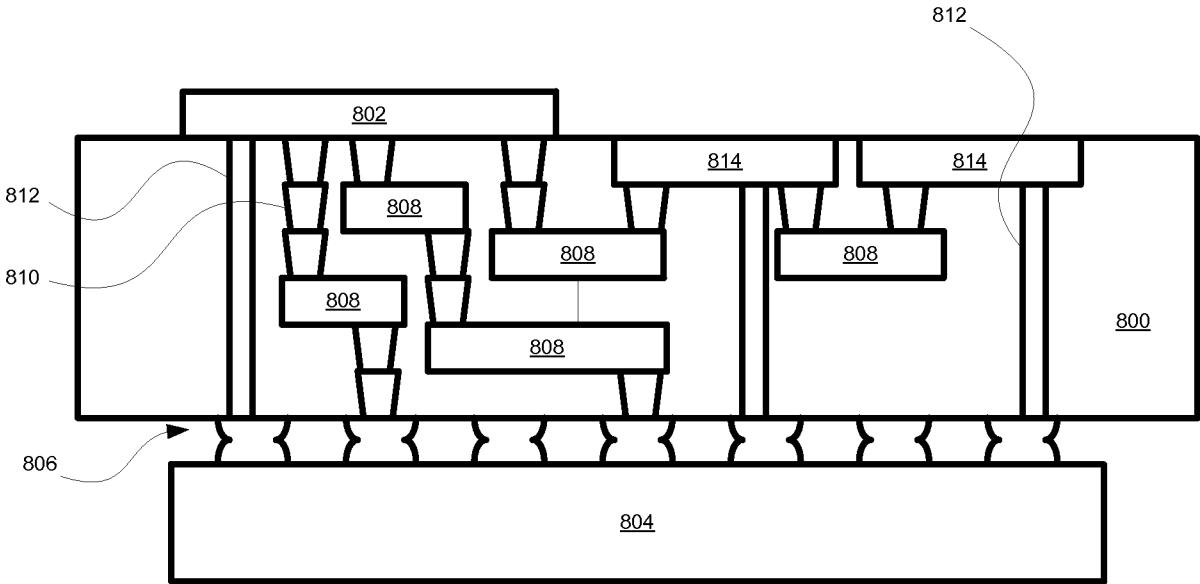


FIG. 8

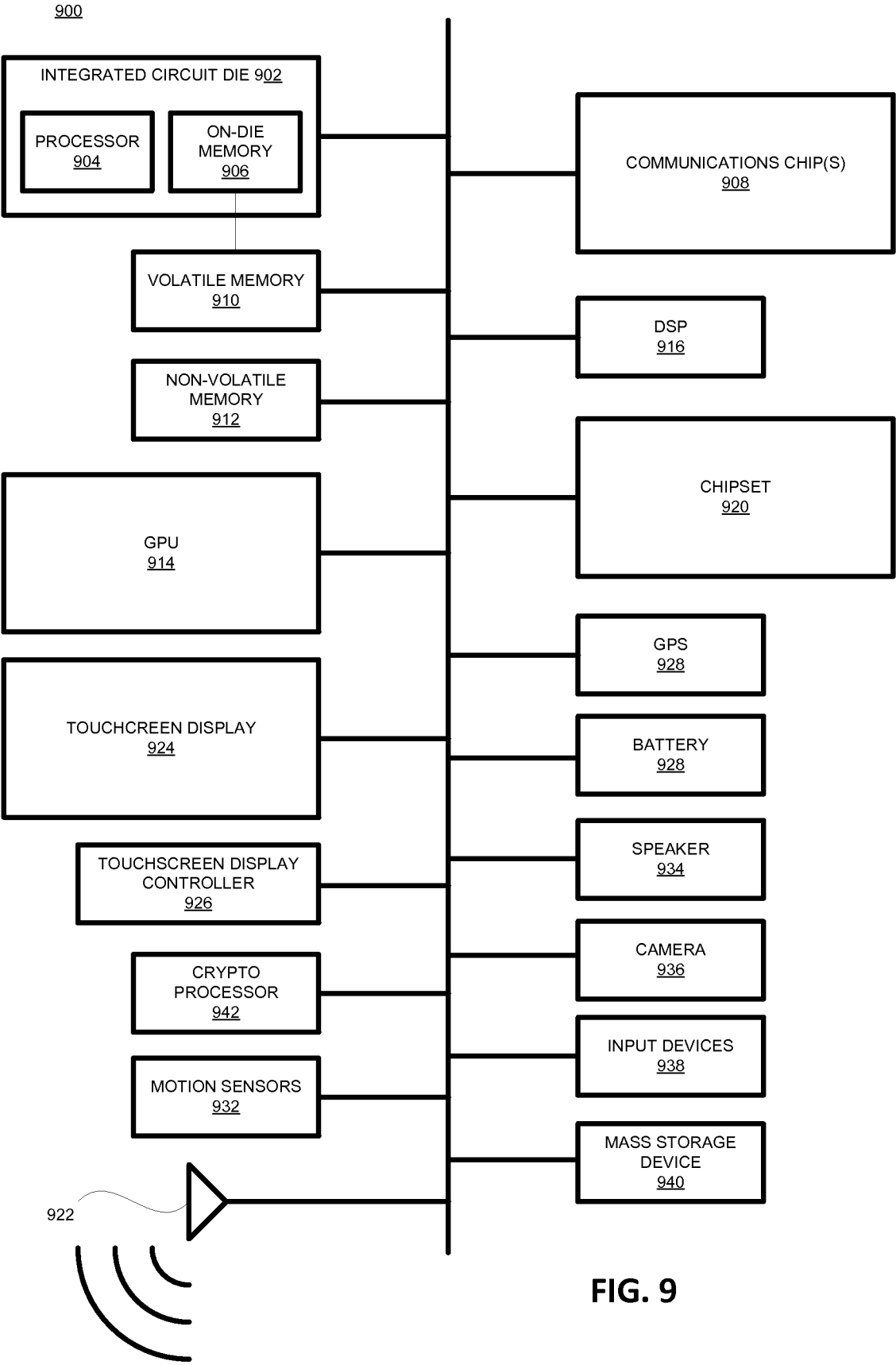


FIG. 9

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/31(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/31; H01L 21/20; H01L 27/148; H01L 21/306; H01L 29/06; H01L 21/02; H01L 21/314; C23C 16/50; G03F 7/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:liquid precursor, cyclic carbosilane, cross-linking agent, oligomer, dielectric film, trisilacyclohexane

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0161295 A1 (DAVID J. MICHALAK et al.) 28 June 2012	1,10-12
A	See abstract, paragraphs [0016]-[0023], [0030], claims 1-9 and figures 1-8.	2-9,13-25
A	US 2005-0194619 A1 (DANIEL C. EDELSTEIN et al.) 08 September 2005	1-25
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A	See abstract, paragraphs [0044]-[0049], claims 16-31 and figures 4A-4C.	
A	US 2013-0217240 A1 (ABHIJIT BASU MALLICK et al.) 22 August 2013	1-25
A	See abstract, paragraphs [0019]-[0040] and figure 1.	
A	US 2012-0122302 A1 (TIMOTHY W. WEIDMAN et al.) 17 May 2012	1-25
A	See abstract, paragraphs [0063]-[0066] and figure 1.	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

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Name and mailing address of the ISA/KR

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International application No.

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