

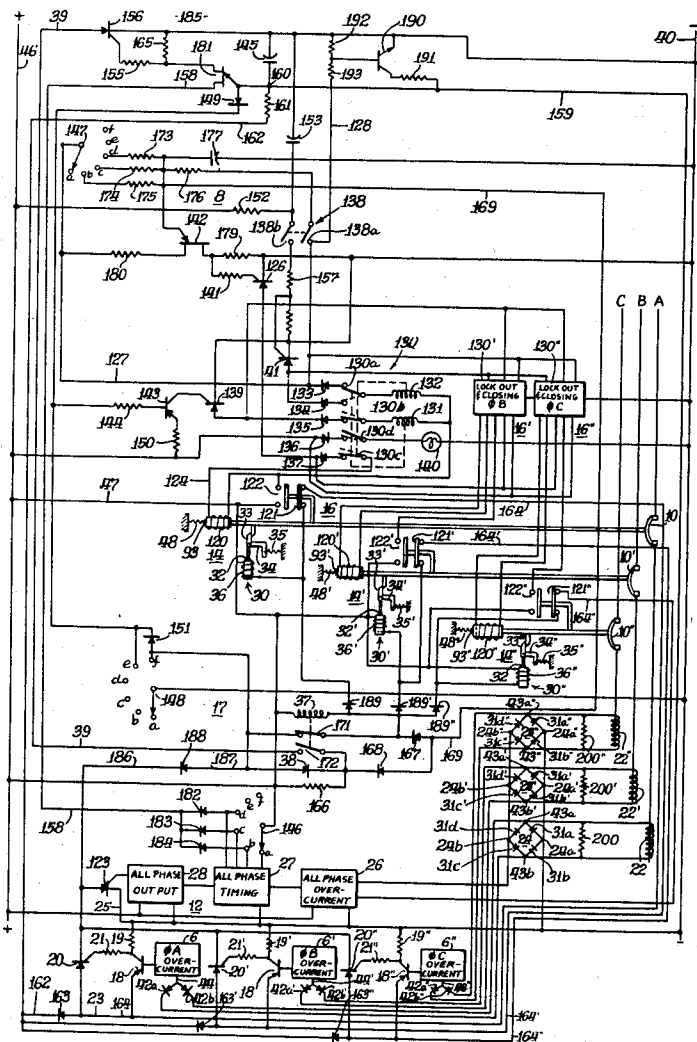
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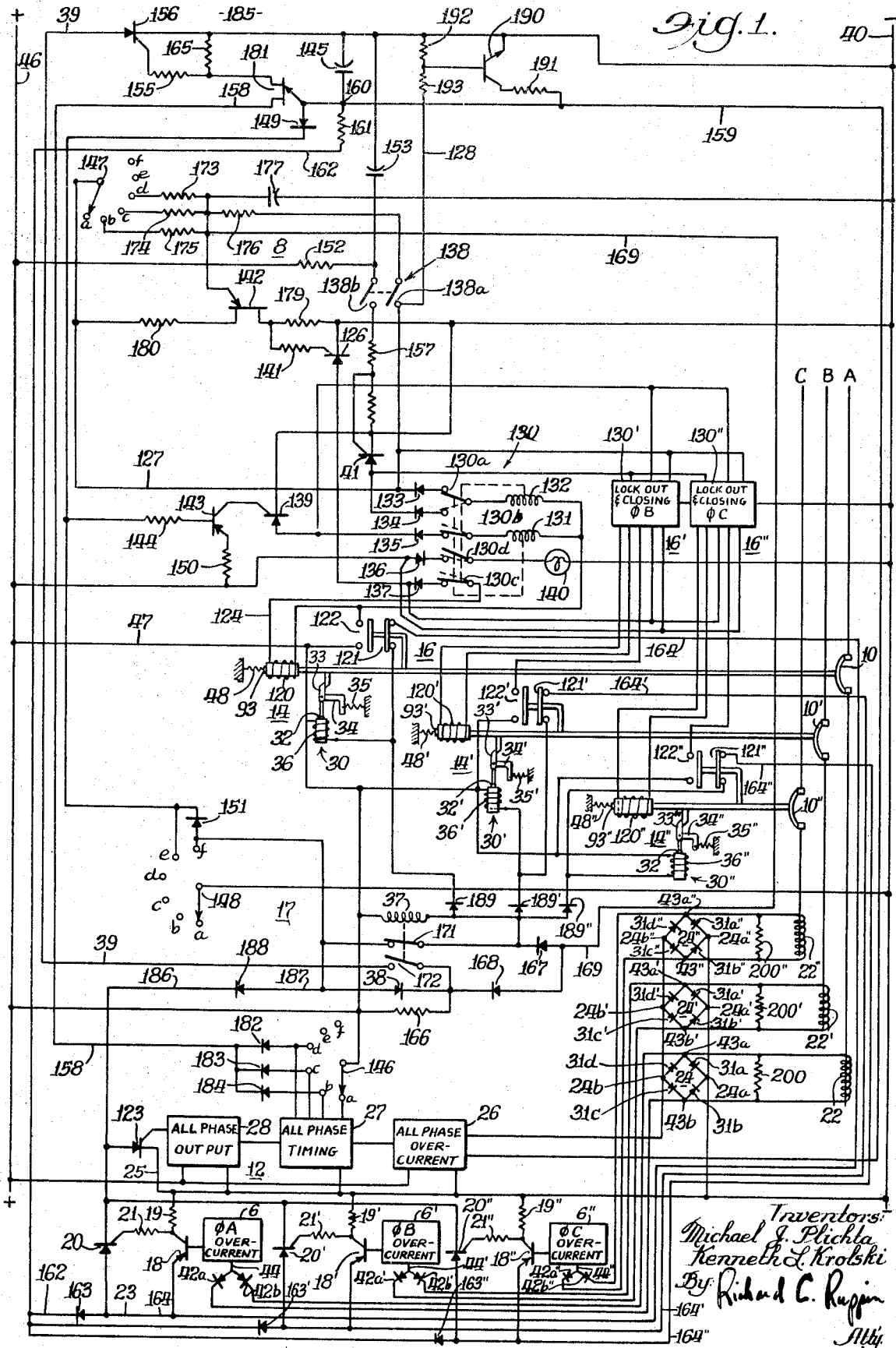
[54] **THREE PHASE REPEATING CIRCUIT
INTERRUPTER HAVING CONTROL MEANS FOR
INDIVIDUALLY INTERRUPTING EACH PHASE**
24 Claims, 2 Drawing Figs.

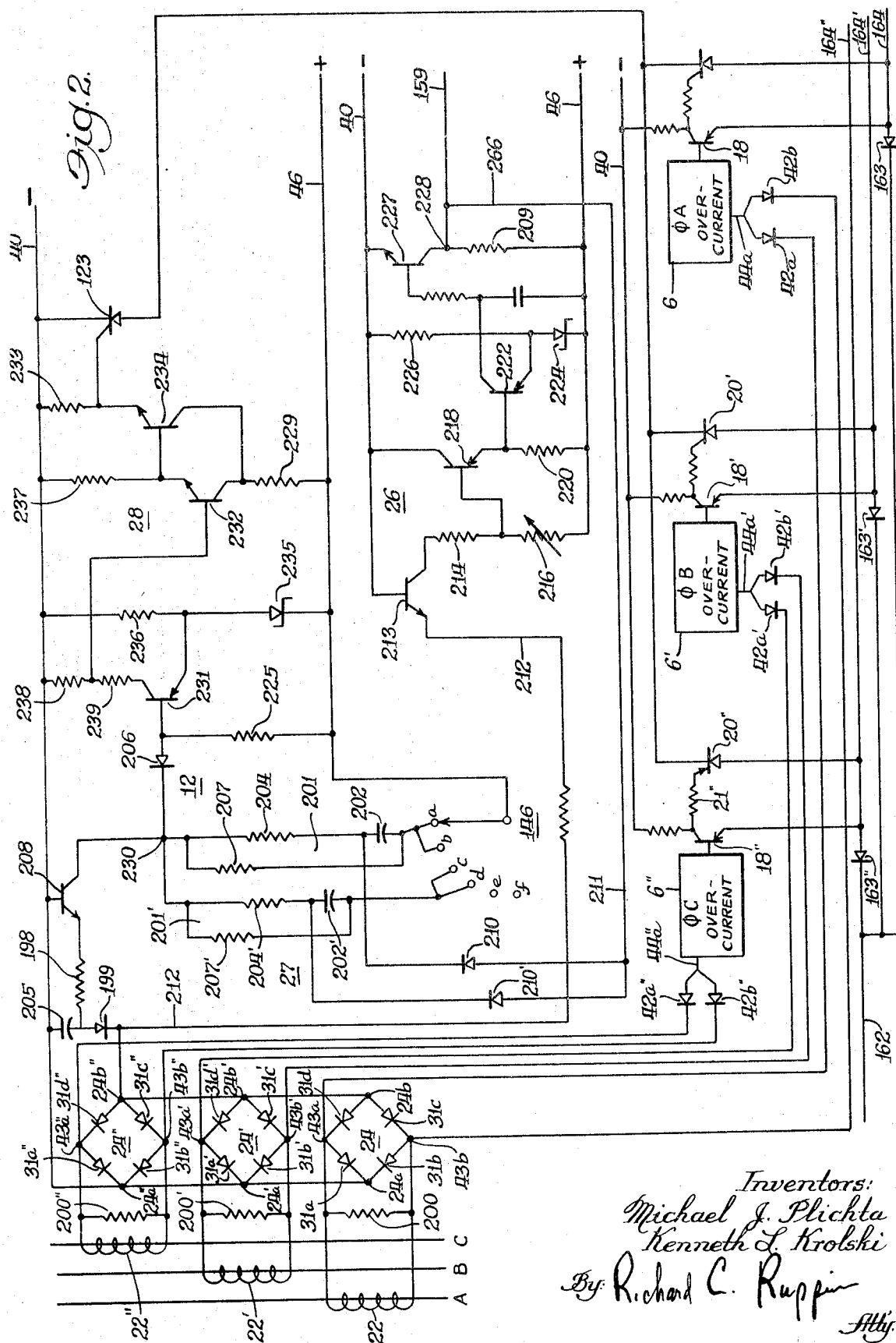
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[50] Field of Search 317/22, 24,
36

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3,191,096 6/1965 Frank 317/24X
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ABSTRACT: A three phase repeating circuit interrupter having an independently operable main switch means for each phase and a control means for separately opening and reclosing each switch means in response to an overcurrent condition in the phase associated with that switch means and without disturbing the closed condition of the other switch means. A separate overcurrent detecting circuit is provided for each phase and a common overcurrent detecting circuit and opening time delay circuit is provided for all phases. When an overcurrent condition is detected by one of the individual phase overcurrent detecting circuits and also by the common phase overcurrent detecting circuit, both circuits produce an output which causes opening of the main switch means in the faulted phase after a predetermined time delay provided by the opening time delay circuit. Common reclosing time delay means, closing means, sequencing means and reset means are provided for each phase. A faulted phase main switch is opened a predetermined number of times after a time delay provided by the common time delay means and reclosed a predetermined number of times after a time delay provided by the common reclose time delay means, the number of such opening and reclosing operations being determined by the common sequencing means. When the full sequence of a faulted phase is completed, its associated lockout means will lock a phase main switch means open while the other phase switch means continue closed. In the event that the fault on a phase clears before the full sequence is completed, the associated main means remains closed and the control circuit is reset after a predetermined time delay to its normal operating condition.







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THREE PHASE REPEATING CIRCUIT INTERRUPTER HAVING CONTROL MEANS FOR INDIVIDUALLY INTERRUPTING EACH PHASE

This invention relates to repeating circuit interrupters and, more particularly, to new and improved control means for individually controlling the main switch means of each phase in a polyphase repeating circuit interrupter.

A repeating circuit interrupter or recloser may be characterized as a circuit protective device having abnormal condition sensing means connected to the system being protected and which is responsive to abnormal circuit conditions to initiate a switch opening operation, switch reclosing means operable after each opening operation, opening time delay means, operation counting or sequencing means which is operable to initiate a predetermined number of time delayed switch opening and time delayed switch closing operations and lockout means to prevent reclosing after the predetermined number of operations is completed. In three phase circuit interrupters, the above operations may be performed to effect opening of all three phases, only one phase, and in some types of devices, only the faulted phase until lockout occurs when all three phases are opened.

Because the majority of faults in this type of system are temporary in nature and will clear in a relatively short period of time, it is common to arrange the switch opening means of the repeating circuit interrupter to execute a series of relatively rapid opening operations so that the period in which the system remains energized is shorter than the time necessary for down line protective devices, such as fuses, to operate. In addition, the circuit interrupter contacts should not be closed immediately in order to allow the backup fuses to cool. If the fault does not clear during this initial series of rapid operations, the time delay means is actuated by the sequencing means so that there follow further operations in which the recloser's contacts remain closed for a period of sufficient length to allow the down line protective devices to operate. If the fault still has not cleared after a predetermined number of such time delayed operations, it is considered permanent and the lockout means is actuated to prevent further operation of the reclosing means so that the device is locked open. On the other hand, should the fault be cleared during any of the rapid or time delayed operations, it is necessary for the sequencing means to be reset to its initial position or stage so that upon the occurrence of a subsequent fault, the recloser will execute the full number of rapid and time delayed operations prior to locking the device open.

The foregoing discussion applies equally to single phase repeating circuit interrupters and to three phase repeating circuit interrupters having a main switch for interrupting each phase. Prior art three phase repeating circuit interrupters or reclosers include both the type where the main switches of all three phases operate when a fault current occurs in only one of the three phases and the type in which only the main switch of the faulted phase is opened, reclosed and locked out while the main switches in the other phases continue to be closed. However, presently known three phase reclosers in which the main switch of each phase is independently controllable and operable usually require a full control circuit for the operation of each phase main switch which is completely independent and duplicative of the control circuits for each of the other phases.

It is an object of this invention to provide a three phase recloser having electroresponsive control means for effecting a sequence of opening and reclosing operations of one or more of the three phases without affecting the continued operation of the remaining phases and, after the sequence is completed, open circuiting said one phase to effect lockout thereof while the remaining phases continue in operation.

Another object of this invention is to provide a three phase recloser having independently controllable and operable switches for each phase and electroresponsive control means commonly utilizable in the independent control of the switches of all three phases.

A further object of this invention is to provide a three phase recloser having individual phase switches, a time delay means for providing an opening time delay for any of the phase switches and means for separately utilizing the time delay in the control of the opening operation of any one of the phase switches.

Another object of this invention is to provide a three phase recloser having individual phase switches, a time delay means for providing a closing time delay for any of the phase switches and means for separately utilizing the closing time delay in the control of the closing operation of any one of the phase switches.

Another object of the invention is to provide a three phase recloser having individual phase switches and lockout control means for effecting the lockout of an individual phase switch while the other phase switches remain closed.

Another object of the invention is to provide a three phase recloser having individually operable phase switches and control means responsive to an overcurrent condition in any one phase which includes opening time delay means and resetting means for restoring the control means to its normal condition after termination of the overcurrent condition in the one phase independently of the operation of the switches of the other phases.

A more specific object of the invention is to provide a three phase repeating circuit interrupter having individually operable phase switches and electroresponsive control means for independently effecting operation of each phase switch and having opening time delay means, closing time delay means, sequencing means and reset timing and actuation means all commonly utilizable in controlling the operation of any one or more of the phase switches.

Another more specific object of the invention is to provide a three phase repeating circuit interrupter having individual phase switches for each phase and separate condition indicating means for each phase switch.

These and other objects and advantages of the instant invention will become more apparent from the detailed description thereof taken with the accompanying drawings, in which:

FIG. 1 schematically illustrates a three phase repeating circuit interrupter incorporating the instant invention; and

FIG. 2 schematically illustrates in greater detail a portion of the repeating circuit interrupter shown in FIG. 1.

Referring now to the drawings in greater detail, FIG. 1 shows a three phase repeating circuit interrupter or recloser having individual phase main interrupting switches 10, 10' and 10'', common overcurrent responsive means 12, individual phase overcurrent means 6, 6' and 6'', individual switch opening means 14, 14' and 14'', common phase closing time delay means 8, individual phase switch closing and lockout means 16, 16' and 16'' and common sequencing means 17. In general terms, the common overcurrent responsive means 12 and any one of the individual phase overcurrent and switch opening means are operable together when an overcurrent condition appears on one of the phase lines A, B or C to open any one or more of the phase interrupting switches 10, 10' or 10''. Upon this event, the reclosing and lockout means associated with the phase having its interrupting switch open is made operable to return the interrupting switch to its closed position after a reclosing time delay determined by the closing time delay means 8. The sequencing means 17 which performs an operation counting function and actuates the reclosing and lockout means to perform its lockout function, includes a sequencing or stepping relay drive coil 37 and step switches 146, 147 and 148.

For a more complete description of a circuit breaker operating mechanism typical of the mechanism usable with the illustrated control circuit, reference is made to U.S. Pat. No. 3,295,017, issued Dec. 27, 1966, and assigned to the assignee of the instant invention.

The common overload responsive means 12 is shown coupled to each phase of the polyphase system being protected and includes an all phase common overcurrent portion 26, an

all phase common timing portion 27 and an all phase common output portion 28. The phase A, phase B and phase C overcurrent sensing and output means 6, 6' and 6'' are respectively connected to phases A, B and C of the polyphase system through current transformers 22, 22' and 22''. It should be noted that the separate elements in each of the phases, such as phase A, B and C overcurrent means 6, 6' and 6'', the individual switch opening means 14, 14' and 14'' and the individual phase reclosing and lockout means 16, 16' and 16'' are identical and, unless otherwise indicated, only the structure and operation of the phase A elements will be discussed. When a predetermined overcurrent is sensed in phase A by the phase A overcurrent means 6, a signal is produced at the base of its output PNP transistor 18 which causes transistor 18 to be turned to an "on" condition. The collector of transistor 18 is connected to the negative bus 40 through resistor 19 which functions to set the output voltage of transistor 18. When transistor 18 conducts, current from its collector provides a gating signal to output silicon controlled rectifier 20 through current limiting resistor 21. However, controlled rectifier 20 will not yet conduct since it is series connected with trip controlled rectifier 123 which has not yet been rendered conductive. When a predetermined overcurrent is sensed in one or more of the phases A, B and C by overcurrent sensing portion 26 of the common overcurrent responsive means 12, a signal is provided to the timing portion 27 and, after a predetermined time delay, the output portion 28 receives a signal and in turn provides a gating signal for trip controlled rectifier 123. The anode-cathode circuit of output controlled rectifier 20 is serially connected between the anode of trip controlled rectifier 123 and the positive bus 46 through conductor 23, contacts 121, trip coil 36 and conductor 47. The stepping relay drive coil 37 and isolating diode 189 are also connected between the positive bus 46 and controlled rectifier 20 in parallel with trip coil 36. As is shown in FIG. 1, the switch opening means 14 includes a coil 36 and an electromagnetic tripper 30 having a plunger 32. The plunger 32 is mechanically coupled to a latch crank 33 which is normally urged in a clockwise direction about pivot point 34 by a reset spring 35 to hold the main switch 10 in closed position against the influence of an opening spring 48. As stated hereinabove, a gating signal is provided to both output controlled rectifier 20 and trip controlled rectifier 123 upon the occurrence of an abnormal current condition in any of the phases A, B or C. When both controlled rectifiers 20 and 123 are gated, they will both conduct and complete a circuit to negative bus 40 through conductor 25 to energize the trip coil 36. Energizing of coil 36 causes rotation of crank 33 counterclockwise to release the main switch 10 for movement toward its open position under the influence of opening spring 48. When the main switch 10 is open, its contacts 121 are also open so that controlled rectifier 20 will no longer conduct and coil 36 will be deenergized. It should be noted that isolating diodes 189, 189' and 189'' respectively prevent the energization of trip coil 36, 36' and 36'' through a phase overcurrent circuit other than that with which each trip coil is associated. When trip coil 36 is deenergized, the crank 33 is returned to its initial position by reset spring 35. The switch opening means 14 is thereby reset in a position to relatch the main switch 10 when it is returned to its closed position. It may be pointed out that the anodes of the output controlled rectifiers 20, 20' and 20'' are respectively connected to the switch opening means 14, 14' and 14'' for individually opening the phase A switch 10, the phase B switch 10' and the phase C switch 10''. However, the cathodes of the controlled rectifiers 20, 20' and 20'' are directly connected to the anode of the trip controlled rectifier 123 so that each of the phase switches may be tripped and opened by completion of the trip circuit through controlled rectifier 123 when the individual phase overcurrent means senses an overcurrent condition.

Before continuing with the discussion of the overcurrent sensing portions of the device, the operation of the common sequencing means 17 will be mentioned briefly. Sequencing

means 17 is schematically illustrated in FIG. 1 to include the stepping relay drive coil 37 and step switches 146, 147 and 148 although any well known type of mechanical or static stepping device may be employed. The sequencing means 17 has a plurality of sequentially operable stages symbolized by the coil 37, a movable wiper and taps or stages *a-f* for each of the step switches. Each time coil 37 is energized it is operable to simultaneously advance each wiper one tap from *a-f* and back to *a*. The tap *a* may be considered as the initial stage and the taps *e* and *f* as the final stage of the sequencing means 17. While it may appear from the schematically illustrated step switches that circuit through each will be momentarily opened when their wipers are between position, in actual practice the switches are of a type wherein the wiper bridges over to the next contact before moving off of a previous one so that circuit integrity is maintained.

Because the stepping relay drive coil 37 is connected in parallel with trip coils 36, 36' and 36'' between the anodes of output controlled rectifiers 20, 20' and 20'' and the positive bus 46, as previously mentioned, said coil 37 will be energized when trip controlled rectifier 123 and any one of the controlled rectifiers 20, 20' or 20'' conduct. Thus, each time any one of the main switches 10, 10' or 10'' execute an opening operation, the coil 37 will advance each of the stepping switches 146, 147 and 148. The stepping relay coil 37 also includes contacts 171 and 172 and the coil 37 is connected through these contacts, isolating diode 38 and conductor 39 to reset controlled rectifier 156. As will be discussed in more detail hereinafter, the coil 37 is energized through the contacts 171, 172 and reset controlled rectifier 156 when reset rectifier 156 is gated to advance the step switches 146, 147 and 148 to their initial or normal positions at stage *a* after the step switches have been advanced to one of their states *b-d* and an overcurrent condition is no longer sensed on any of the phase lines A, B or C.

FIG. 2 shows the details of the overcurrent sensing portion 26, the timing portion 27 and the output portion 28 of the common overcurrent responsive means 12. Overcurrent responsive means 12 is coupled to the respective phases A, B and C by current transformers 22, 22' and 22'' and corresponding full wave rectifiers 24, 24' and 24'' whose output terminals 24a and 24b, 24a' and 24b' and 24a'' and 24b'' are connected in parallel. The rectifier 24 includes diodes 31a, 31b, 31c and 31d and the rectifiers 24' and 24'' include similar diodes. The rectifier 24 has its terminals 43a and 43b respectively connected to the diodes 42a and 42b of phase A overcurrent means 6 and the rectifiers 24' and 24'' are similarly connected to overcurrent means 6' and 6''. Resistors 200, 200' and 200'' are connected across each of the secondaries of current transformers 22, 22' and 22'' respectively so that a voltage will be derived across each which is proportional to the current in their phases. The drop across resistors 200, 200' and 200'' respectively appears between the diodes 42a and 42b, 42a' and 42b' and 42a'' and 42b'' of the individual phase overcurrent portions. The largest of the drops across resistors 200, 200' and 200'' appears across filter capacitor 205 and diode 199.

The timing portion 27 of circuit 12 includes a first timing circuit 201 connected to taps *a* and *b* of step switch 146 and a second timing circuit 201' connected to taps *c* and *d* of said switch. The timing circuits 201 and 201' are identical except for the size of their components, which determine their time delay characteristics and, accordingly, only timing circuit 201 will be discussed in detail, for the sake of brevity. Circuit 201 is shown to include a timing capacitor 202 connected in series with a timing resistor 204 and the series combination connected in parallel with a second timing resistor 207. It will be readily understood by those skilled in the art that the impedance values of capacitor 202 and resistors 204 and 207 determine the charging time for any given fault current. Under normal operating conditions, step switch 146 will be initially connected to tap *a*, so that timing circuit 201 will govern the first opening operation.

In operation, the current flowing to the collector of the charging transistor 208 and through current limiting resistor 198, across capacitor 205, will split between the parallel paths defined by the timing resistor 207 and the series combination of timing resistor 204 and timing capacitor 202. When there is no fault in any of the phases, capacitor 202 is prevented from charging because it is shunted by resistor 209 in overcurrent sensing portion 26 to which it is connected by diode 210 and conductor 211. As a result of this leakage current, the junction 228 adjacent the collector of transistor 227 and the junction 230 adjacent the cathode of diode 206 both have a positive potential close to that of the positive bus 46. The diode 206 serves to prevent stressing of the transistor 231 by the positive bus 46 potential.

The current flowing from the overcurrent sensing portion 26 through conductor 212 is also proportional to the highest peak current in any of the phases A, B or C and results in a proportional transistor 213 collector current flowing through resistors 214 and 216. This produces a potential on the base of transistor 218 which is also proportional to said peak current. Transistor 218 draws emitter current proportional to this potential through a resistor 220 so that its emitter potential is also proportional to said peak current. The emitter comparing transistor 222 is held at a fixed potential by a Zener diode 224 and a resistor 226 while its base is connected to the emitter of transistor 218. Thus, by a proper selection of components, transistor 222 can be rendered conductive when the current of any of the phases A, B or C equals or exceeds the desired minimum actuating current of the device. It may be noted that it is desirable to have the common overcurrent sensing means 12 detect an overcurrent condition in any of the phases at a level somewhat higher than a phase overcurrent is detected by one of the individual phase overcurrent means 6, 6' and 6''. This relationship may be obtained by a component selection and adjustment which allows the common overcurrent sensing means 12 to detect an overcurrent condition at a higher value in the overcurrent wave shape. Conversely, the components of the phase overcurrent means 6, 6' and 6'' may be selected and adjusted such that they detect an overcurrent condition at an earlier time and a lower value in the wave shape of the overcurrent.

Upon the occurrence of an overcurrent in the system, transistor 222 becomes conductive, passing current to the base of an output transistor 227. Upon the latter event, transistor 227 will become conductive to connect the leakage resistor 209 to the negative bus 40. This, in turn, causes junction 228 to assume a negative potential so that resistor 209 no longer effectively shunts capacitor 202. As a result, timing capacitor 202 will begin charging. In this manner, the timing operation is initiated. Diodes 210 and 210 performs the function of preventing reverse current flow from timing capacitor 202 to junction point 228.

As timing capacitor 202 charges up, the potential at the junction point 230 drops to a value below that existing while timing capacitor 202 was shunted by resistor 209. Since this lower voltage value also appears at the base of PNP transistor 231 across resistor 225, the transistor 231 will conduct when the voltage drops below the voltage on its emitter which is held at a fixed value by the resistor 236 and Zener diode 235. When transistor 231 conducts, its collector current flows through resistors 238 and 239 and produces a potential on the base of transistor 232. The emitter current from transistor 232 flows through resistor 237 and produces a voltage at the base of transistor 234 which causes it to conduct a current from positive bus 46 through resistor 229 and resistor 233 to the negative bus 40. The current flowing through resistor 233 produces a potential at the gate of trip controlled rectifier 123. If an overcurrent condition has been detected by any one of the individual phase overcurrent means and a gating signal provided to the corresponding overcurrent sensing means output controlled rectifier 20, 20' or 20'', an energizing circuit will be completed to the trip coil of the phase having the overcurrent condition, as previously discussed. In addition, the

stepping relay coil 37 will also be energized and the step switch 146 will be moved to stage *b*, so that the time delay circuit 201 will be effective during the second switch opening operation. Should the fault persist, requiring a third and fourth opening operation, the switch 146 will be moved to stages *c* and *d*, so that the time delay circuit 201' will be effective, whereby the third and fourth operations may have a longer time delay than the initial operation.

Because each of the phase overcurrent means 6, 6' and 6'' are identical with the common phase overcurrent sensing portion 26, except for the size and adjustment of some components, they will not be discussed in detail for the sake of brevity. It is sufficient for an understanding of the invention to state that when a fault current occurs in phase A, a voltage proportional to the fault current will appear across terminals 43a and 43b and this voltage will be rectified by the diodes 31a, 31b, 42a and 42b so that a substantially constant DC voltage proportional to the fault current appears at the input 44a of the phase A overcurrent means 6. The input 44a of phase A overcurrent sensing means 6 is connected to an input transistor corresponding to the input transistor 213 of the common overcurrent sensing portion 26 and an output signal is produced to the output transistor 18 by the conducting of a transistor corresponding to the output transistor 227 of the overcurrent sensing portion 26.

The reclosing and lockout means 16 includes a closing coil 120, normally open contacts 122 which are mechanically connected to the main switch 10 and lockout latching relay 130. A common reclose controlled rectifier 126 is provided and has its cathode connected to the negative bus 40 and its anode connected to each of the individual phase lockout latching relays 130, 130' and 130''. The conductor 47 connects one side of the contacts 122 to the positive bus 46 and the other side of the contacts 122 are connected to the closing coil 120, the lockout coil 131 and the arm coil 132. The coils 131 and 132 both comprise part of the lockout latching relay 130. The lockout latching relay 130 also includes a single-pole double-throw switch 130a and single-pole single-throw switches 130b13 c, which are mechanically operated by either the lockout coil 131 or the arm coil 132. The contacts 130a—d are in their normal conditions, as shown in full lines in FIG. 1, when the main switch 10 is not in its locked out condition. The contacts are moved to their lockout position, shown in dashed lines, when the lockout coil 131 is energized to effect lockout of main switch 10. The diodes 133, 134, 135, 136 and 137 are connected to switches 130a—d and function to isolate the elements of phase A reclosing and lockout means 16 from phase B and phase C reclosing and lockout means 16' and 16'' through their common connections. One end of the closing coil 120 is connected through conductor 124 and normally closed contacts 130c of lockout latching relay 130 to the anode of closing controlled rectifier 126. The gate of the closing controlled rectifier 126 is connected through the current limiting resistor 141 to base-one of reclosing unijunction transistor 142 of the closing time delay means 8. As will be later discussed in greater detail, the closing time delay means 8 is effective after the main switch 10 opens to provide a time delay and then produce a gating signal to reclose controlled rectifier 126. When the main switch 10 is in its closed position, contacts 122 are open so that the circuit from positive bus 46 to negative bus 40 through closing coil 120 and reclose controlled rectifier 126 is also open. In addition, when the contacts 122 are open the circuit from positive bus 46 through the arm coil 132 and the normally closed contacts 130a of the lockout latching relay 130 to step switch 147 is also open. When the main switch 10 reaches its fully open position, the contacts 122 close to complete the circuit from positive bus 46 through the closing coil 120 to the anode of reclose controlled rectifier 126 and also complete an energizing circuit through stepping switch 147 to closing time delay means 8. After a reclose time delay, the reclose controlled rectifier 126 is gated to complete the energizing circuit through closing coil 120 to the negative bus 40. Energizing of closing coil 120

moves the magnetic plunger 93 toward the right as seen in FIG. 1 to close the main switch 10 and extend the opening spring 48, thereby storing energy for the succeeding opening operation. Also, contacts 122 are opened to deenergize the closing coil 120 and the closing time delay means 8.

The closing time delay means 8 is shown in FIG. 1 to include a resistor-capacitor timing circuit comprising resistors 173, 174, 175 and 176 and capacitor 177. One end of each of the resistors 173, 174 and 175 is respectively connected to taps *d*, *c* and *b* of the stepping switch 147 and the resistor 176 has an end connected to the normally open contacts 138a of manual switch 138. The timing capacitor 177 has its negative terminal connected to the negative bus 40 and its positive terminal connected to each of the resistors 173—176 and to the emitter of reclose unijunction transistor 142. Base-one of reclose unijunction transistor 142 is connected through current limiting resistor 179 to the negative bus 40 and base-two of transistor 142 is connected through bias setting resistor 180, conductor 127, lockout latching relay contacts 130a and main switch contacts 122 to the positive bus 46. As previously stated, the base-one of reclose transistor 142 is also connected to the gate of reclose controlled rectifier 126.

Upon the initial operation of the repeating circuit interrupter, each of the switches 146, 147 and 148 will be at stage *a*. When a fault current occurs on one of the phase lines A, B or C, the output portion 28 of common overcurrent responsive means 12 will produce a gating signal causing trip controlled rectifier 123 to conduct and effect energization of the trip coil 36 and the sequence relay drive coil 37 through the closed contacts 121 of main switch 10. Energizing of the coil 36 causes the main switch 10 to trip open and energizing of the coil 37 advances each of the stepping switches 146, 147 and 148 one step to their *b* stages. The movement of switch 147 to its *b* tap completes an energizing circuit through the now closed contacts 122, arm coil 132, contacts 130a to timing resistor 175 and timing capacitor 177. When the timing capacitor 177 charges to the triggering potential of reclose transistor 142, transistor 142 will conduct to gate reclose controlled rectifier 126. The controlled rectifier 126 will then conduct to cause energizing of closing coil 120 and the reclosing of main switch 10.

Should the fault persist, the output portion 28 will again gate the trip controlled rectifier 123 to energize trip coil 36 and sequence relay drive coil 37. The main switch 10 will again be opened and the step switches 146, 147 and 148 will each be advanced to their stages *c*, whereupon the resistor 174 and capacitor 177 will be energized to cause conduction of reclose controlled rectifier 126 and reclosing of the main switch 10 after a time delay. Similarly, should the fault persist after the second reclosing operation, the trip coil 36 and sequence relay drive coil 37 will be energized after a relatively long time delay to again open the main switch 10 and advance the stepping switches to their *d* stages. The reclose controlled rectifier 126 will again conduct and the closing coil 120 will be energized to reclose the main switch 10 after a time delay provided by the energizing of resistor 173 and charging of capacitor 177. If the fault continues after the third closing operation, the trip coil 36 will again be energized to cause opening of the main switch 10 and the sequence relay drive coil 37 will advance each of the stepping switches to their states *e*. It may be seen in FIG. 1 that diode 167 is connected between the closing time delay means 8 and the anodes of diodes 189, 189' and 189''. The diode 167 functions to maintain reclose timing capacitor 177 in a discharged condition so that a reclose operation cannot take place while a tripping operation is occurring. This is important where tripping of one phase is occurring and it is not desired to reclose that phase with the reclosing of another phase.

It can be seen in FIG. 1 that the *e* taps or stages of switches 146 and 147 are unconnected so that these switches do not perform a function when they advance to the *e* stages. However, the advancement of switch 148 to its *e* stage causes a circuit to be completed from the negative bus 40 to the reset tim-

ing capacitor 145 through isolating diode 149 and to the base of lockout transistor 143 through bias setting resistor 144. Connection of the reset timing capacitor 145 to the negative bus 40 at this time prevents charging of the capacitors 145 and the occurrence of a control reset operation while the control device is in the process of locking open a main switch. Completion of the circuit to transistor 143 causes it to conduct and complete a circuit from positive bus 46 through current limiting resistor 150 to the gate of lockout controlled rectifier 139. When the lockout controlled rectifier 139 is gated, the lockout coil 131 of lockout latching relay 130 is energized through the contacts 122, which are now closed since the main switch 10 is open, and the normally closed contacts 130b of the lockout latching relay 130 so that the lockout coil 131 switches each of the contacts 130a, 130b, 130c and 130d from their normal to their lockout positions. It should be noted that the contacts of the lockout latching relay 130 are mechanically latched in either their normal or lockout positions until switched from one position to another by energizing of the proper coil. In their lockout positions, the contacts 130a connect the arm coil 132 to the anode of the arm controlled rectifier 41. The contacts 130b deenergize the lockout coil 131 after it has moved the contacts to their lockout positions and the contacts 130d close to complete a circuit through the lamp 140 so that it will become energized and indicate that the main switch 10 has completed an opening and closing operation sequence and is in its locked open condition. The contacts 130c open so that the closing coil 120 can no longer be energized through the reclose controlled rectifier 126 in the event that it conducts to allow energization of the closing coils associated with reclosing and lockout means 16' and 16''. It should be understood that only the lockout latching relay 130 is tripped to a lockout position and the operation of the reclosing and lockout means 16 will not affect the reclosing and lockout means 16' and 16'' associated with phases B and C.

In addition to completing a circuit which allows locking open of the main switch 10, the advancement of stepping switch 148 to its stage *e* also completes a circuit from the positive bus 46 through the sequence relay drive coil 37, its normally closed contact 171 and isolating diode 151 to the negative bus 40. The coil 37 is thereby energized and advances the stepping switches 146, 147 and 148 one step to their *f* stages. The stepping switches are advanced one step only because the sequence relay contact 171 opens when the drive coil 37 is energized to deenergize the coil 37. When the coil 37 is deenergized, the contact 171 will again close to complete an energizing circuit through the *f* stage and wiper of stepping switch 148 to the negative bus 40. This causes advancement of the stepping switches 146, 147 and 148 to their *a* stages so that they are again in a position to operate in the event of a fault current occurring on the phase B or phase C line. The isolating diode 151 serves to prevent a second energizing of the circuit to lockout transistor 143 and reset timing capacitor 145 when the switch 148 moves to its *f* stage.

After the lockout latching relay 130 has been tripped to its lockout position to lock the main switch 10 open, the switch 10 can be reclosed only by use of the manual switch 138. The manual switch 138 has a normally open contact 138a, which was previously mentioned and a second normally open contact 138b. One side of the contacts 138b are connected to a resistor-capacitor charging circuit comprising resistor 152 and capacitor 153 serially connected between the positive bus 46 and the negative bus 40. The other side of contacts 138b are connected through current limiting resistor 157 to the gate of arm controlled rectifier 41. The contacts 138a of manual switch 138 have one side connected to positive bus 46 through contacts 130a, arm coil 132, and contacts 122 when the relay 130 and main switch 10 are respectively in their normal and open positions. The other side of contacts 138a is connected through reclose time delay resistor 176 and time delay capacitor 177 to the negative bus 40. As previously stated, the resistor 176 and capacitor 177 are also both connected to the emitter of reclose unijunction transistor 142. When the

manual switch 138 is operated, the contacts 138a and 138b each close to complete two related circuits which result in closure of any locked out main switch, e.g., switch 10. When the contacts 138b are closed, the reset capacitor 153 discharges to gate the arm controlled rectifier 41 and cause it to conduct through a circuit including the closed contacts 122, the arm coil 132 and contacts 130a, as shown in their locked out dashed line position in FIG. 1. The arm coil 132 is thus energized and moves all of the contacts of lockout latching relay 130 to their normal positions in which they are mechanically latched. A circuit is thus completed from the positive bus 46 through the closed contacts 122 of switch 10, the closing coil 120, the closed contacts 130c of the relay 130 to the anode of reclose controlled rectifier 126. Closing of the contacts 138a of the manual switch 138 completes an energizing circuit from the positive bus 46 through the contacts 122 of the switch 10, the arm coil 132 and the contacts 130a in their normal position to the reset timing resistor 176 and capacitor 177. When the timing capacitor 177 charges to the potential required to trigger the reclose unijunction transistor 142, it will conduct and provide a gating signal to reclose controlled rectifier 126. The controlled rectifier 126 will then conduct to energize the closing coil 120 so that the switch 10 closes, the contacts 122 open and the contacts 121 close. The reclosing and lockout means 16 is now in its normal condition in which it is prepared to control a sequence of reclosing operations and lock the main switch 10 in an open condition at the end of the reclosing sequence.

It will be recalled that the recloser will cycle itself to lockout only if the fault current persists for a predetermined number of opening and closing operations. The number of such operations is determined by the number of stages through which the step switch 148 may be moved before it gets to the stage which will cause energization of the lockout coil 131 of the lockout latching relay 130 and the consequent locking of the main switch 10 in its open position. FIG. 1 shows the step switch 148 to have four stages, a, b, c and d, which allow four opening and closing operations before the switch 148 reaches its e stage at which the lockout latching relay 130 is energized and tripped to its lockout position. Sequence relays including switches such as step switch 148 are well known in the art and are adjustable to provide more or less than four operations. In order to reset the recloser should the fault clear after a lesser number of opening and closing operations as determined by stepping switch 148, a resetting circuit 185 is provided. The resetting circuit 185 includes the reset controlled rectifier 156, a reset unijunction transistor 181 and a reset time delay circuit comprising the timing capacitor 145 and resistor 161. The cathode of reset controlled rectifier 156 is connected to negative bus 40 and the sequence relay contacts 171 and 172 and drive coil 37 are serially connected between the positive bus 46 and the anode of controlled rectifier 156 by conductor 39. Conductor 162 connects the reset timing resistor 161 and capacitor 145 through isolating diodes 163, 163' and 163'' to the contacts 121, 121' and 121'' of the main switches 10, 10' and 10''. Thus, when any one of the main switches is closed, a charging circuit from the positive bus 46 through the trip coil 36 is completed to the resistor 161 and capacitor 145. The positive bus 46 is also connected to base-two of reset transistor 181 through conductor 158, diodes 182, 183 and 184 and stepping switch 146 whenever switch 146 is at one of its stages b, c or d. The junction 160 between timing capacitor 145 and resistor 161 is connected by conductor 159 to junction 228 of overcurrent sensing portion 26 so that when a fault exists on one of the phase lines and the output transistor 227 is conducting, the reset timing capacitor 145 will be prevented from charging (see FIG. 2).

Assume, for example, that a fault current occurs in phase A and that after two opening and two reclosing operations, the fault condition disappears. The main switch 10 will be closed so that its contacts 121 are closed and the step switches 146, 147 and 148 will be at their c stages. When the stepping switch 146 is at its c stage, a circuit is completed from the positive bus

46 through conductor 158 to base-two of reset transistor 181 so that it will conduct when a triggering potential is applied to its emitter. Since the contacts 121 are closed when the switch 10 is closed, a circuit is completed from positive bus 46 through the trip coil 36, conductor 164 and conductor 162 to the reset timing circuit so that timing capacitor 145 charges. Since the fault current has cleared, transistor 227 of overcurrent sensing portion 26 will not be conducting so that capacitor 145 is not prevented from charging. When capacitor 145 charges to the trigger potential of unijunction transistor 181, it conducts and current flows through bias setting resistor 165 to the negative bus 40 and through current limiting resistor 155 to the gate of reset controlled rectifier 156. Conducting of controlled rectifier 156 completes a circuit from the positive bus 46 through the sequence relay coil 37, sequence relay contact 171, contact 172, which is closed only when the step switches of the sequence relay 37 are not in their normal positions at stages a, and conductor 39 to the negative bus 40. The coil 37 is thus energized to advance the step switches one step to their d stages. The coil 37 will advance the step switches one step only because the contact 171 will open when the coil 37 is energized to deenergize it, as previously discussed. A holding current resistor 166 is connected in parallel with the coil 37 and contact 171 between the positive bus 46 and contact 172 so that the reset controlled rectifier 156 will continue to be energized even though the contact 171 opens to deenergize coil 37. The isolating diode 38 prevents undesired charging of the reset timing circuit or conducting of the controlled rectifiers 20, 20' and 20'' from the positive bus through the holding current resistor 166. The holding current resistor 166 also allows the reset controlled rectifier 156 to continue conducting even after the step switch 146 moves to its e stage and the controlled rectifier 156 is no longer gated by the reset transistor 181. After the sequence relay coil 37 has been energized and advances the stepping switches to their d stages and the contact 171 has opened to deenergize the coil 37, the contact 171 will again close so that the coil 37 is energized through the contact 171, diode 38, contact 172, conductor 39 and controlled rectifier 156. The stepping switches are then advanced to their e stages and in the same manner to their f and a stages. When the stepping switches reach their a stages, the contact 172 will be opened and remain open so that the coil 37 is no longer energized to advance the step switches. The recloser control is now in its normal condition in which it provides full overcurrent protection to any phase line having its main switch closed.

The conditions for recycling of the recloser to its initial position by the resetting circuit 185 can be summarized as requiring that any one of the main switches 10, 10' and 10'' be closed so that one of their associated contacts 121, 121' and 121'' are also closed, that the overcurrent sensing portion 26 sense normal circuit conditions on the phases A, B and C and that the step switches be neither in their initial or lockout stages and that none of the main switches are open for a reclosing delay. These requirements allow resetting of the recloser control to its normal condition so that it may protect against any future circuit condition if any one phase switch is closed and that phase is functioning normally. Thus, faulted phases can be locked out and nonfaulted phases can continue to provide service while still being protected by the recloser control. In addition, the above requirement for resetting of the recloser control allows the resetting circuit 185 to operate independently of the opening and closing time delays respectively provided by the timing portion 27 and the closing time delay means 8.

As illustrated in FIG. 1, diode 168 is connected through conductor 169 between the closing time delay means 8 and contacts 172. The diode 168 functions to maintain reclose timing capacitor 177 in a discharged condition so that a reclose operation cannot take place while a resetting operation is occurring. The conductors 186 and 187, connected between the contacts 171 and the anode of trip controlled rectifier 123 divert any current flowing to the anode of reset

controlled rectifier 156 so that a reset operation is prevented while a tripping operation is occurring. The diode 188 prevents any current flowing to the anode of reset controlled rectifier 156 from also flowing through trip coil 36 and output controlled rectifier 20 and causing a trip operation.

In the event that a reclosing operation is initiated in one phase before the start of a control resetting operation, it is desirable to prevent the occurrence of the resetting operation until the reclosing operation is completed or lockout occurs. For this purpose, the serial combination of transistor 190 and current limiting resistor 191 are connected in parallel with reset timing capacitor 145 and function to shunt charging current to capacitor 145 so that it cannot trigger reset transistor 181. The base of transistor 190 is connected between bias setting resistors 193 and 192 which are, in turn, connected between the negative bus 40 and positive bus 46 through conductor 128, contacts 130a and arm coil 132 of relay 130, contacts 122 of switch 10 and conductor 47. It can thus be seen that when switch 10 is open, contacts 122 are closed and relay 130 has not tripped to its lockout position, so that switch 10 is about to be reclosed, a circuit through bias resistors 193 and 192 is completed and transistor 190 conducts to prevent a resetting operation.

Although a preferred embodiment of the invention has been illustrated and described, the disclosure is not to be interpreted as limiting, for the invention may be variously embodied and is to be construed in accord with the claims which follow.

We claim:

1. In a repeating circuit interrupter in circuit with a polyphase electrical system and having separate main switch means connected in each phase of said system, the combination of:

control means for opening any of said main switch means upon the occurrence of an abnormal current condition in the phase associated with the opened switch means and for closing the opened switch means; and

condition responsive means coupled to said polyphase system for detecting an abnormal current condition in any one of the phases of the system, said condition responsive means including a single time delay means operative when an abnormal current condition occurs in any of said phases to provide and opening time delay for the main switch means associated with the phase having said current condition and producing an output signal to actuate said control means after the opening time delay.

2. In a polyphase repeating circuit interrupter having separate main switch means connected in circuit with each phase of a polyphase electrical system, the combination of:

control means for opening any one of said switch means upon the occurrence of an abnormal current condition in an associated phase and for closing the opened switch means;

a single sequencing means responsive to the opening of any of said switch means and being operable to sequence said control means and only those switch means opened by said control means through a predetermined number of switch opening and closing operations; and

lockout means responsive to said sequencing means when said sequence of switch opening and closing operations has been completed to lock open only those switch means open at the completion of said sequence, whereby those switch means connected in phases not carrying an abnormal current will continue in a closed condition.

3. The combination according to claim 2 further comprising indicating means responsive to the lockout means for separately indicating only the locked open condition of each main switch.

4. The combination according to claim 2 wherein said lockout means includes relay means actuated by the sequencing means to prevent the control circuit from operating to close those switch means open after completion of said sequence of switch opening and closing operations.

5. The combination according to claim 2 wherein said lockout means includes relay means actuated by the sequencing means upon completion of said sequence of switch opening and closing operations and responsive to the open position of any switch means to disconnect the control means from any open switch means so that the opened switch means does not again close.

6. The combination according to claim 2 wherein:

said sequencing means has a plurality of stages including an initial stage at which it is positioned when current conditions are normal in all of said phases and a final stage at which the lockout means is actuated; and further comprising reset means operative in response to the closing of only one of said switch means when current conditions are normal in all of said phases and the sequencing means is between its initial and final stages to return the sequencing means to its initial stage.

7. The combination according to claim 6 wherein said reset means includes reset time delay means responsive to the closing of any one of said switch means to provide a time delay prior to the returning of the sequencing means to its initial stage.

8. The combination according to claim 2 wherein said sequencing means includes advancing means and a plurality of stages comprising an initial stage at which it is positioned when current conditions are normal in all of said phases and a final stage at which the lockout means is actuated and the advancing means is responsive to effect the return of the sequencing means to its initial stage so that the full sequence of opening and closing operations is again available in the event of the occurrence of an abnormal current condition in any of those phases having closed switch means.

9. The combination according to claim 8 wherein said advancing means comprises an energizing circuit connecting the sequencing means to an energy source when it reaches its final stage and being disconnected from the sequencing means when it reaches its initial stage so that the sequencing means is returned to its initial stage independently of the operation of the control means, lockout means and any of the switch means.

10. The combination according to claim 9 wherein:

said advancing means includes a drive means for advancing the sequencing means when energized; and

said energizing circuit includes a switch movable to a closed position when the drive means is deenergized and movable to an open position when the drive means is energized, said switch, drive means and the final stage of the sequencing means being serially connected to said energy source, said drive means being energized through the switch in its closed position when the sequencing means reaches its final stage whereby the sequencing means is advanced to its initial stage and the switch is moved to its open position, said drive means being deenergized when the switch moves to its open position to cause the switch to return to its closed position.

11. The combination according to claim 2 further comprising common time delay means connected to said control means and operative when an abnormal current condition occurs in any one of said phases to provide an opening time delay for only those switch means connected in a phase having an abnormal current condition and producing an output signal to actuate the control means at the end of the opening time delay.

12. The combination according to claim 11 wherein said control means includes circuit means responsive to the output signal from said common time delay means for limiting the operation of the control means to the opening of only those switch means connected in phases having abnormal current conditions.

13. The combination according to claim 12 wherein:

said polyphase system has three electrical phases and a separate main switch means connected in each phase; and

said circuit means includes first, second and third tripping means each corresponding to a main switch means and being responsive to the output signal from said common time delay means for initiating an opening operation of the corresponding switch means; and further comprising condition responsive means coupled to said system for detecting an abnormal current condition in any of said phases and for producing an actuating signal only to those tripping means corresponding to a main switch means connected in a phase having an abnormal current condition, said corresponding tripping means being actuated when the output and actuating signals from said common time delay means and condition responsive means coincide.

14. The combination according to claim 13 wherein said first, second and third tripping means have corresponding first, second and third switching means each having a nonconductive condition in which its corresponding tripping means is inoperative and a conductive condition in which its corresponding tripping means is operative, each of said switching means being in a nonconductive condition when the corresponding main switch means is closed and the phase in which it is connected is carrying a normal current, each of the switching means being connected to the connected to the condition responsive means and the common time delay means and being conductive in response to the simultaneous production of the actuating signal by the condition responsive means and the output signal by the common time delay means.

15. The combination according to claim 14 wherein each of said switching means included in a tripping means corresponding to a main switch means comprises individual first anode and cathode means and second anode and cathode means commonly connected to all of the first anode and cathode means, both of said anode and cathode means being nonconductive to maintain said tripping means inoperative when said corresponding main switch means is closed and the phase in which it is connected is carrying normal current, both of said anode and cathode means being conductive to effect operation of said tripping means in response to the simultaneous production of the actuating signal from the condition responsive means and the output signal from the common time delay means when an abnormal current condition occurs in the phase in which said corresponding main switch is connected.

16. The combination according to claim 13 wherein said condition responsive means includes first, second and third abnormal current sensing means corresponding to said first, second and third tripping means, each of said abnormal current sensing means being separately coupled to one of said phases and being operative to detect an abnormal current condition only in the coupled phase and produce an actuating signal to the corresponding tripping means.

17 The combination according to claim 16 wherein each of said tripping means includes a first anode and cathode circuit having a first gating means connected to the corresponding abnormal current sensing means and a second anode and cathode circuit serially connected to each of the first anode and cathode circuits and having a second gating means connected to the common time delay means for receiving an output signal from said common time delay means, said first and second anode and cathode circuits each having a nonconduct-

ing condition in which said tripping means is ineffective to initiate a switch opening operation and a conducting condition in which said tripping means initiates the switch opening operation, both of said anode and cathode circuits conducting when said first gating means receives an actuating signal from said corresponding abnormal current sensing means and said second gating means receives an output signal from said common time delay means.

18. In a repeating circuit interrupter in circuit with a polyphase electrical system and having separate main switch means connected in each phase of said system, the combination of:

control means for opening any of said main switch means upon the occurrence of an abnormal current condition in the phase associated with the opened switch means and for closing the opened switch means; and

sequencing means operable to sequence the entire control means and any one of said switch means from an initial condition through a predetermined number of switch opening and closing operations.

19. The combination according to claim 18 further comprising control reset means responsive to any one of said switch means when the latter is closed to reset the control means to its initial condition in the event that no abnormal current condition exists on any phase after any of the switch means has performed on at least one opening and closing operation.

20. The combination according to claim 19 further comprising condition responsive means coupled to said system for detecting an abnormal current condition in any of said phases, said condition responsive means including a circuit connected to said control reset means and energized when abnormal current is detected by the condition responsive means; and said control reset means is maintained inoperative in response to said circuit when energized.

21. The combination according to claim 19 wherein: said switch means includes a switch circuit having a closed condition; and

said control reset means is electrically connected to said switch circuit and is energized in response to the switch circuit in its closed condition to reset the control means.

22. The combination according to claim 18 wherein said sequencing means is a single sequencing means.

23. The combination according to claim 18 wherein said sequencing means includes a switching circuit and a stage at which the switching circuit has a closed condition; and further comprising control reset means electrically connected to said switching circuit and responsive to the switching circuit when the latter is in its closed condition to reset the control means to its initial condition.

24 In a repeating circuit interrupter in circuit with a polyphase electrical system and having separate main switch means connected in each phase of said system, the combination of a single control means for opening any of said main switch means upon the occurrence of an abnormal current condition in the phase associated with the opened switch means and for closing the opened switch means; and sequencing means operable to sequence said control means from an initial condition through a predetermined number of switch opening and switch closing operations.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,558,985 Dated January 26, 1971

Inventor(s) Michael J. Plichta, Kenneth L. Krolski

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

┌ Column 11, line 70, after "switch" add --means--.

Column 13, line 24, delete "to the connected".

Signed and sealed this 18th day of May 1971.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

WILLIAM E. SCHUYLER,
Commissioner of Patent