US 20070249111A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0249111 A1**

Lin (43) **Pub. Date: Oct. 25, 2007**

(54) **TFT ARRAY SUBSTRATE AND PHOTO-MASKING METHOD FOR FABRICATING SAME**

(75) Inventor: **Yao-Nan Lin**, Miao-Li (TW)

Correspondence Address:
WEI TE CHUNG
FOXCONN INTERNATIONAL, INC.
1650 MEMOREX DRIVE
SANTA CLARA, CA 95050

(73) Assignee: **INNOLUX DISPLAY CORP.**

(21) Appl. No.: **11/788,908**

(22) Filed: **Apr. 23, 2007**

(30) **Foreign Application Priority Data**

Apr. 21, 2006 (TW) 95114351

Publication Classification

(51) **Int. Cl.**
H01L 21/338 (2006.01)
H01L 31/112 (2006.01)

(52) **U.S. Cl.** **438/182**; 257/258

(57) **ABSTRACT**

An exemplary TFT array substrate (**2**) includes an insulating substrate (**201**); a transparent conductive line (**221**) formed on the insulating substrate; a plurality of gate lines (**210**) formed on the transparent conductive line, that are parallel to each other and that each extend along a first direction; a plurality of data lines (**220**) formed on the insulating substrate, that are parallel to each other and that each extend along a second direction orthogonal to the first direction. The gate line at an intersection point of the gate line and the data line are disconnected.

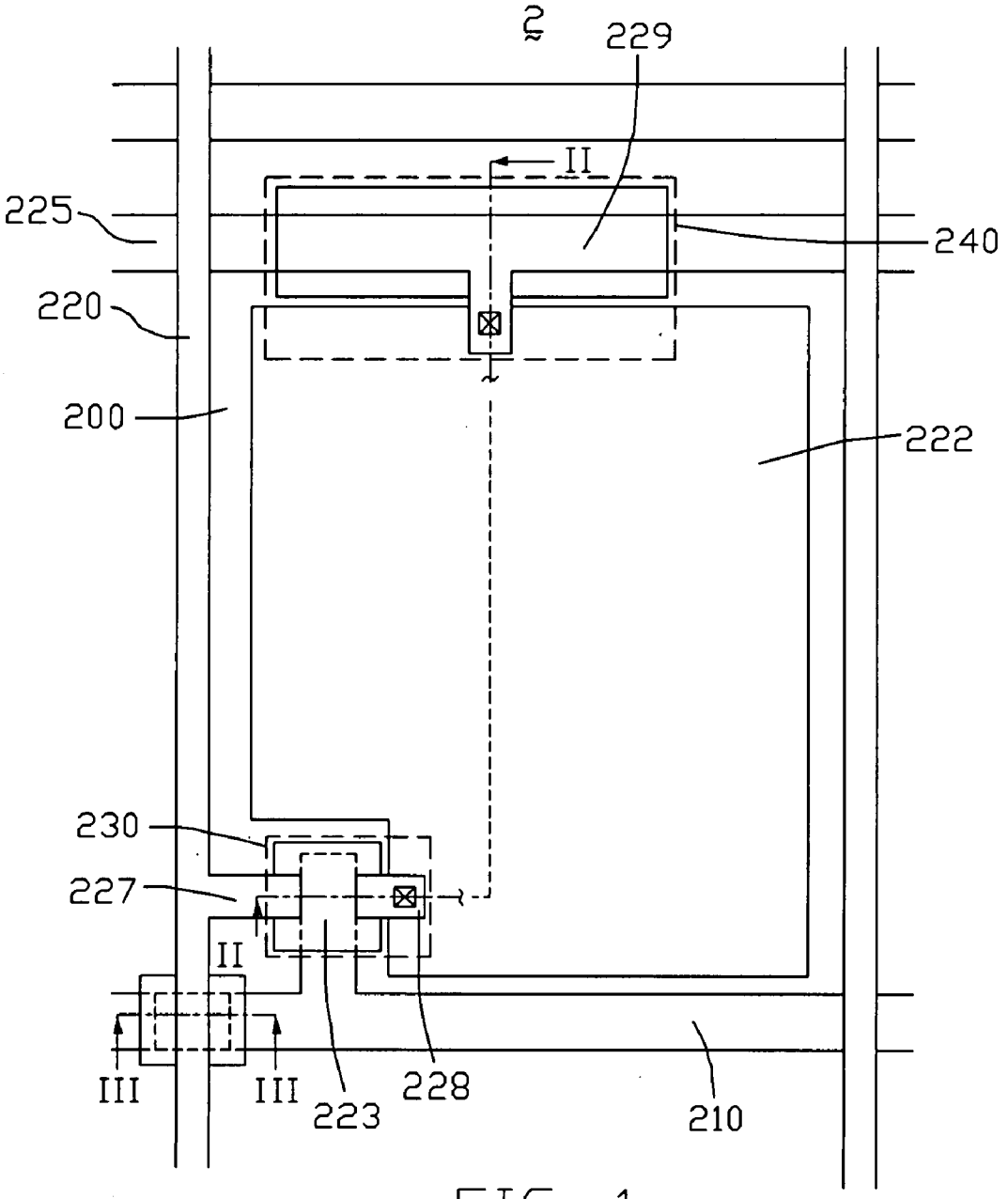

2
229
II
225
240
220
200
222
230
227
II
III
III
223
228
210

FIG. 1

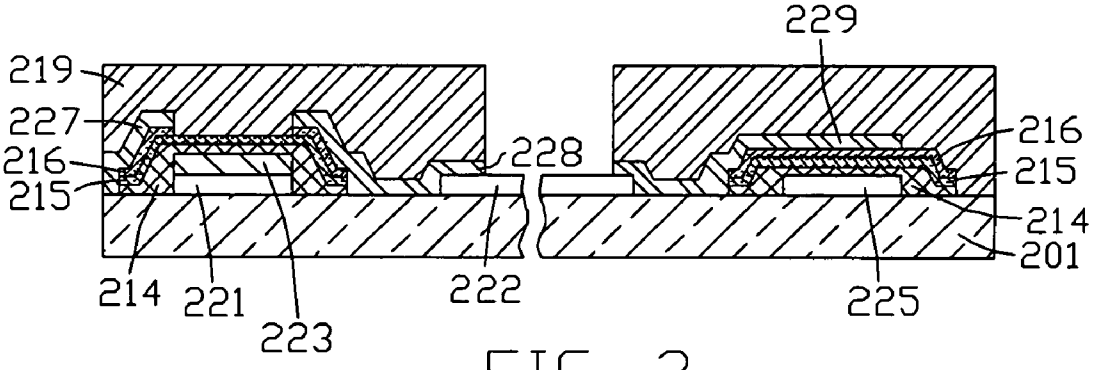

229
219
227
216
215
228
216
215
214
201
214
221
223
222
225

FIG. 2

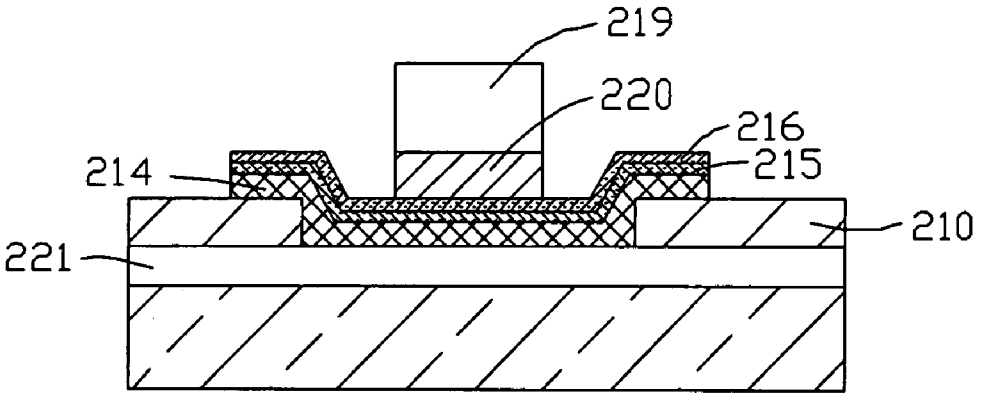

219
220
216
214
215
210
221

FIG. 3

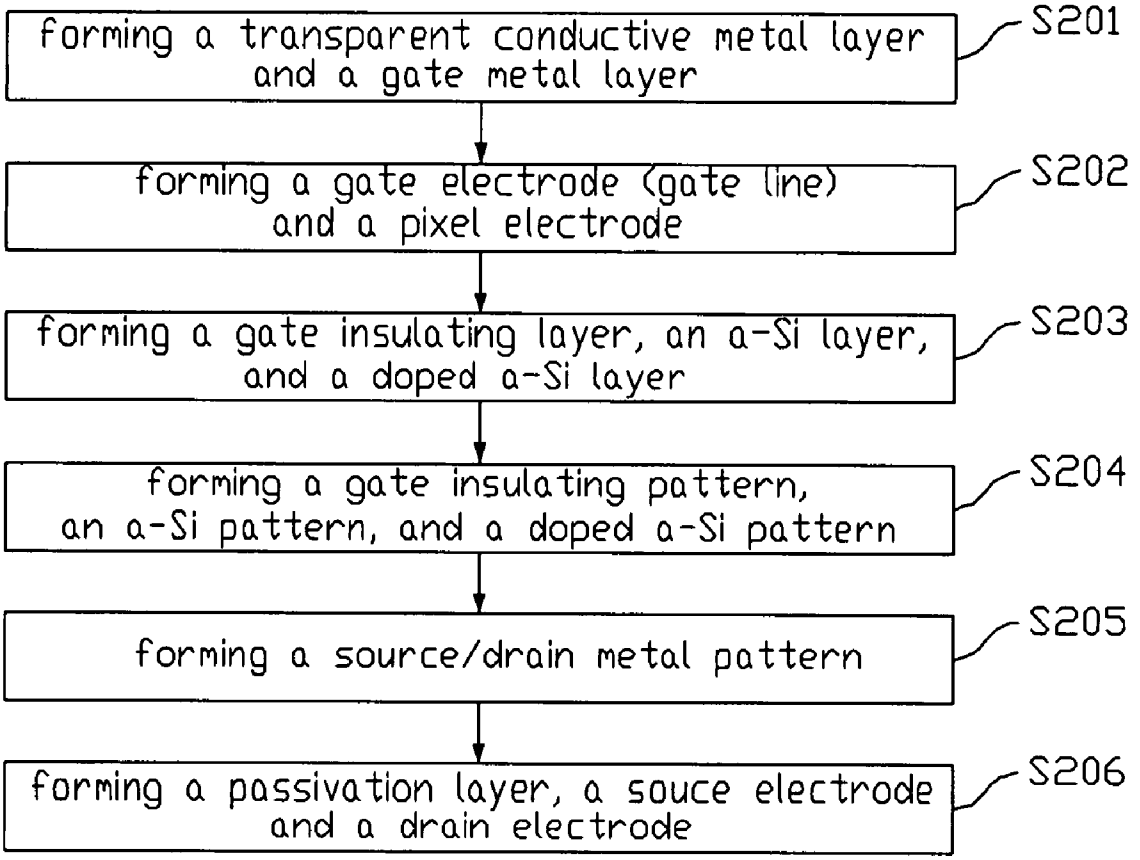

forming a transparent conductive metal layer and a gate metal layer
S201
forming a gate electrode (gate line) and a pixel electrode
S202
forming a gate insulating layer, an a-Si layer, and a doped a-Si layer
S203
forming a gate insulating pattern, an a-Si pattern, and a doped a-Si pattern
S204
forming a source/drain metal pattern
S205
forming a passivation layer, a souce electrode and a drain electrode
S206

FIG. 4

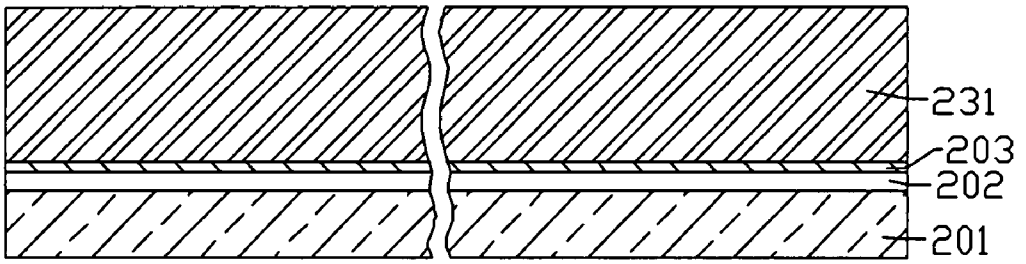
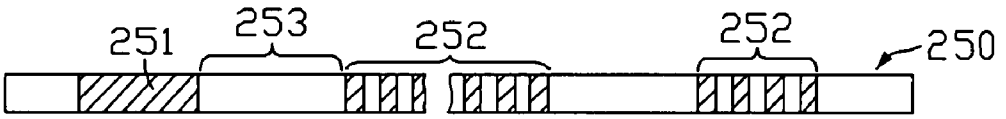


FIG. 5



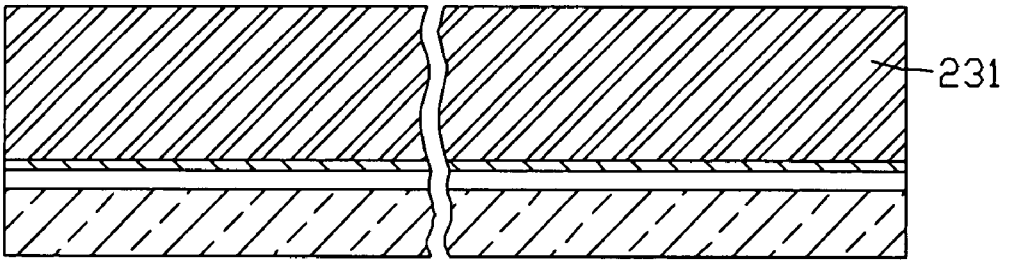


FIG. 6

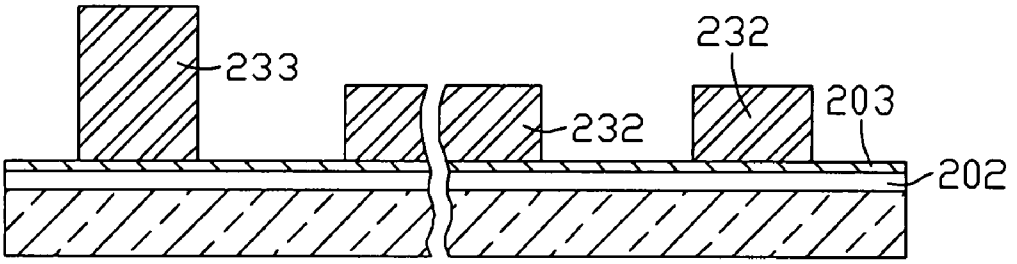


FIG. 7

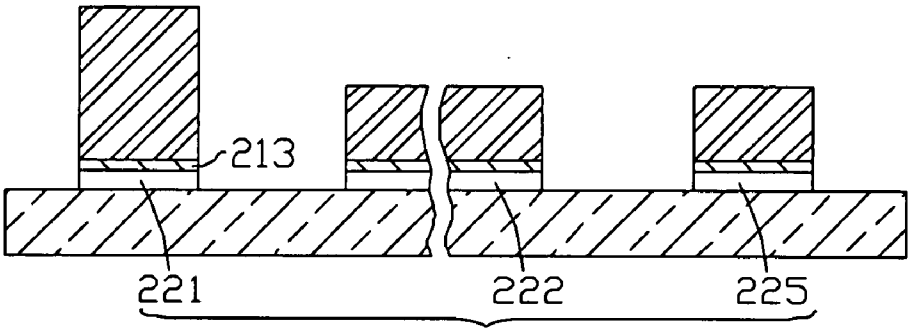


FIG. 8

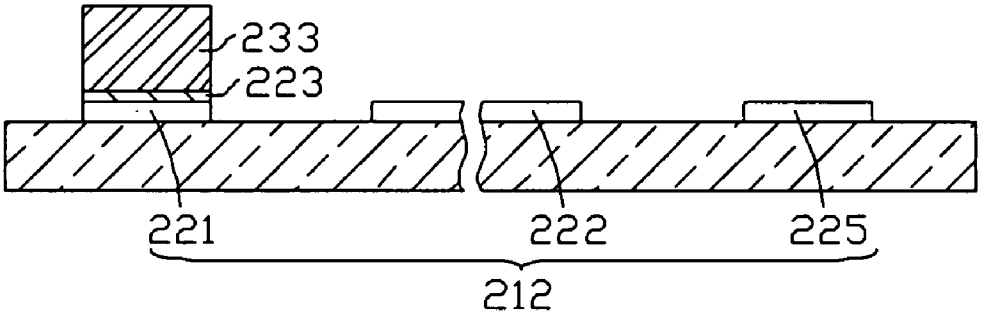


FIG. 9

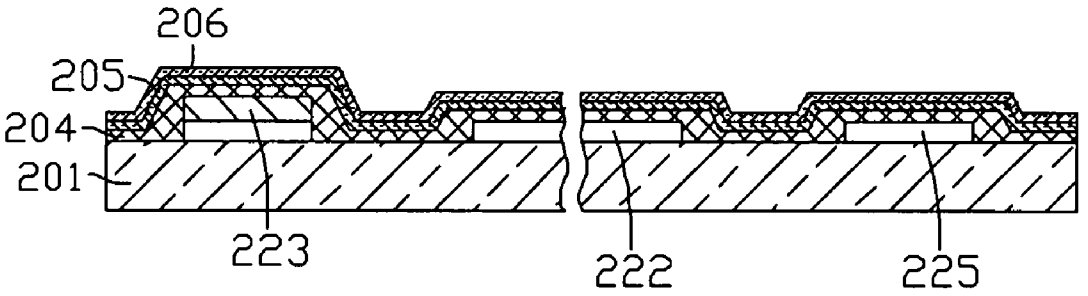


FIG. 10

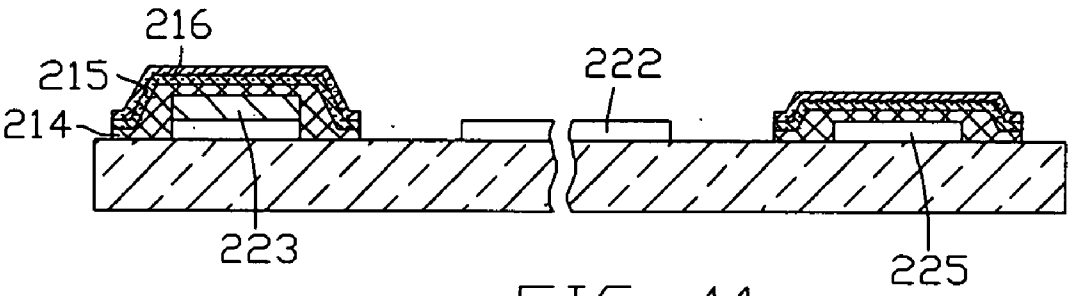


FIG. 11

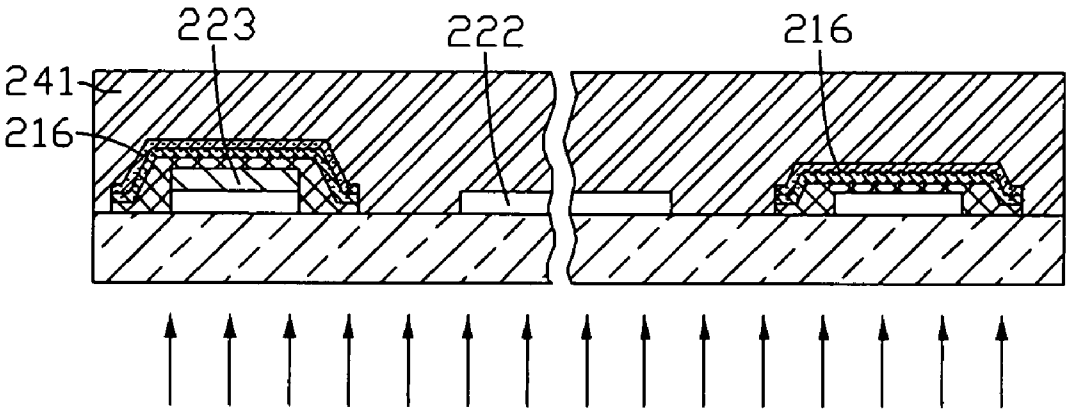


FIG. 12

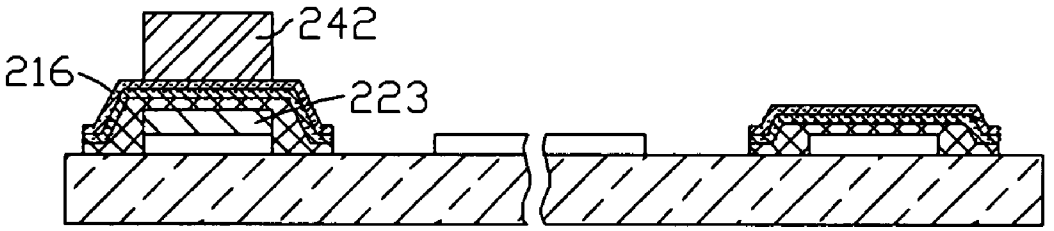


FIG. 13

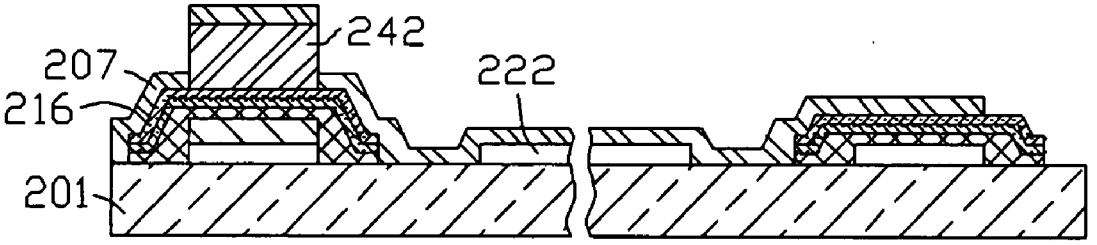


FIG. 14

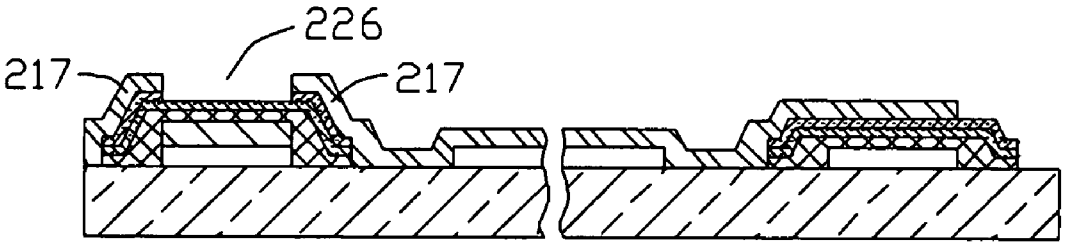


FIG. 15

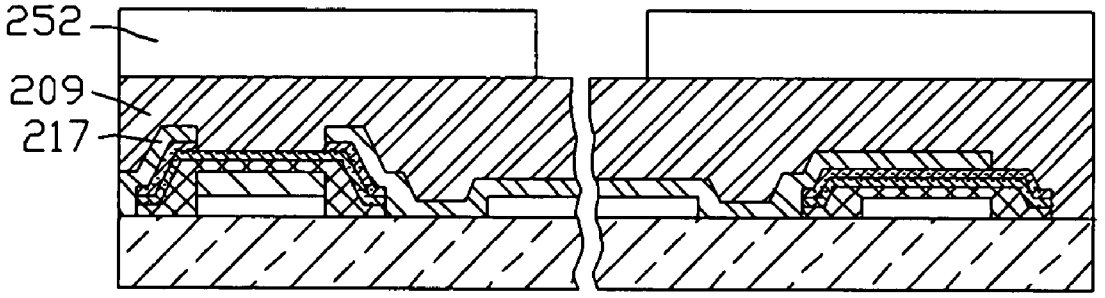


FIG. 16

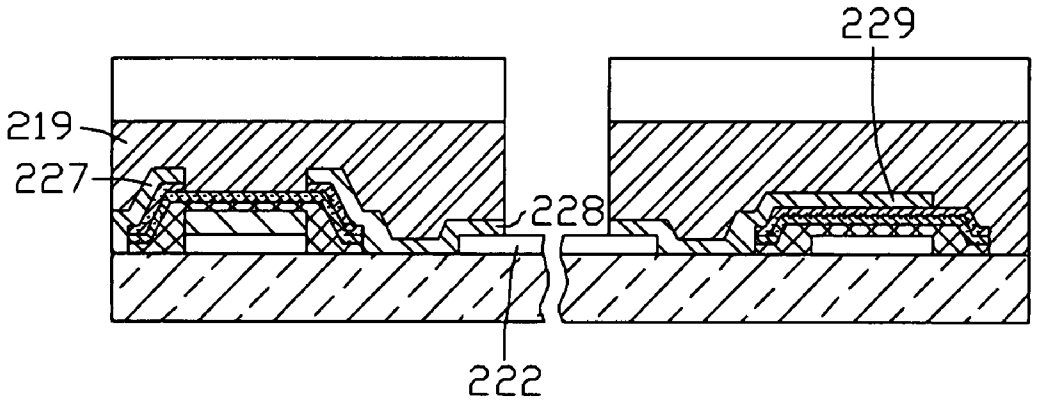


FIG. 17

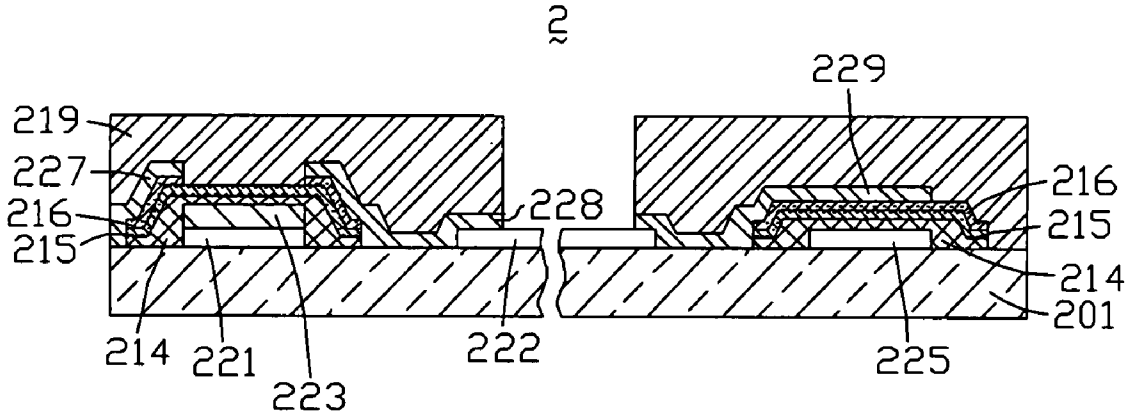


FIG. 18

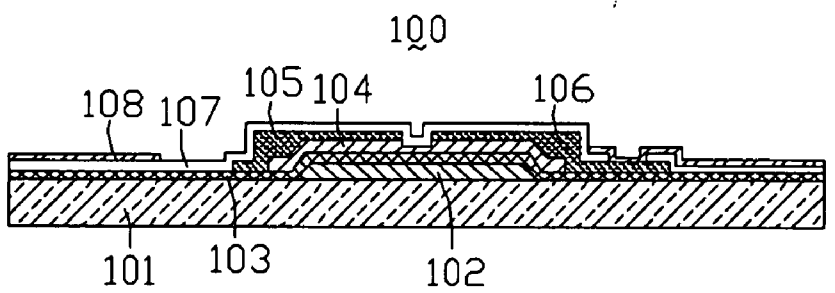


FIG. 19
(RELATED ART)

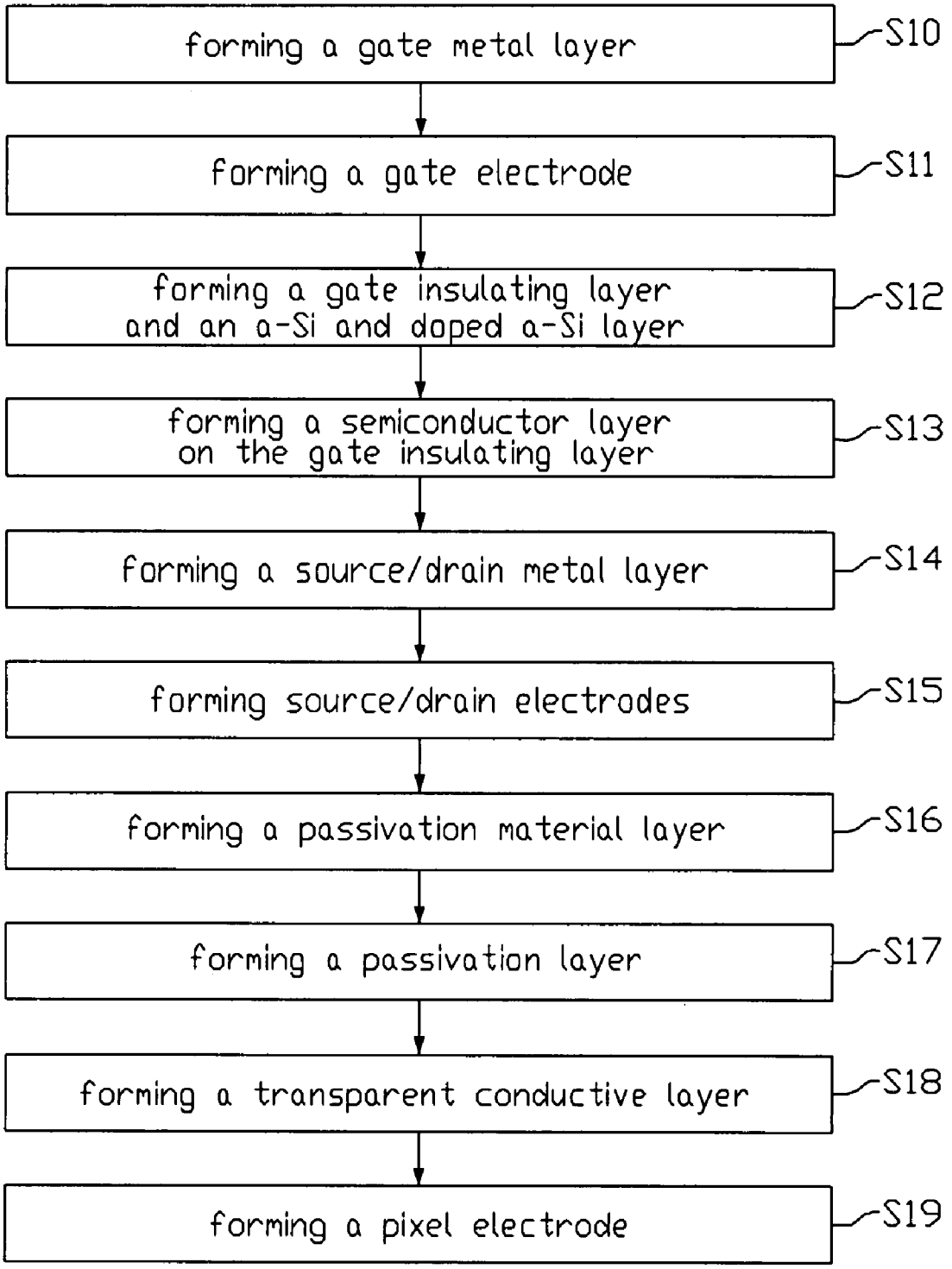


FIG. 20
(RELATED ART)

TFT ARRAY SUBSTRATE AND PHOTO-MASKING METHOD FOR FABRICATING SAME

FIELD OF THE INVENTION

[0001] The present invention relates to thin film transistor (TFT) array substrates used in liquid crystal displays (LCDs) and methods of fabricating these substrates, and particularly to a TFT array substrate and a method for fabricating the substrate which efficiently uses minimal photo-masking.

GENERAL BACKGROUND

[0002] A typical liquid crystal display (LCD) is capable of displaying a clear and sharp image through millions of pixels that make up the complete image. The liquid crystal display has thus been applied to various electronic equipments in which messages or pictures need to be displayed, such as mobile phones and notebook computers. A liquid crystal panel is a major component of the LCD, and generally includes a thin film transistor (TFT) array substrate, a color filter substrate opposite to the TFT array substrate, and a liquid crystal layer sandwiched between the two substrates.

[0003] Referring to FIG. **19**, part of a typical TFT array substrate is shown. The TFT array substrate **100** includes a substrate **101**, a gate electrode **102** formed on the substrate **101**, a gate insulating layer **103** formed on the substrate **101** having the gate electrode **102**, a semiconducting layer **104** formed on the gate insulating layer **103**, a source electrode **105** and a drain electrode **106** formed on the gate insulating layer **103** and the semiconducting layer **104**, a passivation layer **107** formed on the gate insulating layer **103**, the source electrode **105** and the drain electrode **106**, and a pixel electrode **108** formed on the passivation layer **107**.

[0004] Referring to FIG. **20**, this is a flowchart summarizing a typical method for fabricating the TFT array substrate **100**. For simplicity, the flowchart and the following description are couched in terms that relate to the part of the TFT array substrate **100** shown in FIG. **19**. The method includes: step S**10**, forming a gate metal layer; step S**11**, forming a gate electrode; step S**12**, forming a gate insulating layer and an amorphous silicon (a-Si) and doped a-Si layer; step S**13**, forming a semiconducting layer on the gate insulating layer; step S**14**, forming a source/drain metal layer; step S**15**, forming source/drain electrodes; step S**16**, forming a passivation material layer; step S**17**, forming a passivation layer; step S**18**, forming a transparent conductive layer; and step S**19**, forming a pixel electrode.

[0005] In step S**10**, an insulating substrate is provided. The substrate may be made from glass or quartz. A gate metal layer and a first photo-resist layer are formed on the substrate.

[0006] In step S**11**, the first photo-resist layer is exposed by a first photo-mask, and then is developed, thereby forming a first photo-resist pattern. The gate metal layer is etched, thereby forming a pattern of the gate electrode **102**, which corresponds to the first photo-resist pattern. The residual first photo-resist layer is then removed by an acetone solution.

[0007] In step S**12**, a gate insulating layer **103**, an a-Si and doped a-Si layer, and a second photo-resist layer are sequentially formed on the substrate **101** having the gate electrode **102**.

[0008] In step S**13**, the second photo-resist layer is exposed by a second photo-mask, and then is developed, thereby forming a second photo-resist pattern. The a-Si and doped a-Si layer is etched, thereby forming a pattern of the semiconducting layer **104**, which corresponds to the second photo-resist pattern. The residual second photo-resist layer is then removed by an acetone solution.

[0009] In step S**14**, a source/drain metal layer and a third photo-resist layer are sequentially formed on the semiconducting layer **104**.

[0010] In step S**15**, the third photo-resist layer is exposed by a third photo-mask, and then is developed, thereby forming a third photo-resist pattern. The source/drain metal layer is etched, thereby forming a pattern of the source electrode **105** and the drain electrode **106**, which corresponds to the third photo-resist pattern. The residual third photo-resist layer is then removed by an acetone solution.

[0011] In step S**16**, a passivation material layer and a fourth photo-resist layer are sequentially formed on the substrate **101** having the three electrodes **102**, **105**, **106** formed thereon.

[0012] In step S**17**, the fourth photo-resist layer is exposed by a fourth photo-mask, and then is developed, thereby forming a fourth photo-resist pattern. The passivation material layer is etched, thereby forming a pattern of the passivation layer **107**, which corresponds to the fourth photo-resist pattern. The residual fourth photo-resist layer is then removed by an acetone solution.

[0013] In step S**18**, a transparent conductive layer and a fifth photo-resist layer are sequentially formed on the passivation layer **107**.

[0014] In step S**19**, the fifth photo-resist layer is exposed by a fifth photo-mask, and then is developed, thereby forming a fifth photo-resist pattern. The transparent conductive layer is etched, thereby forming a pattern of the pixel electrode **108**, which corresponds to the fifth photo-resist pattern. The residual fifth photo-resist layer is then removed by an acetone solution.

[0015] The method includes five photo-mask processes, each of which is rather complicated and costly. Thus, the method for fabricating the TFT array substrate **100** is correspondingly complicated and costly.

[0016] What is needed, therefore, is a method for fabricating a TFT array substrate that can overcome the above-described problems. What is also needed is a TFT array substrate fabricated by the above method.

SUMMARY

[0017] In one preferred embodiment, a method for fabricating a thin film transistor (TFT) array substrate includes providing an insulating substrate; forming a transparent conductive metal layer and a gate metal layer on the insulating substrate; forming a gate electrode, a gate line and a pixel electrode through a first photolithograph process; forming a gate insulating layer, an amorphous silicon pattern, and a doped amorphous silicon pattern through a second photolithograph process; forming a photo-resist pattern on the gate electrode through a third photolithograph process, using the gate electrode as a photo-mask; forming a source/drain metal layer on the insulating substrate, the doped amorphous silicon layer, the photo-resist pattern and the pixel electrode; forming a source/drain metal pattern through removing the photo-resist pattern and a portion of the source/drain metal layer on the photo-resist pattern; and

forming a passivation layer pattern, a source/drain electrode through a fourth photolithograph process.

[0018] An exemplary TFT array substrate includes an insulating substrate; a transparent conductive line formed on the insulating substrate; a plurality of gate lines formed on the transparent conductive line, that are parallel to each other and that each extend along a first direction; a plurality of data lines formed on the insulating substrate, that are parallel to each other and that each extend along a second direction orthogonal to the first direction. The gate line at an intersection point of the gate line and the data line are disconnected.

[0019] Other advantages and novel features will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. **1** is a schematic, top view of a pixel of a TFT array substrate according to an exemplary embodiment of the present invention.

[0021] FIG. **2** is a schematic, side cross-sectional view of the TFT array substrate of FIG. **1**, taken along the line II-II.

[0022] FIG. **3** is a schematic, side cross-sectional view of the TFT array substrate of FIG. **1**, taken along the line III-III.

[0023] FIG. **4** is a flowchart summarizing an exemplary method for fabricating the TFT array substrate of FIG. **1**.

[0024] FIG. **5** is a schematic, side cross-sectional view relating to a step of providing a substrate and forming a transparent conductive metal layer, a gate metal layer, and a first photo-resist layer on the substrate according to the method of FIG. **4**.

[0025] FIG. **6** is a schematic, side cross-sectional view relating to a next step of exposing a first photo-resist layer using a slit photo-mask according to the method of FIG. **4**.

[0026] FIG. **7** is a schematic, side cross-sectional view relating to a next step of forming a first photo-resist pattern according to the method of FIG. **4**.

[0027] FIG. **8** is a schematic, side cross-sectional view relating to a next step of forming a gate electrode pattern and a transparent conductive metal layer pattern according to the method of FIG. **4**.

[0028] FIG. **9** is a schematic, side cross-sectional view relating to a next step of forming a gate electrode and a gate line according to the method of FIG. **4**.

[0029] FIG. **10** is a schematic, side cross-sectional view relating to a next step of forming a gate insulating layer on the substrate having the gate electrode according to the method of FIG. **4**.

[0030] FIG. **11** is a schematic, side cross-sectional view relating to a next step of forming a third photo-resist layer on the substrate according to the method of FIG. **4**.

[0031] FIG. **12** is a schematic, side cross-sectional view relating to a next step of exposing the third photo-resist layer from a bottom side of the substrate according to the method of FIG. **4**.

[0032] FIG. **13** is a schematic, side cross-sectional view relating to a next step of forming a third photo-resist pattern according to the method of FIG. **4**.

[0033] FIG. **14** is a schematic, side cross-sectional view relating to a next step of depositing a source/drain metal layer on the substrate and the third photo-resist pattern according to the method of FIG. **4**.

[0034] FIG. **15** is a schematic, side cross-sectional view relating to a next step of removing the third photo-resist pattern and a portion of the source/drain metal layer on the photo-resist pattern according to the method of FIG. **4**.

[0035] FIG. **16** is a schematic, side cross-sectional view relating to a next step of depositing a passivation layer and a fourth photo-resist layer on the substrate according to the method of FIG. **4**.

[0036] FIG. **17** is a schematic, side cross-sectional view relating to a step of etching away a portion of the passivation material layer and a portion of the source/drain metal layer pattern according to the method of FIG. **2**.

[0037] FIG. **18** is a schematic, side cross-sectional view relating to a step of removing the remained fourth photo-resist layer according to the method of FIG. **2**.

[0038] FIG. **19** is a schematic, side cross-sectional view of part of a conventional TFT array substrate.

[0039] FIG. **20** is a flowchart summarizing a conventional method for fabricating the TFT array substrate of FIG. **17**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0040] Referring to FIG. **1**, part of a thin film transistor (TFT) array substrate according to an exemplary embodiment of the present invention is shown. The TFT array substrate **2** includes a plurality of gate lines **210** that are parallel to each other and that each extend along a first direction, a plurality of data lines **220** that are parallel to each other and that each extend along a second direction orthogonal to the first direction, and a plurality of common line **225**. The smallest rectangular area formed by any two adjacent gate lines **210** together with any two adjacent data lines **220** defines a pixel region thereat. In each pixel region, a TFT **230** is provided in the vicinity of a respective point of intersection of one of the gate lines **210** and one of the data lines **220**. A pixel electrode **222** is connected to the TFT **230**. Each TFT **230** has a gate electrode **223** electrically connecting with the gate line **210**, a source electrode **227** electrically connecting with the data line **220**, and a drain electrode **228** connected to the pixel electrode **222**. The common line **225** is disposed between the pixel electrode **222** and its adjacent gate line **210**, extending along a direction parallel to the gate line **210**. A storage capacitor **240** is parallel to the gate lines **210** above part of the common line **225**. The storage capacitor **240** has a capacitor electrode **229**, which is connected to one side of the pixel electrode **222**, far away the corresponding TFT **230**.

[0041] The TFT array substrate **2** further includes an insulating substrate **201**, a transparent conductive line **221**, a gate insulating pattern **214**, an amorphous silicon (a-Si) pattern **215**, a doped a-Si pattern **216** and a passivation layer **219**. The transparent conductive line **221**, the pixel electrode **222** and the common line **225** are formed on the insulating substrate **201**. The gate electrode **223** and the gate line **210** are formed on the transparent conductive line **221**. The gate insulating pattern **214** is formed on a part of the intersections of the gate electrode **212**, the common line **225**, the gate line **210** with the data line **220**. The a-Si pattern **215** and the doped a-Si pattern **216** are orderly formed on the gate insulating layer pattern **214**. The source electrode **227** and the drain electrode **228** are formed on the doped a-Si pattern **216**. The capacitor electrode **229** are disposed on the doped amorpuous silicon pattern **216**, corresponding to the common line **225**. The passivation layer **219** is formed on the TFT **230** and the storage capacitor **240**.

[0042] Referring to FIG. **3**, the gate line **210** at the intersection point of the gate line **210** and the data line **220** are disconnected, forming a disconnected region thereat. The gate line **210** keeps electrical connection through the underlie transparent conductive line **221**. The disconnected region of the gate line **210** can prevent a short circuit or open circuit between the gate line **210** and the corresponding data line **220**.

[0043] Referring to FIG. **4**, this is a flowchart summarizing an exemplary method for fabricating the TFT array substrate **2**. For simplicity, the flowchart and the following description are couched in terms that relate to the part of the TFT array substrate **2** shown in FIG. **1**. The method includes: step S**201**, forming a transparent conductive metal layer and a gate metal layer; step S**202**, forming a gate electrode (gate line) and a pixel electrode; step S**203**, forming a gate insulating layer, an a-Si layer, and a doped a-Si layer; step S**204**, forming a gate insulating pattern, an a-Si pattern, and a doped a-Si pattern; step S**205**, forming a source/drain metal pattern; step S**206**, forming a passivation layer, a source electrode and a drain electrode.

[0044] In step S**201**, referring to FIG. **5**, an insulating substrate **201** is provided. The substrate **201** may be made from glass or quartz. A transparent conductive metal layer **202**, a gate metal layer **203**, and a first photo-resist layer **231** are sequentially formed on the substrate **201**. The trans parent conductive metal layer **202** may be Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO). The gate metal layer **203** may be made from material including any one or more items selected from the group consisting of aluminum (Al), molybdenum (Mo), copper (Cu), chromium (Cr), and tantalum (Ta).

[0045] In step S**202**, referring to FIG. **6** to FIG. **8**, a light source (not shown) and a first photo-mask **250** are used to expose the first photo-resist layer **231**. The first photo mask **250** is a slit mask having a light shield area **251**, a slit area **252**, and a transparent area **253**. The first photo-resist layer **231** is exposed using the first photo mask **250**. Then the exposed second photo-resist layer is developed, thereby forming a first photo-resist pattern. A first thickness of a first part **233** of the first photo-resist pattern, corresponding to the shield area **251** is greater than a second thickness of a second part **232** of the first photo-resist pattern, corresponding to the slit area **252**, because the slit area **252** has a larger luminous flux. Using the first photo-resist pattern as a mask, the transparent conductive metal layer **202** and the gate metal layer **203** are etched, thereby forming a gate electrode pattern **213** and a transparent conductive metal pattern **212**. The transparent conductive metal pattern **212** includes the pixel electrode **222**, the common line **225** and the transparent conductive line **221**.

[0046] Then, as shown in FIG. **9**, through an etching process, the second part **232** of the first photo-resist pattern, part of the first part **232** of the first photo-resist pattern, a part of the gate metal pattern **213** corresponding to the second part **232** are etched away. And then, the remained first part **232** of the first photo-resist pattern is removed away, thereby forming the gate electrode **223** and the gate line **210** on the transparent conductive line **221**. The gate line **210** at the intersection point of the gate line **210** and the data line **220** are disconnected, forming a disconnected region thereat. The gate line **210** keeps electrical connection through the underlie transparent conductive line **221**.

[0047] Because the gate metal line **203** are formed on the transparent conductive metal layer **202**, and the gate electrode **223** and the pixel electrode **222** don't overlap with each other, only one photo-mask process is used to form the gate electrode **223** and the pixel electrode **222**, thus saving one photo-mask process.

[0048] In step S**203**, referring to FIG. **10**, a gate insulating layer **204** is formed on the substrate **201** having the gate electrode **223**, the pixel electrode **222** and the common line **225** by a chemical vapor deposition (CVD) process. In this process, silane (SiH_4) reacts with alkaline air (NH4+) to obtain silicon nitride (SiN_x), a material of the gate insulating layer **204**. An amorphous silicon (a-Si) material is deposited on the gate insulating layer **204** by a CVD process. The a-Si layer is doped, thereby respectively forming the a-Si layer **205** and the doped a-Si layer **206**.

[0049] In step S**204**, referring to FIG. **11**, a second photo-resist layer is coated on the doped a-Si layer **206**. An ultra violet (UV) light source and a photo-mask (not shown) are used to expose the second photo-resist layer. Then the exposed second photo-resist layer is developed, thereby forming a second photo-resist pattern. Using the second photo-resist pattern as a mask, portions of the gate insulating layer **204**, the a-Si layer **205** and the doped a-Si layer **206** which are not covered by the second photo-resist pattern are etched away, thereby forming a gate insulating layer pattern **214**, an a-Si pattern **215** and a doped a-Si pattern **216**.

[0050] In step S**205**, referring to FIG. **12**, a third photo-resist layer **241** is coated on the gate insulating layer pattern **214**, the substrate **201** and the pixel electrode **222**. An ultra violet (UV) light source is used to expose the third photo-resist layer **241**, from a bottom side of the substrate **201** which is opposite to a top side where the gate electrode **223** and the pixel electrode **22** are formed thereon, using the gate electrode **223** as a photo-mask. Then the exposed third photo-resist layer **241** is developed, thereby forming a third photo-resist pattern **242** (as shown in FIG. **13**). Referring to FIG. **14**, a source/drain metal layer **207** is then deposited on the doped a-Si pattern **216**, the substrate **201**, the third photo-resist pattern **242** and the pixel electrode **222**. The source/drain metal layer **207** may be made from material including any one or more items selected from the group consisting of aluminum, aluminum alloy, molybdenum, tantalum, and molybdenum-tungsten alloy. After that, the third photo-resist pattern **242** and a portion of the source/drain metal layer **207** on the third photo-resist pattern **242** are removed away, thereby forming a source/drain metal pattern **217**. Using the source/drain metal pattern **217** as a mask, portions of the doped a-Si pattern **216** which are not covered by the source/drain metal pattern **217** are etched away, thereby forming a groove **226** thereof (as shown in FIG. **15**).

[0051] In step S**206**, referring to FIG. **16**, a passivation material layer **209** and a fourth photo-resist layer (not labeled) are deposited on the source/drain metal layer pattern **217** and the groove **226**. A light source and a third photo-mask (not labeled) are used to expose the fourth photo-resist layer, thereby forming a fourth photo-resist pattern **252**. Referring also to FIG. **17**, a portion of the passivation material layer **209** and a portion of the source/drain metal layer pattern **217** which are not covered by the fourth photo-resist pattern **252** is etched away; thereby exposing a portion of the pixel electrode **222** and forming

the source electrode **227**, the drain electrode **228** and the capacitor electrode **229** and the passivation layer **219** (as shown in FIG. **18**).

[0052] In summary, compared to the above-described conventional method, in the above-described exemplary method for fabricating the TFT array substrate **2**, only one photo-mask process is used to form the gate electrode **223** and the pixel electrode **222**. In addition, in the step of forming the source/drain metal layer **217**, the gate electrode **223** is used as a mask, thereby a predetermined mask is saved. That is, the method for fabricating the TFT array substrate **2** only includes a total of four photo-mask processes. Therefore, a simplified method at a reduced cost is provided.

[0053] It is believed that the present embodiments and their advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit and scope of the invention or sacrificing all of its material advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the invention.

What is claimed is:

1. A method for fabricating a thin film transistor (TFT) array substrate, the method comprising:

providing an insulating substrate;

forming a transparent conductive metal layer and a gate metal layer on the insulating substrate;

forming a gate electrode, a gate line and a pixel electrode through a first photolithograph process;

forming a gate insulating layer, an amorphous silicon pattern, and a doped amorphous silicon pattern through a second photolithograph process;

forming a photo-resist pattern on the gate electrode through a third photolithograph process, using the gate electrode as a photo-mask;

forming a source/drain metal layer on the insulating substrate, the doped amorphous silicon layer, the photo-resist pattern and the pixel electrode;

forming a source/drain metal pattern through removing the photo-resist pattern and a portion of the source/drain metal layer on the photo-resist pattern; and

forming a passivation layer pattern, a source/drain electrode through a fourth photolithograph process.

2. The method as claimed in claim **1**, wherein the first photolithograph process comprises coating a photo-resist layer on the gate metal layer, exposing the photo-resist layer using a photo-mask having a plurality of slits, and developing the exposed photo-resist layer to form a photo-resist pattern.

3. The method as claimed in claim **2**, wherein the first photolithograph process comprises etching the transparent conductive metal layer and the gate metal layer which are not covered by the photo-resist pattern, thereby forming a gate metal pattern and a transparent conductive metal pattern.

4. The method as claimed in claim **3**, wherein the photo-resist pattern comprises a first part and a second part, a first thickness of the first part being greater than a second thickness of the second part of the first photo-resist layer.

5. The method as claimed in claim **4**, wherein the first photolithograph process comprises etching away the second part of the first photo-resist layer pattern.

6. The method as claimed in claim **5**, wherein the first photolithograph process comprises etching a part of gate metal layer pattern corresponding to the second part of the first photo-resist layer pattern, thereby forming the integrated gate electrode and the gate line.

7. The method as claimed in claim **6**, wherein the gate line at the intersection point of the gate line and a data line of the TFT array substrate is disconnected, forming a disconnected region thereat.

8. The method as claimed in claim **7**, wherein the gate line keeps electrical connection through the underlie transparent conductive line.

9. The method as claimed in claim **6**, wherein the transparent conductive metal layer pattern includes the pixel electrode, a common line and a transparent conductive line.

10. The method as claimed in claim **1**, wherein the third photolithograph process comprises using an ultra violet (UV) light source to expose a photo-resist layer, from a bottom side of the substrate, which is opposite a top side where the gate electrode and the pixel electrode are formed thereon.

11. The method as claimed in claim **1**, wherein the substrate is made from glass or quartz.

12. The method as claimed in claim **1**, wherein the transparent conductive layer is made from indium tin oxide or indium zinc oxide.

13. The method as claimed in claim **1**, wherein the gate metal layer is made from material including any one or more items selected from the group consisting of aluminum, molybdenum, copper, chromium, and tantalum.

14. The method as claimed in claim **1**, wherein the source/drain metal layer is made from material including any one or more items selected from the group consisting of aluminum, aluminum alloy, molybdenum, tantalum, and molybdenum-tungsten alloy.

15. A TFT array substrate comprising:

an insulating substrate;

a transparent conductive line formed on the insulating substrate

a plurality of gate lines formed on the transparent conductive line, that are parallel to each other and that each extend along a first direction,

a plurality of data lines formed on the insulating substrate, that are parallel to each other and that each extend along a second direction orthogonal to the first direction;

wherein the gate line at the intersection point of the gate line and the data line are disconnected.

16. The TFT array substrate as claimed in claim **15**, wherein the gate line keeps electrical connection through the underlie transparent conductive line.

17. The TFT array substrate as claimed in claim **15**, wherein the disconnected region of the gate line can prevent a short circuit or open circuit between the gate line and the corresponding data line.

* * * * *