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(54) **Title**: INDUCED THERMAL GRADIENTS

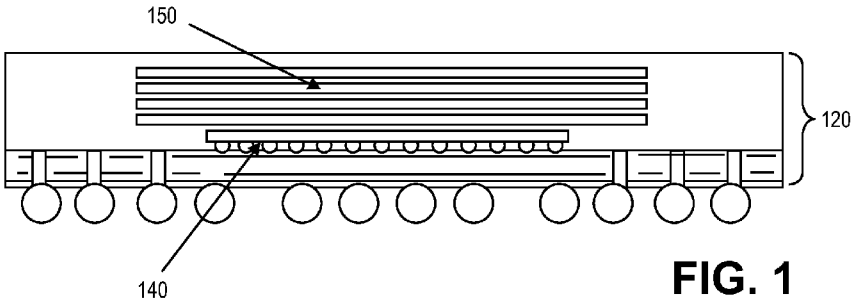

FIG. 1

(57) **Abstract**: A temperature difference between a first thermal sensor and a second thermal sensor on a first die is determined. The temperature difference is transmitted from the first die to a circuit on a second die. A temperature from a thermal sensor on the second die is determined. The temperature difference and the temperature from the thermal sensor are utilized on the second die to modify operational characteristics of one or more circuits on the second die.

INDUCED THERMAL GRADIENTS

TECHNICAL FIELD

Embodiments of the invention relate to semiconductor devices. More particularly, embodiments of the invention relate to techniques for tolerating induced thermal gradients in semiconductor devices.

BACKGROUND

Semiconductor devices produce thermal energy when operating. Because the thermal energy may not be uniform, a thermal gradient may exist. As systems become smaller and semiconductor devices are more closely packed, which may result in mechanical coupling between devices. This tight mechanical coupling may result in unexpected induced thermal gradients between one and another of the semiconductor devices.

These unexpected thermal gradients may result in operating errors. For example, in a dynamic random access memory (DRAM), unexpected thermal gradients may result in inappropriate refresh frequencies and even data loss.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a block diagram of one embodiment of a package having one or more memory dies stacked with a processor/logic die.

Figure 2 is a block diagram of one embodiment of a first die having a single sensor and a second die having multiple sensors.

Figure 3 is a flow diagram of one embodiment of a technique to operate a memory array using temperature difference information.

Figure 4 is a block diagram of one embodiment of an electronic system.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth. However, embodiments of the invention may be practiced without these specific details. In other instances,

well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

When a processor (or System on a Chip, SoC) and DRAM dies are stacked there may be little thermal gradient between the DRAM and the logic chip. Logic chips typically contain several thermal sensors that are used to monitor the temperature on various parts of the logic chip and are typically placed where localized hot spots are expected. Logic chips may exhibit high thermal gradients across the die corresponding to more and less active regions in the logic chip.

DRAM chips may exhibit variable retention times based on temperature. Lower-power DRAM chips may use this property in a feature called "temperature compensated self refresh." This may reduce the refresh frequency during self refresh thereby reducing standby power consumption at lower temperatures. Typically a DRAM chip has a single thermal sensor because DRAM chips typically have a relatively uniform power distribution. However, when closely coupled with a logic chip that has a non-uniform power distribution, the DRAM thermal sensor may not be located near the hottest spot of the DRAM chip. This may cause the DRAM to refresh at an inappropriately low rate, which may lead to data loss.

The techniques described herein address this problem by one or more strategies. In one embodiment, the location of a thermal sensor may be standardized for all devices on a stack. The location may be specified, for example, as a certain offset from a standardized vertical interconnect array in an area that cannot be used for the memory array in the DRAM. In one embodiment, a SoC (or other computational element) may calculate a temperature difference between a hottest spot and the standard location. In one embodiment, a mode register may be utilized by the SoC (or other computational element) to communicate with the DRAM regarding the temperature difference between the standard location and the hot spot. The DRAM can then utilize this difference to set refresh rates accordingly.

In alternate embodiments, the techniques may be adapted to function without a standard thermal sensor location. In these embodiments, the SoC (or other computational element) may calculate a maximum temperature gradient across its die and use that information to program the DRAM offset temperature. This may allow the DRAM to refresh its contents more often than absolutely necessary, which may lead to increased power consumption, but would prevent data loss.

Figure 1 is a block diagram of one embodiment of a package having one or more memory dies stacked with a processor/logic die. In the example of Figure 1, several dies containing memory arrays (e.g., DRAM) are illustrated; however any number of memory dies may be supported.

Integrated circuit package 120 may be any type of package known in the art with any type of interface known in the art (e.g., ball grid array, etc.). Within package 120, logic die 140 may be electrically coupled to the interface. One or more memory modules 150 may be electrically coupled with logic die 140. Logic die 140 may be, for example, a processor die, a system on a chip (SoC) die, or any other die that may have uneven thermal patterns.

One or more memory modules 150 may also be physically connected to logic die 140, which my have thermal consequences for one or more of the dice. Because logic die 140 may have an uneven thermal gradient the physical connection between logic die 140 and one or more of memory modules 150, the thermal gradient of one or more of memory modules 150 may not be as expected. Typically, memory modules, for example DRAMs, have a relatively consistent temperature across the die because circuit utilization on the memory module is relatively distributed.

Because of this, the placement of a thermal sensor on the memory module die may be relatively unimportant. That is, when the memory module is operating without any outside thermal influences, a single thermal sensor may be sufficient and the location of thermal sensor may be relatively flexible.

In contrast to memory modules, logic dice have circuits that are used consistently and frequently which result in higher operating temperatures in those regions. Therefore, logic dice typically have thermal sensors located a places of higher expected temperature so that these hot spots may be monitored. When a logic die comes in to physical contact with another die, for example, memory die 150, the hot spots on the logic die may create corresponding hot spots on the memory die. Thus, the thermal information from the memory die thermal sensor may be inaccurate.

In one embodiment, memory die 150 has a thermal sensor in a known location. That is, each memory die may have the same thermal sensor location. Logic die 140 may have a corresponding thermal sensor in a location that is immediately adjacent to or substantially adjacent to the thermal sensor of memory die 150. Logic die 140 may also have thermal sensors in other locations, for example, corresponding to one or more hot spots.

In one embodiment, logic die may determine a temperature difference between a thermal sensor at a hot spot and a thermal sensor corresponding to a thermal sensor in the memory module. The temperature difference between the thermal sensors on the logic die may be used by the memory module to determine an adjustment to the temperature indicated by the thermal sensor on the memory module. The behavior of the memory module may be modified based on the adjusted temperature rather than the measured temperature.

Figure 2 is a block diagram of one embodiment of a first die having a single sensor and a second die having multiple sensors. The example of Figure 2 illustrates two dice that may be stacked so that the heat from one die may transfer to the other die. The example of Figure 2 illustrates only two dice, but the concepts illustrated are applicable to any number of stacked dice.

Die 220 may include any type of circuitry, for example, DRAM arrays, or other memory structures 235. Die 220 includes thermal sensor 240 coupled with management logic 230. In one embodiment, when die 220 includes DRAM, management logic 230 may operate to read temperature information from thermal sensor 240 and may use that temperature information to modify behavior or operation of memory array 235. In one embodiment, the refresh rate of memory array 235 may be adjusted by management logic 230 based on information from thermal sensor 240.

Die 250 may include logic circuitry, for example, a processor core, a graphics processor, a system on a chip (SoC), or other logic 275. Die 250 may have multiple types of circuits, for example, a processor core, a cache memory, a transceiver, etc. Because die 250 may have circuits with irregular thermal gradients, die 250 may have multiple thermal sensors (e.g., 260, 265), one of which is to be aligned with thermal sensor 240.

In one embodiment, thermal sensor 240 may be placed in a predetermined location on die 220 that is known to designers and/or manufacturers of die 250. Thermal sensor 260 is positioned so that when die 220 is stacked on die 250, thermal sensors 240 and 260 will be aligned or close enough spatially that temperature information from thermal sensor 260 may be utilized with temperature information from thermal sensor 240.

Control circuit 270 is coupled with thermal sensors 260 and 265 to collect temperature information. In one embodiment, control circuit 270 determines a temperature difference between thermal sensor 265 and thermal sensor 260. Control circuit 270 may transmit this difference (or information indicating a difference range), to management logic 230. In one embodiment, a bit in a register in management logic 230 is set to indicate a temperature difference (e.g., 0 indicates 0-10 degree difference, 1 indicates a 10+ degree difference). In another embodiment, more bits may be used to provide a more granular range, or an actual temperature difference may be transmitted.

Management logic 230 uses the temperature difference information from control circuit 270 with temperature information from thermal sensor 240 to manage operation of memory array 235. In one embodiment, management logic 230 controls a refresh rate for memory array 235. Management logic 230 may combine the temperature difference information with the temperature information from thermal sensor 240 to determine an operational temperature value

that is used for management of memory array 235. For example, if the temperature difference indicates a higher temperature, management logic 230 may increase the refresh rate for memory array 235.

Figure 3 is a flow diagram of one embodiment of a technique to operate a memory array using temperature difference information. The operations described with respect to Figure 3 may be performed by control and/or management circuitry spread across one or more dice.

The operation of Figure 3 is applicable to a configuration of multiple dice that are physically in contact with one another so that thermal transfer may occur. In one embodiment, at least one thermal sensor on the lower die is aligned with at least one sensor on the upper die. In one embodiment, the lower die contains a logic circuit, for example, a processor core or a system on a chip. The upper die may contain a memory structure, for example, a DRAM. In an alternate embodiment, the logic circuit is on the upper die and the memory module is on the lower die.

Temperature information from two or more thermal sensors is collected on the logic die, 310. The logic die may have any number of thermal sensors and, one or more circuits on the logic die may manage operation of the logic die by utilizing the temperature information collected from the multiple thermal sensors.

Temperature difference information is determined for at least one pair of thermal sensors on the logic die, 320. In one embodiment, at least one of the thermal sensors for which a temperature difference is determined is aligned with a corresponding thermal sensor on the memory module die.

The temperature difference information is transmitted between the logic die and the memory die, 330. In one embodiment, the temperature difference may be communicated by one or more bits that indicate temperature differential ranges, or a number indicating an actual temperature difference may be transmitted. For example, in a single-bit embodiment, a 0 may indicate a temperature difference in a first range (e.g., 0-5 degrees, 0-10 degrees, 0-12 degrees) and a 1 may indicate a temperature difference in a second range (e.g., >5 degrees, >10 degrees, >12 degrees).

In a two-bit embodiment, four ranges may be supported. For example, a 00 may indicate a first range (e.g., 0-5 degrees, 0-7 degrees, 0-10 degrees), a 01 may indicate a second range (e.g., 6-10 degrees, 8-15 degrees, 11-20 degrees), a 10 may indicate a third range (e.g., 11-15 degrees, 16-20 degrees, 21-25 degrees), and a 11 may indicate a fourth range (e.g., >15 degrees, >20 degrees, >25 degrees). Other embodiments with different numbers of bits may be similarly supported.

Temperature information is gathered for the memory module, 340. In one embodiment, the memory module has only one thermal sensor that is aligned with one of the thermal sensors of the logic die. In alternate embodiments, the memory module may have multiple thermal sensors. The memory module may have management (or other control) circuitry that utilizes temperature information to manage operation of the memory module. In one embodiment, the refresh rate for the memory array is determined based, at least in part, on the operating temperature of the memory module.

The management circuitry utilizes the temperature information from the memory module thermal senor and the temperature difference information to adjust, if necessary, the operational parameters of the memory module, 350. In one embodiment, the refresh rate of the memory module may be determined based on the measured temperature as adjusted by the temperature difference information. Other operational parameters may also be adjusted.

In alternate embodiments, other adjustments may be made utilizing the temperature difference information. For example, if two logic dice are stacked and the respective thermal sensors are not aligned, temperature difference information may be shared between the dice, which will allow the respective control circuits to have more accurate information upon which to base operational parameters.

Figure 4 is a block diagram of one embodiment of an electronic system. The electronic system illustrated in Figure 4 is intended to represent a range of electronic systems (either wired or wireless) including, for example, desktop computer systems, laptop computer systems, cellular telephones, personal digital assistants (PDAs) including cellular-enabled PDAs, set top boxes. Alternative electronic systems may include more, fewer and/or different components.

One or more of the components illustrated in Figure 4 may be on dice that are in physical contact as described above. For example, one or more of processors 410 and one or more DRAM modules that are part of memory 420 may be arranged as described above. Other components may be similarly arranged.

Electronic system 400 includes bus 405 or other communication device to communicate information, and processor 410 coupled to bus 405 that may process information. While electronic system 400 is illustrated with a single processor, electronic system 400 may include multiple processors and/or co-processors. Electronic system 400 further may include random access memory (RAM) or other dynamic storage device 420 (referred to as main memory), coupled to bus 405 and may store information and instructions that may be executed by processor 410. Main memory 420 may also be used to store temporary variables or other intermediate information during execution of instructions by processor 410.

Electronic system 400 may also include read only memory (ROM) and/or other static storage device 430 coupled to bus 405 that may store static information and instructions for processor 410. Data storage device 440 may be coupled to bus 405 to store information and instructions. Data storage device 440 such as a magnetic disk or optical disc and corresponding drive may be coupled to electronic system 400.

Electronic system 400 may also be coupled via bus 405 to display device 450, such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to a user. Alphanumeric input device 460, including alphanumeric and other keys, may be coupled to bus 405 to communicate information and command selections to processor 410. Another type of user input device is cursor control 470, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 410 and to control cursor movement on display 450.

Electronic system 400 further may include network interface(s) 480 to provide access to a network, such as a local area network. Network interface(s) 480 may include, for example, a wireless network interface having antenna 485, which may represent one or more antenna(e). Network interface(s) 480 may also include, for example, a wired network interface to communicate with remote devices via network cable 487, which may be, for example, an Ethernet cable, a coaxial cable, a fiber optic cable, a serial cable, or a parallel cable.

In one embodiment, network interface(s) 480 may provide access to a local area network, for example, by conforming to IEEE 802.11b and/or IEEE 802.11g standards, and/or the wireless network interface may provide access to a personal area network, for example, by conforming to Bluetooth standards. Other wireless network interfaces and/or protocols can also be supported.

IEEE 802.11b corresponds to IEEE Std. 802.11b-1999 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Higher-Speed Physical Layer Extension in the 2.4 GHz Band," approved September 16, 1999 as well as related documents. IEEE 802.11g corresponds to IEEE Std. 802.11g-2003 entitled "Local and Metropolitan Area Networks, Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, Amendment 4: Further Higher Rate Extension in the 2.4 GHz Band," approved June 27, 2003 as well as related documents. Bluetooth protocols are described in "Specification of the Bluetooth System: Core, Version 1.1," published February 22, 2001 by the Bluetooth Special Interest Group, Inc. Associated as well as previous or subsequent versions of the Bluetooth standard may also be supported.

In addition to, or instead of, communication via wireless LAN standards, network interface(s) 480 may provide wireless communications using, for example, Time Division, Multiple Access (TDMA) protocols, Global System for Mobile Communications (GSM)

protocols, Code Division, Multiple Access (CDMA) protocols, and/or any other type of wireless communications protocol.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first die having a thermal sensor;

a second die having a first thermal sensor and a second thermal sensor, the second die in close physical proximity with the first die and the thermal sensor of the first die aligned with the first thermal sensor of the second die;

control logic coupled with the first thermal sensor on the second die and the second thermal sensor on the second die, the control logic to determine a temperature difference between the first thermal sensor on the second die and the second thermal sensor on the second die;

management logic coupled with the control logic and the thermal sensor on the first die, the management logic to receive the temperature difference and a temperature measurement from the thermal sensor on the first die and to manage operational characteristics of the first die based on the temperature difference communicated from the second die and the temperature measurement from the thermal sensor on the first die.

2. The apparatus of claim 1 wherein the first die comprises a dynamic random access memory (DRAM) array.

3. The apparatus of claim 2 wherein the management logic modifies refresh rates of the DRAM array based on the temperature gradient on the second die and the temperature measurement from the thermal sensor on the first die.

4. The apparatus of claim 2 wherein the second die comprises a processor core.

5. The apparatus of claim 2 wherein the second die comprises a system on a chip (SoC).

6. A system comprising:

wireless transceiver circuitry coupled with an antenna;

a first die having a thermal sensor;

a second die having a first thermal sensor and a second thermal sensor, the second die in physical proximity with the first die and the thermal sensor of the first die aligned with the first

thermal sensor of the second die, the second die further coupled with the wireless transceiver circuitry;

control logic coupled with the first thermal sensor on the second die and the second thermal sensor on the second die, the control logic to determine a temperature difference between the first thermal sensor on the second die and the second thermal sensor on the second die;

management logic coupled with the control logic and the thermal sensor on the first die, the management logic to receive the temperature difference from the second die and a temperature measurement from the thermal sensor on the first die and to manage operational characteristics of the first die based on the temperature difference on the second die and the temperature measurement from the thermal sensor on the first die.

7. The system of claim 6 wherein the first die comprises a dynamic random access memory (DRAM) array.

8. The system of claim 7 wherein the management logic modifies refresh rates of the DRAM array based on the temperature difference and the temperature measurement from the thermal sensor on the first die.

9. The system of claim 7 wherein the second die comprises a processor core.

10. The system of claim 7 wherein the second die comprises a system on a chip (SoC).

11. A method comprising:

determining a temperature difference between a first thermal sensor and a second thermal sensor on a first die;

transmitting the temperature difference from the first die to a circuit on a second die;

determining a temperature from a thermal sensor on the second die;

utilizing the temperature difference and the temperature from the thermal sensor on the second die to modify operational characteristics of one or more circuits on the second die.

12. The method of claim 11 wherein the second die comprises a dynamic random access memory (DRAM) array.

13. The method of claim 12 wherein the circuit modifies refresh rates of the DRAM array based on the temperature measurement from the thermal sensor on the second die.

14. The method of claim 12 wherein the first die comprises a processor core.

15. The method of claim 12 wherein the second die comprises a system on a chip (SoC).

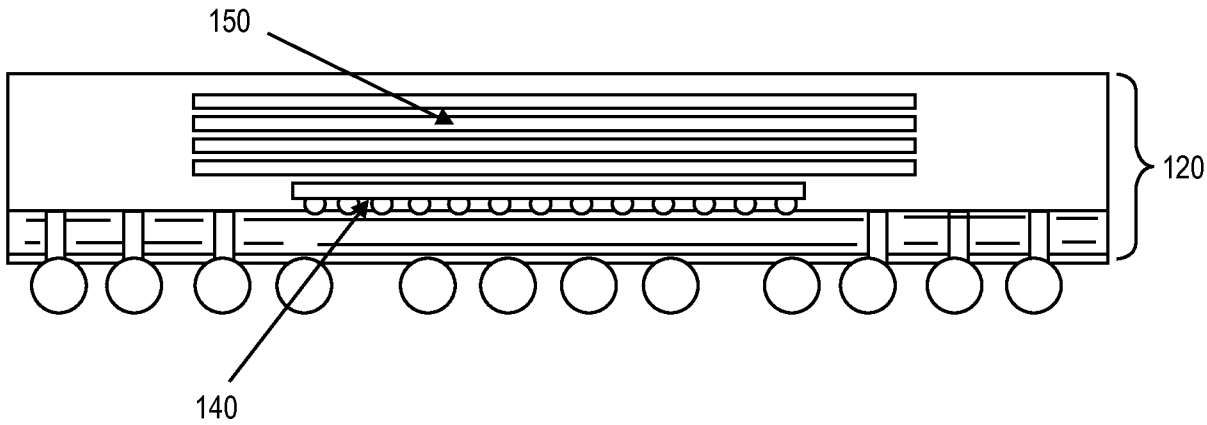

FIG. 1

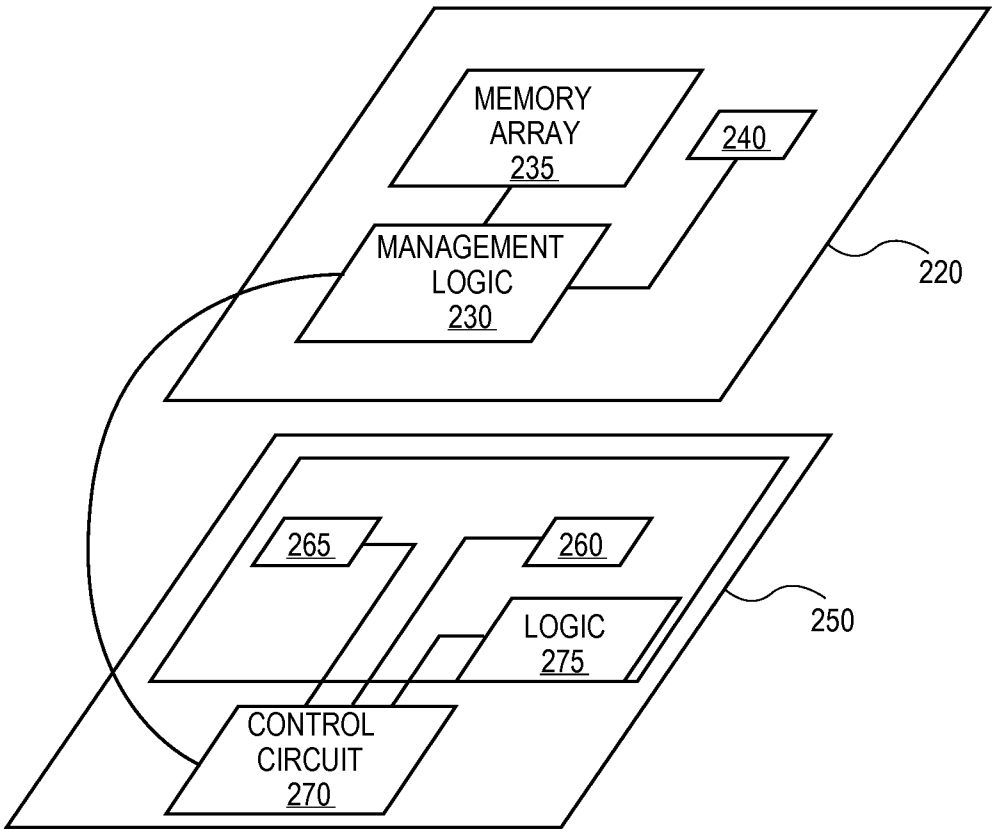
MEMORY
ARRAY
235
240
MANAGEMENT
LOGIC
230
220
265
260
LOGIC
275
250
CONTROL
CIRCUIT
270

FIG. 2

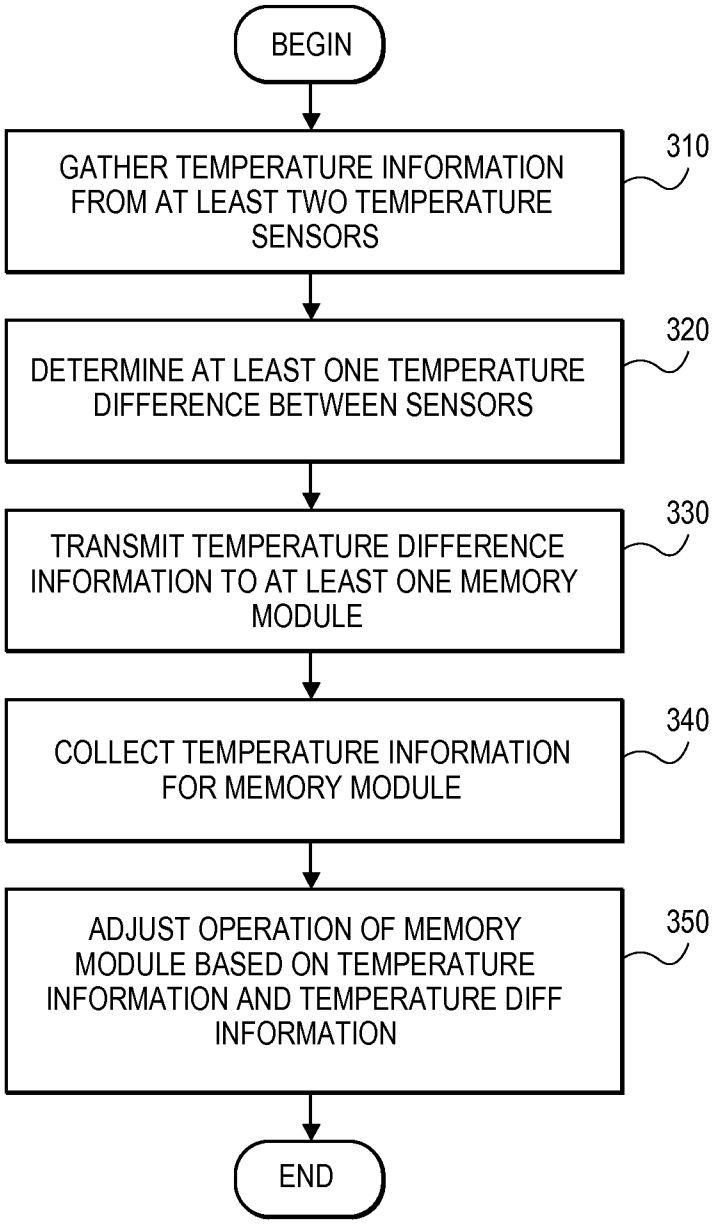
BEGIN
GATHER TEMPERATURE INFORMATION FROM AT LEAST TWO TEMPERATURE SENSORS
310
DETERMINE AT LEAST ONE TEMPERATURE DIFFERENCE BETWEEN SENSORS
320
TRANSMIT TEMPERATURE DIFFERENCE INFORMATION TO AT LEAST ONE MEMORY MODULE
330
COLLECT TEMPERATURE INFORMATION FOR MEMORY MODULE
340
ADJUST OPERATION OF MEMORY MODULE BASED ON TEMPERATURE INFORMATION AND TEMPERATURE DIFF INFORMATION
350
END

FIG. 3

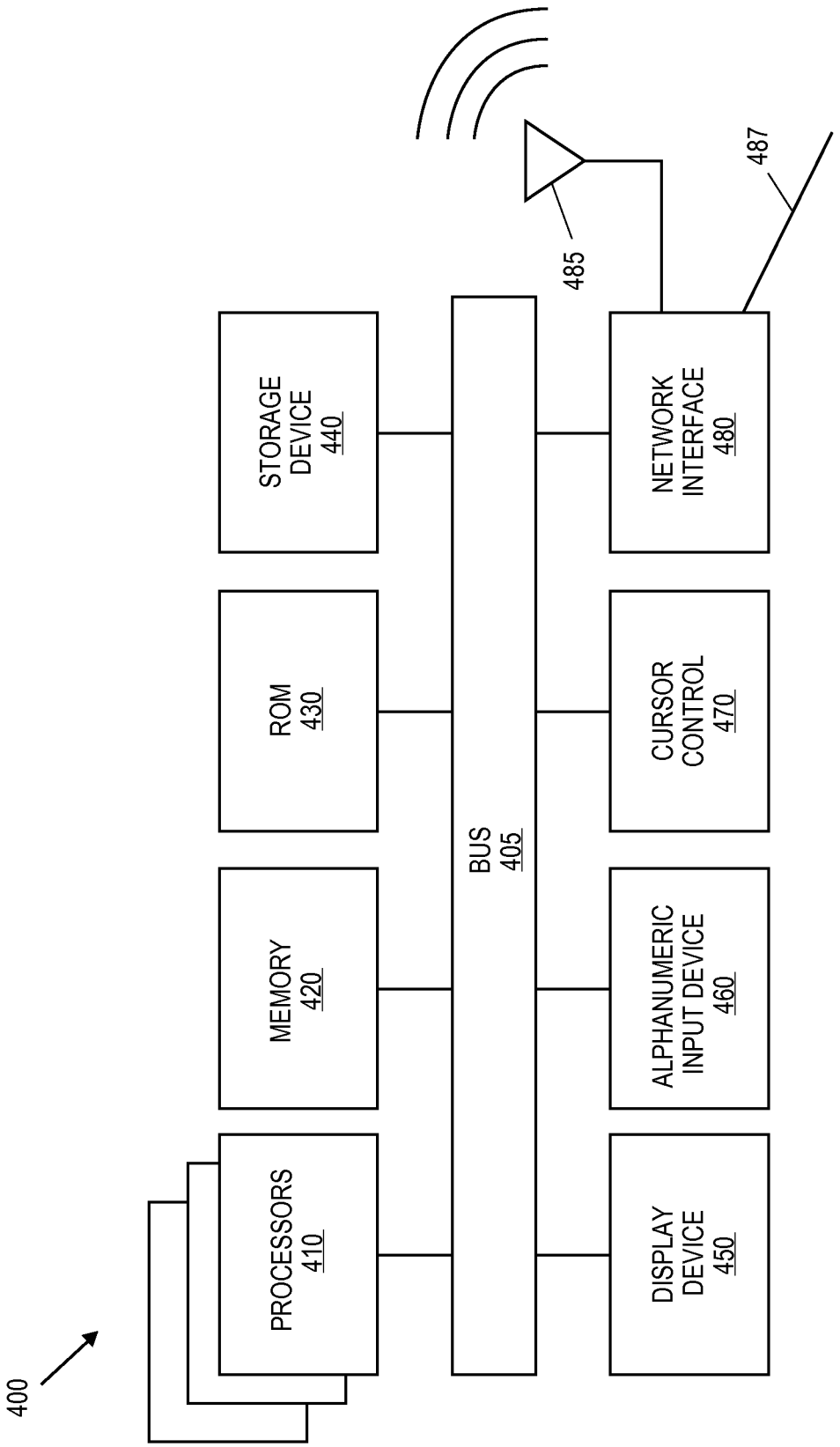
400
PROCESSORS 410
MEMORY 420
ROM 430
STORAGE DEVICE 440
BUS 405
DISPLAY DEVICE 450
ALPHANUMERIC INPUT DEVICE 460
CURSOR CONTROL 470
NETWORK INTERFACE 480
485
487

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/024340

A. CLASSIFICATION OF SUBJECT MATTER

H01L 25/16(2006.01)i, H01L 23/12(2006.01)i, H01L 27/108(2006.01)i, H01L 21/8242(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/16; G11C 7/00; G06F 1/04; H01L 23/34; H01L 23/12; G05D 23/00; H01L 25/07; H01L 25/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: temperature, die, sensor, thermal gradient

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0191993 A1 (DAVID A. WYATT) 16 August 2007 See abstract; paragraphs [0018]-[0065]; claims 1-2; and figure 2.	1-15
A	KR 10-2008-0091941 A (HYNIX SEMICONDUCTOR CO., LTD.) 15 October 2008 See abstract; paragraphs [0019]-[0024]; claims 1-4; and figure 1.	1-15
A	US 2007-0045825 A1 (NANCY CHAN et al.) 01 March 2007 See abstract; paragphs [0019]-[0022]; claims 1,9,12; and figure 1.	1-15
A	JP 2006-108256 A (MITSUBISHI ELECTRIC CORP.) 20 April 2006 See abstract; and claims 1,3.	1-15
A	US 2010-0142291 A1 (JOO JAE HOON et al.) 10 June 2010 See abstract; paragraphs [0040]-[0046]; cliams 1-4; and figure 1.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 SEPTEMBER 2012 (07.09.2012)	**07 SEPTEMBER 2012 (07.09.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Sang Keol

Telephone No. 82-42-481-5742

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/024340

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