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(54) Title: TILE BASED ARCHITECTURE FOR FPGA

(57) Abstract

An FPGA architecture offers logic elements with direct connection to neighboring logic elements and indirect connection through a routing matrix. A logic element and a portion of the routing matrix are formed as part of a tile, and tiles are joined to form arrays of selectable size. The routing matrix includes routing lines which connect just from one tile to the next and routing lines which extend longer distances through several tiles or through the entire chip. This combination is achieved by the formation of individual tiles, all of which are identical.

TILE BASED ARCHITECTURE FOR FPGA

6 FIELD OF THE INVENTION

7   The invention relates to programmable logic devices

8 formed in integrated circuits and more particularly to an

9 architecture of a programmable logic device in which logic

10 blocks are provided in a repeating pattern.

11

12 BACKGROUND OF THE INVENTION

13   Field programmable gate arrays (FPGAs) are well known in

14 the art. An FPGA comprises an array of configurable logic

15 blocks (CLBs) which are programmably interconnected to each

16 other to provide a logic function desired by a user. U.S.

17 Patent 4,870,302, reissued as U.S. Patent Re.34,363, and

18 incorporated herein by reference, describes a well known FPGA

19 architecture. Other publications, such as U.S. Patent

20 4,758,745, U.S. Patent 5,243,238, and published application WO

21 93/05577, also incorporated herein by reference, describe

22 other FPGA architectures. The Xilinx 1993 Data Book entitled

23 "The Programmable Logic Data Book", available from Xilinx,

24 Inc., 2100 Logic Drive, San Jose, California 95124, also

25 incorporated herein by reference, describes several products

26 which implement a number of FPGA architectures.

27   An FPGA is considered to be a general purpose device,

28 i.e. being capable of performing any one of a plurality of

29 functions, and is programmed by an end user to perform a

30 selected function. Because of this design flexibility, a

31 general purpose FPGA includes a significant number of wiring

32 lines and transistors which remain unused in most

33 applications. Moreover, FPGAs include overhead devices which

34 facilitate programing of the FPGA to do the specified

35 function. These overhead devices undesirably add area to the

36 FPGA chip. To compensate for this overhead, it is

37 commercially important to reduce the cost of the FPGA. One

38 way to reduce the cost is to make the FPGA less general

39 purpose, that is, to eliminate some configuration options

40 which are less commonly used. However, this reduction in

1 configuration options reduces the value of the FPGA to

2 customers, who may not be able to predict which options will

3 be needed. Therefore, a need arises to eliminate area while

4 maximizing configuration options.

5

6 SUMMARY OF THE INVENTION

7   In accordance with the present invention, a field

8 programmable gate array (FPGA) architecture includes

9 repeatable tiles. Each tile comprises a programmable routing

10 matrix and a configurable logic block matrix. The

11 configurable logic block matrix is programmably connectable to

12 the programmable routing matrix, as well as to the

13 configurable logic block matrices in adjacent tiles. The

14 programmable routing matrix is programmably connectable to the

15 programmable routing matrices adjacent to the tile, as well as

16 to long lines which extend across the tile. Thus, each tile

17 provides a combination of logic, connection to nearby tiles,

18 and connection to a general routing structure. A plurality of

19 these tiles are joined together to form an array of tiles

20 which make up the functional portion of an FPGA chip. With

21 this architecture, devices of different sizes are produced by

22 simply joining together different numbers of tiles, thereby

23 eliminating an expensive and time consuming design effort.

24 Moreover, in accordance with the present invention, the

25 programmable routing matrix and configurable logic block

26 matrix minimize the number of programmable interconnection

27 points (PIPs), thereby reducing expensive chip area and

28 maximizing density of the entire chip. In further accordance

29 with the present invention, proper positioning of the PIPs

30 ensures the necessary routing flexibility, thereby maximizing

31 functionality of the FPGA.

32   A tile architecture has a set of signal lines exiting the

33 tile at the boundaries. Thus, for example, signal lines

34 exiting at the right of one tile connect with signal lines

35 exiting at the left of another tile. In one embodiment,

36 adjacent tiles are identical, forming a repeating pattern. In

37 another embodiment, adjacent tiles are not identical but have

1 signal lines at least most of which match at the tile

2 boundaries. Thus, a chip can be formed as an array of modular

3 units which match at their boundaries, and additional

4 flexibility of designing tiles for use in a plurality of chip

5 designs is easily available.

6

7 BRIEF DESCRIPTION OF THE DRAWINGS

8   Fig. 1 shows an FPGA chip which includes components

9 according to the present invention.

10   Fig. 2A shows a single core tile which populates a

11 majority of the FPGA chip illustrated in Fig. 1.

12   Fig. 2B shows four adjacent core tiles of the type

13 illustrated in Fig. 2A.

14   Fig. 3A illustrates a configurable logic block matrix

15 which is part of the tile of Fig. 2A.

16   Fig. 3B illustrates a multiplexer structure which

17 implements all PIPs which connect the output lines of a

18 configurable logic block to one output line.

19   Fig. 3C shows one embodiment of a multiplexer structure

20 which drives a configurable logic block input line.

21   Fig. 4C illustrates the configurable logic block in the

22 matrix of Fig. 3A.

23   Fig. 4B illustrates tri-state buffer block 302 of Fig.

24 3A.

25   Fig. 4C illustrates the output enable block 309 of Fig.

26 3A.

27   Fig. 4D shows a look up table embodiment of the F, G, H

28 and J function generators of Fig. 4A.

29   Fig. 4E shows another look up table embodiment of the F,

30 G, H and J function generators of Fig. 4A.

31   Fig. 4F shows one Karnaugh map for the look up table

32 function generator of Fig. 4D or 4E.

33   Fig. 4G shows one of the 2^{16} logic functions which can be

34 implemented by the look up table function generator of Fig. 4D

35 or 4E.

36   Figs. 5A-5C illustrate application of the configurable

37 logic block of Fig. 4A to form a carry chain, a cascadable

1   decode circuit, and two 5-input combinational functions,
2   respectively.
3   Fig. 6 illustrates the programmable routing matrix of
4   Fig. 2A.
5   Fig. 7A illustrates an example of the connectivity
6   achieved by a programmable routing matrix of the invention
7   such as shown in Fig. 6.
8   Fig. 7B illustrates an example of the connectivity
9   achieved by the combination of the programmable routing matrix
10 of Fig. 6 and the tile structure of Fig. 2A or 2B.
11   Fig. 8 illustrates connections from global signal pads
12 near corners of a chip to global signal lines which extend
13 near four edges of the chip and connect to global lines which
14 drive core tiles.
15   Fig. 9 illustrates long line splitters which are provided
16 on long lines in one embodiment of the invention.
17   Figs. 10A-10D illustrate, respectively, left, top, right,
18 and bottom edge tiles according to one embodiment of the
19 invention.
20   Figs. 11A-11D illustrate upper left, upper right, lower
21 right, and lower left corner tiles for the same embodiment.
22   Fig. 12 illustrated a logic diagram for one embodiment of
23 the oscillator structure used in Fig. 11B.
24
25 DETAILED DESCRIPTION OF THE DRAWINGS
26   The following drawing conventions are used throughout the
27 figures. A small solid black dot at the intersections of two
28 lines indicates a permanent electrical connection between the
29 crossing lines. An open circle enclosing an intersection
30 between two lines indicates a programmable connection between
31 the lines (for example, a pass transistor which is turned on
32 to make the connection). Open circles represent bidirectional
33 signal flow between the two lines. An open triangle at an
34 intersection of two lines indicates a programmable connection
35 with signal flow going onto the line pointed to by the apex of
36 the triangle. (The signal is of course then present on the
37 full length of the line. Thus, a triangle pointing in the

1 opposite direction would have the same signal flow because the
2 triangle points to the same wire.)   In accordance with one
3 embodiment of the present invention, programmable connections
4 are provided by using programmable interconnection points
5 (PIPs), wherein each PIP includes at least one transistor.
6   A triangle on a line which is not intersected by another
7 line indicates a buffer which produces signal flow in the
8 direction indicated by the apex of the triangle. Except for
9 global lines ENOUT and ENLL (illustrated in Fig. 3A), a line
10 which ends within the tile or matrix structure (i.e. does not
11 extend to the border of a tile or matrix) is physically
12 terminated within the tile. A line which extends to the
13 border of the tile or matrix connects to a line on the next
14 tile, which it contacts when two tiles are abutted together.
15 Note that some lines which extend to an edge of a tile and
16 thus into an adjacent tile change names at the tile boundary.
17 Lines in the configurable logic block matrix and the
18 programmable routing matrix are given the same reference
19 numeral to indicate these lines are physically connected to
20 each other.
21   Fig. 1 shows an FPGA chip 100 according to the present
22 invention. In the center portion of chip 100 are a plurality
23 of identical core tiles 101, which are interconnected by
24 conductive lines (described in detail below). Along the four
25 edges of chip 100 are west, north, east, and south edge tiles
26 103, 104, 105, 106, respectively. In the four corners of the
27 chip are four corner tiles 113, 114, 115, and 116. Chip 100
28 includes pads, i.e. pads P1-P56, for connecting edge tiles
29 103, 104, 105, 106, and corner tiles 113-116 to external pins
30 of a package (which holds chip 100). Note that each edge tile
31 is further connected to a core tile 101.   As shown in Fig. 1,
32 edge tiles are connected to different numbers of pads P,
33 typically from zero to four pads (explained in detail in
34 reference to Figs. 10a-10d). Fig. 1 also illustrates high
35 voltage source pads VCC and low voltage source pads GND.
36 Power and ground connections (not shown) are provided in a
37 conventional manner throughout chip 100.

1   Fig. 2A shows a core tile 101. Core tile 101 includes a

2 programmable routing matrix 201 and a configurable logic block

3 matrix 202. Programmable routing matrix 201 is described in

4 detail in reference to Fig. 6, whereas configurable logic

5 block matrix 201 is described in detail in reference to Fig.

6 3A.

7   Extending to the west from programmable routing matrix

8 201 are twelve lines with suffixes 0 through 11. These

9 include single length west lines W1-W5, W7-W11, and double

10 length west lines DW0 and DW6 (described in detail below).

11 Extending to the north from programmable routing matrix 201

12 are single length north lines N1-N5, N7-N11 and double length

13 north lines DN0 and DN6. Extending to the east are single

14 length east lines E1-E5 and E7-E11 and double length east

15 lines DE0 and DE6. Extending to the south are single length

16 south lines S1-S5 and S7-S11 and double length south lines DS0

17 and DS6. Extending east to west across tile 101 are double

18 length horizontal lines DH0 and DH6. Extending north to south

19 across tile 101 are double length vertical lines DV0 and DV6.

20   Fig. 2B shows four adjacent core tiles 101a, 101b, 101c

21 and 101d having a configuration identical to tile 101

22 illustrated in Fig. 2A. For clarity in Fig. 2B, most lines

23 are not labeled. As mentioned previously, lines extending to

24 the edges of tile 101 connect to lines in adjacent tiles. For

25 example, single length west line W1b in tile 101b extending to

26 the west from programmable routing matrix 201b connects to

27 single length east line E1a in adjacent tile 101a. Double

28 length horizontal line DH6a of tile 101a is coupled to double

29 length west line DW6b of tile 101b, and is further coupled to

30 a double length east line DE6 of a tile not shown in Fig. 2B

31 but which is located directly west of tile 101a (hence the

32 terminology "double length"). Line Q0c extending east from

33 CLB matrix 202c in tile 101c connects to line QW0d extending

34 west from CLB matrix 202d in tile 101d. Fig. 2B also

35 illustrates that horizontal global lines GH0 and GH1 and

36 vertical global lines GV0 and GV1 extend continuously from one

37 tile 101 to the next. These global lines may be connected to

1   a common line at the edge of the tile so that a signal on a

2   global line such as GH0 extends through all tiles. As shown

3   in Fig. 2B, vertical global lines GV0 and GV1 and horizontal

4   global lines GH0 and GH1 are coupled to both programmable

5   routing matrix 201 and configurable logic block matrix 202.

6   Returning to Fig. 2A, configurable logic block (CLB)

7   matrix 202 is connected to the CLB matrix in the west tile

8   (not shown) by output lines Q0-Q3 and input lines QW0-QW3, to

9   the CLB matrix in the north tile (not shown) by output lines

10 Q0-Q3 and input lines QN0-QN3, to the CLB matrix in the east

11 by output lines Q0-Q3 and input lines QE0-QE3, and to the CLB

12 matrix in the south tile (not shown) by output lines Q0-Q3 and

13 input lines QS0-QS3. Note that output lines Q0-Q3 carry the

14 same signals from CLB matrix 202 to adjacent tiles in four

15 directions and thus have the same names. Carry-in line CIN

16 and carry-out line COUT, which extend vertically in tile 101,

17 connect to carry-out and carry-in lines, respectively, in

18 adjacent tiles to form a fast carry path for arithmetic

19 functions, as discussed in detail in U.S. Patent No.

20 5,349,250, "LOGIC STRUCTURE AND CIRCUIT FOR FAST CARRY", which

21 is incorporated herein by reference.

22

23 Configurable Logic Block Matrix 202

24   Fig. 3A illustrates configurable logic block (CLB) matrix

25 202 of Fig. 2a. CLB matrix 202 includes a CLB 301, a tristate

26 buffer block 302, an input interconnect structure 303, a CLB

27 output interconnect structure 304, a feedback interconnect

28 structure 305, a general input interconnect structure 306, a

29 register control interconnect structure 307, an output

30 interconnect structure 308, and an output enable block 309.

31

32 Sparse Pipulation

33   Programmable connections are provided by using

34 programmable interconnection points (PIPs), wherein each PIP

35 includes at least one transistor. As is well known in the

36 art, each transistor occupies valuable space on the chip

1 substrate.   Thus, in accordance with the present invention and

2 referring to Fig. 3A, a majority of the horizontal and

3 vertical lines in input interconnect structure 303, feedback

4 interconnect structure 305, general input interconnect

5 structure 306, and register control interconnect structure 307

6 are not programmably connectable.   In other words, these

7 structures are sparsely populated with PIPs, or are sparsely

8 "pipulated". Sparse pipulation minimizes chip area used by

9 PIPs, thereby maximizing density of the entire chip.   In

10 further accordance with the present invention, proper

11 positioning of the PIPs significantly increases routing

12 flexibility, thereby effectively compensating for the reduced

13 number of PIPs in the interconnect structures.

14   For example, referring to input interconnect structure

15 303, PIPs are positioned to allow connection from each output

16 line Q0-Q3 from CLB output interconnect structure 304 to one

17 of the function generators F, G, H, or J of an adjacent tile

18 in each of the four compass directions.   In this embodiment,

19 general input interconnect structure 306 provides four to six

20 PIPs for each CLB input line (J0-J3, JB, H0-H3, HB, G0-G3, GB,

21 F0-F3 and FB) to CLB 301.   Feedback interconnect structure 305

22 provides direct connections from two of output lines Q0-Q3 to

23 one of the function generator input terminals in CLB 301.   As

24 shown in Fig. 3A, 24 PIPs in output interconnect structure 308

25 connect output lines Q0-Q7 to tile interconnect lines M0-M23.

26 In this manner, signals on tile interconnect lines M0-M23 are

27 selectively transferred between CLB 301 and programmable

28 routing matrix 201 (via CLB output interconnect structure 304,

29 general input interconnect structure 306, and output

30 interconnect structure 308).   In this embodiment, less than

31 one intersection in eight is provided with a PIP, thereby

32 minimizing silicon area.   Yet, connectivity from any output

33 line to any input line is ensured by the PIPs provided.

34

35 Configurable Logic Block 301

36   A configurable logic block (CLB) 301 is illustrated in

37 Fig. 4A.   In this embodiment, CLB 301 includes four function

1 generators F, G, H, and J, wherein each function generator
2 comprises a 16-bit look up table that generates an output
3 signal determined by the four input signals provided to the
4 function generator and the values stored in the look up table.
5 Thus, function generator F generates an output signal
6 determined by the input signals provided on lines F0-F3,
7 function generator G generates an output signal determined by
8 the signals provided on CLB input lines G0-G3, function
9 generator H generates an output signal determined by the
10 signals provided on CLB input lines H0-H3, and function
11 generator J generates an output signal determined by the
12 signals provided on CLB input lines J0-J3.
13
14 Look Up Table
15   Operation of the look up table function generators will
16 be described in connection with Figs. 4D-4G. These figures
17 were first discussed by Freeman in U.S. Patent 4,870,302 now
18 reissued as U.S. Patent Re 34,363, incorporated herein by
19 reference.
20   Fig. 4D illustrates a look up table, in this embodiment a
21 16-bit RAM, which provides an output signal in response to any
22 one of sixteen possible combinations of four input signals.
23 Specifically, input signals A and B control the X decoder to
24 select any one of the four columns in the 16-bit RAM. In a
25 similar manner, input signals C and D control the Y decoder to
26 select any one of the four rows in the 16-bit RAM. The 16-bit
27 RAM provides an output signal representative of the bit at the
28 intersection of the selected row and the selected column.
29 There are 16 such intersections and thus sixteen such bits.
30 It logically follows that 16 bits provide 2^{16} possible
31 combinations. Thus, if a 4-input NOR gate is to be simulated
32 by the 16 bit RAM, the Karnaugh map for the look up table
33 would be as shown in Fig. 4F. In Fig. 4F, all bits are "0"
34 except the bit at the intersection of the first row
35 (representing A=0, B=0) and the first column (representing
36 C=0, D=0). If a logic "1" output signal is desired for A=1,
37 B=0, C=0, D=0, then a logic "1" is stored at the intersection

1 of the second row and the first column. If a logic "1" is

2 desired for A=0, B=0, C=0, and D=0 and also for A=1, B=0, C=0

3 and D=0, then a logic "1" is stored at each of the

4 intersections of the first column with the first row and the

5 second row. The logic circuit represented by this loading of

6 the look up table is shown in Fig. 4G. Thus, the look up

7 table of Fig. 4D represents an elegant and simple

8 implementation of any one of 2^{16} logic functions.

9   Fig. 4E shows a register configuration for yielding any

10 one of sixteen select bits. Each of registers 0-15 in the

11 vertical column to the left labeled "16 Select Bits", contains

12 a selected signal, either a logic 1 or 0. By selecting the

13 appropriate combination of signals A, B, C, and D and their

14 complements, a particular bit stored in a particular one of

15 the sixteen locations in the 16 Select Bits register is

16 transmitted to the output lead OUT. Thus, for example, to

17 transmit the bit in the "1" register to the output lead, the

18 signal A, B, C, D is applied to the leads so labeled. To

19 transmit the signal labeled "15" in the sixteenth location in

20 the 16 Select Bits register to the output lead, the signal A,

21 $\bar{B}$, $\bar{C}$, $\bar{D}$ is applied to the appropriate columns. Thus, this

22 register configuration also provides any one of 2^{16} logic

23 functions.

24   Referring back to Fig. 4A, the memory bits in look up

25 tables F, G, H and J are typically loaded during configuration

26 of the chip, for example through a shift register, or

27 alternatively by an addressing means. In some embodiments,

28 the memory bits are also loaded during operation of the chip,

29 thereby reconfiguring the chip on the fly. A reconfigurable

30 memory structure is discussed in commonly assigned, U. S.

31 Patent No. 5,343,406 invented by Freeman et al. and entitled

32 "Distributed Memory Architecture for a Configurable Logic

33 Array and Method for Using Distributed Memory", which is

34 incorporated herein by reference.

35   Function generators F, G, H, and J provide output signals

36 on CLB output lines X, Y, Z, and V, respectively. These

37

1 output signals from function generators F, G, H, and J control
2 multiplexers C1, C2, C3, and C4, thereby providing a
3 cumulative carry-out function COUT. Multiplexer C1 receives a
4 carry-in signal on line CIN and an input signal on line FB,
5 and generates an output signal on line CF. Multiplexer C2
6 receives the signal on line CF and an input signal on line GB,
7 and generates an output signal on line CG. Multiplexers C3
8 and C4 are connected in the same manner as Multiplexers C1 and
9 C2. Multiplexer C4 provides an output signal on line COUT
10 from CLB 301. For a detailed discussion of the implementation
11 of arithmetic functions, see commonly assigned U.S. Patent No.
12 5,349,250 invented by Bernard E. New, entitled "LOGIC
13 STRUCTURE AND CIRCUIT FOR FAST CARRY", which is incorporated
14 herein by reference.
15   In addition to function generators F, G, H, and J, each
16 CLB 301 includes four storage devices RX, RY, RZ, and RV.
17 These storage devices RX, RY, RZ, and RV each comprise flip
18 flops with master and slave stages and an output multiplexer
19 which takes outputs from the master and slave stages as
20 inputs. Thus devices RX, RY, RZ, and RV can be configured by
21 the multiplexer to serve as either flip flops or as latches.
22   Typically, periodic repowering of the carry signal is
23 necessary. In this embodiment, to provide this repowering, a
24 repowering buffer comprising inverters I121 and I122 is
25 positioned every four multiplexers in the carry path, or once
26 every CLB 301. In another embodiment, a repowering buffer is
27 provided every two multiplexers in the carry path, thus two
28 repowering buffers are provided in every CLB 301.
29   In this embodiment, CLB 301 includes five input lines per
30 function generator. For example, referring to function
31 generator F, CLB input lines F0-F3 provide input signals to
32 function generator F, and a fifth CLB input line FB provides a
33 multiplexer control input signal. Function generators G, H,
34 and J are configured in a similar manner. Three input lines
35 CLK, CE, and RST provide clock, clock enable, and reset
36 signals, respectively, to registers RX, RY, RZ, and RV.

1   As shown in Fig. 4A, four groups of three output signals
2 are provided from CLB 301, one group associated with each
3 function generator. The three output signals include:
4   •a direct, unregistered output signal from the function
5   generator (provided on CLB output lines X, Y, Z, or V),
6   •an alternative, unregistered output signal which may be
7   derived from one of the CLB input signals, a signal from
8   the carry chain, or in two cases a signal from a
9   multiplexer which provides an output signal of a five-
10   input function (provided on CLB output lines XB, YB, ZB,
11   or VB), and
12   •a registered, output signal which may be loaded by the
13   function generator or by one of the sources of the
14   alternative output signal (provided on CLB output lines
15   XQ, YQ, ZQ, or VQ).
16 For example, CLB output line X receives a direct unregistered
17 output signal from function generator F. CLB output line XB
18 receives either the signal on CLB input line FB or the output
19 signal of multiplexer S1 (as determined by multiplexer B1),
20 which in turn is derived from either the carry-out signal CF
21 or the five-input function-generator output signal from
22 multiplexer FG (see discussion of Fig. 5C below). CLB output
23 line XQ receives the registered output signal from register
24 RX, which derives its D input signal either directly from
25 function generator F (the signal on output line X) or the
26 alternative output signal on line XB as determined by
27 multiplexer D1. Finally, output line K provides a constant
28 signal, which may be high or low, as selected by multiplexer
29 PG.
30   In the embodiment of Fig. 4A, multiplexers D1-D4
31 selectively provide either the output signals from function
32 generators F, G, H, and J (the same signals on CLB output
33 lines X-V) or the output signals from multiplexers B1-B4 to
34 registers RX-RV, respectively. If multiplexers S1 and S3 are
35 set to forward the carry signals of multiplexers C1 and C3,
36 respectively, then multiplexers B1-B4 select between the input

1   signals on CLB input lines FB-JB, respectively, and the output

2   signals of multiplexers C1-C4.

3   Multiplexers C1-C4, in addition to being used for the

4   carry function in an arithmetic operation, also generate wide

5   AND and OR functions. To generate the AND function, a logic 0

6   is placed on line FB to program multiplexer C1 to generate an

7   AND function of the F function generator output signal on CLB

8   output line X and the carry-in signal on line CIN.

9   Alternatively, to generate the OR function, a logic 1 is

10 placed on CLB input line FB to program multiplexer C1 to

11 generate an OR function of the complement of the output signal

12 on CLB output line X and the carry-in signal on line CIN.

13 With a truth table architecture, the OR function is achieved

14 by loading the inverse values into the truth table. The

15 function of multiplexers C1-C4 and their interaction with the

16 logic block are further discussed in application serial no.

17 08/116,659 [M-2565] incorporated by reference.

18

19 Example Applications of CLB 301

20   Figs. 5A-5C illustrate applications using CLB 301

21 (described in detail in reference to Fig. 4A) to form a carry

22 chain, a cascadable decode circuit and 2 five-input functions,

23 respectively. These figures use heavy lines to illustrate

24 lines of CLB 301 which are used for the particular selected

25 function and thin dashed lines to indicate lines and elements

26 not used for the particular function.

27   In Fig. 5A, CLB 301 is configured to compute a half sum

28 H3H2H1H0 (where H3, H2, H1, and H0 are the four bits of a

29 four-bit half-sum) and the carry bits C3C2C1C0 of two numbers

30 A3A2A1A0 and B3B2B1B0. Another CLB (not shown), preferably

31 positioned in the tile to the right or left of the one shown,

32 will be used to complete the sum. Operands A3 and B3 are

33 placed on any two of CLB input lines J0-J3. Operands A2 and

34 B2 are placed on any two of CLB input lines H0-H3. A1 and B1

35 are placed on any two of CLB input lines G0-G3. A0 and B0 are

36 placed on any two of CLB input lines F0-F3. Unused lines are

37 either held high or held low. Each of function generators F,

1   G, H, and J is loaded with the truth table of the XOR function
2   (which is the half sum of its input signals). The truth table
3   takes into account the values applied to unused input lines.
4   If there are lower order bits than those applied to function
5   generator F, the carry-out of those bits is placed on carry in
6   line CIN. Multiplexers C1, C2, C3, and C4 are controlled by
7   the output signals of function generators F, G, H and J,
8   respectively. Specifically, if the function generator output
9   signal is a logic 1 (signals A and B are not equal), the
10 carry-in value is forwarded to the carry-out of that bit, and
11 if the function generator output signal is a logic 0 (signals
12 A and B are equal), the value of signal A or signal B is
13 forwarded to the carry-out of that bit. Multiplexers B1-B4,
14 S1 and S3 are controlled to forward the carry-out of each bit
15 to the "B" CLB output line (i.e. CLB output lines XB, YB, ZB,
16 and VB) of that bit. The function generator output signal for
17 each bit (on CLB output lines X, Y, Z, and V) is provided as
18 the half sum output for that bit.
19   In another application shown in Fig. 5B, CLB 301 is
20 configured to operate as a cascadable decoder. A 16-bit
21 address represented by signals A0-A15, is placed on CLB input
22 lines F0-F3, G0-G3, and J0-J3. CLB input lines FB, GB, HB,
23 and JB are grounded. The 16 bits of each of function
24 generators F, G, H, and J include a single logic 1 to reflect
25 a portion of a predetermined address. A logic 1 signal is
26 placed on carry in line CIN. If all four function generators
27 F, G, H, and J output their respective logic 1s (i.e.
28 indicating an address "match"), then multiplexers C1-C4 all
29 forward a logic 1 and produce a logic 1 signal on carry out
30 line COUT.
31   In yet another application shown in Fig. 5C, CLB 301 is
32 configured to generate two functions of five input signals
33 each. Function generators F and G generate a first function
34 of five input signals on CLB output line XB and function
35 generators H and J generate a second function of five input
36 signals on CLB output line ZB. For the first function, four
37 input signals A0-A3 are provided on the CLB input lines to

14

1   both function generators F and G and the fifth input signal A4
2   is provided to line FB. Input signal A4 causes multiplexer FG
3   to select the output signal of function generator F or
4   function generator G. In this embodiment, multiplexer S1 is
5   programmed by its memory cell to select the output signal of
6   multiplexer FG, and multiplexer B1 is programmed by its memory
7   cell to select the output signal of multiplexer S1. Thus, the
8   five-input function output signal from function generators F
9   and G is provided on CLB output line XB. In a similar manner,
10 the function of the five input signals B0-B4 provided to
11 function generators H and J is generated on CLB output line
12 ZB.
13   Loading the appropriate truth tables into the two
14 associated function generators F and G produces the desired
15 function of five input signals. Specifically, in one
16 embodiment, a 32-bit look up table is stored in function
17 generators F and G (i.e. two 16-bit look up tables). Thus, a
18 large number of functions are alternatively provided by
19 loading different values into the memory cells which form the
20 truth tables of the function generators and control
21 multiplexers FG and HJ.
22
23 Tristate Buffer 302
24   Fig 4B illustrates a schematic drawing of tri-state
25 buffer block 302 (Fig. 3A) which includes tristate buffers B4-
26 B7. Note that the line names are identical to those
27 referenced in Fig. 3A. Output signals from AND gates A4-A7
28 control tristate buffers B4-B7, respectively. If AND gate A5,
29 for example, provides a logic 0 output signal, buffer B5 is
30 enabled and provides a buffered output signal on line TQ5
31 which matches its corresponding input signal on line Q5. On
32 the other hand, if AND gate A5 provides a logic 1 output
33 signal, buffer B5 is disabled and provides a high impedance
34 at the output terminal. The output signals provided by AND
35 gates A4-A7 are determined either globally by the output
36 signal from OR gate OR1 or individually by memory cells
37 MM4-MM7, respectively. If memory cells MM4-MM7 store logic

15

1 0's, then the output signals of AND gates A4-A7 will also be

2 logic 0's regardless of the signal from OR gate OR1. OR gate

3 OR1 provides a high output signal if·the ENLL signal is low or

4 if the signal on line TS is high. Referring back to Fig. 3A,

5 the signal on tristate line TS is programmably selected from

6 any of tile interconnect lines M16-M23.

7   The ENLL signal is a global signal provided to all

8 buffers 302 in all tiles 101. The ENLL signal is held low

9 during configuration and as other signals are being enabled

10 after configuration in order to prevent contention which could

11 result if various TS lines which are to connect input signals

12 to the same long line are switching unpredictably during

13 configuration.

14   If buffers B4-B7 are to be used during operation as

15 repowering buffers (always enabled) for placing a signal onto

16 a long line, memory cells MM4-MM7 are loaded with low values

17 during configuration. This means that during configuration,

18 AND gates A4-A7 will enable buffers B4-B7. However, no

19 contention occurs because the input signals Q4-Q7 which drive

20 signals TQ4-TQ7 onto long lines all carry a common signal

21 during configuration, as will now be discussed in connection

22 with Fig. 4C.

23

24 Output Enable Block 309

25   The buffers in output enable block 309 are disabled

26 during configuration of the device so that lines driven by

27 these buffers will not experience contention. Fig. 4C

28 illustrates the structure of block 309. Each buffer in output

29 enable block 309 comprises a two-input AND gate. One input of

30 each AND gate is driven by a global enable signal ENOUT. The

31 other input is provided by a line Q0'-Q7' which is in turn

32 provided by output signals from CLB 301 (Fig. 3A). During

33 configuration, unexpected lines may be connected to these

34 lines Q0-Q7. Therefore, to prevent contention, the ENOUT

35 signal is held low during configuration so that all output

36 signals on lines Q0-Q7 are low and unexpected connection of

1   other lines does not produce contention because all signals

2   have a low value.

3

4   <u>Neighbor Input Matrix 303</u>

5   Referring back to Fig. 3A, in accordance with this

6   embodiment of the present invention, adjacent CLBs 301 are not

7   connected via direct connections, only via PIPs. For example,

8   input signals are selectively provided to CLB 301 from input

9   interconnect structure 303. Thus, each input line QS0-QS3 is

10   connectable to one of the CLB input lines of one function

11   generator. In this embodiment, line QS0 is connectable to CLB

12   input line F1 of function generator F, line QS1 is connectable

13   to CLB input line G1 of function generator G, line QS2 is

14   connectable to CLB input line H1 of function generator H, and

15   line QS3 is connectable to CLB input line J1 of function

16   generator J. Because each function generator F, G, H or J is

17   configurable to provide any function based on its input

18   signals, a particular signal can be provided to any input

19   terminal of a function generator and the look up table of that

20   function generator loaded accordingly. Thus, it is not

21   important which input signal is available to which function

22   generator input terminal.

23   A signal on input line QW0 drives both CLB input lines F0

24   and FB. Similarly, a signal on input line QW1 drives CLB

25   input lines G0 and GB, a signal on input line QW2 drives CLB

26   input lines H0 and HB, and a signal on input line QW3 drives

27   CLB input lines J0 and JB. Each signal on input lines QE0,

28   QE1, QE2, and QE3 also drives two CLB input lines.

29   Specifically, a signal on input line QE0 drives CLB input

30   lines F1 and FB, a signal on input line QE1 drives lines G1

31   and GB, a signal on input line QE2 drives lines H1 and HB, and

32   a signal on input line QE3 drives lines J1 and JB.

33   Signals on input lines QN0-QN3 and QS0-QS3 each drive

34   only one CLB input line. Specifically, a signal on input line

35   QN0 drives CLB input line F0, a signal on input line QN1

36   drives CLB input line G0, a signal on line QN2 drives CLB

37   input line H0, and a signal on line QN3 drives CLB input line

1 J0. A signal on input line QS0 drives CLB input line F1, a
2 signal on input line QS1 drives CLB input line G1, a signal on
3 input line QS2 drives CLB input line H1, and a signal on input
4 line QS3 drives CLB input line J1. This embodiment is
5 particularly desirable for horizontal flow of many signals
6 because each input line QE0-QE3 and QW0-QW3 is programmably
7 connected to two CLB input lines. Other embodiments of the
8 present invention, having a different number and positioning
9 of programmable connections, are optimized for a different
10 signal flows.
11
12 Output Matrix 304
13   CLB 301 provides output signals on CLB output lines X,
14 XQ, XB, Y, YQ, YB, Z, ZQ, ZB, V, VQ, and VB. Note that CLB
15 301 also determines whether it provides the signal on carry
16 out line COUT or whether the signal on carry in line CIN is
17 transferred to the next CLB in the tile above. PIPs on CLB
18 output lines X, XQ, XB, Y, YQ, YB, Z, ZQ, ZB, V, VQ, VB, and K
19 are selectively programmed to drive any number of output lines
20 Q0-Q7 through a CLB interconnect structure 304. Note that CLB
21 interconnect structure 304 is fully pipulated (i.e., any of
22 the 13 output signals of CLB 301, excluding the signal on
23 carry out line COUT, can drive any of output lines Q0-Q7).
24 Note that interconnect structure 304 also buffers its output
25 signals for driving further lines. Full pipulation of
26 interconnect structure 304 requires 108 (13 x 8) PIPs. In
27 contrast, structures 303, 305, 306, and 307 in combination use
28 200 PIPs, even though they are sparsely pipulated.
29 Flexibility of CLB 301 to access a particular input signal
30 from tile interconnect lines M0-M23 is ensured by:
31   •fully pipulating CLB output interconnect structure 304
32   so that any CLB output signal can be provided to any of
33   tile interconnect lines M0-M23;
34   •pipulating programmable routing matrix 201 so that each
35   line M0-M23 is connected to at least one line M0-M23 in
36   each adjacent routing matrix 201 (see discussion of Fig.
37   6 below);

1   •pipulating CLB matrix 202 so that each output line of
2   one CLB can be connected to at least one input line of
3   each adjacent CLB; and
4   •forming function generators F, G, H, and J as look up
5   tables, thereby allowing all input signals to each look
6   up table to be interchangeable.
7   •Moreover, except for five-input functions, function
8   generators F, G, H, J are also interchangeable.
9   Thus, in accordance with the present invention, the above-
10   described sparsely pipulated structures 303, 305, 306 and 307
11   significantly reduces chip area while maximizing flexibility.
12   Signals on output lines Q0-Q3 drive the input lines of
13   CLBs in neighboring tiles. For example, by placing two core
14   tiles 101 of Fig. 2A side by side, as in shown in Fig. 2B,
15   output line Q0 on the left edge of core tile 101b connects to
16   input line QE0 on the right edge of tile 101a. Other lines
17   are correspondingly connected. Thus, referring to Figs. 2A,
18   2B, and 3 in combination, CLB output line X (Fig. 3A) of CLB
19   301 in CLB matrix 202c (see Fig. 2B) is programmably connected
20   to output line Q0c, which extends east (as well as other
21   directions) from CLB matrix 202c in core tile 101c, which in
22   turn is connected to input line QW0d of CLB matrix 202d in
23   core tile 101d. PIPs are provided (as discussed above) for
24   connecting input line QW0 to CLB input lines F0 and FB of CLB
25   301. Thus, in this manner, a path is established from the
26   output lines of CLB 301 in CLB matrix 202c to the input lines
27   of CLB 301 in CLB matrix 202d using only two PIPs, which in
28   one embodiment includes two transistors.
29   In another embodiment, shown in Fig. 3B, a PIP in CLB
30   output interconnect structure 304 requires a signal on a CLB
31   output line to propagate through two transistors (note that
32   signal K, a constant power or ground signal, propagates
33   through four transistors). Fig. 3B illustrates a multiplexer
34   structure 400 which implements all PIPs which connect the
35   twelve CLB output lines (X, XQ, XB, Y, YQ, YB, Z, ZQ, ZB, V,
36   VQ, VB) of CLB 301 and one power/ground output signal line K
37   to output line Q0. Multiplexer structure 400 includes memory

1 cells 31, 32, and 33 which control a first bank of twelve

2 transistors 351 and select signal K if no transistor in bank

3 351 is selected. A logic 1 stored in one of memory cells 31,

4 32, and 33 selects one signal from each group of three signals

5 in bank 351. If all memory cells 31, 32, and 33 store a logic

6 0, then signal K is provided to node 30. In a second stage,

7 memory cells 34 and 35 control AND gates AND1-AND4 to select

8 the output signal from one of output lines VQ, ZQ, YQ, and XQ

9 and to provide the selected signal on output line Q0. If

10 memory cells 31, 32, and 33 store a logic 0, thereby selecting

11 signal K, then memory cells 34 and 35 must be programmed to

12 provide the signal at node 30. Thus, thirteen PIPs are

13 implemented using only 5 memory cells and sixteen transistors,

14 each path requiring only two transistors for all signals

15 except the constant value K, which travels a longer path. The

16 signal on line K is not harmed by having a longer signal path

17 since it is not a switching signal. A multiplexer structure

18 400, which selects one of thirteen output signals of CLB 301

19 to drive a predetermined output line, is provided for each of

20 output lines Q0-Q7. Note that although it is possible for

21 none of the thirteen output signals to drive an output line

22 Q0-Q7, multiplexer structure 400 cannot select more than one

23 of the thirteen output signals. In this manner, contention on

24 output lines Q0-Q7 is avoided. In another embodiment of

25 multiplexer structure 400, thirteen memory cells are provided,

26 each memory cell controlling a single transistor. In this

27 manner, each path requires only one transistor, thereby

28 increasing signal speed. However, note that this embodiment

29 increases silicon area.

30

31 Feedback Interconnect Structure 305

32   Referring back to Fig. 3A, feedback interconnect

33 structure 305 selectively connects output lines Q0-Q3 to CLB

34 input lines F2, G2, H2, and J2 within configurable logic block

35 matrix 202. Thus, in this embodiment, any output signal from

36 CLB 301 can be fed back to selected CLB input lines of any

37 function generator F, G, H and J in CLB 301. Feedback

1 interconnect structure 305 provides a PIP pattern that

2 supports a counter (a counter feeds back its own signal) or a

3 shift register (a shift register requires its neighbor's

4 signal). The above-described PIP pattern prevents contention

5 between signals on CLB input lines F2, G2, H2 and J2 and

6 signals on CLB input lines F0, G0, H0, J0, F1, G1, H1, and J1

7 which are provided on other input lines to CLB matrix 202,

8 such as input lines QW0 and QN3. Other embodiments of the

9 present invention provide different combinations of PIPs in

10 feedback interconnect structure 305. ·

11

12 General Input Matrix 306

13   General input matrix 306 receives input signals on tile

14 interconnect lines M0-M23 and includes PIPs for placing these

15 input signals onto CLB input lines F0-F3, FB, G0-G3, GB, H0-

16 H3, HB, J0-J3, and JB. Optionally, a PIP pattern allows a

17 signal on any tile interconnect line M0-M23 in general input

18 interconnect structure 306 to drive one input line of each

19 function generator F, G, H, and J. Because function generator

20 input signals are interchangeable, (Lookup table inputs are

21 interchangeable.) no tile interconnect line M0-M23 need be

22 coupled to more that one input line of a function generator.

23 In this embodiment of general input interconnect structure

24 306, PIPs are provided so that each CLB input line FB, GB, HB,

25 and JB is driven by a signal on one of six tile interconnect

26 lines M0-M23.

27   As another criterion in this embodiment, no CLB input

28 line includes more than eight PIPs. Thus, referring to Fig.

29 3C, a multiplexer structure 401, using only three memory cells

30 36, 37 and 38, selects one of eight possible signals to

31 control a first bank of transistors 361. Specifically, memory

32 cell 38 selects one each of the paired signals on input lines

33 QW0 or QN0, M15 or M14, M9 or M8, and M7 or M6. Memory cells

34 36 and 37 provide signals to the input terminals of AND gates

35 AND5-AND8, which in turn control a second bank of transistors

36 362 to select a single signal to place on CLB input line F0.

1   In this embodiment of the present invention, the pattern
2   of PIPs also provides a function of five inputs (discussed
3   above in connection with Fig. 5C). For example, a signal on
4   tile interconnect line M18 or M19 drives input line FB, a
5   signal on tile interconnect line M14 or M15 drives lines F0
6   and G0, a signal on tile interconnect line M12 or M13 drives
7   lines F1 and G1, a signal on tile interconnect line M16 or M17
8   drives input lines F2 and G2 and a signal on tile interconnect
9   line M20 or M21 drives input lines F3 and G3. In this
10 configuration, five-input functions are easily implemented
11 with the PIP pattern provided.
12   In further accordance with the present invention, and
13 referring to Figs. 3A and 6, PIPs allow connection from long
14 horizontal lines LH0-LH7 and long vertical lines LV0-LV7, as
15 well as global (horizontal and vertical) lines GH0, GH1, GV0,
16 and GV1 to registers RV, RZ, RY, and RX without going through
17 function generators J, H, G, and F. Specifically, long
18 horizontal lines LH0-LH7 and long vertical lines LV0 and LV7
19 as well as global horizontal lines GH0, GH1 and global
20 vertical lines GV0, GV1 are selectively coupled to tile
21 interconnect lines M0-M23 (Fig. 6). These tile interconnect
22 lines, if coupled to CLB input lines FB, GB, HB and JB, bypass
23 function generators F, G, H and J, respectively, and provide
24 signals (via intermediate multiplexers) to registers RX, RY,
25 RZ, RV, respectively (Fig. 3A). Note that global lines GH0,
26 GH1, GV0, and GV1 are also selectively coupled to registers
27 RX, RY, RZ and RV via register control interconnect structure
28 307. Allowing all tile interconnect lines M0-M23 to connect
29 to one CLB input line FB, GB, HB or JB and providing
30 connections from every long line to one tile interconnect line
31 M0-M23 (discussed below in connection with Fig. 6) assures
32 that signals on those long and global lines can drive the
33 necessary registers. In the present invention, this PIP
34 pattern also allows signals on all long lines and global lines
35 to drive input lines to function generators F, G, H and J via
36 general input interconnect structure 306.
37

1 <u>Output Interconnect Matrix 308</u>

2   In this embodiment, output lines Q4-Q7 also provide

3 output signals to programmable interconnect matrix 201 (Fig.

4 2A) via tile interconnect lines M0-M11 or via lines TQ4-TQ7.

5 Output lines Q0-Q3 also provide output signals to selected

6 ones of tile interconnect lines M12-M23. In the embodiment

7 shown in Fig. 3A, output interconnect structure 308 allows

8 signals on each output line Q0-Q7 to drive up to three tile

9 interconnect lines M0-M23. The full pipulation of CLB output

10 interconnect structure 304 allows any output line of CLB 301

11 to be connected to any tile interconnect line M0-M23. Note

12 that general input interconnect structure 306 also provides

13 selected feedback signals on output lines Q0-Q3 to CLB 301.

14

15 <u>Register Control Interconnect Structure 307</u>

16   Clock line CLK, clock enable line CE, reset line RST and

17 tristate line TS may be driven by signals provided on selected

18 tile interconnect lines M0-M23 (from programmable routing

19 matrix 201). In addition, for a low skew control, clock line

20 CLK is driven directly by signals on global horizontal lines

21 GH0 and GH1 or from global vertical lines GV0 and GV1.

22

23 <u>No Contention</u>

24   In accordance with the present invention, if one PIP on a

25 predetermined CLB input line is programmed on, then no other

26 PIP on that CLB input line should be turned on. For example,

27 if the PIP at the intersection of input line QW0 and CLB input

28 line F0 is programmed on (i.e. a signal on input line QW0

29 drives CLB input line F0), then the PIPs on tile interconnect

30 lines M6, M7, M8, M9, M14, M15, and input line QN0 remain

31 turned off, thereby ensuring no contention on CLB input line

32 F0. Typically, contention is avoided either by using a

33 convenient decode method for selecting which PIP on a single

34 input line is turned on or by using rules provided in the

35 software which programs the memory cells to avoid turning on

36 more than one PIP on an input line. In other embodiments,

37 alternative input selection means are possible. For example,

1   in one embodiment one memory cell is loaded to specify whether
2   each PIP is turned on or not.
3
4   Programmable Routing Matrix 201
5   Fig. 6 illustrates the programmable routing matrix 201 of
6   Fig. 2a. Note that whereas all PIPs in CLB matrix 202 are
7   shown as triangles to indicate signal flow onto one line, in
8   Fig. 6, most PIPs in programmable routing matrix 201 are shown
9   as open circles to indicate signal flow on both lines. The
10 exceptions are PIPs which connect lines TQ4 through TQ7
11 (output lines from tristate buffer block 302 of Fig. 3A) to
12 long horizontal lines LH0-LH7 and long vertical lines LV0-LV7,
13 and PIPs which place signals from global signal lines GH0,
14 GH1, GV0, and GV1 onto tile interconnect lines M0 through M3.
15   Extending into programmable routing matrix 201 are global
16 lines, long lines, double length lines, and single length
17 lines. Each of these lines is connectable to selected tile
18 interconnect lines M0-M23. Programmable routing matrix 201
19 provides connection to programmable routing matrices in
20 adjacent tiles through single length lines extending in the
21 four compass directions, i.e. single length north lines N1-
22 N11, single length east lines E1-E11, single length south
23 lines S1-S11, and single length west lines W1-W11. Connection
24 to programmable routing matrices one tile away are provided by
25 double length north lines DN0 and DN6, double length east
26 lines DE0 and DE6, double length south lines DS0 and DS6, and
27 double length west lines DW0 and DW6 (see Fig. 2A). Each long
28 vertical line LV0-LV7 and long horizontal line LH0-LH7 which
29 extends through the tile is connectable to one of tile
30 interconnect lines M0-M23.
31   The particular pattern of PIPs illustrated in Fig. 6 is
32 sparse, yet provides significant signal transferability.
33 Specifically, programmable routing matrix 201, which in this
34 embodiment includes only 124 PIPs, is sparse relative to the
35 approximately 4200 PIPs which could be provided to connect
36 every line in Fig. 6 to every other line. However, the PIP
37 pattern ensures that any line is connectable to any other line

1 if enough intermediate PIPs are used. For example, as shown
2 in Fig. 6, west line W1 is connectable to east line E1 by
3 turning on two PIPs which connect tile interconnect line M1 to
4 these two lines. In contrast, to make a connection between
5 west line W1 and east line E2 requires 8 PIPs and 9 lines,
6 i.e. connecting west line W1 to tile interconnect line M1 to
7 east line E1 to tile interconnect line M20 to west line W9 to
8 tile interconnect line M9 to north line N9 to tile
9 interconnect line M21, and finally to east line E2. Although
10 a path of this length is typically undesirable, in some
11 applications delay is unimportant. In those applications, the
12 availability of such a path allows completion of a design.
13 Easy paths requiring only two PIPs are available to connect
14 lines N1, S1, E1, and W1 to tile interconnect line M1; lines
15 N2, S2, E2, and W2 to tile interconnect line M2 and so forth
16 through tile interconnect line M5. Tile interconnect line M6
17 connects to double length lines DN6, DS6, DE6, and DW. Tile
18 interconnect lines M7 through M11 connect to correspondingly
19 numbered single length lines extending north, south, east and
20 west.
21   PIPs on tile interconnect lines M12-M23 implement a
22 pattern of cross connecting that facilitates signal transfer
23 flexibility with minimal sacrifice of speed, and the sparse
24 pipulation achieves valuable reduction of chip area. For
25 example, tile interconnect line M12 connects to double length
26 north line DN0, to south line S3, to east line E5, and to west
27 line W1, whereas tile interconnect line M15 connects to north
28 line N3, east line E8, double south line DS6, and west line
29 W4. In this manner, the present invention provides a
30 predetermined pattern to minimize the number of PIPs, thereby
31 allowing any line to be connected to any other line. Thus,
32 the present invention ensures that a path is always provided,
33 while minimizing silicon area.
34
35 Routing Matrix Model
36   Each of tile interconnect lines M0-M23 is connectable to
37 five or six other lines. Thus, as shown in Fig. 7A, each tile

1 interconnect line M0-M23 is represented as a star with five or
2 six points. In this model, eight tile interconnect lines M0
3 through M7 are programmably connectable to selected ones of
4 north lines N0-N3, east lines E0-E3, south lines S0-S3 and
5 west lines W0-W3. Tile interconnect lines M0 through M3 are
6 connectable to north, south, east and west lines of the same
7 numerical suffix. Tile interconnect lines M4 through M7 are
8 connectable to staggered ones of the north, south, east and
9 west lines. Thus, tile interconnect lines M0-M3 provide a
10 means for interconnecting north, east, south and west lines of
11 the same suffix, while tile interconnect lines M4-M7 provide
12 an opportunity for cross-connecting lines from four compass
13 directions. Also, tile interconnect lines M0-M7 provide means
14 for connecting programmable routing matrix 201 to configurable
15 logic block matrix structure 202 (Fig. 3A).
16
17 Connectivity Model for Routing Matrix and Logic Blocks
18   Fig. 7B illustrates the "star structure" of the present
19 invention. In a star structure, each CLB 301 is associated
20 with a particular star 201 (i.e the programmable routing
21 matrix 201) from which radiate lines connecting to other stars
22 201 and from there to other CLBs 301. In Fig. 7B, double
23 length and single length lines are illustrated. In other
24 embodiments, lines of other lengths are provided in the star
25 structure. Thus, the star structure of the present invention
26 ensures good connectivity between its related CLBs and other
27 parts of the device.
28
29 Global Interconnect Structure
30   Fig. 8 illustrates hard connections from global signal
31 pads P113, P114, P115, and P116, which are positioned near the
32 corners of chip 100 (Fig. 1), to global signal lines GTL, GTR,
33 GBR, and GBL, respectively, which are typically located near
34 the four edges of chip 100. Each global signal line is
35 programmably connectable to a plurality of lines extending
36 vertically or horizontally through each row or column of core
37 tiles 101. For example, top left global signal line GTL is

1 connectable to global vertical lines GV1-a through GV1-n, via

2 PIPs PV1-a through PV1-n, respectively, i.e. one PIP for each

3 column of core tiles 101. Top right global signal line GTR is

4 connectable via PIPs PH0-a through PH0-m, respectively, i.e.

5 one PIP for each row of core tiles 101 to global horizontal

6 lines GH0-a. Bottom right global signal line GBR is

7 connectable to global vertical lines GV0-a through GV0-n.

8 Finally, bottom left global signal line GBL is connectable to

9 global horizontal lines GH1-a through GH1-m. Note that the

10 global vertical and horizontal lines with reference labels

11 beginning with GV or GH are connectable to programmable

12 routing matrices 201 and CLB matrices 202 in core tiles 101

13 through which the global lines pass, as discussed above in

14 connection with Figs. 2A, 3, and 7.

15   As also shown in Fig. 8, long lines LV0L, LV7L, LH0T,

16 LH7T, LV0R, LV7R, LH0B, and LH7B which extend through the edge

17 tiles (not shown in Fig. 8 for simplicity but shown in Figs.

18 10A through 10D) of chip 100 (Fig. 1) are also connectable to

19 the global lines. Specifically, bottom right global signal

20 line GBR can be driven by signals on bottom horizontal long

21 lines LH0B and LH7B via PIPs PGBR0 and PGBR7, respectively.

22 Bottom left global signal line GBL can be driven by signals on

23 left vertical long lines LV0L and LV7L via bottom left buffer

24 BBL via PIPs PGBL0 and PGBL7, respectively. Equivalent

25 connections are provided for the top and right edges of the

26 chip. Left, top, right, and bottom long lines are connectable

27 to each other through PIPs, such as PIP PBR7. Because long

28 lines LV0L, LV7L, etc. are driven by signals provided by any

29 of the pads at the perimeter of the chip (through edge tiles

30 103-106 discussed below in connection with Figs. 10A-10D), any

31 pad can provide a global signal. Moreover, any of core tiles

32 101 can also provide a global signal through edge tiles 103-

33 106.

34

35 Optional Long Line Splitter

36   Figs. 1 and 9 illustrate one embodiment of the present

37 invention which includes long line splitters LLS which may be

1 positioned partly through a line. Two columns of tiles are

2 illustrated in Fig. 9, each column comprising a top edge tile

3 104, six core tiles 101, and a bottom edge tile 106. Long

4 vertical lines LV0-LV7 traverse all core tiles 101, and in

5 each of the two columns terminate in edge tiles 104 and 106.

6 Long vertical lines LV0-LV7 are also connectable to selected

7 ones of tile interconnect lines M0-M15 and lines TQ0-TQ3 in

8 edge tiles 104 and 106, as will be discussed below in

9 connection with Figs. 10A-10D. Furthermore, as discussed

10 above in connection with Figs. 2A and 6, long lines LV0-LV7

11 are connectable to selected lines in programmable routing

12 matrices 201. For clarity, horizontal long lines LH0-LH7 are

13 not illustrated in Fig. 9, but are illustrated in Figs. 2A and

14 6.

15   In the embodiment shown in Fig. 9, vertical long lines

16 LV0-LV7 in the three upper core tiles 101 are separated from

17 the portions in the three lower core tiles 101 by long line

18 splitters LLS. An inset illustrates that a long splitter LLS

19 in one embodiment comprises an n-type transistor which is

20 turned off by providing a low voltage to a control gate CG,

21 thereby separating the vertical long line into top and bottom

22 segments. Long line splitters LLS are typically used in large

23 chip embodiments to allow top and bottom long lines to be

24 separately driven in different portions of the chip. As shown

25 in Fig. 1, horizontal long lines LH0-LH7 are also separated in

26 the middle of chip 100 by long line splitters LLS. In other

27 embodiments, several long line splitters such as long line

28 splitters LLS and LLSA are provided along the same long line,

29 or long line splitters LLSB are provided between an end of a

30 long lines in one edge tile and an end of a long line in an

31 adjacent edge tile, thereby programmably connecting these long

32 lines.

33

34 Edge Tiles for Embodiment of Fig. 2A

35   Figs. 10A-10D illustrate in greater detail the edge tiles

36 shown in Fig. 2A. Specifically, Figs. 10A-10D show left edge

37 tile 103, top edge tile 104, right edge tile 105, and bottom

1 edge tile 106, respectively. Each edge tile in these

2 embodiments is typically but not always connected to at least

3 one of pads PV, PZ, PY or PX. In other embodiments described

4 in detail below in reference to Fig. 1, at least one edge tile

5 is not connected to any pad.

6   In Fig. 10A, four pads, PV, PZ, PY, and PX are connected

7 to edge tile 103 via input/output (I/O) devices IOBV, IOBZ,

8 IOBY and IOBX, respectively. Each of I/O devices IOBV, IOBZ,

9 IOBY and IOBX is connected to edge tile 103 by three lines.

10 For example, I/O device IOBV is connected to edge tile 106 by

11 an I/O input line IV, an I/O output line OV, and a tri-state

12 line TSV. Note that the output signal provided to pad P42 by

13 output line OV is controlled by a signal on I/O tri-state line

14 TSV. Similar lines are provided for I/O devices IOBZ, IOBY

15 and IOBX.

16   A fully pipulated I/O input interconnect structure 1001

17 allows signals on I/O input lines IV, IZ, IY, and IX to drive

18 edge tile input lines QIN0-QIN3. Neighbor output interconnect

19 structure 1004 allows signals on output lines QE0-QE3 from a

20 core tile 101 to be provided to pads PV, PZ, PY and PX. I/O

21 output interconnect structure 1002 allows signals from the

22 neighboring core tiles (in edge tile 103, provided by north

23 lines 100-N7, south lines S0-S7, and east lines E1-E5 and E7-

24 E11) as well as signals on long lines LH0-LH7 and LV0-LV7 and

25 double length lines DHO, DH6, to be provided to the pads.

26 Note that I/O output interconnect structure 1002 has a

27 substantially complete pipulation, thereby allowing any signal

28 coming into left edge tile 103 from elsewhere in the chip

29 interior to be placed on any of pads PV, PX, PY or PZ in spite

30 of a sparse general interconnect structure 1006 between lines

31 coming from other parts of the chip interior into or out of

32 left edge tile 103 and a set of edge tile interconnect lines

33 M0-M15.

34   Intermediate interconnect structure 1003 allows signals

35 which come from one of tile interconnect lines M0-M15 to be

36 placed on one of edge tile input lines QIN0-QIN3, buffered

37 onto a corresponding output line Q0 through Q3, and provided

29

1 through tristate buffer block 302 to a corresponding line TQ0-
2 TQ3. A signal can thence be provided to horizontal long lines
3 LH0-LH7 and vertical long lines LV0-LV7. Thus, signals on
4 edge tile input lines QIN0-QIN3 drive output lines Q0-Q3
5 directly and drive lines TQ0-TQ3 through tri-state buffer
6 block 302.

7   Feedback interconnect structure 1005 allows signals on
8 output lines Q0-Q3 to drive tile interconnect lines M0-M15
9 which are in turn selectively connected to north lines N0-N7,
10 south lines S0-S7, east lines E1-E11, ·double length lines DE0,
11 DE6, DH0, and DH6 and to long lines LV0-LV7. In this manner
12 edge tile 103 allows connection to pads which in turn have
13 external connections to chip 100, as well as on an adjacent
14 core tile 101 chip and to adjacent edge tiles (or an adjacent
15 corner tile, explained in detail below). Pads PV, PZ, PY, and
16 PX represent pads P42, 41, 40 and P39, respectively, which are
17 shown in Fig. 1.

18   Figs. 10B, 10C, and 10D show embodiments of edge tiles
19 104, 105, and 106, respectively. Because these tiles are
20 similar in structure, except for orientation, and have
21 identical numerical references to that shown in Fig. 10A, the
22 detail of the interface structures in Figs. 10B, 10C, and 10D
23 will not be discussed herein.

24

25 <u>I/O Interface for Use With Optional Pad</u>
26   Fig. 10C illustrates a combination of connected and
27 unconnected pads, thereby illustrating the flexibility
28 available at the mask level.

29   In this embodiment, one unconnected pad PZ and connected
30 pads PV, PY, PX implement a configuration which is represented
31 in Fig. 1 by pads P6, P7 and P8 (connected to edge tile 105).
32 As shown in Fig. 1, each edge tile has a predetermined number
33 of pads connected to it. For example, pad P17 is the only pad
34 connected to its edge tile 106. Therefore, as shown in Fig.
35 10D, only one of pads PV, PZ, PY and PX (in this embodiment,
36 pad PV) is connected to edge tile 106.

1   Referring back to Fig. 10C, pad PZ and its input/output
2 buffer structure IOBZ are eliminated, thereby reducing total
3 chip size by reducing the total number of pads on the chip.
4 Input line IZ and output line OZ are shorted together in a
5 region which in one embodiment is outside tile 105. In this
6 manner, all tiles 105 are identically laid out, regardless of
7 how many pads PV, PZ, PY, or PX are provided. Referring back
8 to Fig. 1, pads P6, P7 and P8 are connected to a single edge
9 tile 105. In Fig. 10D, pad PY and related structures IOBY and
10 ESDY are not provided. Thus, the embodiment of Fig. 10D
11 represents pads P26 through P28 of Fig. 1. In other
12 embodiments of the present invention, other pads are removed,
13 up to and including removal of all four pads. For example,
14 Fig. 1 includes certain edge tiles to which no pads have been
15 connected (two of edge tiles 103, one of edge tiles 104, and
16 one of edge tiles 105 have no pads at all connected to them).
17
18 Corner Tiles
19   Figs. 11A through 11D illustrate the four corner tiles
20 113, 114, 115, and 116, respectively, of chip 100 (Fig. 1).
21 Fig. 11A includes a conventional boundary scan block BSCAN
22 compatible with IEEE 1149.1 described in detail in a Xilinx
23 Application Note by Luis Morales entitled, "Boundary Scan in
24 XC4000 Devices" and available from Xilinx, Inc., 2100 Logic
25 Drive, San Jose, CA 95124, which is herein incorporated by
26 reference in its entirety. In Fig. 11A, top left corner tile
27 113 includes hard connections from single length east lines
28 E0-E7 to single length south lines S0-S7, respectively, and
29 programmable connections from long horizontal lines LH0-LH7 to
30 long vertical lines LV0-LV7, respectively. Fig. 11A further
31 shows one embodiment of an interconnect structure 1101 which
32 provides the programmable connection of boundary scan block
33 BSCAN to the above-described single length and long lines.
34 Corner tile 113 also includes a programmable connection to an
35 external pin P43 that provides a global clock signal SGCK1.
36   Corner tile 114, illustrated in Fig. 11B, is similar in
37 configuration to corner tile 113 (Fig. 11A). Specifically,

1   tile 114 (Fig. 11B) includes hard connections for connecting

2   single length west lines W0-W7 to single length south lines

3   S0-S7, respectively, and programmable connections for

4   connecting long horizontal lines LH0-LH7 to long vertical

5   lines LV0-LV7, respectively. In both Figs. 11A and 11B, long

6   vertical line LV0 connects to long horizontal line LH0, but

7   because of the layout of tiles 113 and 114, the lines are

8   drawn in a different position on the page, and therefore

9   corner tiles 113 and 114 have a different appearance in Figs.

10   11A and 11B. Corner tile 114 includes a clock input pin P1

11   that provides clock signal SGCK4. Corner tile 114 includes an

12   interconnect structure 1102 which provides a programmable

13   connection between a conventional oscillator/counter circuit

14   DIV used for counting bits during configuration of chip 100

15   and the above-described single length and long lines. In one

16   embodiment, circuit DIV is used during chip operation to

17   provide an on-chip oscillator or a counter-divider. Circuit

18   DIV is typically configured to divide an internal oscillator

19   signal or a user-provided signal. Corner tile 114 further

20   includes a boundary scan update signal BSUPD, which is part of

21   the standard boundary scan circuitry (most of the circuitry

22   being located in tile 113). In this embodiment, signal BSUPD

23   is programmably placed on west lines W2 and W3 (and thus south

24   lines S2 and S3) as well as long horizontal lines LH2 and LH3

25   (and thus long vertical lines LV2 and LV3).

26   Fig. 12 illustrates one embodiment of a circuit which

27   implements oscillator/counter circuit DIV of Fig. 11B. Two

28   output taps, OSC1 and OSC2 are provided, which together can be

29   configured to provide twelve frequencies which are divisions

30   of the original input frequency. An internal oscillator OSC

31   provides an oscillator signal to NAND gate 1231. NAND gate

32   1231 is enabled by a memory cell OSCRUN. When enabled, the

33   output signal from oscillator OSC is provided to multiplexer

34   1201.

35   Memory cell 1202 determines whether multiplexer 1201

36   provides the output signal from internal oscillator OSC or a

37   signal on one of single length west lines W0-W3 (equal to a

1 signal on single length south lines S0-S3, respectively, see
2 Fig. 11B), or a signal on one of long horizontal lines LH0-LH3
3 (equal to a signal on long vertical lines LV0-LV3).
4 Multiplexer 1201 provides an output signal which is then
5 available to be divided by flip flops 1214 through 1220.
6   Multiplexers 1225 and 1226 provide a choice of divide
7 factors on the data input terminals of flip flops 1227 and
8 1228 respectively. The outputs of these flip flops are
9 provided as signals on taps OSC1 and OSC2. Flip flops 1227
10 and 1228 are clocked from the original input signal and serve
11 to reduce the skew of the output signals from multiplexers
12 1225 and 1226. Multiplexer 1225, under control of memory
13 cells OSC1A and OSC1B, provides a switching signal which can
14 be the input signal from multiplexer 1201 divided by 4, 16,
15 64, or 256. Depending upon the setting in memory cell 1203,
16 multiplexer 1204 can forward the original clock signal output
17 from multiplexer 1201 or can provide a divided signal (the
18 original frequency divided by 512) which is output from flip
19 flop 1213. If multiplexer 1204 is set to provide the output
20 signal of multiplexer 1201, then the original clock signal is
21 alternatively provided by multiplexer 1226 as divided by 2, 8,
22 32, or 128. If multiplexer 1204 is set to provide a divided
23 signal from flip flop 1213, multiplexer 1226 will provide an
24 output signal which has the frequency of the original input
25 signal on multiplexer 1201 divided by 1024, 4096, 16,384, or
26 65,536. Thus, the signals on output taps OSC1 and OSC2 are
27 programmed to oscillate at many different choices of
28 frequency.
29   Fig. 11C shows lower right corner tile 115. Corner tile
30 115 programmably connects long horizontal lines LH0-LH7 and
31 long vertical lines LV0-LV7, respectively, and connects north
32 lines N0-N7 to west lines W0-W7. Corner tile 115 further
33 includes a programmable interconnect structure 1103 which
34 programmably connects a start-up block STARTUP to north lines
35 N0-N7 (and thus west lines W0-W7) and long vertical lines LV0-
36 LV7 (and thus long horizontal lines LH0-LH7). Start-up block
37 STARTUP includes circuitry to sequence the signals and control

1   timing of the start-up function as chip 100 (Fig. 1) is
2   activated.
3   During the start-up function, three events are necessary
4   to move from configuration mode to operating mode: release of
5   the signal on a global tri-state signal terminal GTS, release
6   of the signal on a global reset signal terminal GSR, and
7   release of a signal on a load complete terminal DONE
8   (indicating that all configuration bits have been loaded into
9   their appropriate locations in the FPGA). The start-up block
10 STARTUP allows the user to program the order in which these
11 signals are released, as well as the timing of these signals
12 (for example separating each signal from another signal by
13 one, two, or three clock cycles).
14   Fig. 11D shows lower left tile 116 with single length and
15 long lines connected similarly to the other three corner
16 tiles. In addition, lower left corner tile 116 includes a
17 read-back unit RDBK. Read-back unit RDBK allows the user to
18 read the content of the configuration memory onto any data
19 line and out onto any external pin through the data line
20 terminal DATA of readback unit RDBK. The trigger terminal
21 TRIG in read-back unit RDBK carries a signal that triggers
22 copying of one row of configuration data from the
23 configuration memory into the same shift register which loaded
24 the configuration memory. The signal on a clock terminal CLK
25 controls shifting out of that data onto line DATA. The signal
26 on a read-in-progress terminal RIP prevents the chip from
27 sending another signal from trigger terminal TRIG while data
28 are still being shifted out. With this circuit, depending on
29 the original configuration paths to corner tile 116, the
30 configuration data for the entire chip is shifted out of the
31 chip onto almost any one of the external pins while the chip
32 is operating.
33   In light of the above description, many other embodiments
34 of the present invention will be apparent to those skilled in
35 the art. For example, although the above description relates
36 to an embodiment in which core tiles are rectangular or

1   square, another embodiment of the present invention includes
2   tiles having six sides.
3   As mentioned above, core tiles need not be identical. A
4   set of tile designs may be provided which have different logic
5   content from each other. If all tile designs follow common
6   boundary constraints, chips can be formed by combining the
7   tile designs in a variety of patterns. To be successful, each
8   tile design must have a good distribution of signals within
9   the tile. The routing matrix of the tile must efficiently
10 distribute the incoming signals to the logic block input
11 terminals and take the logic block output signals to the tile
12 edges. Indeed a chip may be composed in which some tiles
13 include RAM memory and no logic, or a combination of tiles
14 having logic, tiles having memory only, and tiles having
15 routing with no logic or memory. Further, a tile may be
16 designed which includes an input/output pad physically within
17 its structure, and tile designs including a pad may be
18 combined with other tile designs to achieve distributed access
19 to logic. Such other embodiments are intended to fall within
20 the scope of the present invention. The present invention is
21 set forth in the claims.

1   CLAIMS

2   1. An FPGA tile architecture having a plurality of core

3   tiles, each core tile comprising:

4   a configurable logic block matrix;

5   a programmable routing matrix;

6   connection means for connecting said configurable logic

7   block to other configurable logic block matrices in

8   adajacent core tiles;

9   inter-matrix lines for connecting said configurable logic

10   block to said programmable routing matrix; and

11   routing lines for connecting said programmable routing

12   matrix to programmable routing matrices in adjacent

13   core tiles.

14

15   2. The FPGA tile architecture of Claim 1 wherein said

16 core tiles are identical.

17

18   3. The FPGA tile architecture of Claim 1 wherein one

19 core tile is different from another core tile.

20

21   4. The FPGA tile architecture of Claim 1 in which said

22 adjacent core tiles are positioned north, south, east, and

23 west of said core tile.

24

25   5. The FPGA tile architecture of Claim 1 further

26 including a plurality of long lines extending horizontally

27 through said core tile, wherein at least one of said plurality

28 of long lines is coupled to at least one of said inter-matrix

29 lines.

30

31   6. The FPGA tile architecture of Claim 5 further

32 including a plurality of long lines extending vertically

33 through said core tile, wherein at least one of said plurality

34 of long lines is coupled to at least one of said inter-matrix

35 lines.

36

1   7.   The FPGA tile architecture of Claim 6 further
2   including a global horizontal line coupled to said
3   configurable logic block matrix and said programmable routing
4   matrix.
5
6   8.   The FPGA tile architecture of Claim 7 further
7   including a global vertical line coupled to said configurable
8   logic block matrix and said programmable routing matrix.
9
10   9.   The FPGA tile architecture of Claim 8 further
11   including a multiple length line, wherein said multiple length
12   line couples programmable routing matrices that are not in
13   adjacent core tiles.
14
15   10. The FPGA tile architecture of Claim 9 wherein said
16   multiple length line is a double length line.
17
18   11. The FPGA tile architecture of Claim 1 wherein said
19   connection means includes a carry-out line and a carry-in
20   line, wherein said carry-out line is coupled to a carry-in
21   line in an adjacent core tile.
22
23   12. The FPGA tile architecture of Claim 11 wherein said
24   carry-in line is coupled to a carry-out line in an adjacent
25   core tile.
26
27   13. The FPGA tile architecture of Claim 9 wherein said
28   connection means includes:
29   a plurality of input lines to said configurable logic
30   block matrix;
31   a plurality of output lines from said configurable logic
32   block matrix, wherein at least one of said plurality
33   of input lines is coupled to one of said plurality
34   of output lines in an adjacent core tile, and at
35   least one of said plurality of output lines is
36   coupled to one of said plurality of input lines in
37   an adjacent core tile.

1
2   14. The FPGA tile architecture of Claim 13 wherein said
3   configurable logic block matrix comprises:
4   a plurality of logic block input lines programmably
5   connected to said plurality of input lines through
6   an input interconnect structure; and
7   a plurality of logic block output lines programmably
8   connected to said plurality of output lines through
9   an output interconnect structure.
10
11   15. The FPGA tile architecture of Claim 14 wherein said
12 configurable logic block matrix further includes a
13 configurable logic block coupled between said plurality of
14 logic block input lines and said plurality of logic block
15 output lines.
16
17   16. The FPGA tile architecture of Claim 15 wherein said
18 output interconnect structure is more fully pipulated than
19 said input interconnect structure.
20
21   17. The FPGA tile architecture of Claim 16 wherein said
22 input interconnect structure is sparsely pipulated.
23
24   18. The FPGA tile architecture of Claim 17 wherein said
25 output interconnect structure is fully pipulated.
26
27   19. The FPGA tile architecture of Claim 15 wherein said
28 configurable logic block matrix further includes a feedback
29 interconnect structure for programmably connecting said output
30 lines to said logic block input lines.
31
32   20. The FPGA tile architecture of Claim 19 wherein said
33 configurable logic block matrix further includes a general
34 interconnect structure for programmably connecting said inter-
35 matrix lines to said logic block input lines.
36

1   21. The FPGA tile architecture of Claim 20 wherein at
2   least one of said inter-matrix lines includes a buffer.
3
4   22. The FPGA tile architecture of Claim 20 wherein said
5   configurable logic block includes a plurality of function
6   generators, each function generator coupled to a subset of
7   said logic block input lines.
8
9   23. The FPGA tile architecture of Claim 22 wherein said
10 configurable logic block further includes a plurality of
11 multiplexers, wherein at least one of said plurality of
12 function generators provides a signal to at least one of said
13 plurality of multiplexers.
14
15   24. The FPGA tile architecture of Claim 23 wherein said
16 configurable logic block further includes a plurality of
17 register means, and wherein at least one of said plurality of
18 multiplexers provides a signal to at least one of said
19 plurality of registers.
20
21   25. The FPGA tile architecture of Claim 24 wherein at
22 least one function generator is coupled to one logic block
23 output line.
24
25   26. The FPGA tile architecture of Claim 25 wherein at
26 least one multiplexer is coupled to one logic block output
27 line.
28
29   27. The FPGA tile architecture of Claim 26 wherein at
30 least one register is coupled to one logic block output line.
31
32   28. The FPGA tile architecture of Claim 27 wherein at
33 least one multiplexer is coupled to said carry-out line.
34
35   29. The FPGA tile architecture of Claim 28 wherein at
36 least one multiplexer is coupled to said carry-in line.
37

39

1   30.   The FPGA tile architecture of Claim 22 wherein said
2 configurable logic block further includes groups of
3 multiplexers, each group of multiplexers coupled to one of
4 said plurality of function generators.
5
6   31.   The FPGA tile architecture of Claim 30 wherein said
7 configurable logic block further includes a plurality of
8 register means, and wherein each group of multiplexers
9 provides a signal to one of said plurality of register means.
10
11   32.   The FPGA tile architecture of Claim 31 wherein each
12 function generator is coupled to one logic block output line.
13
14   33.   The FPGA tile architecture of Claim 32 wherein at
15 least one multiplexer of each group of multiplexers is coupled
16 to one logic block output line.
17
18   34.   The FPGA tile architecture of Claim 33 wherein each
19 register is coupled to one logic block output line.
20
21   35.   The FPGA tile architecture of Claim 34 wherein at
22 least one multiplexer is coupled to a carry-out line of said
23 configurable logic block.
24
25   36.   The FPGA tile architecture of Claim 35 wherein at
26 least one multiplexer is coupled to a carry-in line of said
27 configurable logic block.
28
29   37.   The FPGA tile architecture of Claim 20 wherein said
30 output interconnect structure includes a first plurality of
31 transistors, each transistor provided on one logic block
32 output line.
33
34   38.   The FPGA tile architecture of Claim 35 wherein said
35 output interconnect structure includes a first plurality of
36 memory devices, each memory device controlling the state of a
37 subset of said plurality of transistors.

1   39.   The FPGA tile architecture of Claim 38 wherein said
2   output interconnect structure includes a second plurality of
3   transistors, each of said second plurality of transistors
4   coupled between a subset of said plurality of logic block
5   output lines and one output line.
6
7   40.   The FPGA tile architecture of Claim 39 wherein said
8   output interconnect structure further includes a second
9   plurality of memory devices that control the state of said
10 second plurality of transistors.
11
12   41.   The FPGA tile architecture of Claim 20 wherein said
13 input interconnect structure and said general interconnect
14 structure include a first plurality of transistors, said first
15 plurality of transistors provided on a subset of said
16 plurality of inter-matrix lines and on a subset of said
17 plurality of input lines.
18
19   42.   The FPGA tile architecture of Claim 41 wherein said
20 input interconnect structure and said general interconnect
21 structure include at least one memory device that controls the
22 state of said first plurality of transistors.
23
24   43.   The FPGA tile architecture of Claim 41 wherein said
25 input interconnect structure and said general interconnect
26 structure include a second plurality of transistors, each of
27 said second plurality of transistors coupled between either a
28 further subset of said plurality of inter-matrix lines or a
29 further subset of said plurality of input lines and one logic
30 block input line.
31
32   44.   The FPGA tile architecture of Claim 43 wherein said
33 input interconnect structure and said general interconnect
34 structure further includes a second plurality of memory
35 devices that control the state of said second plurality of
36 transistors.
37

45. The FPGA tile architecture of Claim 20 wherein said programmable routing matrix includes a programmable interconnect structure for coupling said routing lines to said inter-matrix lines.

46. The FPGA tile architecture of Claim 45 wherein said programmable interconnect structure further couples said plurality of long lines extending horizontally through said core tile to said inter-matrix lines.

47. The FPGA tile architecture of Claim 46 wherein said programmable interconnect structure further couples said plurality of long lines extending vertically through said core tile to said inter-matrix lines.

48. The FPGA tile architecture of Claim 47 wherein said programmable interconnect structure further couples said multiple length line to said inter-matrix lines.

49. The FPGA tile architecture of Claim 48 wherein said programmable interconnect structure further couples said global horizontal line to an inter-matrix line.

50. The FPGA tile architecture of Claim 49 wherein said programmable interconnect structure further couples said global vertical line to an inter-matrix line.

51. The FPGA tile architecture of Claim 6 wherein at least one of said long lines, either extending horizontally or vertically across said core tile, includes a long line splitter, wherein said long line splitter includes means for preventing conduction of said at least one long line.

52. The FPGA tile architecture of Claim 51 wherein said means for preventing conduction includes a transistor.

1   53.   The FPGA tile architecture of Claim 52 wherein said
2 transistor is an n-type transistor.
3
4   54.   The FPGA tile architecture of Claim 20 further
5 including a plurality of edge tiles, wherein each edge tile is
6 coupled to at least one other edge tile and one core tile.
7
8   55.   The FPGA tile architecture of Claim 54 wherein each
9 edge tile is further coupled to an input/output (I/O) device.
10
11   56.   The FPGA tile architecture of Claim 55 wherein said
12 I/O device is coupled to a pad which provides an external
13 connection to said chip.
14
15   57.   The FPGA tile architecture of Claim 56 wherein an
16 electrostatic discharge device connects to said pad.
17
18   58.   The FPGA tile architecture of Claim 56 wherein said
19 edge tile includes means for coupling said I/O device to said
20 routing lines, said input lines, said output lines, and said
21 multiple length line.
22
23   59.   The FPGA tile architecture of Claim 58 wherein said
24 means for coupling couples either said global horizontal line
25 or said global vertical line to said I/O device.
26
27   60.   The FPGA tile architecture of Claim 56 wherein said
28 means for coupling includes a first interconnect structure.
29
30   61.   The FPGA tile architecture of Claim 54 further
31 including a plurality of corner tiles, wherein each corner
32 tile is connected to two adjacent edge tiles.
33
34   62.   The FPGA tile architecture of Claim 61 wherein said
35 corner tile connects said plurality of long lines extending
36 horizontally across said core tile to said plurality of long
37 lines extending vertically across said core tile.

1   63. The FPGA tile architecture of Claim 61 wherein said
2   corner tiles further connect a first subset of said plurality
3   of routing lines to a second subset of said plurality of
4   routing lines.
5
6   64. The FPGA tile architecture of Claim 61 wherein said
7   corner tile includes a corner tile interconnect structure for
8   programmably connecting said plurality of long lines extending
9   horizontally across said core tile and said first subset of
10   said plurality of routing lines to a selected circuit.
11
12   65. The FPGA tile architecture of Claim 64 wherein said
13   selected circuit is a boundary scan block.
14
15   66. The FPGA tile architecture of Claim 64 wherein said
16   selected circuit is an oscillator/counter circuit.
17
18   67. The FPGA tile architecture of Claim 64 wherein said
19   selected circuit is a start-up block.
20
21   68. The FPGA tile architecture of Claim 64 wherein said
22   selected circuit is a read-back unit.
23
24   69. The FPGA tile architecture of Claim 61 wherein said
25   edge tiles further includes means for programmably connecting
26   an external pin to at least one of said long lines extending
27   horizontally across said core tile.
28
29   70. An FPGA tile architecture comprising:
30   a plurality of paired structures, each paired structure
31   including a configurable logic block matrix and a
32   programmable routing matrix;
33   a plurality of lines for connecting said configurable
34   logic block matrix to said programmable routing
35   matrix; and

1   means for connecting said programmable routing matrix to
2   other programmable routing matrices in other paired
3   structures.
4
5   71. The FPGA tile architecture of Claim 70 further
6   comprising means for connecting said configurable logic block
7   matrix in one paired structure to a plurality of configurable
8   logic block matrices in other paired structures without using
9   said programmable routing matrix.
10
11   72. The FPGA tile architecture of Claim 70 wherein said
12 means for connecting comprises:
13   a plurality of single length lines which connect a first
14   programmable routing matrix to adjacent programmable
15   routing matrices;
16   a plurality of double length lines which connect said
17   first programmable routing matrix to non-adjacent
18   programmable routing matrices.
19
20   73. The FPGA tile architecture of Claim 70 further
21 comprising:
22   a plurality of long lines, each long line being
23   programmably connectable to a plurality of adjacent
24   programmable routing matrices.
25
26   74. An interconnect structure comprising:
27   a plurality of signal lines;
28   a first plurality of transistors, each transistor
29   provided on one signal line;
30   at least one memory device for controlling the state of
31   said plurality of transistors;
32   a second plurality of transistors, each transistor
33   coupled to a subset of said first plurality of
34   transistors; and
35   means for controlling the states of said second plurality
36   of transistors, wherein said means for controlling

1   determines which of said second plurality of transistors
2   provides a signal on an output line.
3
4   75.   The interconnect structure of Claim 74 further
5   comprising a third plurality of transistors coupled in series
6   to one subset of said first plurality transistors.
7
8   76.   The interconnect structure of Claim 75 wherein said
9   at least one memory device includes a plurality of memory
10   devices, and wherein each memory device controls the state of
11   one of said third plurality of transistors.
12
13   77.   The interconnect structure of Claim 76 wherein said
14   plurality of memory devices provide a signal to said first
15   plurality of transistors and the complement of said signal to
16   said third plurality of transistors.
17
18   78.   An interconnect structure comprising:
19   a plurality of lines;
20   a first plurality of transistors, each transistor
21   provided on one signal line;
22   a first memory device for controlling the state of said
23   first plurality of transistors, wherein said means
24   for controlling provides a signal to a first group
25   of said first plurality of transistors and provides
26   the complement of said signal to a second group of
27   said first plurality of transistors;
28   a second plurality of transistors, each transistor
29   coupled to a subset of said first plurality of
30   transistors;
31   a second memory device for controlling the state of said
32   second plurality of transistors, wherein said means
33   for controlling provides a signal to a first group
34   of said second plurality of transistors and provides
35   the complement of said signal to a second group of
36   said second plurality of transistors;

1   a third plurality transistors, each transistor coupled to
2   a subset of said second plurality of transistors;
3   a third memory device for controlling the state of said
4   third plurality of transistors, wherein said means
5   for controlling provides a signal to a first group
6   of said third plurality of transistors and provides
7   the complement of said signal to a second group of
8   said third plurality of transistors, wherein one of
9   said third plurality of transistors provides a
10   signal on an output line.
11
12   79. A tile based FPGA architecture including:
13   a plurality of core tiles formed in rows and columns,
14   wherein each core tile includes a configurable logic
15   block matrix and an associated programmable routing
16   matrix;
17   a plurality of edge tiles formed on the north, east,
18   south, and west perimeters of said plurality of core
19   tiles; and
20   a plurality of corner tiles formed adjacent said
21   plurality of edge tiles.
22
23   80. The tile based FPGA architecture of Claim 79 further
24 including a plurality of horizontal long lines extending
25 through each row of said core tiles and said edge tiles formed
26 on the north and south perimeters.
27
28   81. The tile based FPGA architecture of Claim 80 further
29 including a plurality of vertical long lines extending through
30 each column of said core tiles and said edge tiles formed on
31 the east and west perimeters.
32
33   82. The tile based FPGA architecture of Claim 81 wherein
34 the horizontal long lines extending through said edge tiles
35 formed on the north and south perimeters are coupled to said
36 vertical long lines extending through said edge tiles formed

1 on the east and west perimeters by said plurality of corner
2 tiles.

3

4   83. The tile based FPGA architecture of Claim 82 wherein
5 each core, edge, or corner tile includes at least two lines;
6 wherein one corner tile includes a north line coupled to an
7 east line, another corner tile includes a south line coupled
8 to an east line, another corner tile includes a west line
9 coupled to a south line, and another corner tile includes a
10 north line coupled to a west line; wherein one edge tile on
11 said south perimeter includes a north line coupled to an east
12 line and a west line, another edge tile on said west perimeter
13 includes an east line coupled to a north line and a south
14 line, another edge tile on said north perimeter includes a
15 south line coupled to an east line and a west line, and
16 another edge tile on said east perimeter includes an east line
17 coupled to a north line and a south line; wherein a core tile
18 includes a north line coupled to an east line, a south line,
19 and a west line, wherein the west line of a corner tile is
20 coupled to the east line of an edge tile formed on said north
21 perimeter or said south perimeter, wherein the east line of a
22 corner tile is coupled to the west line of an edge tile formed
23 on said north perimeter or said south perimeter, wherein the
24 south line of a corner tile is coupled to the north line of an
25 edge tile formed on said east perimeter or said west
26 perimeter, wherein the north line of a corner tile is coupled
27 to the south line of an edge tile formed on said east
28 perimeter or said west perimeter; wherein the south line of an
29 edge tile formed on said north perimeter is coupled to the
30 north line of a core tile, wherein the west line of an edge
31 tile formed on said east perimieter is coupled to the east
32 line of a core tile, wherein the north line of an edge tile
33 formed on said south perimeter is coupled to the south line of
34 a core tile, and wherein the east line of an edge tile formed
35 on said west perimeter is coupled to the west line of a core
36 tile.

37

1   84. The tile based FPGA architecture of Claim 83 wherein
2 each edge tile includes a general interconnect structure,
3 wherein said plurality of horizontal long lines, said
4 plurality of vertical long lines, and said at least two lines
5 are programmably connected to said general interconnect
6 structure.
7
8   85. The tile based FPGA architecture of Claim 84 further
9 including at least one pad, wherein said at least one pad is
10 programmably connected to the general interconnect structure
11 of an edge tile.
12
13   86. The tile based FPGA architecture of Claim 85 further
14 including a plurality of pads, wherein each pad is
15 programmably connected to the general interconnect structure
16 of an edge tile.
17
18   87. The tile based FPGA architecture of Claim 85 wherein
19 said at least one pad is programmably connected to the general
20 interconnect structure via a pad interconnect structure.
21
22   88. The tile based FPGA architecture of Claim 87 wherein
23 both said general interconnect structure and said pad
24 interconnect structure include programmable interconnection
25 points (PIPs).
26
27   89. The tile based FPGA architecture of Claim 88 wherein
28 said pad interconnect structure provides more PIPs than said
29 general interconnect structure.
30
31   90. The tile based FPGA architecture of Claim 89 wherein
32 said pad interconnect structure is substantially fully
33 pipulated.
34
35   91. The tile based FPGA architecture of Claim 90 wherein
36 said general interconnect structure is sparsely pipulated.
37

```
 1        92.  A method of forming a tile based FPGA architecture,
 2   said method comprising the steps of:
 3        forming a configurable logic block matrix in a core tile;
 4        forming a programmable routing matrix in said core tile;
 5        coupling said configurable logic block matrix and said
 6             programmable routing matrix;
 7        coupling said configurable logic block matrix to a
 8             configurable logic block matrix in an adjacent core
 9             tile;
10        coupling said programmable routing matrix to a
11        programmable routing matrix in another core tile.
12
13        93.  The method of forming a tile based FPGA architecture
14   of Claim 92 wherein said another core tile is adjacent said
15   programmable routing matrix in said core tile.
16
17        94.  The method of forming a tile based FPGA architecture
18   of Claim 92 wherein said another core tile is not adjacent
19   said programmable routing matrix in said core tile.
20
```

100
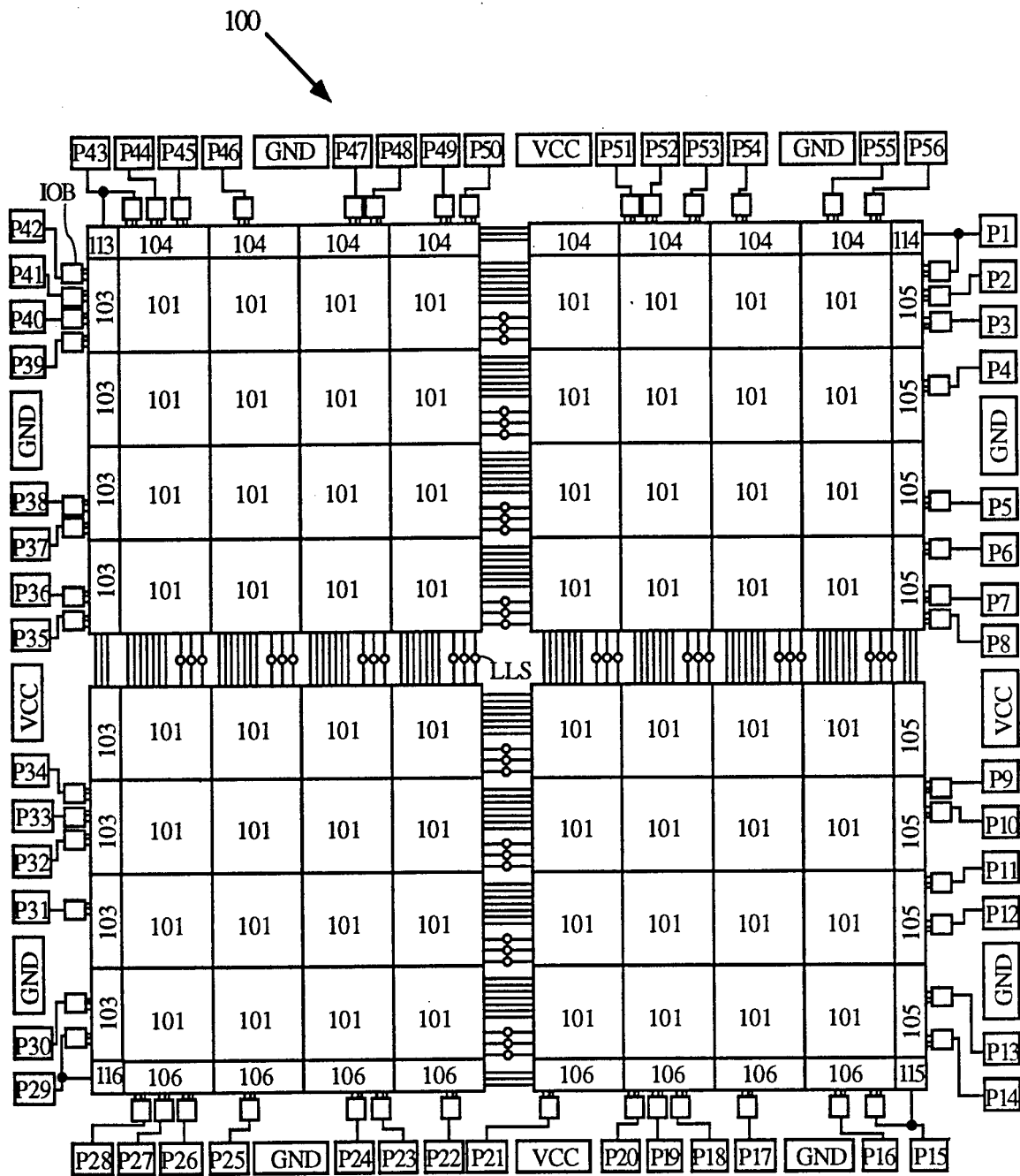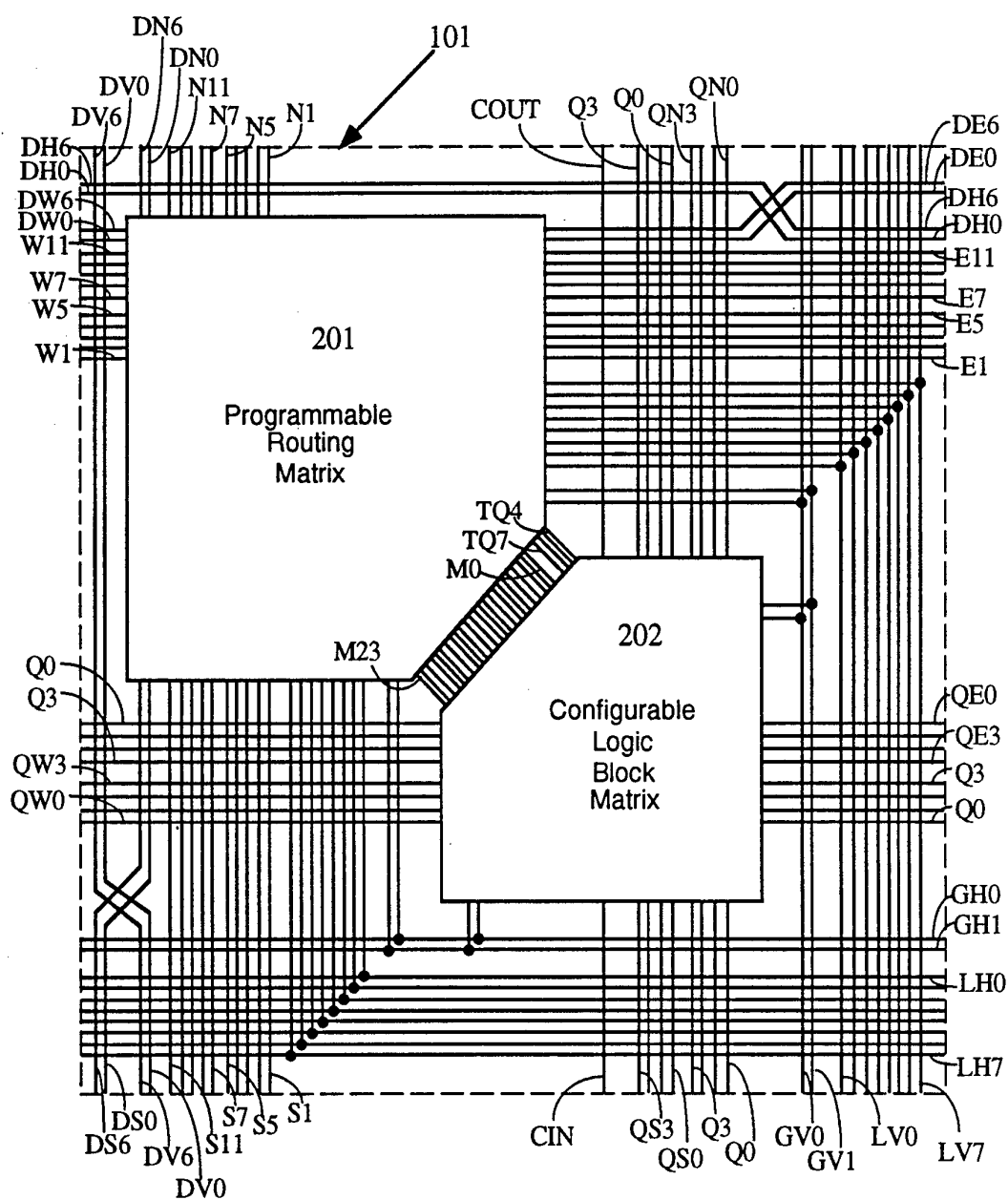
Fig. 1

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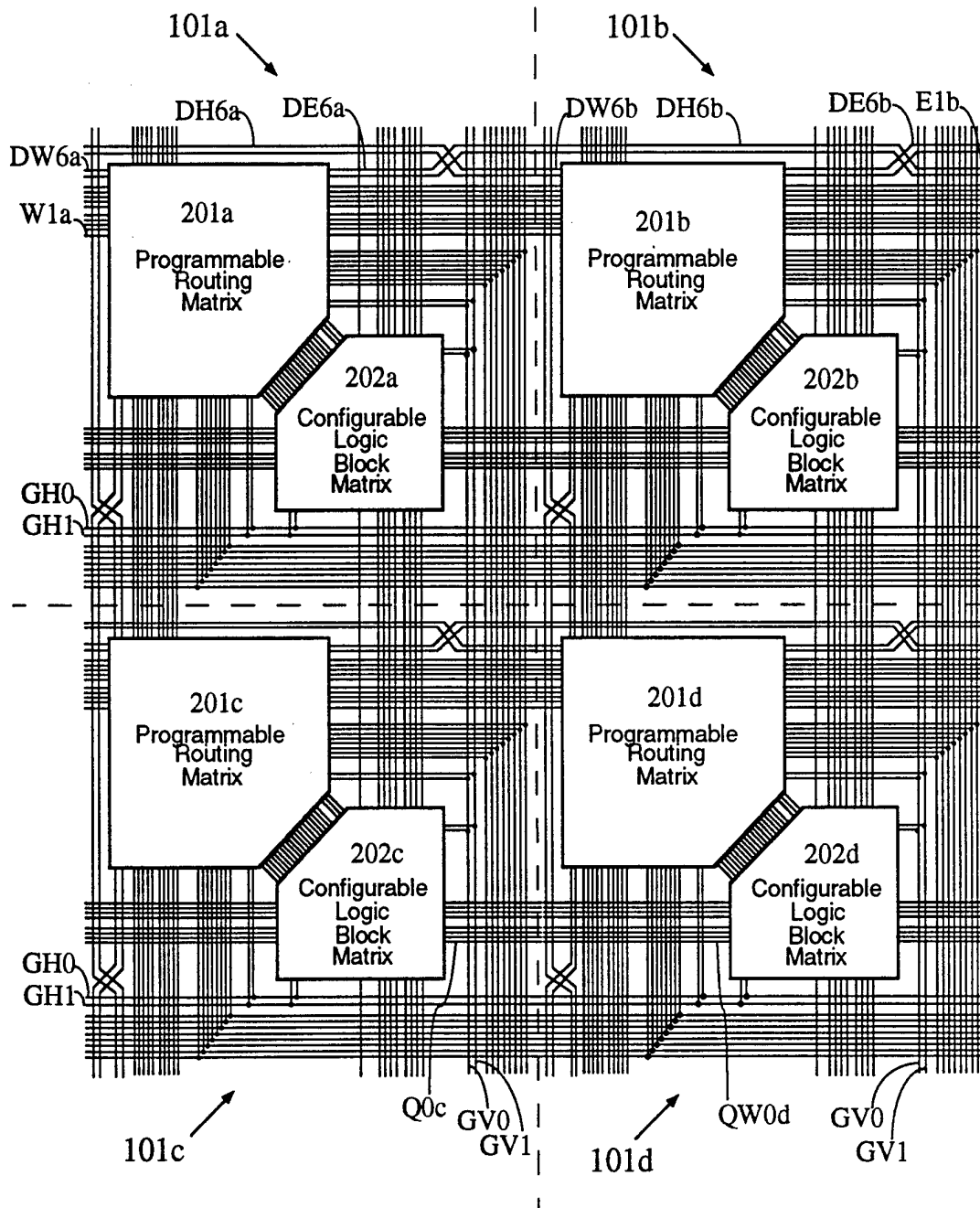
Fig. 2B

Fig. 3A

Fig. 3B

Fig. 3C

Fig. 4A

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TQ7   TQ6   TQ5   TQ4

MM7   A7 B7   MM6   A6 B6   MM5   A5 B5   MM4   A4 B4

OR1

ENLL TS   Q7   Q6   Q5   Q4

Fig. 4B

309

Q7   Q6   Q5   Q4   Q3   Q2   Q1   Q0

ENOUT

Q7'   Q6'   Q5'   Q4'   Q3'   Q2'   Q1'   Q0'
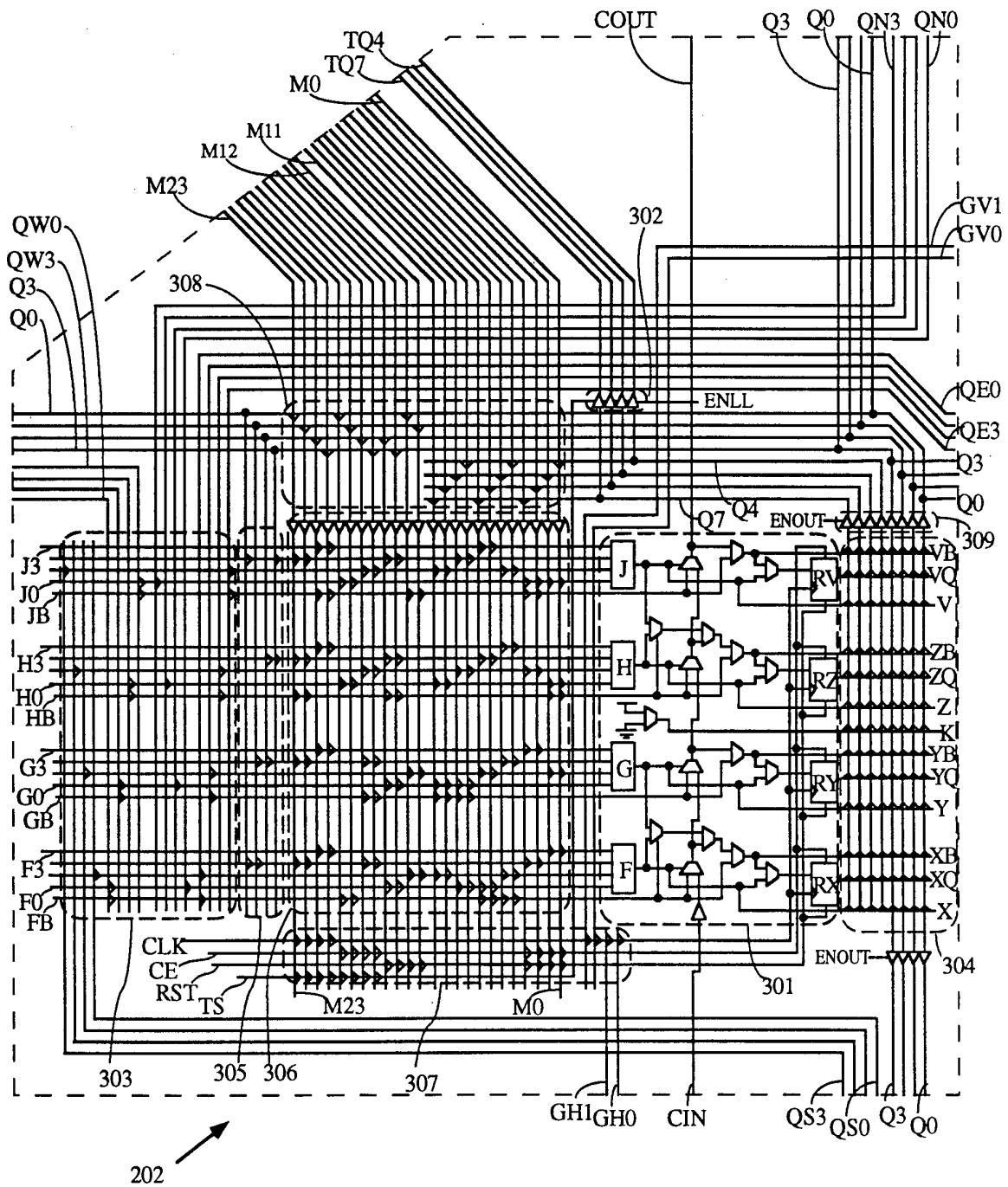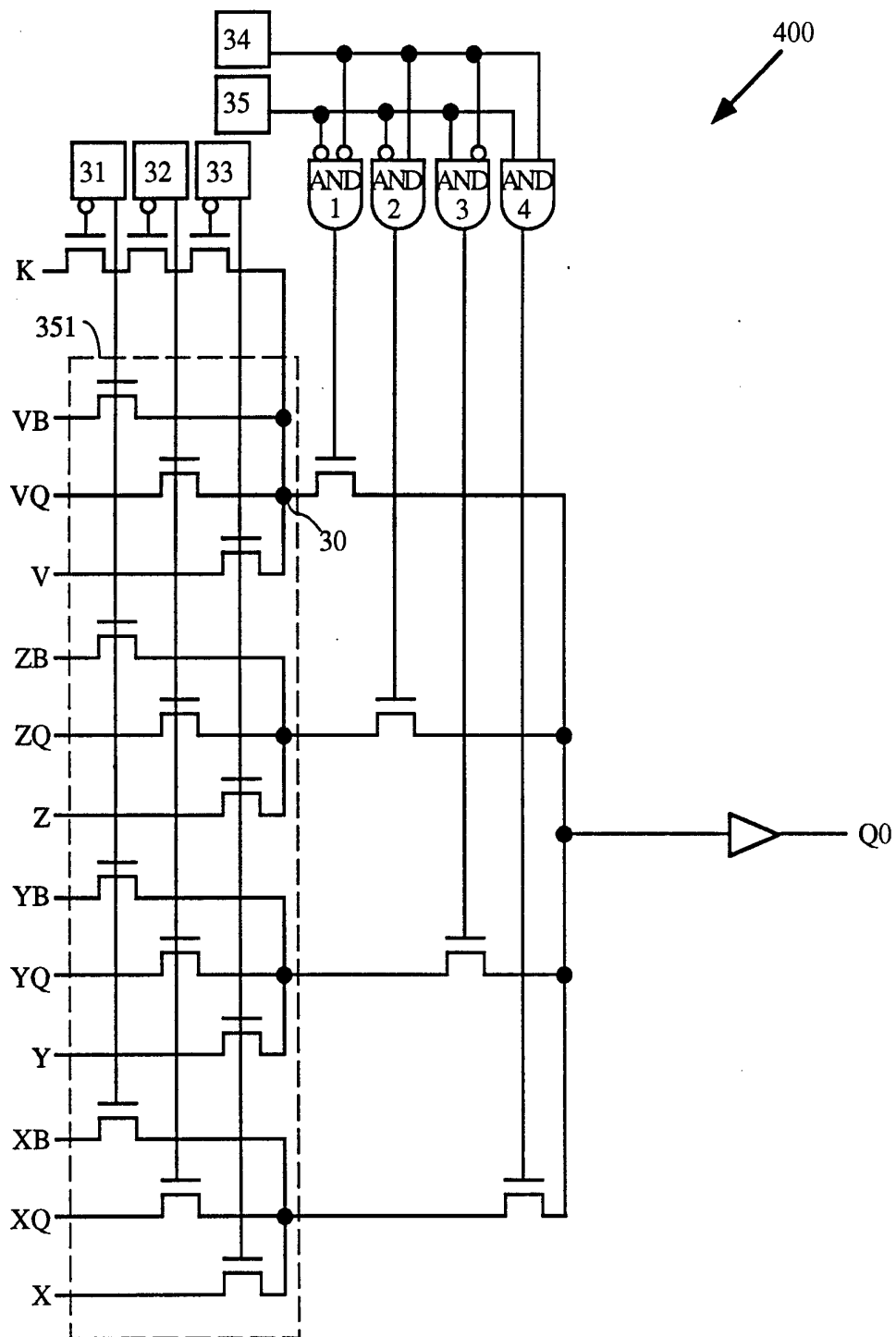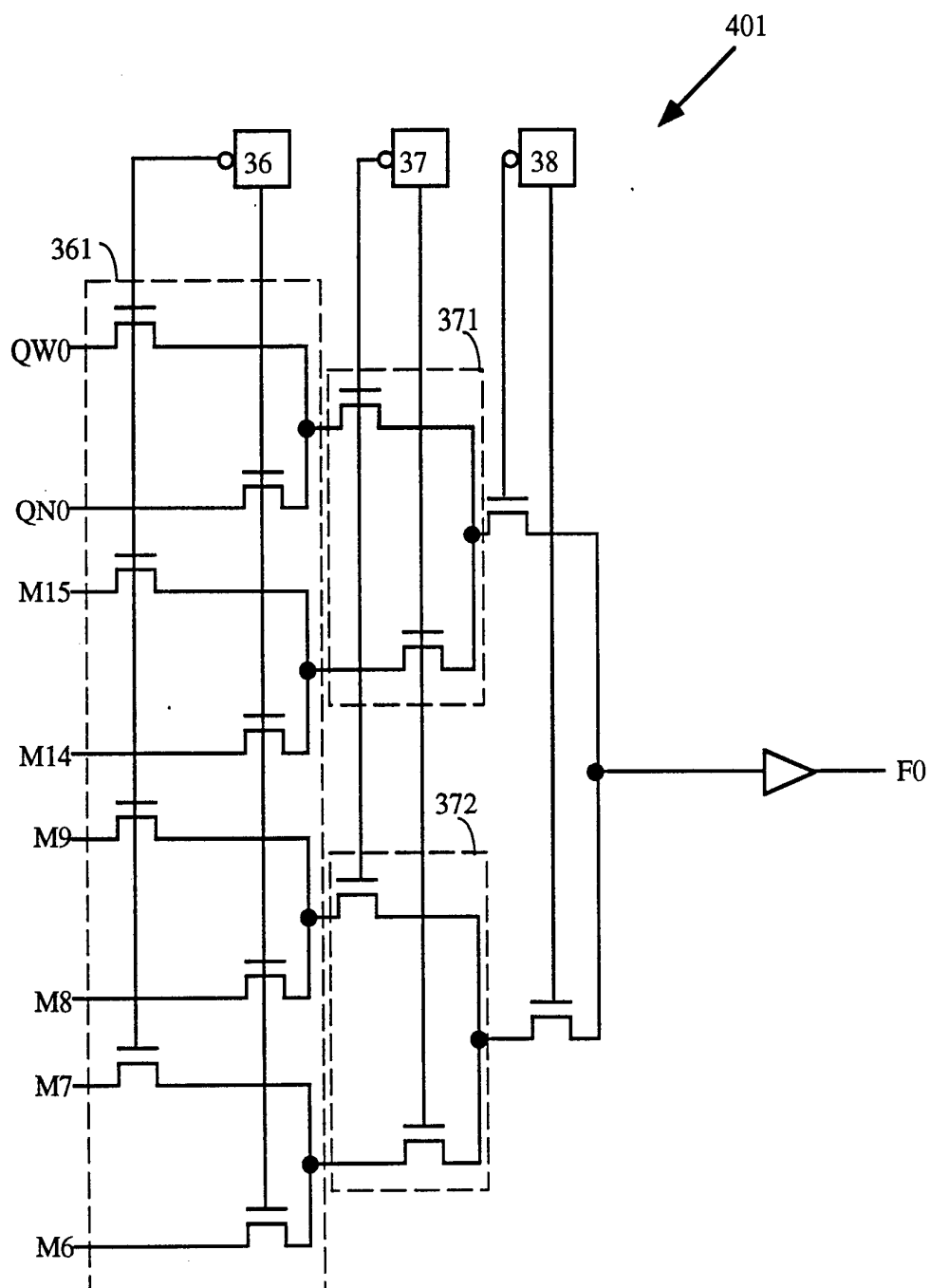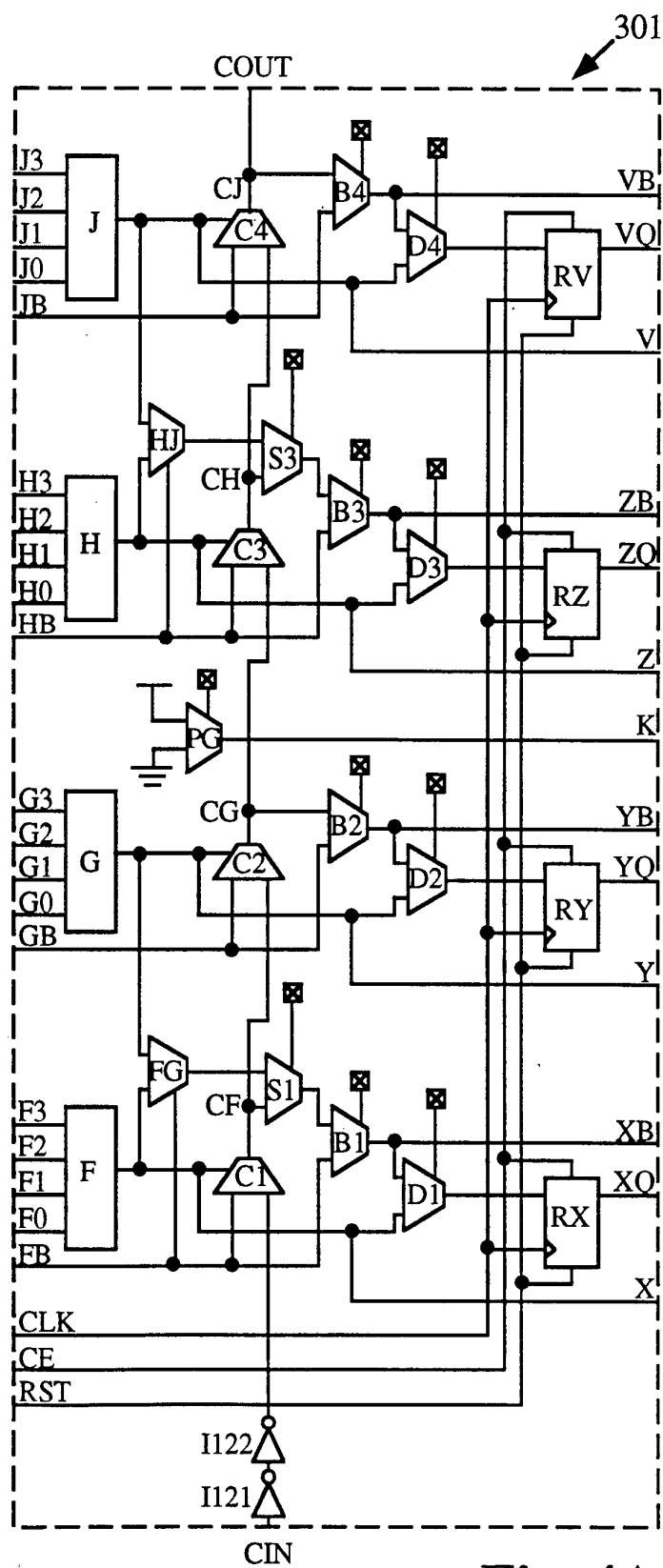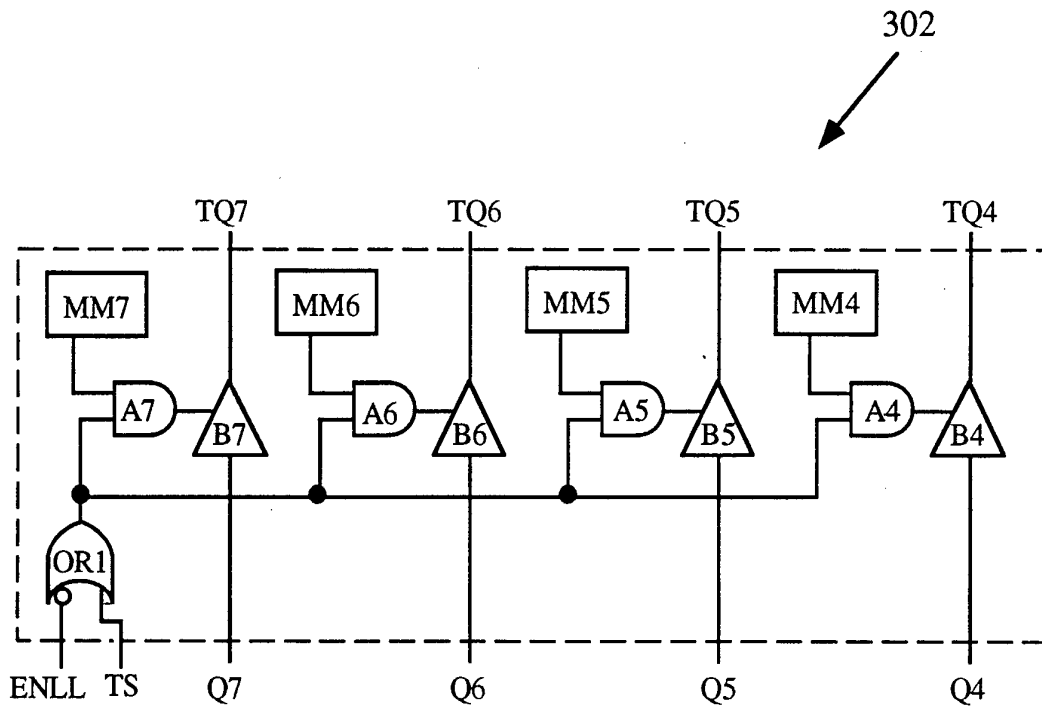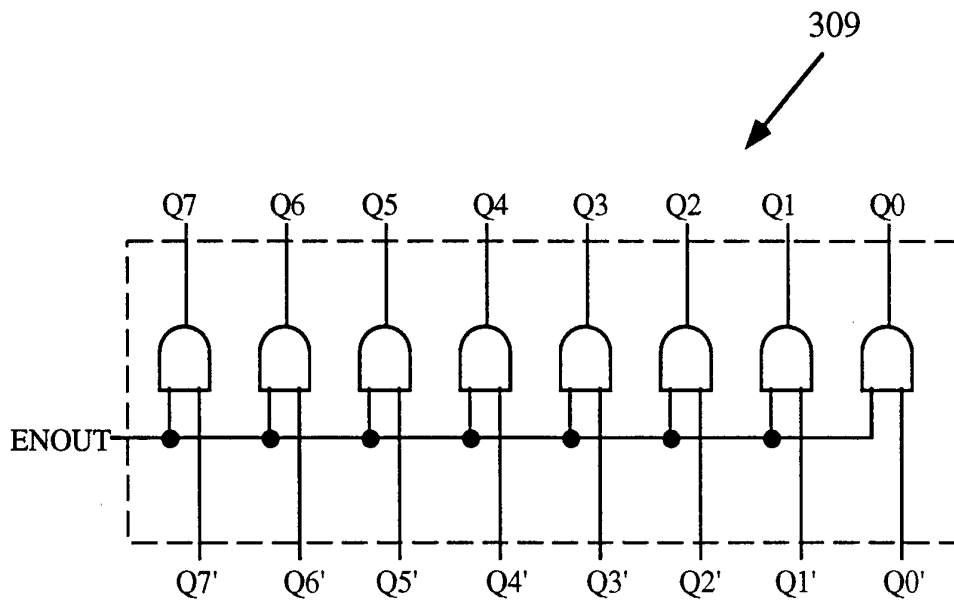
Fig. 4C

Fig. 4E
Prior Art

16 SELECT BITS
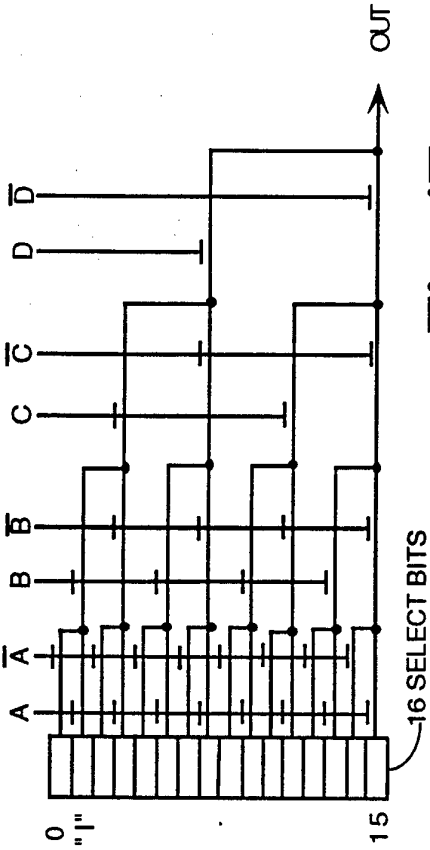
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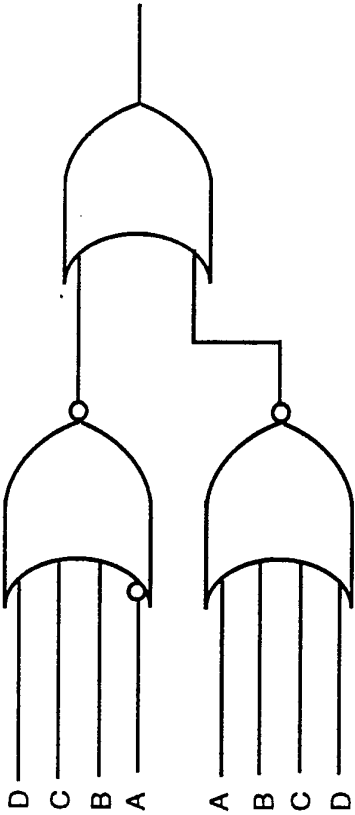
Fig. 4G
Prior Art
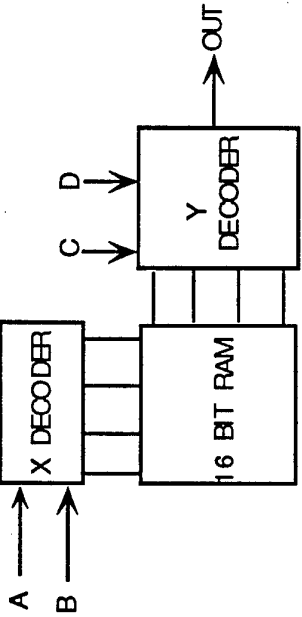
Fig. 4D
Prior Art

Fig. 4F
Prior Art
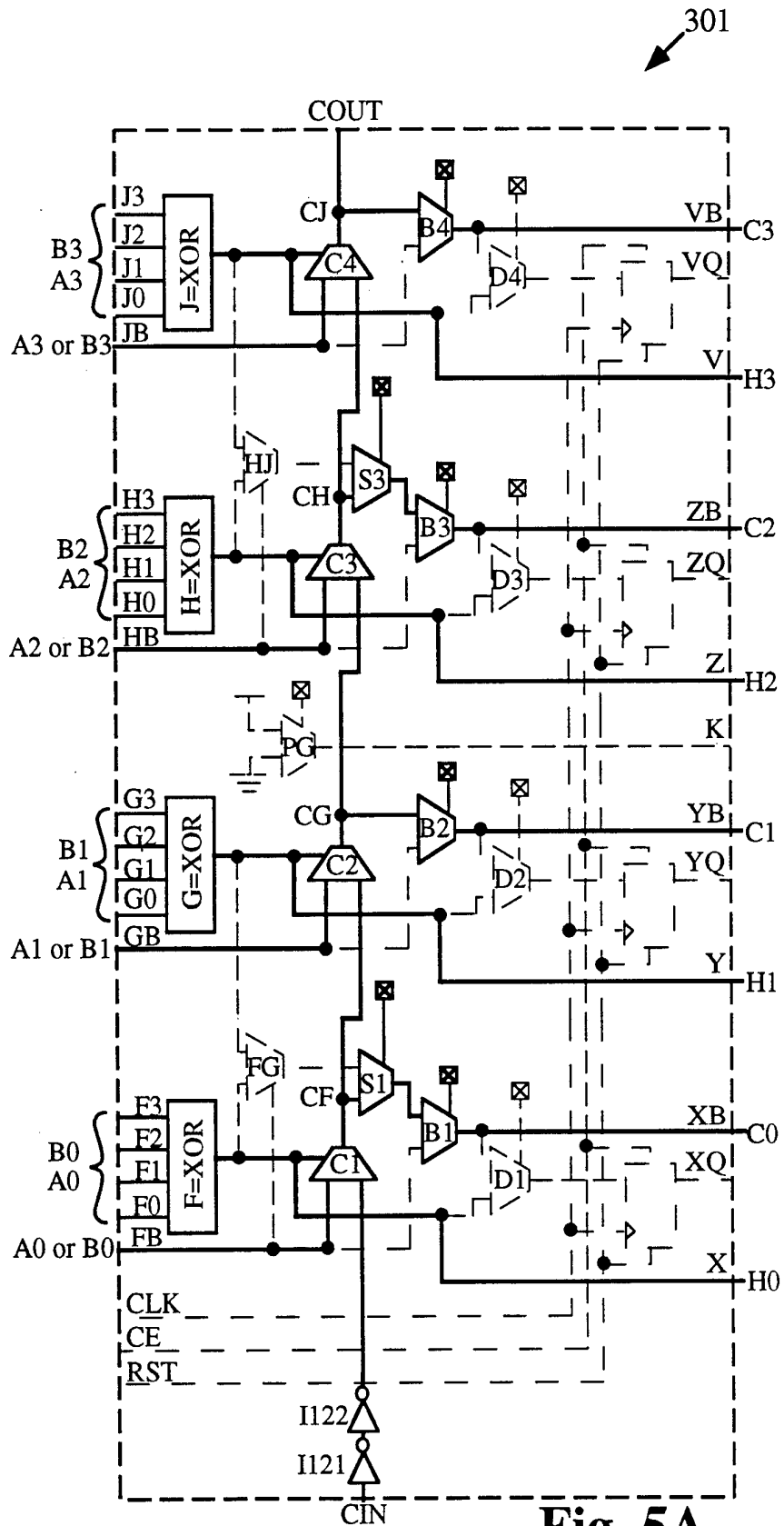
Fig. 5A

Fig. 5B

Fig. 5C

Fig. 6

13/26

Fig. 7A

14/26

Fig. 7B

15/26

Fig. 8

Fig. 9

17/26
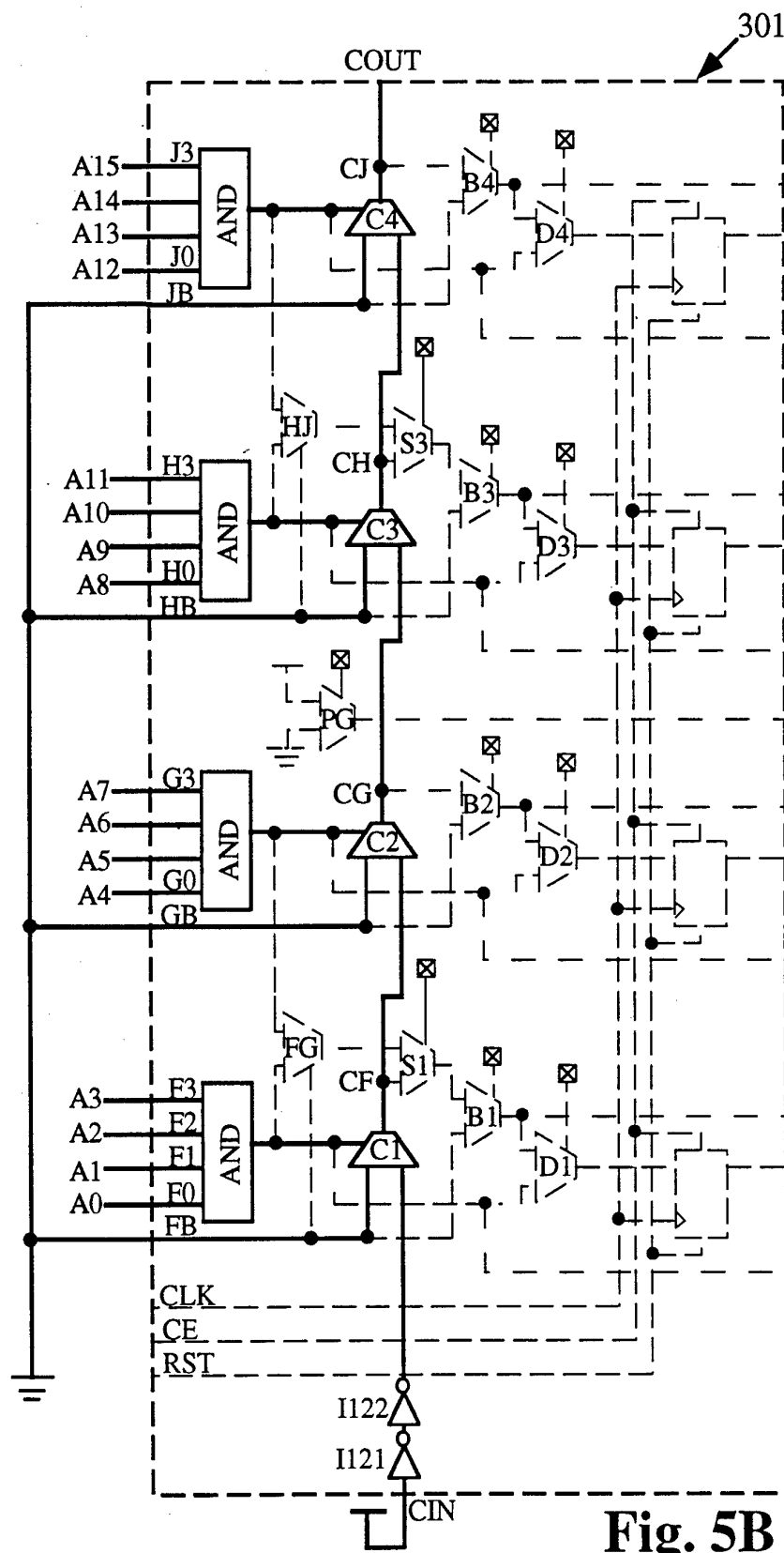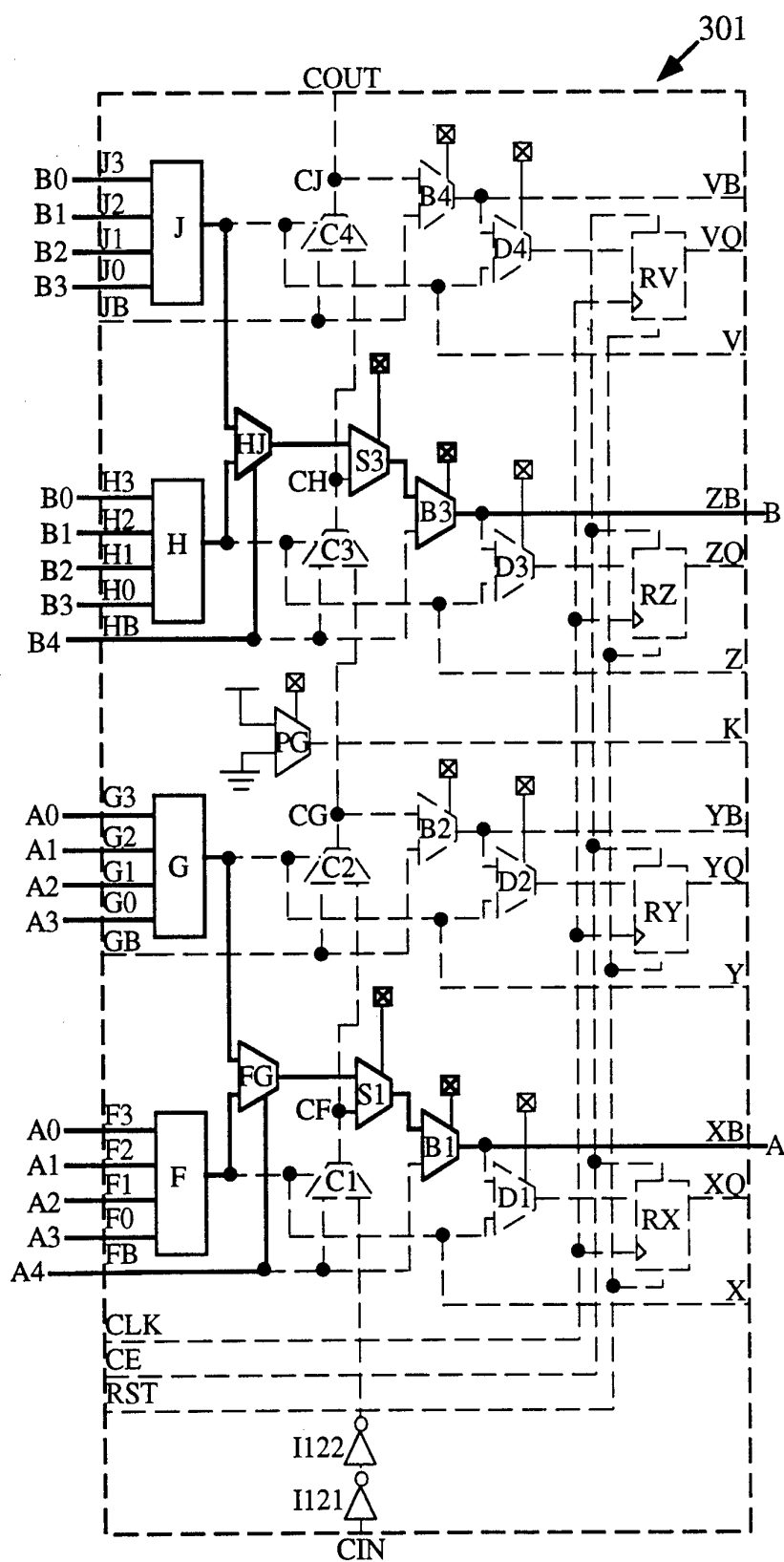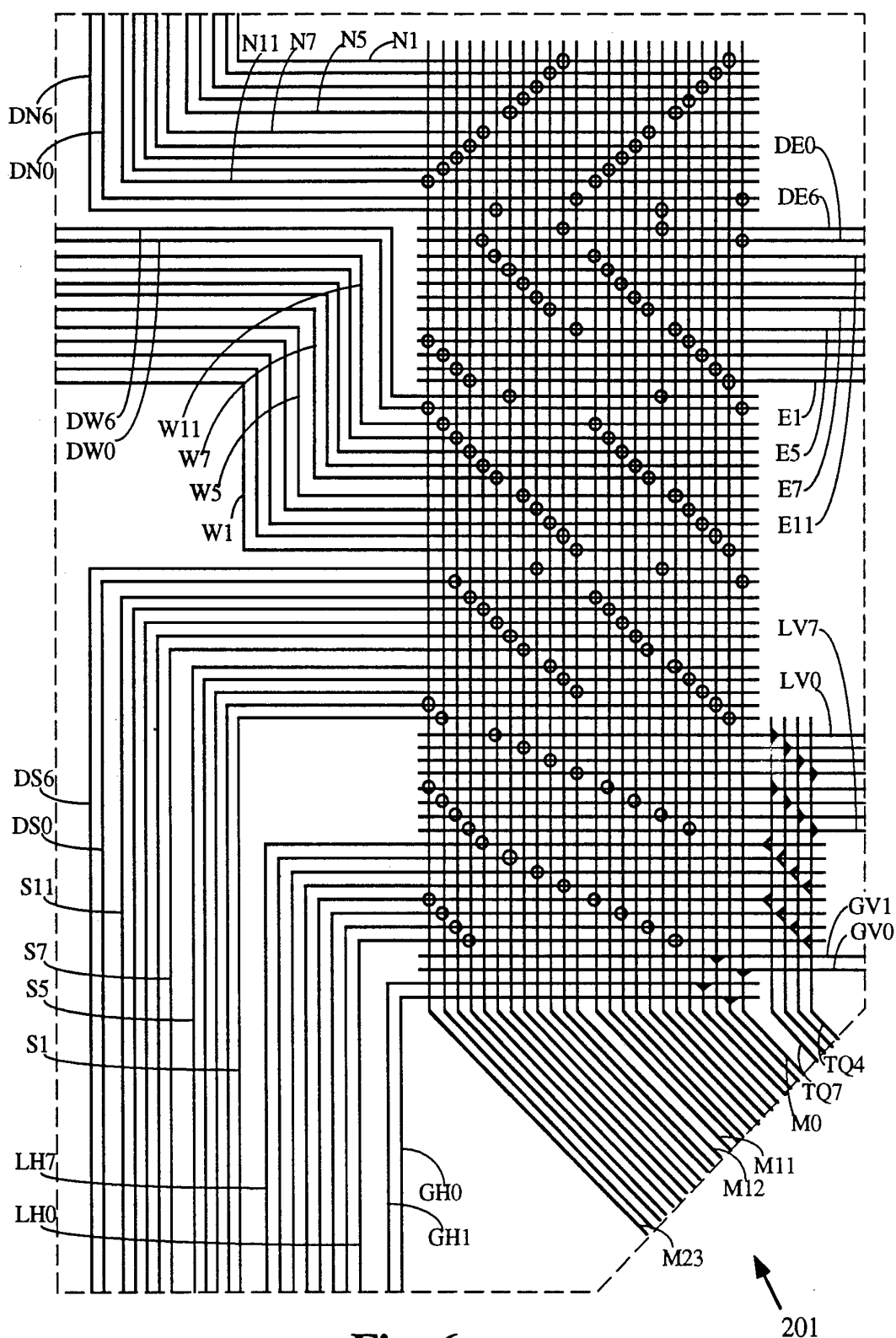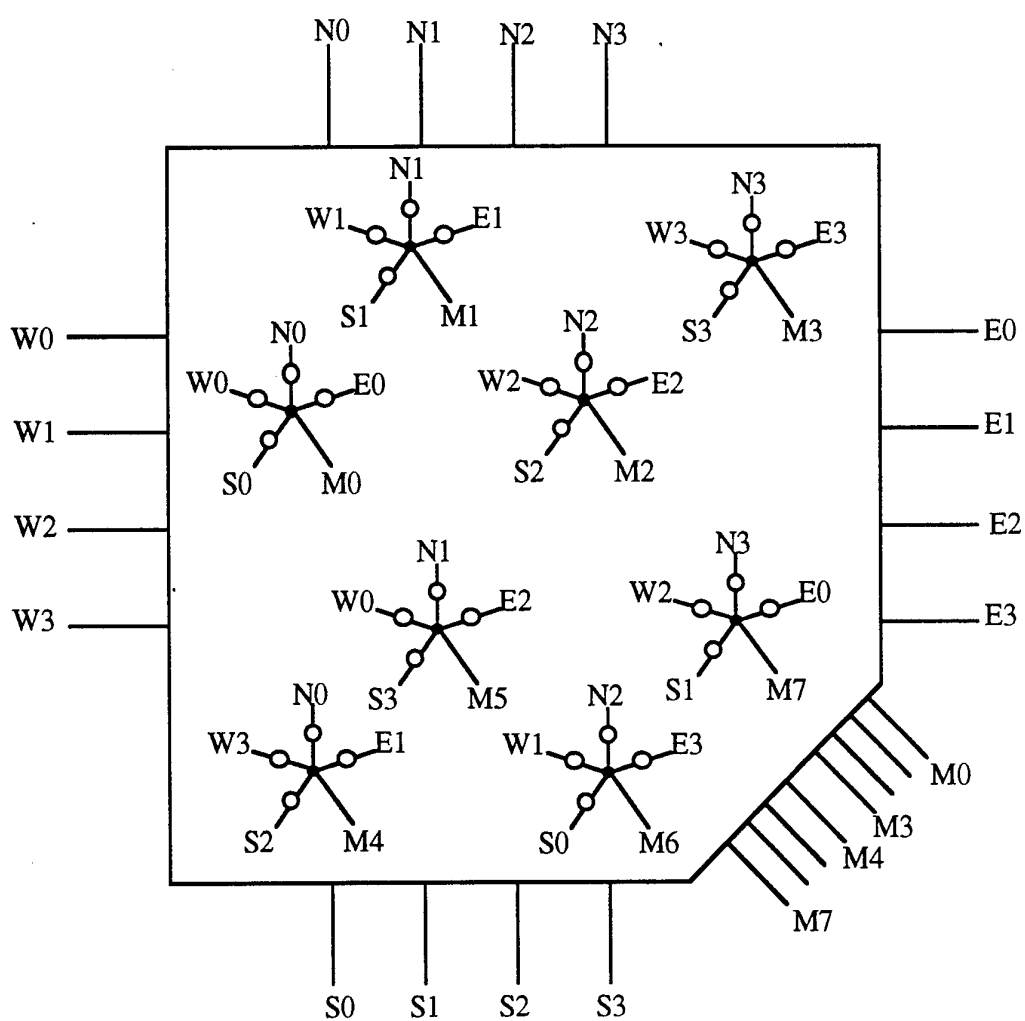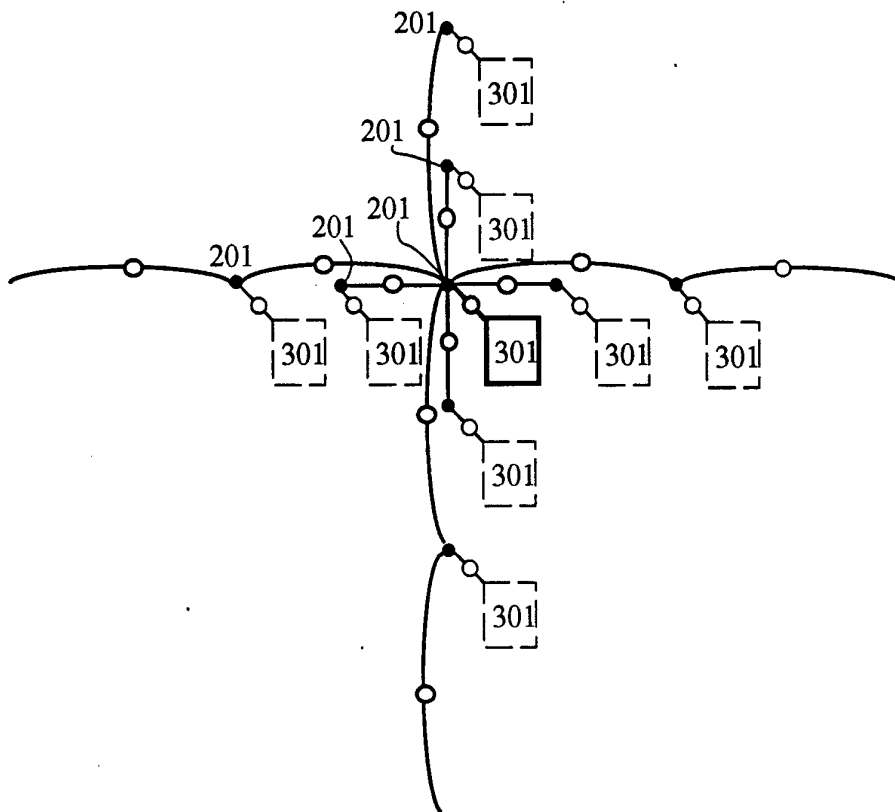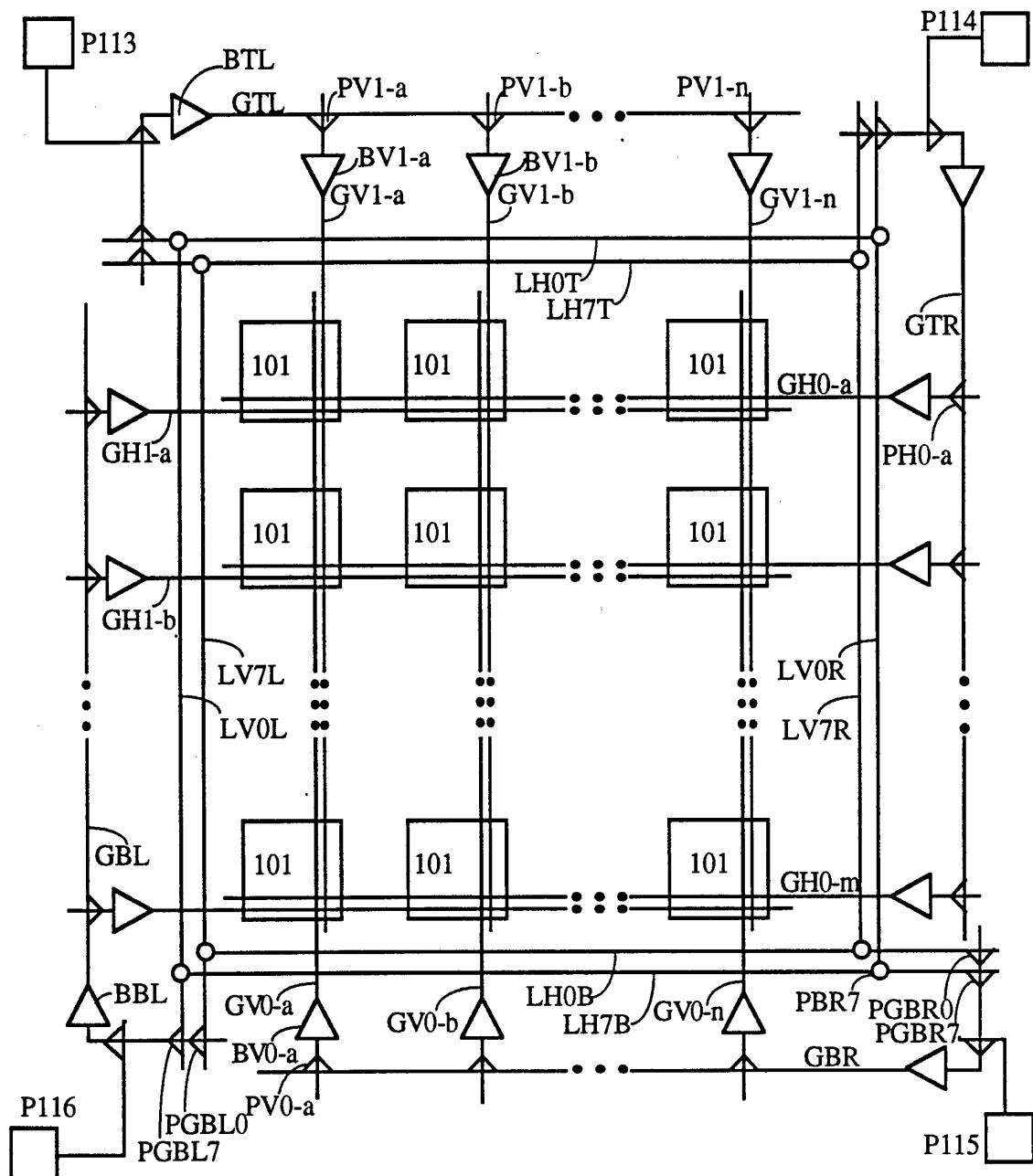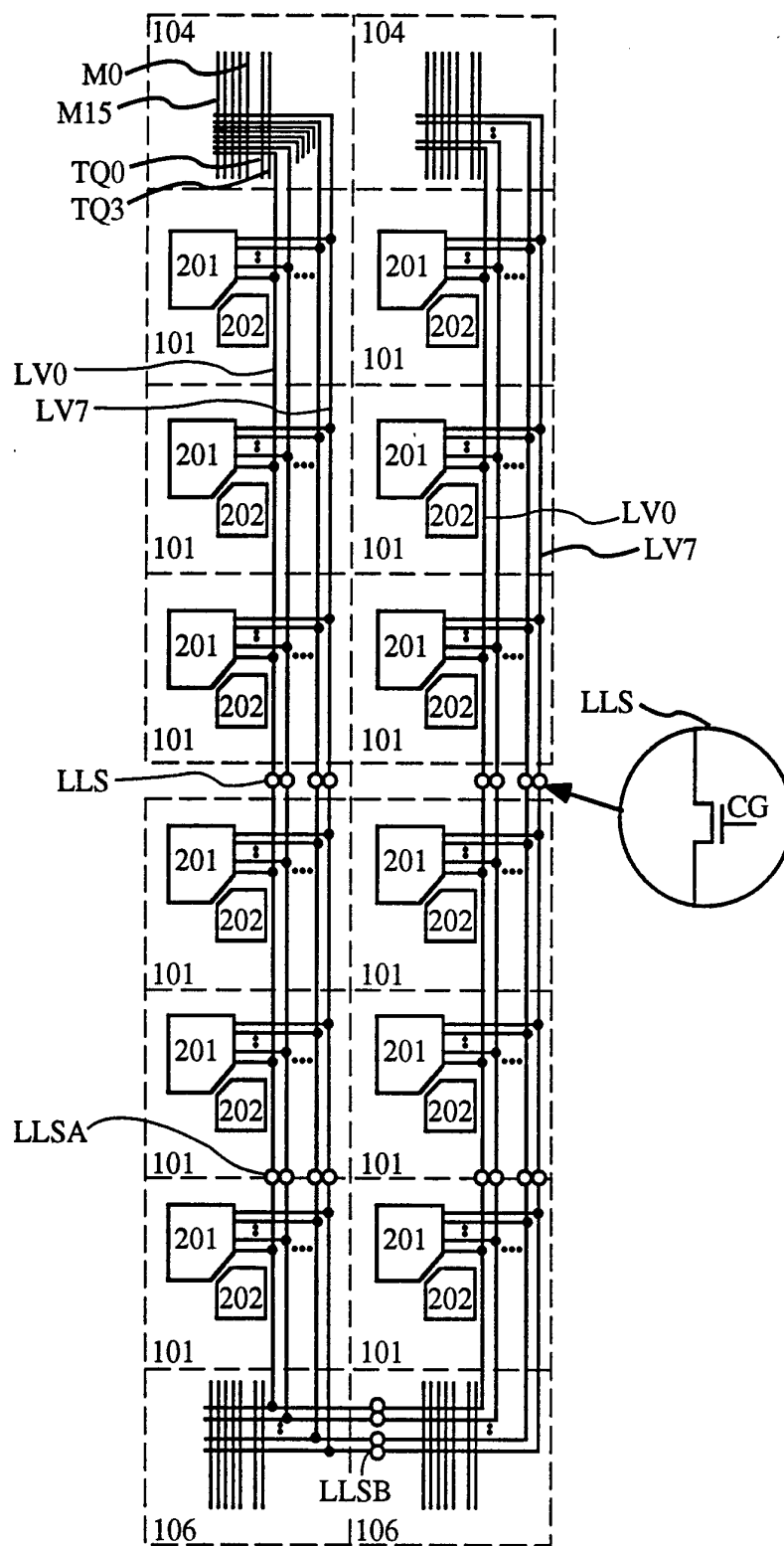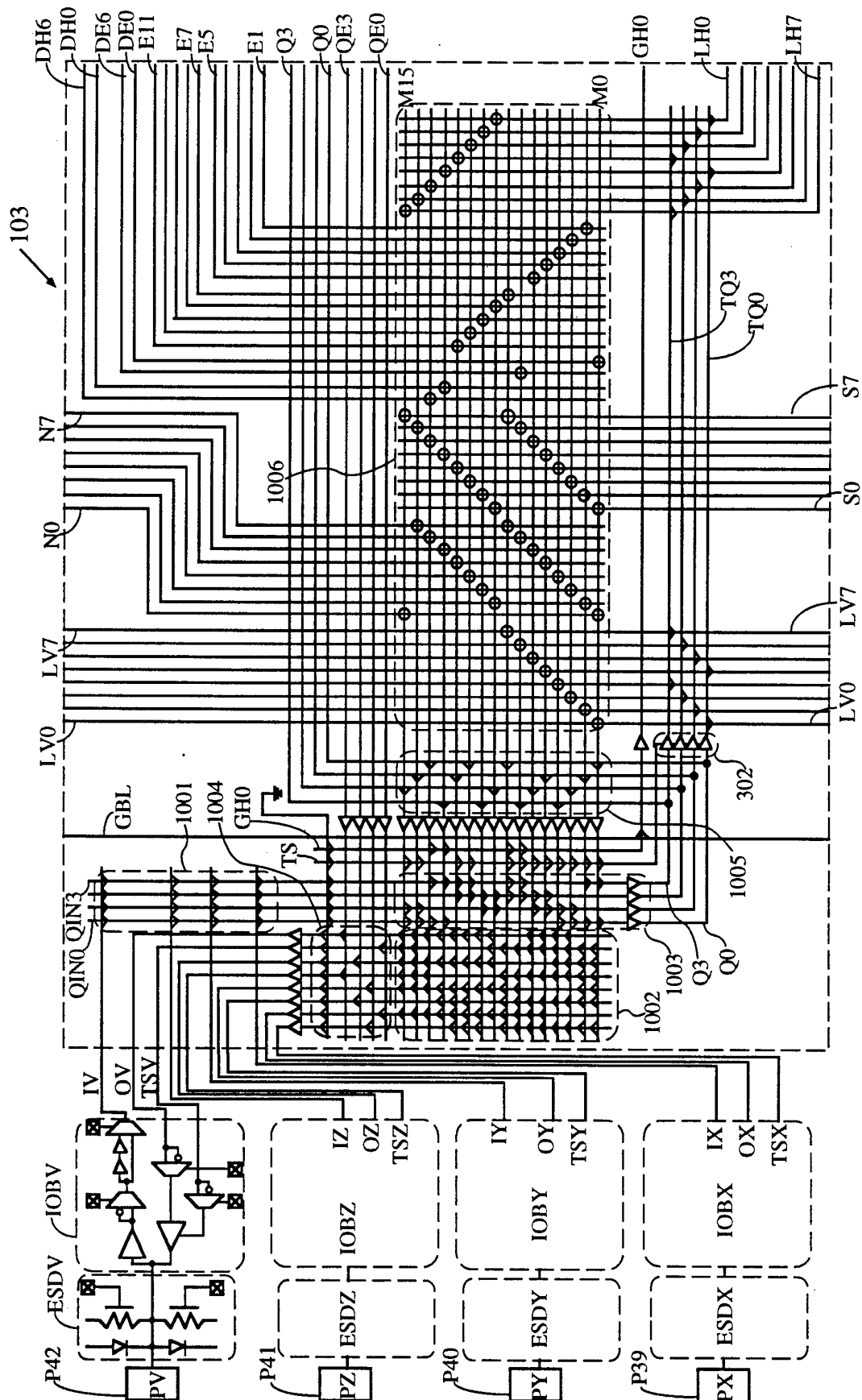
Fig. 10A

Fig. 10B   19/26

Fig. 10C

Fig. 10D

Fig. 11A

114
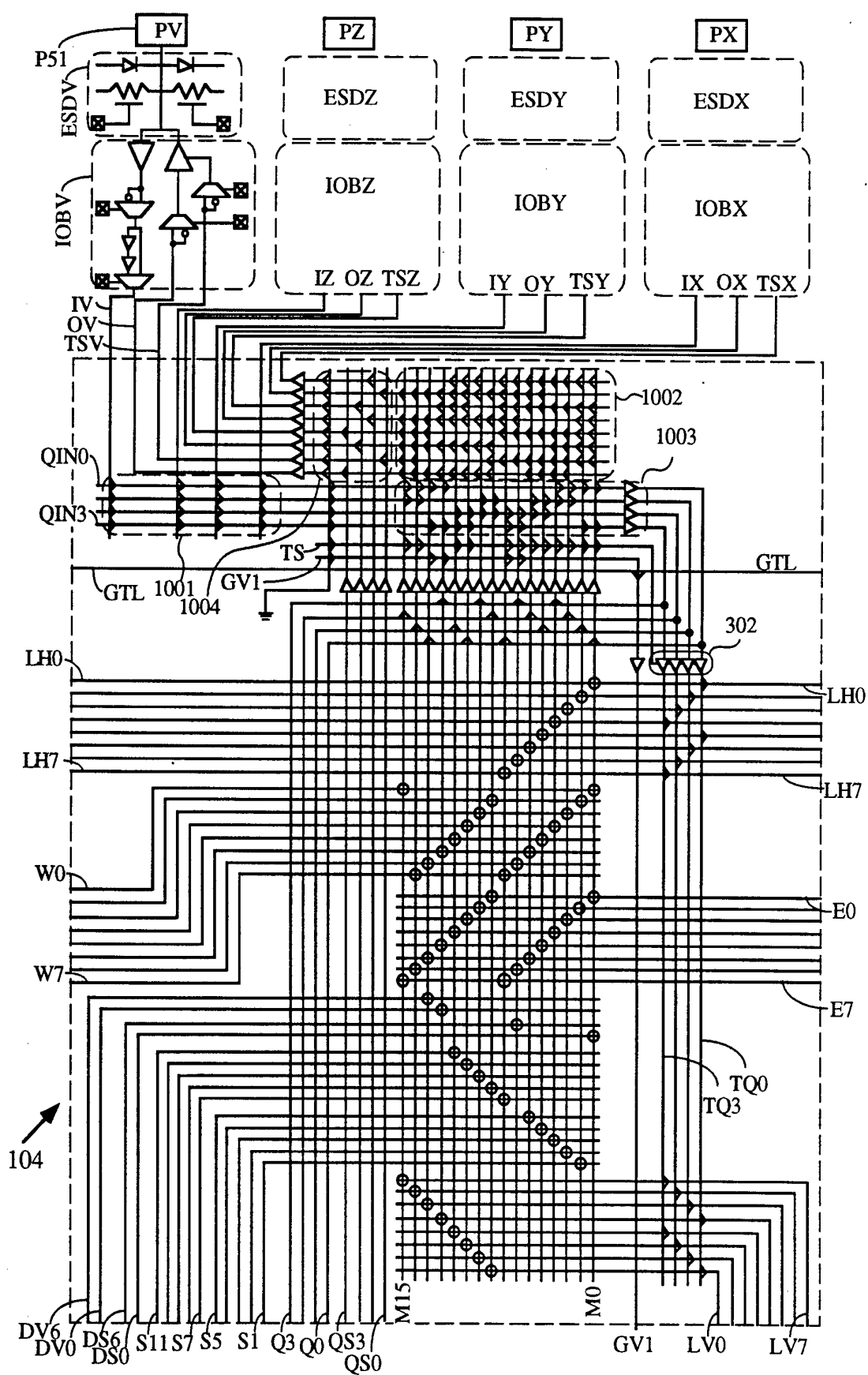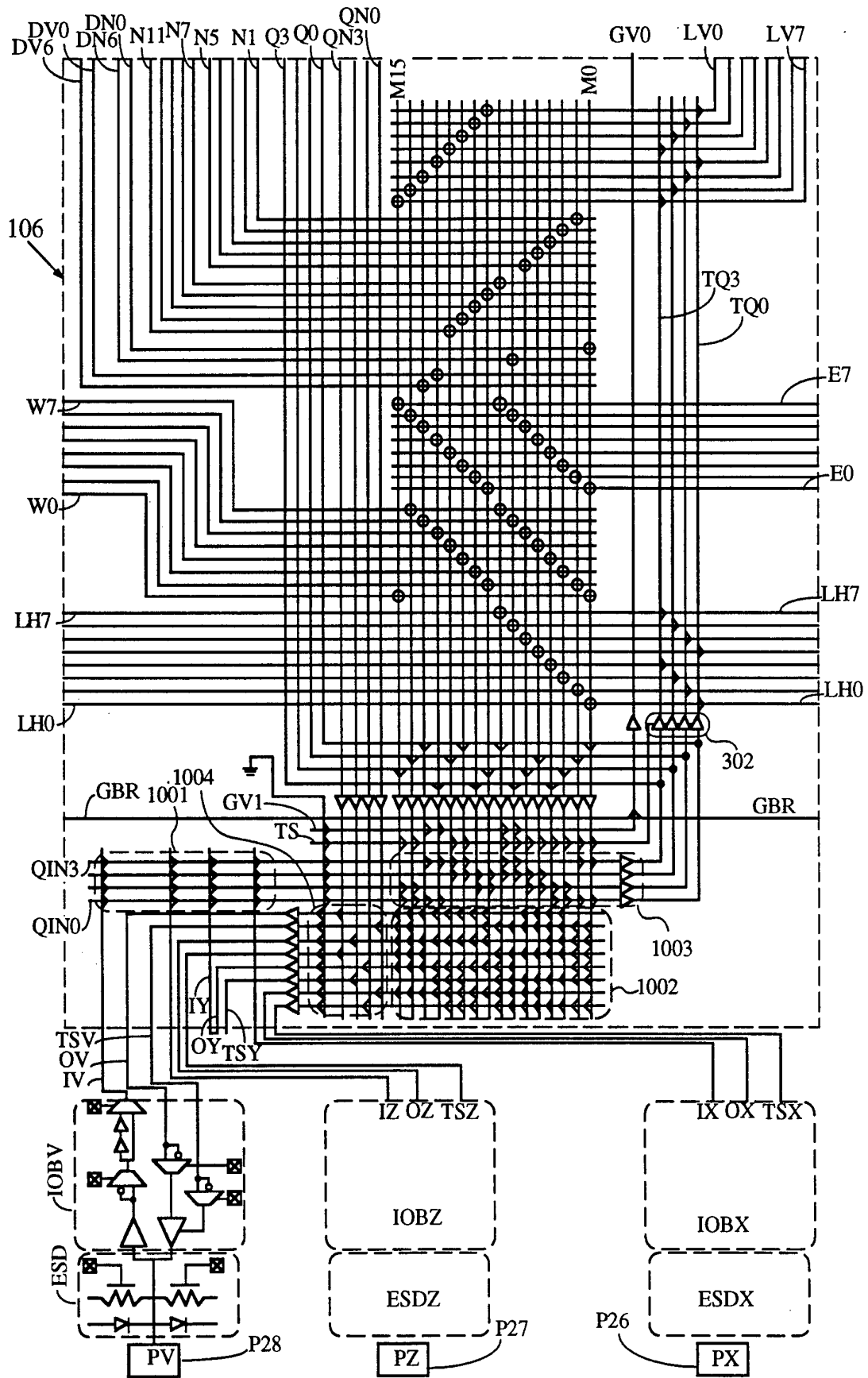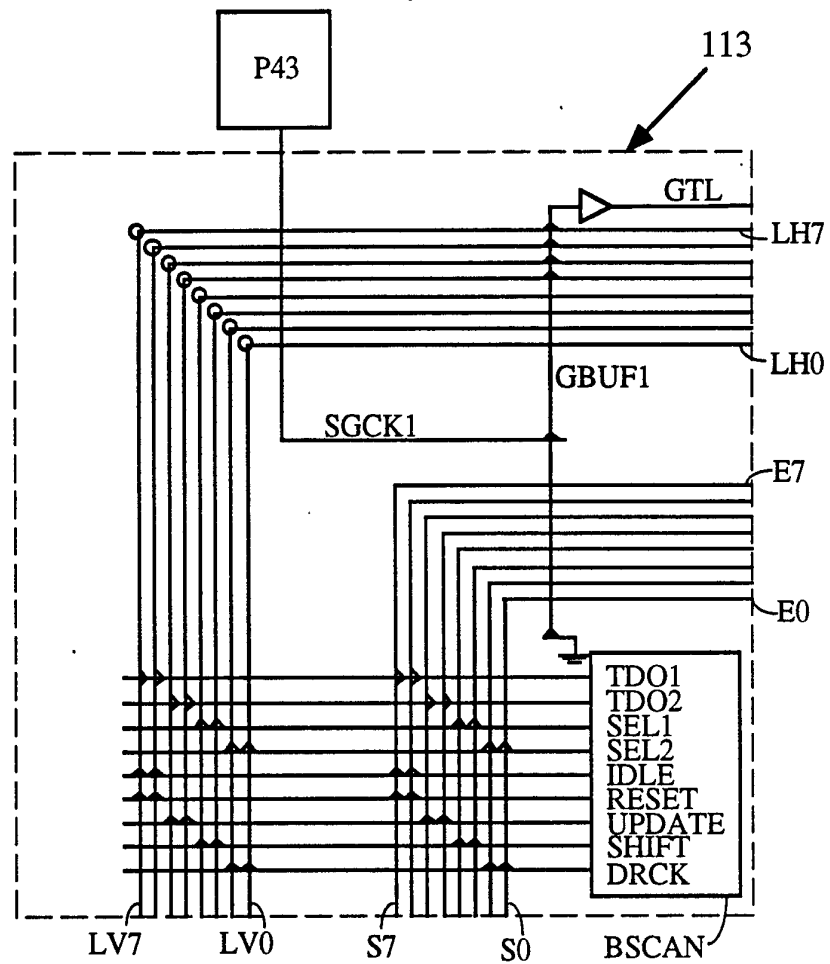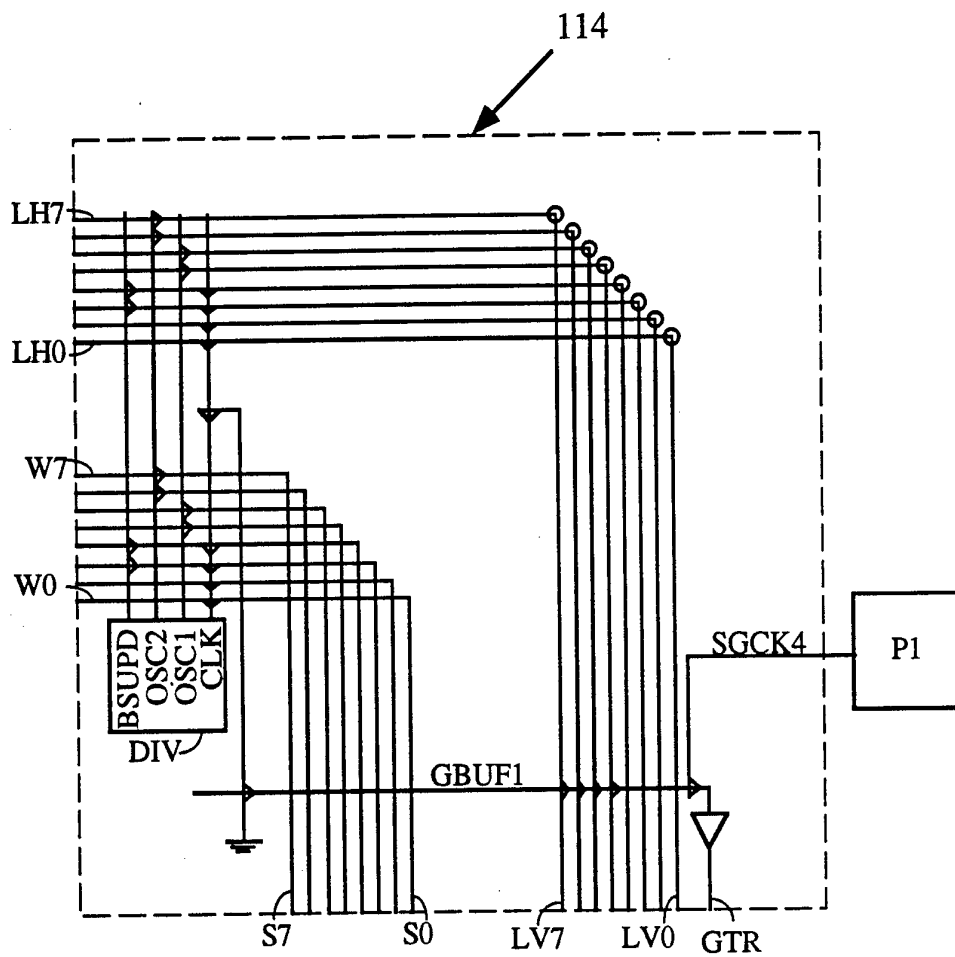
Fig. 11B

Fig. 11C

Fig. 11D
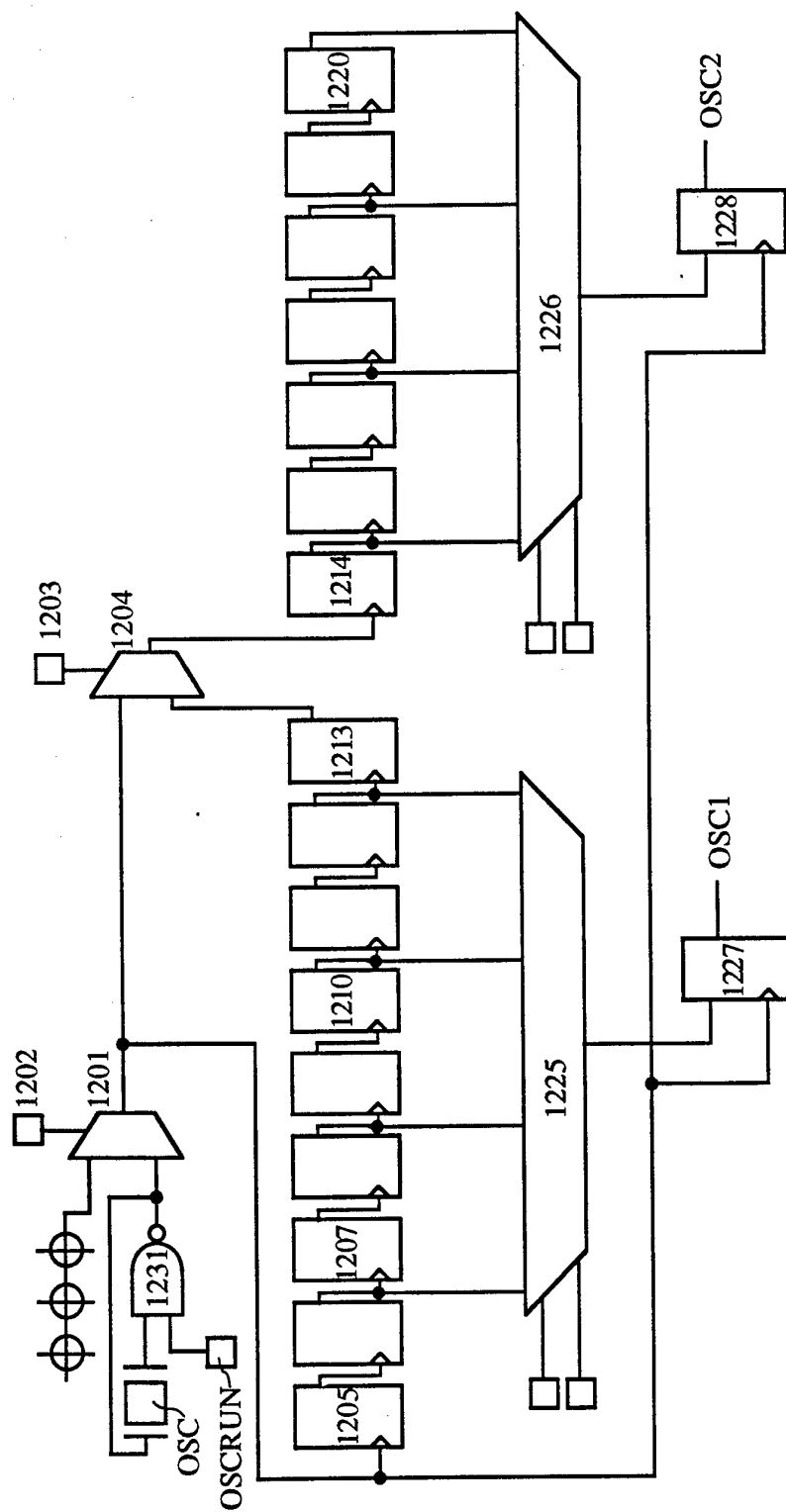
Fig. 12

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
H 03 K 19/177

According to International Patent Classification (IPC) or to both national classification and IPC 6

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

    H 01 L,H 03 K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP, A, 0 461 798 (AMD) 18 December 1991 (18.12.91), the whole document.	1-94
A	US, A, 5 260 610 (PEDERSEN et al.) 09 November 1993 (09.11.93), the whole document.	1-94
A	US, A, 5 260 611 (CLIFF et al.) 09 November 1993 (09.11.93), the whole document.	1-94
A	US, A, 5 241 224 (PEDERSEN et al.) 31 August 1993 (31.08.93), abstract; fig. 1-4D.	1,74, 78,79, 92

[X] Further documents are listed in the continuation of box C.   [ ] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
23 May 1995	19. 06. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	FELLNER e.h.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5 280 202 (CHAN et al.) 18 January 1994 (18.01.94), abstract; figs..	1,74, 78,79, 92

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