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(54) Antenna arrangement

(57) A novel multiplex system is disclosed which overcomes the disadvantage of a parasitic diode which occurs upon use of MOS FET switches to switch between channels. A preferred embodiment of the invention is effected by connecting the power MOS FET 18,20 to the antenna 10,12 via a serially connected capacitor 14,16. Thus, in a disabled channel, the serially connected capacitor 14 may be charged up to the peak positive D.C. voltage of the antenna resonator circuit 24 of the enabled channel, via the parasitic diode. The capacitor 14 in the disabled channel is charged via the parasitic diode while a different transmit channel has been selected and when the antenna resonator 24 of that different channel, builds up the antenna resonance voltage. Once the voltage at the antenna resonator 24 is at the maximum, the capacitor 14 in the disabled channel is also charged up to the maximum voltage and

therefore, the antenna resonance voltage of the enabled channel minus the stored voltage of the disabled channel capacitor 14 will never be less than zero. In conclusion, because the drain of the FET is held to a positive voltage, and the parasitic diode needs a negative voltage to conduct, the parasitic voltage stops conducting and will not conduct while the capacitor is charged to that positive voltage. Therefore, the FET is blocked to negative voltages.

The disabled MOS FET 18 is also blocked for positive voltages because that is the basic function of the MOS FET switch 18. The parasitic diode is not conducting in this situation, because the diode is reversed biased in this case and therefore needs a negative voltage to conduct.

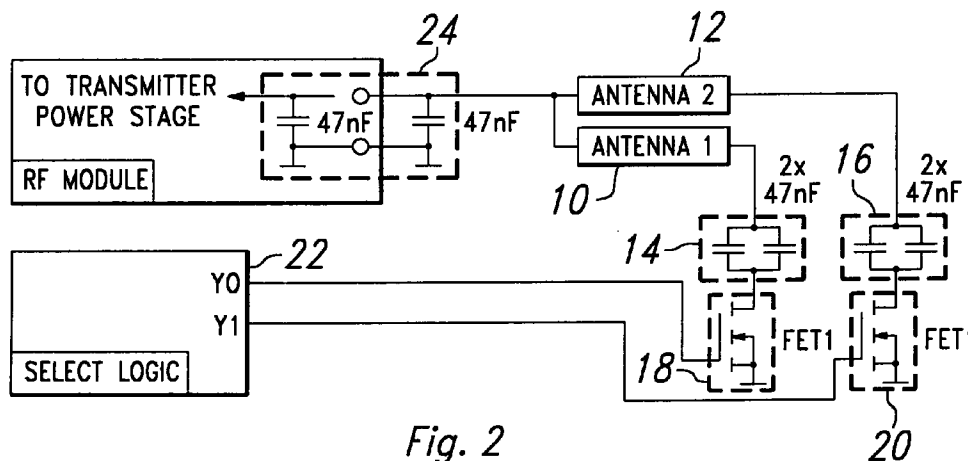


Fig. 2

Description

FIELD OF THE INVENTION

This invention generally relates to multiple antenna capability in transceiver systems.

BACKGROUND OF THE INVENTION

In a standard Radio Frequency-Identification (RF-ID) system, an interrogating antenna, sometimes called the transmitter antenna, transmits a power burst signal of some predetermined duration to power up the passive transponder in the field to respond. Once the transponder is fully charged from the interrogation signal, the power burst signal is damped at the interrogator, and the transponder transmits its response telegram. The response telegram is received by a receive antenna in the interrogation unit and generally consists of identification information and/or sensor or other data. Often-times, not only is a single interrogation antenna and a single receive antenna necessary for the operation of any given transceiver system, but more realistically, several receive antennas and perhaps more than one interrogation antenna are necessary for optimal operation of more complex transceiver systems.

The problems associated with connecting more than one antenna to a single RF Module exist in the particular method used to multiplex the antennas to the RF module or interrogation unit. Generally switches are used to connect the antennas to the RF Module. Due to low power losses and the high reliability associated with power MOS FETs, power MOS FETs are generally the switch of choice. Power MOS FETs, however, have the disadvantage that a parasitic anti-parallel diode exists across the drain to source pins of the FETs while the device is not conducting. The anti-parallel diode is automatically generated in the production of the Power MOS FETs and manifests itself as a P-N junction barrier in the silicon substrate of the MOS FET. The disadvantageous characteristics of the diode are the conducting and non-conducting features of the diode upon proper application of voltage applied across the diode, such that the diodes enhance conduction of the MOS FETs when the MOS FETs are not conducting.

Current solutions to the diode behavior exhibited by the Power MOS FETs during non-conduction are to connect anti-serial MOS FETs across the drain to source pins of the MOS FETs. Anti-serial connection of the MOSFETs is shown in Figure 1, where the two MOS FETs are connected in series, but the second MOS FET is reversed (anti-serial) such that the order of the MOS FET pins is drain1 - source1 - source2 - drain2. Anti-serial connection of the MOS FETs creates anti-serial connection of the parasitic diodes as well and therefore the cathode of the parasitic diode always appears at the drain pin of the MOS FET, and the anode of the parasitic diode exists at the source pin of the MOS FET, resulting in only one parasitic diode in con-

duction at a time. However, connecting MOSFETs anti-serial creates the additional requirement of having to use a driver circuit, to operate the gate pin of the power MOSFETs, which is not referenced to ground, or is floating, as shown in Figure 1. This greatly increases the cost of the Multiplexer and transceiver system due to the expensive nature of the floating driver circuit. A floating driver circuit is expensive and not commonly used, because it is not referenced to ground. Unable to reference a signal to ground, the floating driver circuit requires the use of a transformer to galvanically separate the digital control signals from the driver circuit for each channel. The transformer must also withstand high voltages which also makes it more expensive. In conclusion, the additional MOSFETs used to solve the parasitic diode problem, created a much more significant cost and feasibility burden.

SUMMARY OF THE INVENTION

A preferred embodiment of the invention overcomes the disadvantage of the parasitic diode by connecting the power MOS FET to the antenna via a serially connected capacitor. Thus, in a disabled channel, the serially connected capacitor may be charged up to the peak positive D.C. voltage of the antenna resonator circuit of the enabled channel, via the parasitic diode. The capacitor in the disabled channel is charged via the parasitic diode while a different transmit channel has been selected and when the antenna resonator of that different channel, builds up the antenna resonance voltage. Once the voltage at the antenna resonator is at the maximum, the capacitor in the disabled channel is also charged up to the maximum voltage and therefore, the antenna resonance voltage of the enabled channel minus the stored voltage of the disabled channel capacitor will never be less than zero. In conclusion, because the drain of the FET is held to a positive voltage, and the parasitic diode needs a negative voltage to conduct, the parasitic voltage stops conducting and will not conduct while the capacitor is charged to that positive voltage. Therefore, the FET is blocked to negative voltages.

The disabled MOS FET is also blocked for positive voltages because that is the basic function of the MOS FET switch. The parasitic diode is not conducting in this situation, because the diode is reversed biased in this case and therefore needs a negative voltage to conduct.

One advantage of this invention is a replacement of the excessive number of expensive additional components previously necessary to solve the parasitic diode problem with fewer significantly less expensive components.

A second advantage of this configuration is the ease in implementation and facilitation of the new improved solution.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be explained in greater detail with reference to an example of an embodiment shown in the drawings, in which:

Figure 1 is schematic of a multiplex configuration showing the floating gate driver circuit characteristic generated.

Figure 2 is a schematic of the multiplex configuration according to a preferred embodiment according to the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A preferred embodiment of the invention is shown in Figure 2. In Figure 2, the Transmit/Receive (Tx/Rx) Multiplexed parts of the Radio Frequency (RF) module which are necessary to describe the invention are shown. A two channel multiplexed is shown. Channel 1 consists of antenna 1,10, capacitor 14, and transistor 18. Channel 2 consists of antenna 2,12, capacitor 16, and transistor 20. Each channel is connected to a different port of logic circuit 22. In addition, both channels are connected to the resonant circuit 24 of the transmitter stage.

In operation, assume that the RF Module's transmitter is now switched on and that channel 1 of the TX/RX multiplexed is selected i.e. enabled. Transistor 18 is conducting and transistor 20 is switched off or not conducting. Although transistor 20 is not conducting, the parasitic diode across the drain-source pins of transistor 20 is present and conducting for negative voltages. Even in more detail, when the RF Module's transmitter is switched on, the first positive sine halfwave is coupled to antenna resonator 24. For the positive half of the sinewave, no problem exists for the non-conducting transistor 20, because the parasitic diode will only conduct for negative voltages. Therefore, the problem exists upon the coupling of the negative half of the sinewave to antenna resonator 24. During the negative half of the sinewave, transistor 20 is conducting via the parasitic diode across the drain to source pins of transistor 20. Due to the parasitic diode phenomena, effectively, there are two antennas connected in parallel to the antenna resonator 24. This in turn detunes resonator 24 and inhibits antenna resonator's 24 ability to generate the high voltages necessary to charge up the transponder.

Without the series capacitors 14,16, the above-mentioned result is effected.

However, with the series capacitors 14,16 in place as shown in Figure 2, while channel 1 is selected and transistor 18 is conducting, the capacitor 16 is charged up to the peak voltage of the antenna resonator 24 via the parasitic diode across transistor 20. The polarity of the voltage charged onto capacitor 16 is positive with

respect to the ground of antenna 2,12 (which is also at the same potential as the source pin of the MOSFET). Therefore, the source pin of transistor 20 is at a positive potential due to the voltage at the antenna resonator 24 plus the positive voltage charged onto capacitor 16 and therefore transistor 20 will not conduct via the parasitic diode.

A few preferred embodiments have been described in detail hereinabove. It is to be understood that the scope of the invention also comprehends embodiments different from those described, yet within the scope of the claims.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

Claims

1. A multiplex system for connecting more than one antenna to a transmitter/receiver comprising:
 - control circuitry for selecting an antenna resonator via enabling and disabling circuitry;
 - more than one antenna resonator for transmission of a charge-up pulse to a transponder in dependence upon being selected via said control circuitry and upon reaching a maximum resonator voltage;
 - a transmitter for charging up a selected antenna resonator to said maximum resonator voltage;
 - a switch circuit, connected to said antenna resonator, for conducting when enabled via said control circuit, and not conducting when disabled via said control circuit;
 - at least one serially connected capacitor corresponding to each of said switch circuits, for storing substantially said maximum resonator voltage, in dependence upon said corresponding switch circuit being disabled.
2. The system of Claim 1, wherein said switch circuit is a MOS FET circuit.
3. The system of Claim 2, wherein said MOS FET circuitry has a gate and wherein further said control circuit controls the voltage on said gate of said MOS FET circuitry.
4. The system of Claim 1, wherein said at least one serially connected capacitor is a parallel combination of two capacitors.

5. The system of Claim 1, wherein said at least one serially connected capacitor is connected in between said antenna resonator and said switch circuitry.

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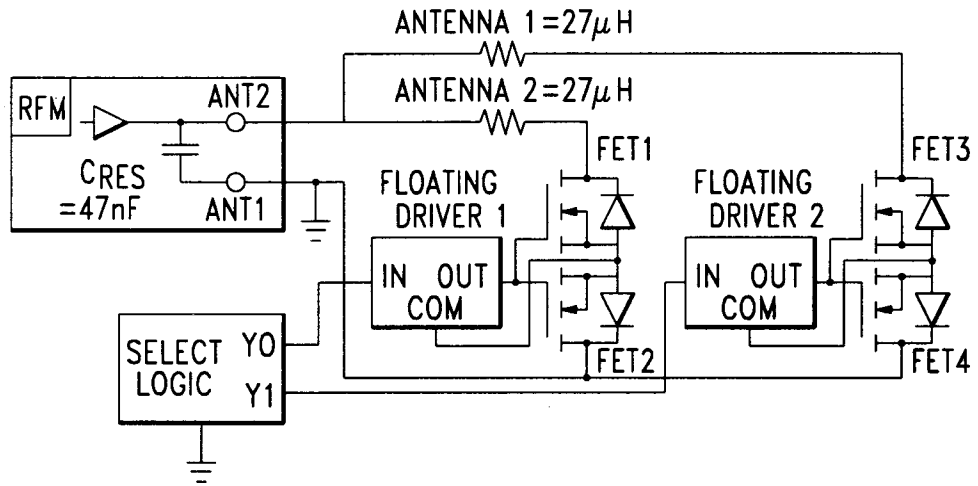


Fig. 1 PRIOR ART

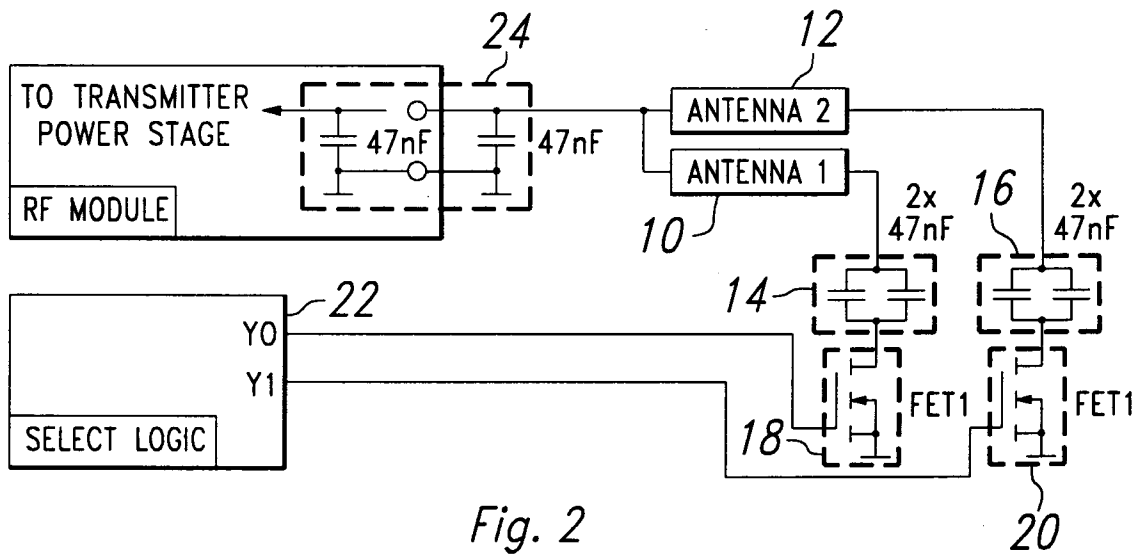


Fig. 2