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Section 29

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PATENT REQUEST: STANDARD PATENT/PATENT OF ADDITION

We, being the person(s) identified below as the Applicant, request the grant of a patent to the person identified below as the Nominated Person, for an invention described in the accompanying standard complete specification.
Full application details follow.

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(54) Invention Title - "LOGICAL MACHINE FOR PROCESSING CONTROL INFORMATION OF TELECOMMUNICATION TRANSMISSION FRAMES"

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(60) Application Number(s) and Date(s)

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Drawing number recommended to accompany the abstract.. ..

ALCATEL N.V.

(Signature)

December 15th, 1992

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Section 29(1)
Regulation 3.1(2)

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NOTICE OF ENTITLEMENT

We, ALCATEL N.V.
of Strawinskylaan 341, 1077 xx Amsterdam, The Netherlands,
being the applicant in respect of Application No.
for an invention entitled "LOGICAL MACHINE FOR PROCESSING CONTROL INFORMATION OF TELECOMMUNICATION TRANSMISSION FRAMES"
described in the accompanying specification, state the following:

1. The company nominated for the grant of the patent has entitlement from the actual inventor by mesne assignment.

2. The company nominated for the grant of the patent has entitlement from the applicant of the basic application listed on the patent request form by assignment.

3. The basic application listed on the request form is the first application made in a Convention country in respect of the invention.

ALCATEL N.V.

December 15th, 1992

B. O'CONNOR

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LOGICAL MACHINE FOR PROCESSING CONTROL INFORMATION OF TELECOMMUNICATION TRANSMISSION FRAMES

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(57) Claim

1. A logical machine operating according to a predetermined state diagram wherein state transitions are performed as a function of concatenation information carried by telecommunication transmission frames, said frames carrying also data information and pointer informationwhich is indicative of the location of said data information in said frames, said concatenation information being indicative of the structure of said data information in said frames and being repeated in a same frame, wherein said logical machine performs said state transitions in said predetermined state diagram as a function of, simultaneously, all the concatenation informations of said transmission frame.

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Regulation 3.2

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ORIGINAL
COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

"LOGICAL MACHINE FOR PROCESSING CONTROL INFORMATION OF TELECOMMUNICATION TRANSMISSION FRAMES"

The following statement is a full description of this invention, including the best method of performing it known to us:-

This invention relates to a logical machine operating according to a predetermined state diagram wherein state transitions are performed as a function of concatenation information carried by telecommunication transmission frames, said frames carrying also data information and pointer information which is indicative of the location of said data information in said frames, said concatenation information being indicative of the structure of said data information in said frames and being repeated in a same frame.

Such a telecommunication transmission frame is for instance the so-called Synchronous Transport Module (STM) frame STM-4c used in the Synchronous Digital Hierarchy(SDH) protocol and standardised according to the CCITT Recommendations G.707, G.708 and G.709. This frame STM-4c includes a control field storing the pointer information and the repeated concatenation information, and a data field storing a single user data block, or at least a first part thereof. The pointer information indicates the start location of the data block, whilst the concatenation information indicates that the data information is constituted by a single block.

Another type of frame is the frame STM-4, also standardised according to the CCITT Recommendations G.707,G.708 and G.709, and wherein the control field stores four distinct pointer informations but no concatenation information. The data field of the frame STM-4 stores four byte-interleaved user data blocks which are thus each four times smaller than the single data block of the frame STM-4c and of which the start locations in the frame are given by respective ones of the four pointer informations.

The control field of the frame STM-4 differs from that of the frame STM-4c in that in the latter the locations of the three last pointer information are filled with three identical concatenation informations.

According to Annex B (pages 53 to 55) of the CCITT Recommendation G.783, a concatenation information as wellas a pointer information are processed by a logical machine according to a first and a second state diagrams respectively. A logical machine operating according to four identical second state diagrams in function of the pointer informations is for instance required to process the four pointer informations of the frame STM-4.

Based on the teaching of the pointer processing of a frame STM-4, a logical machine performing the state transitions of one second state diagram and of three first state diagrams should also be necessary to process the single pointer information and the three concatenation informations of the frame STM-4c respectively.

Such a logical machine is relatively expensive and occupies a relatively large surface when integrated on an electronic chip.

An object of the present invention is to provide a logical machine of the above known type, but which allows to process the information of the control field of the frame STM-4c in a more efficient way while using relatively little surface on the chip.

According to the present invention, there is provided a logical machine of the aforementioned type, wherein said logical machine performs said state transitions in said predetermined state diagram in function of, simultaneously, all the concatenation informations of said transmission frame.

In this way, the first state diagram according to the above CCITT Recommendations is used as predetermined state diagram for the processing of the three concatenation informations of each frame STM-4c.

Preferably, said repeated concatenation informations are considered as a single word of control information by said logical machine.

By handling simultaneously the three identical concatenation informations as a single word of control information, the logical machine operates only according to one state diagram, namely the first state diagram, instead of three as mentioned above. This more efficient way of processing also leads to a reduction of the surface occupied by the logical machine on the chip.

A further object of the present invention is to make the logical machine even more efficient and to reduce even more the surface occupied on the chip.

According to a further aspect of the present invention, this further object is achieved by processing pointer information according to a second predetermined state diagram which comprises substantially identical states and similar state transitions than these of the first mentioned state diagram so that a single predetermined state diagram may be derived from both said first and second predetermined state diagrams, and that said logical machine performs state transitions according to said single predetermined state diagram in function of,simultaneously, both said pointer information and said concatenation information.

This is the case of the frame STM-4c wherefore the first state diagram of the concatenation information and the second state diagram of the pointer information both have states "NORMal pointer", "Loss Of Pointer" and"Alarm Indication Signal" and corresponding state transitions, as will be explained in more detail later.

Preferably, both said pointer information and said repeated concatenation informations are considered as a single word of control information by said logical machine.

The solution proposed in the present invention has the advantage of using little hardware concentrating all the processing in the single state diagram. Moreover, by concentrating the necessary intelligence in this single state diagram, the pointer/concatenation information is processed very simply, i.e. any possible overhead in either complexity or chip area, incurred by processing the different parts of this information separately is avoided.

Preferably, said logical machine checks whether said concatenation information differs from a predetermined bit sequence indicating said data structure, in which case an error indication is generated and said logical machine simultaneously checks said pointer information according to predetermined rules.

In this way the logical machine with the abovementioned advantageous features is specifically used for recognizing a frame STM-4c. Indeed, the bytes forming the concatenation information should then equal the predetermined bit sequence. As mentioned earlier this is moreover done simultaneously taking into account the pointer information according to predetermined rules.

Preferably, said logical machine detects errors in any part of said single word of control information and changes the state of said single predetermined state diagram to a loss of pointer state (LOP) when said errors are detected in a predetermined number (8) of consecutive ones of said transmission frames.

In so doing any error in the single word processed by the logical machine is taken into account for reaching a predetermined number of consecutive errors irrespective of the fact in which part of the single word this error occurred.

Preferably, said predetermined state diagram includes the state transitions of:

- changing from a loss of pointer state (LOP) to a normal pointer state (NORM) when said control information is correct in X consecutive frames;
- changing from either said loss of pointer state (LOP) or said normal pointer state (NORM) to an alarm indication signal state (AIS) if said control information is in Y consecutive frames equal to an alarm indication (AIS_IND), said alarm indication (AIS_IND) being a word having a predetermined bit pattern; and
- changing from said normal pointer state (NORM) to said loss of pointer state (LOP) when an invalid pointer (INVALID_A_P) is detected in Z consecutive frames, said invalid pointer being detected when said control information is not correct and is different from said alarm indication (AIS_IND).

It can be verified that as long as the three concatenation informations are correct, i.e. that they are equal to a predetermined bit sequence, the single state

diagram behaves as the second state diagram mentioned above, i.e. in function of the pointer information. Additionally, when at least one of the concatenation informations is incorrect the single state diagram deviates from the behaviour of this second state diagram in that ittakes also into account the concatenation informations forming part of the single word. In conclusion it may be said that the single state diagram maintains a suitable performance regarding the processing of the pointer information, simultaneously checking the concatenation informations, while only introducing a little overhead with respect to the above second state diagram.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawing which shows a state diagram to be executed by a logical machine according to the present invention.

This logical machine operates on control information of telecommunication transmission frames and according to the state diagram shown.

The telecommunication transmission frame is the so-called Synchronous Transport Module (STM) frame STM-4c used in the Synchronous Digital Hierarchy (SDH) protocol and standardised according to the CCITT Recommendations G.707, G.708 and G.709. The frame STM-4c includes a control field also called Administrative Unit OverHead AUOH and storing the control information which includes a pointer information and three identical concatenation informations, and a data field which stores a single user data block, or at least a part thereof. The pointe rinformation indicates the start location of the data block in the frame, whilst the concatenation information indicates that the data information is contained in a single data block, i.e. indicates the structure of the data information in the data field.

The frame STM-4c carries multiplexed data information at a transmission rate of 622 Mbit/s.

The SDH protocol multiplexes data information, and control information, needed for supervisory and other functions, in standardised blocks and puts them respectively in the data field and partly in the control field AUOH which occupy predetermined locations in the frame. However, the data block is not restricted to be multiplexed in a single frame and its place in the bitstream is only determined by a pointer value indicating, relatively to the location of this pointer, the start location of the data block in the frame. As the length of the part of the data block stored in the data field of a particular frame is not fixed since its start location may vary, this data block may cross

the boundaries of the data field of the frame to which it belongs and its end location may therefore be in the data field of the next frame to be transmitted or received.

It is to be noted that there exists another Synchronous Transport Module frame STM-4 also standardised by the above CCITT Recommendations. This frame STM-4 differs from the frame STM-4c in that the control field AUOH thereof stores four distinct pointers instead of one pointer and three concatenation informations and that the data field is able to store four data blocks which are byte interleaved and of which the lengths are obviously four times shorter than that of the data block which can be stored in the frame STM-4c. The four different pointers of the frame STM-4 are pointing to the start locations of four different data blocks or containers carrying the data information of four different sources respectively.

By comparing these two frames, one can see that the locations occupied, in the frame STM-4, by the three further pointers correspond, in the frame STM-4c, to the three concatenation informations. These three concatenation informations are identical and should equal a standardised bit sequence to be correct. As a consequence, they may be used for distinguishing a frame STM-4c from a frame STM-4 whereby the validity of the received frames, either STM-4cor STM-4, can be continuously checked.

Referring again to the frame STM-4c and according to the Annex B, pages 53 to 55, of the CCITT Recommendation G.783, a logical machine is to be provided for processing the pointer and the concatenation informations of each frame according to well defined and respective state diagrams. However, since the three concatenationinformations stored in the control field AUOH of a frameSTM-4c are identical, the logical machine according to the present invention will process these three informations simultaneously. In more detail, instead of processing three times the same concatenation information, the logical machine will take the three concatenation informations as a single word and use this single word only once in the state diagram of the concatenation information. Moreover, owing to similitudes between the states and between the state transitions in the state diagrams of both the pointer information and the concatenation informations, the logical machine will process the control field AUOH of a frame STM-4c according to a single state diagram in function of a single word constituted by the three concatenation informations and the pointer information. This single state diagram has the same states and similar state transitions as the above two state diagrams of the pointer information and the concatenation information respectively.This logical machine will be described in more detail below.

The control field AUOH of the frame STM-4c is received serially at an input of

the logical machine and has the following byte sequence:

H A A A S S S S S S S S L B B B S S S S S S S S

wherein each H, A, S, L and B represents a byte.

This byte sequence contains first and second pointer bytes H and L forming together the aforementioned pointer information, three concatenation informations each built-up of first and second concatenation bytes A and B, the combination AB forming one concatenation information, and stuffed bytes S which are irrelevant for further processing in the present logical machine.

The HL bytes, also called H1H2 bytes in the CCITT Recommendations, of the pointer have the following bits equence:

H	L
[*nnnnssID*]	[*IDIDIDID*]

wherein:

- n n n n : is a so-called New Data Flag NDF which is said to be enabled when it has the value 1 0 0 1, and disabled or normal when it has the value 0 1 1 0. It is to be noted that in this case of pointer information it is sufficient that three of the four NDF bits match with 1 0 0 1 for enabling the NDF;
- s s : are so-called "ss" bits which are said to be correct when they have the value 1 0;
- I : are increment bits;
- D : are decrement bits; and
- I D I D I D I D : is a pointer value which is valid when it is in a predetermined range from 0 to 782.

The AB bytes of each concatenation information havethe following bit sequence:

A	B
[*nnnnxx*11]	[11111111]

wherein:

- n n n n : is the above new data flag NDF which has to be enabled for validating the concatenation information;
- x x : are non relevant bits for the present application; and
- the remaining bits all have the binary value 1 for indicating that the concatenation information is correct, i.e. that a frame STM-4c is received.

The logical machine discards the stuffed bytes S and forms a single word H A A A L B B B which is processed according to the state diagram shown in the drawing

and which will be described hereafter.

It is to be noted that in the following part of thedescription, the names and symbols used correspondgenerally to those defined in the above CCITT Recommendations.

The state diagram comprises three states:

- a NORMal pointer state "NORM";
- a Loss Of Pointer state "LOP"; and
- an Alarm Indication Signal state "AIS".

In these states, the word "pointer" refers to theabove single word constituted by the pointer information and the three concatenation informations, whereas thelogical machine latches a current pointer which indicatesthe current start location of the data block in the frame STM-4c.

State transitions linking these states may be generated when a following type of single word is received one or more consecutive times, i.e. during one or during consecutive frames, in the logical machine:

- a NORMAL Arriving Pointer "NORMAL_A_P";
- a New Data Flag ENABLE "NDF_ENABLE";
- an Alarm Indication Signal "AIS_IND";
- an INCRement INDication "INCR_IND";
- a DECRement INDication "DECR_IND"; and
- an INVALID Arriving Pointer "INVALID_A_P".

In more detail, a normal arriving pointer NORMAL_A_Pis considered to be received when the new data flag NDF is disabled, the ss bits are correct, the received pointer value is in the predetermined range and the three concatenation informations are correct.

A new data flag enable NDF_ENABLE is considered tobe received when the NDF is enabled, the ss bits arecorrect, the received pointer value is in the predetermined range, and the three concatenation informations arecorrect.

An alarm indication signal AIS_IND is considered to be received when the control information, i.e. the single word H A A A L B B B, contains only binary ones (1).

An increment/decrement indication INCR_IND/DECR_INDis considered to be received when the NDF is disabled, the ss bits are correct, a majority of I/D-bits is inverted, a majority of D/I-bits is not inverted, a previousINCR_IND/DECR_IND or NDF_ENABLE has occurred more than three frames ago and the three concatenation informations are correct respectively. A majority of, e.g., I-bits is said inverted when at

least three I-bits of the five are inverted with respect to the I-bits received in the previous frame.

Finally, an invalid arriving pointer INVALID_A_P isconsidered to be received for any other than the above defined single words or for a NORMAL_A_P for which the received pointer value is not equal to the current pointer.

In the present logical machine the following state transitions may occur:

* from the normal pointer state NORM to this same normal pointer state NORM when:

- one increment/decrement indication INCR_IND/DECR_IND is received: the new current pointer is then equal to the previous current pointer +/- 1, modulo 782;

- 3 identical normal arriving pointers 3xNORMAL_A_P are received in three consecutive frames: the new current pointer is then equal to the received pointer value;

or

- one new data flag enable NDF_ENABLE is received: the new current pointer is equal to the received pointer value;

* from the normal pointer state NORM to the loss of pointer state LOP when:

- N invalid arriving pointers NxINVALID_A_P are received in N consecutive frames; or

- N new data flag enable NxNDF_ENABLE are received in N consecutive frames;

* from the loss of pointer state LOP to the normal pointer state NORM when:

- 3 identical normal arriving pointers 3xNORMAL_A_P are received in three consecutive frames: the new current pointer is then equal to the received pointer value;

* from the normal pointer state NORM to the alarm indication signal state AIS when:

- 3 alarm indication signals 3xAIS_IND are received in three consecutive frames;

and

* from the alarm indication signal state AIS to the normal pointer state NORM when:

- 3 identical normal arriving pointers 3xNORMAL_A_P are received in three consecutive frames: the new current pointer is then equal to the received pointer value;

or

- one new data flag enable NDF_ENABLE is received: the new current pointer is then equal to the received pointer value;

* from the loss of pointer state LOP to the alarm indication signal state AIS when:

- 3 alarm indication signals 3xAIS_IND are received in three consecutive frames;

and

* from the alarm indication signal state AIS to the loss of pointer state LOP when:

- N invalid arriving pointers NxINVALID_A_P are received in N consecutive frames.

In the above, N is an integer of which the value iscomprised between 8 and 10. When the logical machine is in the state LOP, the current pointer is undefined and an indication is given to a maintenance device (not shown) and the data informationof the frame is discarded. Similarly, when the logicalmachine is in the state AIS, an alarm is indicated to themaintenance device and the data information of the frame isdiscarded.

The above logical machine reacts to the contents ofthe control information of the frame STM-4c in almost thesame way as a logical machine for the frame STM-4 reacts tothe contents of each of the four pointers of that frame,except that the extra demand for the correctness of theconcatenation informations is now checked simultaneously.The overhead introduced by checking these concatenationinformations is thus minimal with regards to chip area and circuit complexity. Indeed, in the present logical machineonly the four single words NORMAL_A_P, NDF_ENABLE, INCR_INDand DECR_IND are, with respect to their definitions given for a pointer only, redefined to take into account the three concatenation informations.

It is to be noted that another embodiment of thepresent logical machine could equally well be used in thecase of mixed frames STM-4 and STM-4c over a same transmission link. This logical machine should then for instance process the first pointer, i.e. the most left pointer in the control field, simultaneously with the other bytes of the single word, i.e. the above AB bytes, and thereby make a distinction between a frame STM-4c and aframe STM-4. From the above description, it will be relatively simple to realize such a variant of the presentlogical machine and the latter will therefore not bedescribed in more detail.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

The claims defining the invention are as follows:

1. A logical machine operating according to a predetermined state diagram wherein state transitions are performed as a function of concatenation information carried by telecommunication transmission frames, said frames carrying also data information and pointer informationwhich is indicative of the location of said data information in said frames, said concatenation information being indicative of the structure of said data information in said frames and being repeated in a same frame, wherein said logical machine performs said state transitions in said predetermined state diagram as a function of, simultaneously, all the concatenation informations of said transmission frame.

2. A logical machine as claimed in claim 1,wherein said repeated concatenationinformations are considered as a single word of control information by said logical machine.

3. A logical machine as claimed in claim 1,wherein said pointer information is processed as claimed in a second predetermined state diagram which comprises substantially identical states and similar state transitions than these of the first mentioned state diagram so that a single predetermined state diagram may be derived from both said first and second predetermined state diagrams, and that said logical machine performs state transitions according to said single predetermined state diagram as a function of, simultaneously, both said pointer information and said concatenation information.

4. A logical machine as claimed in claim 3, wherein both said pointer information and said repeated concatenation informations are considered as a single word of control information by said logical machine.

5. A logical machine as claimed in claim 3, wherein said logical machine checks whether said concatenation information differs from a predetermined bit sequence indicating said data structure, in which case an error indication is generated and said logical machine simultaneously checks said pointer information according to predetermined rules.

6. A logical machine as claimed in claim 4, wherein said logical machine detects errors in any part of said single word of control information and changes the state of said single predetermined state diagram to a loss of pointer state when said errors are detected in a predetermined number of consecutive ones of said transmission frames.

7. A logical machine as claimed in claim 4, wherein said single predetermined state diagram includes the state transitions of·

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- changing from a loss of pointer state to a normal pointer state when said control information is correct in X consecutive frames;

- changing from either said loss of pointer state or said normal pointer state to an alarm indication signal state if said control information is in Y consecutive frames equal to an alarm indication, said alarm indication being a word having a predetermined bit pattern; and

- changing from said normal pointer state to said loss of pointer state when an invalid pointer is detected in Z consecutive frames, said invalid pointer being detected when said control information is not correct and is different from said alarm indication.

8. A logical machine as claimed in claim 7,wherein X is an integer equal to 3, Y is an integer equal to 3 and Z is an integer comprised between 8 and 10.

9. A logical machine as claimed in claim 4,wherein said single predetermined state diagram includes the state transitions of:

- changing from said alarm indication signal state to said normal pointer state when said control information is correct in P consecutive frames; and

- changing from said alarm indication signal state to said loss of pointer state when an invalid pointer is detected in Q consecutive frames.

10. A logical machine as claimed in claim 9, wherein P is an integer equal to 3 and Q is an integer comprised between 8 and 10.

11. A logical machine as claimed in the claims 7 or 9, wherein said telecommunication transmission frames are transmitted as claimed in the Synchronous Digital Hierarchy protocol and have a structure according to the Synchronous Transport Module STM-4c of the CCITT Recommendation G.709, and that said single word of control information contains one pointer information and three concatenation informations.

12. A logical machine as claimed in claim 11,wherein said control information is interpreted as:

- a normal arriving pointer when the new data flag is disabled, the "ss" bits are correct, the received pointer value is in a predetermined range and the three concatenation informations are correct;

- a new data flag enable when the new data flag is enabled, the "ss" bits are correct, the received pointer value is in said predetermined range, and the three concatenation informations are correct;

- an alarm indication signal when said control information contains only binary ones;

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- an increment/decrement indication when the new data flag is disabled, the "ss" bits are correct, a majority of "I-bits"/"D-bits" is inverted, a majority of "D-bits"/"I-bits" is not inverted, a previous increment/ decrement indication or new data flag enable has occurred more than three frames ago and the three concatenation informations are correct; and

- an invalid arriving pointer for any other than the above defined control information or for a normal arriving pointer with a received pointer value which is not equal to the current pointer; and that said single predetermined state diagram includes the following state transitions:

* from the normal pointer state to the same normal pointer state for:

- an increment/decrement indication, the new current pointer becomes then equal to the previous current pointer +/- 1, modulo 782;

- 3 normal arriving pointers, when three identical normal arriving pointers are received in three consecutive frames, the new current pointer being equal to the received pointer value; and

- a new data flag enable, when the new data flag is enabled, the new current pointer becomes equal to the received pointer value;

* from the normal pointer state to the loss of pointer state for:

- N invalid arriving pointers, when an invalid pointer information is received in N consecutive frames; and

- N new data flag enable, when the new data flag is enabled during N consecutive frames;

* from the normal pointer state to the alarm indication signal state for:

- 3 alarm indication signals, when an alarm indication signal is received in three consecutive frames;

* from the loss of pointer state to the normal pointer state for:

- 3 normal arriving pointers;

* from the loss of pointer state to the alarm indication signal state for:

- 3 alarm indication signals;

* from the alarm indication signal state to the normal pointer state for:

- 3 normal arriving pointers; and

- a new data flag enable; and

* from the alarm indication signal state to the loss of pointer state for:

- N invalid arriving pointers.

13. A logical machine as claimed in claim 12, wherein N is an integer between 8 and

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10.

14. A logical machine as claimed in any one of the preceding claims, integrated on an electronic chip.

15. A logical machine substantially as herein described with reference to the figure of the accompanying drawing.

DATED THIS SEVENTH DAY OF DECEMBER 1994

ALCATEL N. V.

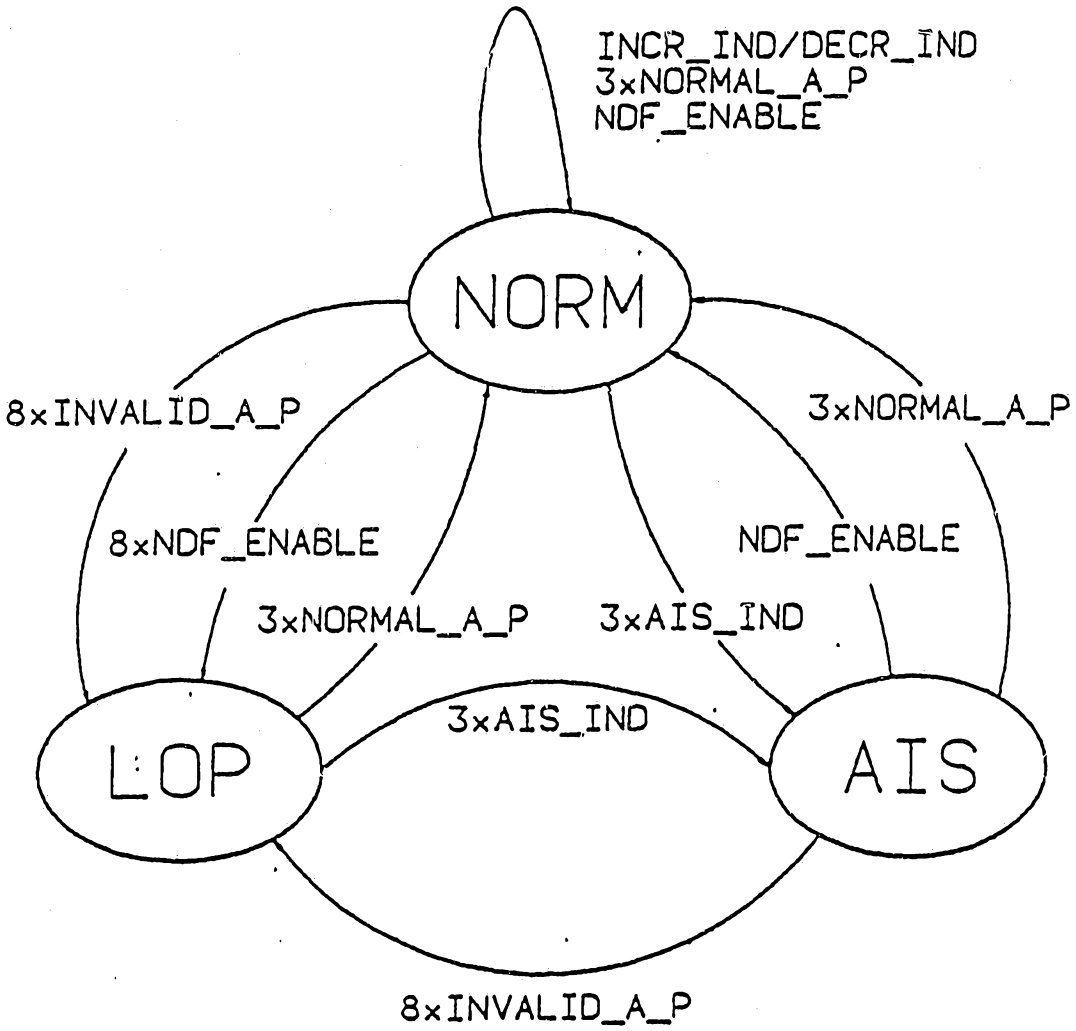
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ABSTRACT

A logical machine for processing SynchronousTransport Module (STM) frames STM-4c transmitted as claimed in the Synchronous Digital Hierarchy (SDH) protocol. Each frame STM-4c carries data information and control information which includes a pointer information and concatenation informations. The pointer information indicates the start location of the data information in the frame and the concatenation informations indicate the structure of this data information.

The logical machine is relatively simple since it operates as claimed in a single state diagram in function of a single word comprising both the pointer information and the concatenation informations of a same frame.

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INCR_IND/DECR_IND
3xNORMAL_A_P
NDF_ENABLE
NORM
8xINVALID_A_P
3xNORMAL_A_P
8xNDF_ENABLE
NDF_ENABLE
3xNORMAL_A_P
3xAIS_IND
3xAIS_IND
LOP
AIS
8xINVALID_A_P