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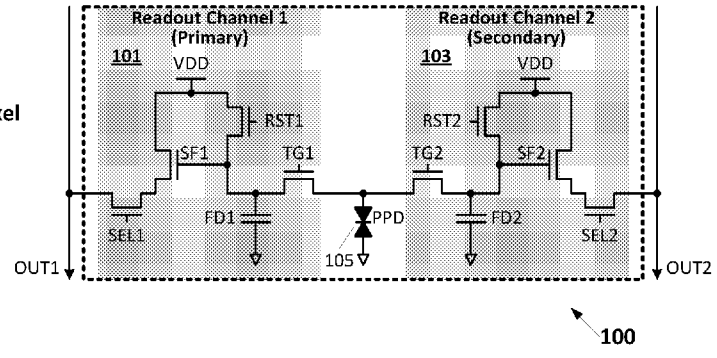
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(54) Title: SPLIT-READOUT IMAGE SENSOR

FIG. 1
Split-Readout Pixel



(57) **Abstract:** First and second readout circuits, each having a respective floating diffusion node, are coupled to a photodetection element within a pixel of an integrated-circuit image sensor. Following an exposure interval in which photocharge is accumulated within the photodetection element, a first portion of the accumulated photocharge is transferred from the photodetection element to the first floating diffusion node to enable generation of a first output signal within the first readout circuit, and a second portion of the accumulated photocharge is transferred from the photodetection element to the second floating diffusion node to enable generation of a second output signal within the second readout circuit. A digital pixel value is generated based on the first and second output signals.

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SPLIT-READOUT IMAGE SENSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application hereby claims priority to and incorporates by reference U.S. provisional application No. 62/721,183 filed August 22, 2018.

TECHNICAL FIELD

[0002] The disclosure herein relates to high dynamic range image sensors.

INTRODUCTION

[0003] Dynamic range in modern CMOS (complementary metal oxide semiconductor) image sensors is generally constrained by pixel full well capacity in bright light conditions and by input-referred read noise in low-light conditions. In 4-transistor (4T) pixels, input-referred read noise can be reduced by raising the conversion gain of the photocharge transfer from photodiode to floating diffusion read-out node – that is, reducing capacitance of the floating diffusion relative to the photodiode so that each transferred photocarrier (electron in an N-type MOS pixel implementation) yields a larger read-out voltage step. On the other hand, increasing conversion gain beyond a given point prevents complete photocharge transfer (the floating diffusion will reach its output voltage limit with fewer transferred electrons), reducing the effective full well capacity of the pixel and compromising bright light sensitivity.

DRAWINGS

[0004] The various embodiments disclosed herein are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0005] Figure 1 illustrates an embodiment of a split-readout pixel that enables high-conversion-gain readout without compromising the full photocharge transfer required for maximum bright light performance;

[0006] Figure 2 illustrates exemplary photocharge transfer operations within the split-readout pixel of Figure 1 under bright-light and low-light conditions;

[0007] Figure 3 illustrates an embodiment of an integrated-circuit imaging system having an array of split-readout pixels;

[0008] Figure 4 illustrates an alternative readout sequence that may be implemented by readout controller of Figure 3;

[0009] Figure 5 illustrates an alternative imaging IC architecture in which column readout logic is shared among multiple (or all) columns of split-readout pixels within a pixel array;

[0010] Figure 6 illustrates another imaging architecture in which a single-slope A/D converter is distributed across readout logic paths of multiple (or all) split-readout pixel columns within a pixel array;

[0011] Figure 7 illustrates exemplary pipelining of primary and secondary channel readouts, showing time-staggered primary channel correlated-double-sampling (CDS) operations and secondary channel CDS operations;

[0012] Figure 8 illustrates embodiments of per-column memory elements and read-merge logic that may be used to implement the memory and read-merge logic components shown in Figure 3;

[0013] Figure 9 illustrates an alternative read-merge logic embodiment that selectively zeroes the contribution of the secondary readout channel according to an under/over-threshold condition of the primary channel output;

[0014] Figure 10 illustrates an embodiment of a split-readout pixel having non-uniform primary and secondary readout-channel conversion gains and corresponding floating-diffusion node capacities that collectively match the photodiode full-well capacity;

[0015] Figure 11 illustrates a split-readout image sensor embodiment in which the primary-channel/secondary-channel designation within each pixel may be selectively and programmatically swapped according to a calibration-time noise assessment;

[0016] Figure 12 illustrates an embodiment of a split-readout pixel array in which the secondary readout channel for one pixel serves as the primary readout channel for an adjacent pixel -- a shared readout-channel arrangement that extends across the pixel array to maintain the total transistor count at or near that of a conventional single-readout-channel pixel array;

[0017] Figure 13 illustrates a channel multiplexing arrangement that may be implemented in the column-readout logic of an imager having a shared-channel split-readout pixel array per Figure 12;

[0018] Figure 14 illustrates an exemplary operation of channel multiplexers corresponding to those shown in Figure 13;

[0019] Figure 15 illustrates a portion of a split-readout pixel array having four shared readout channels per pixel; and

[0020] Figure 16 illustrates an exemplary channel multiplexing arrangement with respect to the four different channel readouts from each of the pixels within a given row of the Figure 15 pixel array.

DETAILED DESCRIPTION

[0021] Integrated-circuit image sensors having two or more readout channels per photodetection element – a primary readout channel and one or more secondary readout channels – are disclosed in various embodiments herein. In a number of embodiments, each of the readout channels coupled to the photodetection element includes a respective transfer gate/floating diffusion node pair and the primary readout channel, at least, has an exceptionally high conversion gain that enhances low-light sensitivity (extremely low input-referred noise) in exchange for photocharge transfer capacity below the full well capacity of the photodetection element. Readout via the one or more secondary readout channels drains any residual photocharge (after primary channel readout) from the photodetection element, effecting a combined primary/secondary channel photocharge transfer (and readout) up to the full well capacity of the photodetection element and thus maximizing bright-light sensitivity (and dynamic range). Accordingly, bright-light pixel readout is split into at least two phases: a phase-one readout via the primary channel in which a portion of the photodetector-accumulated charge is transferred to the primary-channel floating diffusion node to generate a primary readout signal, followed by a phase-two readout via the secondary channel readout in which the residual/remaining charge within the photodetector is transferred to the floating diffusion node of the secondary channel to generate a secondary readout signal. The split readout signals – primary and secondary – are combined before or after digitization to yield a composite readout signal corresponding to the total photocharge accumulated within the photodetector during a given exposure interval. In embodiments having multiple secondary readout channels, the primary readout signal is combined with two or more successively generated secondary readout signals to produce the composite readout signal. In other embodiments, the primary and/or secondary readout channels may be iteratively enabled to yield three or more readout signals that are combined to yield the composite readout signal (e.g., primary channel readout, secondary channel readout, and then another primary channel readout, etc.). In yet other embodiments, constituent operations within the primary channel readout and secondary channel readout are pipelined (executed in staggered but overlapping time intervals) to reduce multi-phase readout time, primary and secondary channels may be implemented with non-uniform conversion gains, channel-shared or non-shared analog-to-digital conversion circuitry may be implemented, conversion gain calibration operations are carried out to normalize constituent readout

signals/values prior to or as part of their combination into the composited output signal/value, readout channels are programmatically established as primary or secondary based on noise assessment (carried out at device startup or during device production) or other factors, and/or readout circuitry is shared between two or more split-readout (multi-readout-channel) pixels to reduce transistor count/increase fill-factor within the pixel array. These and other features and embodiments are described in greater detail below.

[0022] Figure 1 illustrates an embodiment of a split-readout pixel 100 that enables high-conversion-gain readout without compromising the full photocharge transfer required for maximum bright light performance and thus achieves higher dynamic range than conventional pixel architectures. Split-readout pixel 100 includes two readout channels, primary 101 and secondary 103, coupled to a photodetection element 105 – a pinned photodiode (PPD) in this example and others presented below, though any other practicable charge accumulating photodetector may be used in all cases. Except for possible differences in component sizing and physical layout, the primary and secondary readout channels are identically implemented with each channel including a respective transfer gate (TG1, TG2), floating diffusion node (FD1, FD2), source-follower transistor (SF1, SF2), reset transistor (RST1, RST2) and read-select transistor (SEL1, SEL2).

[0023] When operated in a deterministic readout mode, the primary readout channel and secondary readout channel are enabled in succession (i.e., after photocharge accumulation within photodiode 105 during an exposure interval) to produce primary and secondary output signals, respectively, on column output lines OUT1 and OUT2. Primary channel readout commences with a RST1 pulse (designations of transistors and their gate signals are used interchangeably herein) to reset floating diffusion FD1, and also with SEL1 assertion to couple the source terminal of the source-follower transistor (SF1) to output line OUT1 via the read-select transistor. Floating diffusion node FD1 is coupled to the gate of source-follower transistor SF1 which is biased (e.g., by a constant current source on column-output line OUT1) to drive a signal onto OUT1 that tracks (e.g., rises and falls in proportional to) the FD1 potential. Thus, after SEL1 assertion and RST pulse, the primary channel generates an output signal (on OUT1) corresponding to the reset potential of FD1 – a reset-state signal that, in a correlated double-sample (CDS) readout, is sampled by downstream readout circuitry to establish a baseline for subsequent readout signal generation. Shortly after FD1 reset, transfer gate TG1 is switched on (TG1 pulse) to enable photocharge transfer from the pinned photodiode to FD1 and thereby change the potential of the floating diffusion according to the number of transferred carriers

(electrons in the NMOS pixel implementation of Figure 1) multiplied by the voltage step per carrier, the latter being the conversion gain of the charge transfer operation.

[0024] In the Figure 1 implementation, primary channel 101 (at least) is implemented with an exceptionally high conversion gain (yielding correspondingly low input-referred noise that enables enhanced low-light sensitivity) at the cost of reduced photocharge transferability. That is, transfer of a photocharge quantum less than the full well capacity of photodiode 105 will drive FD1 to the photodiode pinning voltage (at which point charge transfer ceases) so that, under relatively bright-light conditions, a portion of accumulated photocharge will remain in the photodiode after primary channel readout. Said another way, the primary readout signal is driven to the same output limit for any photocharge accumulation beyond the quantum that drives FD1 to the photodiode pinning voltage – in effect hitting the capacity limit of the floating diffusion node – and thus lacks resolution at the bright end of the charge-accumulation range. An ensuing readout via the secondary channel avoids this loss of dynamic range, transferring the residual photocharge from photodiode 105 to floating diffusion node FD2 (after resetting FD2, switching on SEL2 and optionally reading the FD2 reset level) to yield a secondary readout signal that may be merged with the primary signal before or after digitization to produce a composite readout signal (or digital readout value) representative of total accumulated photocharge.

[0025] Figure 2 illustrates exemplary photocharge transfer operations within the split-readout pixel of Figure 1 under bright-light and low-light conditions (note that a high contrast scene may simultaneously expose some pixels to bright light and others to dim or no light). In the bright-light example, photocharge Q approaching the well capacity of the pinned photodiode is accumulated during an exposure interval (131) followed by primary and second readouts (139 and 147). In primary readout 139, photocharge is transferred with high conversion gain from the pinned photodiode to the primary-channel floating diffusion (FD1) until FD1 reaches the pinning potential of the photodiode, a point of equilibrium at which charge flow (current) ceases due to lack of electric field. In the depicted example, a number of carriers q1 are transferred to FD1 according to FD1's maximum output voltage swing, Vpin-Vrst1 (where Vrst1 is, for example, the VDD supply voltage less the threshold drop across transistor RST1), divided by the primary channel conversion gain (CG1), leaving q2 (=Q-q1) carriers within the photodiode. In secondary readout 147, the residual photocharge q2 is transferred to FD2, emptying the photodiode. In both the primary and secondary readouts, the floating diffusion nodes are reset prior to charge transfer with the reset-states thereof optionally read-out to enable correlated double sampling (CDS) with respect to the primary and secondary "charge-state" signals

generated respectively on OUT1 and OUT2 in response to the primary and secondary channel photocharge transfers. In any case, the primary and secondary channel readouts are merged in the digital or analog domain to yield a composite signal indicative of net photocharge accumulated within the photodiode during exposure interval 131.

[0026] Low-light exposure yields a much smaller photocharge accumulation – below the output-swing-limited capacity of (q1) of the primary channel floating diffusion node (FD1) so that the high-conversion-gain primary readout completely empties the pinned photodiode. In a number of embodiments, the secondary channel readout is skipped in this case, conserving power and, in some embodiments, reducing total readout latency. When the photocharge accumulation in the photodiode is lower than the q1 limit (the effective capacity of FD1), the entirety of the accumulated photocharge can be transferred to FD1 without any charge transfer lag induced by potential barriers or defects. Similarly, when the photocharge remaining within the photodiode after the transfer to FD1 is below the FD2 capacity that photocharge can be transferred to FD2 without charge transfer lag.

[0027] Although floating diffusion nodes FD1 and FD2 are implemented with nominally uniform (equal) capacities in the embodiment of Fig. 2, the two floating diffusion nodes and thus the primary and secondary readout channels are implemented with imbalanced (non-equal/non-uniform) but complementary conversion gains in alternative embodiments – an arrangement that raises the conversion gain of the primary readout channel to enable high performance low-light readout (high conversion gain, low input-referred noise) and correspondingly lowers the conversion gain of the secondary readout channel low to ensure that the combined primary-channel/secondary-channel charge transfer capacity matches (or nearly matches or exceeds) the photodiode full well capacity. Also, regardless of whether the two readout channels are implemented with nominally equal or complementary/imbalanced conversion gains, provision of two readout channels enables pipelined readout operations not possible with a single-channel implementation. For example, photocharge transfer may commence in the secondary readout channel shortly or immediately after photocharge transfer in the primary channel and thus without waiting for the primary readout signal to settle – avoiding a relatively long delay between primary and secondary charge-state readouts that might otherwise produce motion artifacts (i.e., objects in scene moving in interval between primary and secondary readouts) or other distortion. Additionally, in applications requiring high frame rate (rapid pixel array scan), single-channel readout may be implemented to reduce row readout time – for example, executing a readout only via the secondary readout channel (via FD2 and not via FD1) where that channel has a larger charge transfer limit or, in low light conditions, executing readout only

via the primary channel where that channel has a lower charge transfer limit and higher conversion gain.

[0028]

[0029] Figure 3 illustrates an embodiment of an integrated-circuit imaging system 160 (e.g., complementary MOS imager) having an array of split-readout (SR) pixels 161, readout controller 163 and readout logic 165 for a column-wise slice of the pixel array. As shown, readout logic 165 includes a channel multiplexer 171, analog gain element 173, analog-to-digital converter (ADC) 175, storage memory (or buffer) 177 and read-merge logic 179, all or most of which operate in response to control signals from readout controller 163 (the analog gain component optionally receives one or more gain control signals (GC) that may be used to alternate between gains for primary and secondary channel readout and/or provide calibration control for selected gains). The readout controller additionally outputs control signals to pixel array 161, including a transfer gate signal pair (one for each channel), read-select signal pair and reset signal pair for each pixel row to enable row-sequenced, column-parallel readout.

[0030] Still referring to Figure 3, channel multiplexer 171 sequentially feeds the primary and secondary output signals (Out1 and Out2) to the analog gain component in response to an alternating (toggling) channel-select signal (CS). In one embodiment, analog gain component 173 includes both a current source to bias the selected readout channel (i.e., enable source-follower operation within the readout channel as discussed above) and a voltage-mode or current-mode amplifier to amplify the readout signal in preparation for analog-to-digital (A/D) conversion within ADC 175. In alternative embodiments, the source-follower-bias current source may be implemented separately from the amplifier component of gain circuitry 173 or the amplifier component may be omitted (leaving only the source-follower-bias current source). Analog-to-digital converter 175 (ADC) may be implemented by a successive-approximation register (SAR), single-slope ADC (SSADC), sigma-delta ADC or any other practicable A/D conversion circuitry. Also, though not specifically shown, sample-and-hold circuitry may be provided within readout logic 165 (e.g., prior to the channel multiplexer, between the channel multiplexer and gain component, or between the gain component and analog-to-digital converter) to enable analog-signal sample and hold operation. The sample and hold circuitry may include a subtraction/differencing unit (also not shown) to enable analog-domain charge-state/reset-state signal correlation (i.e., by subtracting the reset-state sample from the corresponding charge-state sample) and thus feed a CDS sample to ADC 175. Alternatively, the reset-state signal and charge-state signal may be sequentially digitized by ADC175 and then differenced in the digital domain (digital CDS operation). In either case, a stream of digitized

CDS readout values are supplied to memory 177 for storage (i.e., triggered by a store-enable signal (SE) from readout controller) with successively stored primary and secondary readout values forwarded to read-merge logic for combination into a pixel output value 180 (triggered by merge-enable (ME) from readout controller).

[0031] In low-latency column readout implementations, respective (separate, dedicated) analog gain and ADC components may be provided for the primary and secondary readouts as shown at 185 to enable time-staggered, concurrent processing of the two readouts. Also, in embodiments (or configurations) that implement selective secondary channel readout, a threshold comparator 181 may be provided to signal an over-threshold condition OT (or under-threshold condition) to readout controller 163 and thus enable the readout controller to selectively generate (or refrain from generating) secondary channel readout control signals (RST2, SEL2, TG2). Though shown in the digital domain (after ADC), the threshold comparison may be implemented in the analog domain in alternative embodiments.

[0032] In the exemplary operational sequence shown at 200 (Figure 3), readout controller 163 commences split-channel readout at 201 by configuring channel multiplexer 171 to couple the primary channel output line to the downstream column readout circuitry (i.e., raising or lowering channel-select signal, CS, as the case may be). At 203, the readout controller deterministically asserts readout control signals, convert-enable signal (CE) and store-enable signal (SE) to enable primary channel readout (resetting the primary floating diffusion (FD) node, sampling the FD reset-state, enabling primary channel charge transfer and sampling the FD charge-state), A/D conversion of the primary readout signal and storage of the CDS primary readout value within memory 177 (with the reset-state/charge-state differential being effected in the analog domain prior to ADC or in the digital domain after). In a selective readout embodiment, the output of comparator 181 is evaluated at 205, with affirmative over-threshold determination (over-threshold signal OT asserted) triggering channel multiplexer switchover at 209, secondary channel readout, digitization and storage (211) and finally merger of the CDS primary and secondary readout values at 213. If the primary readout is determined not to exceed the two-phase readout threshold (negative determination at 205), secondary channel readout is skipped, and the CDS primary readout value is forwarded as the finalized pixel readout result (e.g., skipping the readout merge or merging the primary readout value with a null or zeroed secondary value). In a deterministic readout embodiment, the secondary readout operations at 209 and 211 are executed without condition (i.e., skipping assessment at 205), though a threshold evaluation of the primary readout and/or secondary readout may still be carried out to selectively merge the primary and secondary readout results (e.g., skipping the merge operation

at 213 if the primary readout is below a near-max threshold and/or if the secondary readout is below a noise-floor threshold). In any case, a row pointer is incremented (215) at readout completion to select a subsequent pixel row for readout in the next loop iteration.

[0033] Figure 4 illustrates an alternative readout sequence that may be implemented by readout controller 163 of Figure 3, for example, in a revised implementation or in response to a programmed readout policy setting. In this case, primary channel readout is executed in the operations at 231 and 233 (which correspond to the operations at 201 and 203 in the operational flow of Figure 3), followed by threshold evaluation at 235, flipping the channel multiplexer to enable alternate channel readout (i.e., the secondary channel in the first pass) and incrementing a readout counter (N) if the threshold evaluation indicates a readout channel saturation (i.e., that photocharge remains or likely remains in the photodiode after the preceding readout). After flipping the channel multiplexer (i.e., changing the state of the channel-select signal to select the alternate pixel readout channel) and incrementing the readout count, the readout (including digitization and result storage) and threshold evaluation operations at 233 and 235 are repeated with respect to the newly selected readout channel (the secondary readout channel in the second pass), with this readout loop continuing – alternating between the primary and secondary channel – until either a maximum readout count is reached (i.e., N reaches a predetermined maximum corresponding to a photocharge level at or above the full well capacity of the photodiode) or an under-threshold readout is detected (negative determination at 235). By this operation, pipelined low-latency readouts of the primary and secondary channels (which may be implemented with equal conversion gains for readout uniformity) may be executed iteratively (1, 2, 3, 4, …, or N=max individual channel readouts) to progressively drain photocharge from the photodiode via individual transfers (photodiode to floating diffusion node) with exceedingly high conversion gain and correspondingly low input-referred noise. Upon loop exit (negative determination at 235 or readout count reaching maximum), the multiple readouts (N readouts) are merged at 239 and then the row pointer is incremented at 241 to proceed to the next row. To provide deterministic readout timing (e.g., in a rolling shutter imager), a fixed time may be allotted to enable a predetermined number K of channel readouts per pixel row (i.e., with K=2 corresponding to the dual-channel readout shown in Figure 3), with one or more channel readout intervals unused in low-light exposures.

[0034] Figure 5 illustrates an alternative imaging IC architecture 260 in which column readout logic 261 is shared among multiple (or all) columns of split-readout pixels within pixel array 161. In the depicted embodiment a channel multiplexer receives primary and secondary readout signals from 'n' pixel columns and thus multiplexes 2n readout signals to a shared

readout path implemented generally as discussed in reference to Figure 3. The channel-select signal (CS) delivered to multiplexer 263 and other control signals generated by readout controller 265 (e.g., store-enable to memory 267) may be implemented by multi-bit signals as necessary to capture multi-channel pixel readout data for each of the n pixel columns.

[0035] Figure 6 illustrates another imaging architecture 300 in which a single-slope ADC 301 is distributed across readout logic paths of multiple (or all) split-readout pixel columns within pixel array 161. In the embodiment shown, a column-shared ramp generator 303 outputs digital and analog ramp signals (e.g., the digital ramp signal being a monotonic multi-bit count value and the analog ramp signal being a digital-to-analog conversion of that count value) to per-column register elements 305 and per-column comparators 307, respectively. Readout controller 309 operates all the split-readout pixels of a selected row in lock step so that the primary (and then secondary) readout signal for each pixel column is simultaneously routed (via channel multiplexer 171 and optional gain element 173) to a respective one of comparators 307. As the analog and digital ramp signals progress stepwise from minimum to maximum levels (the analog ramp may be a monotonically decreasing signal, with the maximum level being a less positive voltage than the minimum), the outputs of comparators 307 will transition as the analog ramp exceeds (e.g., falls below) the incoming readout signal, triggering capture of the corresponding digital ramp value (digital count) within register 305 as the A/D conversion result. In the single SSADC implementation of Figure 3, the ramp generator is restarted following primary channel A/D conversion (i.e., after the ramp outputs have progressed from minimum to maximum values and/or after all comparators/registers have been triggered and the ADC results transferred to downstream memory) to implement secondary channel A/D conversion and, in a digital CDS embodiment, may be restarted four-times per dual-channel readout to digitize the reset-state and charge-state readout signals for both channels. In embodiments having more than two readout channels per pixel (or in which two or more readout channels are iteratively enabled as in Figure 4) the SSADC operation may be completed as many times as necessary (up to the readout channel count or iteration limit) to digitize incoming readout signals. In digital CDS implementations, reset-state SSADC ramps may progress through a shorter range than charge-state SSADC ramps (i.e., in view of the much smaller range of valid reset-state signals) to reduce overall A/D conversion time.

[0036] Still referring to Figure 6, separate per-readout-channel SSADCs 301 may be provided in alternative embodiments to enable pipelined primary and secondary channel A/D conversion. For example, ramp generation for the primary channel SSADC may commence shortly after primary channel transfer (e.g., after a settling delay sufficient to yield stable

primary readout signals at the inputs of comparators 307) with ramp generation for the secondary channel SSADC commencing shortly thereafter – before the primary-channel ramp has completed so that the two time-staggered ramp generations overlap for at least part of their progression.

[0037] Figure 7 illustrates exemplary pipelining of primary and secondary channel readouts, showing time-staggered primary channel CDS operations (upper row) and secondary channel CDS operations (lower row). For ease of explanation, constituent floating-diffusion reset, reset-state sampling, charge transfer, charge-state sampling and ADC operations are shown as consuming identical time intervals (in reality the different operations may consume different amounts of time), with secondary channel operations being delayed relative to primary channel operations by the time allotted to a single operation. Thus, the primary channel floating diffusion node is reset at 341 followed by simultaneous (or at least concurrent) execution of primary-channel reset-state sampling 343 and secondary channel FD reset 344. Continuing this parallel, but time-staggered sequencing, primary-channel charge transfer is carried out at 345 concurrently with reset-state sampling in the secondary channel (346), followed by concurrent primary-channel charge-state sampling (347) and secondary-channel charge transfer (348), then concurrent primary channel A/D conversion (349) and secondary-channel charge-state sampling 350. The row-i split-channel readout is concluded (at least through A/D conversion) with the secondary-channel ADC operation at 352 (e.g., executed concurrently with the start of row i+1 readout – primary-channel FD reset). Note that the reset-state and charge-state sampling operations (343, 346, 347, 350) are shown as analog-domain sample-and-hold actions (which may include possible analog-domain subtraction of the reset-state sample from the charge-state sample). In other embodiments, those sampling operations may be carried out in the digital domain (direct A/D conversion of the output signals for a given readout channel without analog sample/hold). In any case, the pipelined primary and secondary channel readouts not only shorten the overall per-row readout latency (enabling more rapid row sequencing and thus shorter minimum exposure times, higher oversampling rates, etc.) but also shrink the time between primary and secondary charge transfer operations 345 and 348 relative to the time that would be required for successive rather than parallelized execution of the primary and secondary readout sequences, thus reducing likelihood of motion artifacts or other temporal distortion.

[0038] Figure 8 illustrates embodiments of per-column memory elements 361 and read-merge logic 363 that may be used to implement the memory and read-merge logic components shown in Figure 3. In the example shown, registers 367 and 369 are provided within memory 361 to store digitized primary and secondary readout values (e.g., CDS values), respectively,

with the stored readout values supplied to read-merge logic 363 for combination. Read-merge logic optionally applies gain calibration (gc1, gc2) or digital weighting (w1, w2) to the incoming readout values before summing those values (375) to produce a composite pixel value 180. In one embodiment, gain calibration values may be uniform across the split-pixel array (or relatively large sub-regions thereof) so that a relatively small number of calibration values and/or weight values may be applied to all or a large number of the pixel readouts, making on-die gain-calibration value and/or weight value storage readily feasible (i.e., storage on same die as split-readout pixel array). In other embodiments per-pixel (or per-pixel sub-group) gain calibration values and/or weight values may be stored in an off-die memory – for example, in an SRAM or DRAM storage within an IC stacked with (and interconnected to) the split-readout imager die to enable low power/low-latency gain-calibration value/weight value delivery to read-merge logic 363. Also, the gain-calibration values and/or weight values may be applied elsewhere in the column readout logic, including in the analog readout path (e.g., within analog gain component 173 shown in Figure 3).

[0039] Still referring to Figure 8, in the case of selective secondary channel readout (i.e., where secondary channel readout may be skipped if the primary channel readout yields an under-threshold signal or value), the readout value within register 369 may be zeroed to yield a zero secondary-readout contribution to summing element 375. In the embodiment shown in Figure 9 for example, an under/over-threshold comparison result (i.e., indicating an under-threshold or over-threshold primary readout) may be stored within memory 385 (i.e., within element 386) and applied within read-merge logic 387 to zero the secondary contribution. Though shown conceptually as a selection of a zero-value within multiplexer 388, secondary-channel contribution nulling may instead be implemented in various ways and at various points along the column-readout path (zeroing in register 369, zeroing the secondary-path gain-calibration and/or weighting multipliers) or by selecting the output of the primary channel readout path as the finalized pixel value instead of the output of summer 375, etc. In all cases, logic circuitry unused in under-threshold (primary-channel-only) readouts may be disabled to save power. Also, the under/over-threshold determination may be implemented in the digital domain as shown by comparator 181 or in the analog domain, with the determination/comparison result being applied to read-merge logic 387 directly (without prior storage) or via storage element 386. While charge-state and reset-state sample-and hold elements 391 and 393 (and an analog differencing/subtraction element 395) are depicted in Figure 8 to support analog-domain CDS operation, charge-state and reset-state signals may be

digitized within ADC 175 prior to differencing (digital domain CDS) with or without prior sample-and-hold.

[0040] Figure 10 illustrates an embodiment of a split-readout pixel having non-uniform primary and secondary readout-channel conversion gains and corresponding floating-diffusion node capacities that collectively match the photodiode full-well capacity. Primary and secondary readout channel components generally match those shown in Figure 1, but with substantially lower capacitance in the primary floating diffusion node than in the secondary floating confusion node and thus higher primary-channel conversion gain than secondary-channel conversion gain. In one embodiment, for example, the primary-channel conversion gain is approximately eight times that of the secondary channel at, for example, 400 μv/e- (400 microvolts per electron) vs 50μv/e- for the secondary channel. Assuming a CMOS process that yields a 1.5 volt output swing on both readout channels (i.e., FD reset voltage minus photodiode pinning voltage = 1.5 volts), the collective charge-transfer capacity of the primary and secondary channels is 1.5v/(400 μv/e-) + 1.5v/(50μv/e-) = 33,750e-. By designing the pinned photodiode (PPD) to have a full-well capacity (Q) of roughly that same electron count, the photowell can be completely emptied through split-channel readout (avoiding loss of dynamic range), while achieving exceptional low-light sensitivity through charge transfer exclusively (or predominantly) via the high-conversion-gain primary channel.

[0041] The voltage noise within the in-pixel source-follower transistors (SF1 and SF2) shown in Figure 1 and other embodiments herein tend to have device-wise (per transistor) variation that constitutes the predominant source of pixel-to-pixel read-noise variation in the image sensor as a whole. This noise variation is caused by randomly distributed fabrication-related defects or non-ideal atomic structures in the pixel detectors so that some readout channels may show extremely high noise due to the random telegraph noise (RTN) and flicker noise caused by the defects, and other readout channels exhibiting substantially lower noise (fewer and/or less significant defects) – variation that may occur even between the two (or more) channels of a single split-readout pixel. Figure 11 illustrates a split-readout CMOS image sensor embodiment 420 in which the primary-channel/secondary-channel designation within each pixel (readout channels having nominally equal conversion gains) may be selectively and programmatically reversed (flipped or swapped) according to a calibration-time noise assessment, thus enabling operation of the lowest-noise readout channel as the primary readout channel. In one embodiment, for example, the noise characteristics of each of the nominally primary and secondary readout channels within each split-readout pixel are evaluated to determine which channel exhibits the best input-referred-noise performance, recording for each

pixel a "reverse" bit in either an asserted state that reverses the primary/secondary designation if the secondary channel exhibits better low-light noise performance or in a deasserted state that leaves the a dual-readout-channel pixels in the default primary/secondary designation if the primary channel exhibits better noise characteristics (or if noise characteristics are deemed indistinguishable). In the implementation shown, multiplexers 421 and 423 are provided with respect to each split-readout pixel to swap the default primary/secondary pixel control signals delivered to the corresponding split-reset pixel if the reverse bit ("Rev") for the corresponding pixel column is asserted (logic '1' in this example) and to pass those signals to the pixel without swapping if the reverse bit is deasserted. Exclusive OR gate 425 similarly reverses the state of the channel-select signal (CS) supplied to channel multiplexer 171 if the reverse bit is set. If per-readout-channel ADCs are provided as in 185 of Figure 3, output path multiplexers similar to 421 and 423 may be provided to selectively route the column output signals (Out1 and Out2) to either of the ADCs according to reverse bit state or circuitry within the readout controller may operate one readout path or the other as primary (and the other as secondary) according to the reverse bit, for example triggering A/D conversion first within the designated primary column output path. As pixel readout progress from one row to the next, a new page of calibration data (set of N reverse bits according to pixel-row width) may be retrieved from calibration data store 430 to establish primary/secondary designation for that next pixel row. In sensors having sufficient die area, calibration data store 430 may be implemented on the same die as the split-readout pixel array. In other embodiments, calibration data store 430 (which may additionally store weighting or other per-pixel values) may be implemented in a separate chip stacked with (and interconnected to) the die containing the split-readout pixel array.

[0042] In a number of embodiments, the additional transistors and floating diffusion node(s) provided to enable multi-channel readout consume little additional area relative to the photodiode footprint and thus do not significantly impact sensor fill-factor (e.g., photodiode relatively large and/or overlaps floating diffusion nodes or other structures in whole or part). In embodiments having smaller photodiodes and/or for which even a relatively small fill-factor impact is undesirable, readout channel resources may be shared between neighboring pixels to reduce the net transistor count within a split-readout pixel array. Figure 12 illustrates an embodiment of a split-readout pixel array in which the secondary readout channel for one pixel serves as the primary readout channel for an adjacent pixel -- a shared readout-channel arrangement that extends across the pixel array (each adjacent pair of pixels shares a readout channel) to maintain the total transistor count (and thus raise the imager fill factor) at or near that of a conventional single-readout-channel pixel array. In the depicted embodiment (an

excerpt along one row of split-readout pixels), floating diffusion node FD34, reset transistor RST34, source-follower transistor SF34 and read-select transistor SEL34 collectively serve as both a secondary readout channel for photodiode PPD3 and primary readout channel for photodiode PPD4. Separate transfer gates TGa and TGb are provided with respect to PPD3 and PPD4 and more generally with respect to each shared readout channel so that the net extra die-area consumption required for split-readout operation resolves to an extra transfer gate per pixel (to enable photocharge transfer to two different floating diffusion nodes), and unshared readout circuitry for pixels at the periphery (end-of-row locations) of the split-readout pixel array.

[0043] Still referring to Figure 12 and assuming a two-phase readout within pre-assigned primary and secondary readout channels having equal conversion gains, primary-channel readout within the pixel row commences with reset-state output via all readout channels – switching on the row-select transistors (SEL34, SEL45, SEL56, etc.) and pulsing the reset transistors (RST34, RST45, RST56, etc.). Shortly thereafter (long enough for reset-state output signal signalization and sampling), photocharge is transferred via the primary-channel transfer gates (TGa) to the adjacent floating diffusion node to produce a charge-state output via the shared readout channel. Thus, photocharge is transferred (in part or whole according to accumulation level) from PPD4 to FD34 to yield a primary-channel charge-state output signal on Out34; from PPD5 to FD45 to yield a primary-channel charge-state output signal on Out45, from PPD6 to FD56 to yield a primary-channel charge-state output signal on Out56, and so forth. After those output signals are sampled (e.g., through analog sample-and-hold or direct A/D conversion), secondary channel readout commences with repetition of the floating-diffusion reset and reset-state output signal generation, followed by residual photocharge transfer via the secondary-channel transfer gates (TGb) to the other floating diffusion node adjacent each photodiode. That is, photocharge remaining after the primary channel readout is transferred from PPD4 to FD45 to yield a secondary-channel charge-state output signal on Out45; from PPD5 to FD56 to yield a secondary-channel charge-state output signal on Out56 and so forth to conclude the split-readout operation with respect to the pixel array.

[0044] Figure 13 illustrates a channel multiplexing arrangement that may be implemented in the column-readout logic of an imager having a shared-channel split-readout pixel array per Figure 12. As shown, each of the shared-channel output lines (Out01, Out12, Out23, etc.) is coupled to a respective input of a two-input channel multiplexer 501 that serves adjacent pixel columns. As the channel-select signal (CS) is alternated between primary and secondary channel selections, each multiplexer 571 routes corresponding primary and secondary readout signals from adjacent, pixel-shared readout lines to the column logic path for the appropriate

pixel column. In the depicted example, the column logic path includes a channel-shared gain element 173 and channel-shared ADC 175 as shown in Figure 3. In alternative embodiments, a dedicated gain element (if any) and ADC may be provided for each column output line, with post-ADC multiplexers provided to route the ADC result to pre-merge storage elements for the subject pixel column.

[0045] Figure 14 illustrates an exemplary operation of channel multiplexers 501 corresponding to those shown in Figure 13. As shown, readout operations are sequenced from row to row within the pixel array (row i, row i+1, etc.) with each row readout split into successive primary and secondary channel readouts. During primary channel readout, the channel-select signal (CS) is driven low to route the reset-state and charge-state signals corresponding to the primary channel for each pixel in the selected row to downstream column readout logic – that is to select the reset-state and charge-state signal outputs for the leftmost of the two photodiodes that share the readout channel (i.e., the readout channel to which photocharge is transferred via transfer gate TGa in Figure 13). After primary channel readout is complete (e.g., after digitization or analog sample-and-hold), the channel-select signal is raised to route, to the downstream readout logic, the reset-state and charge-state signals corresponding to the secondary channel for each pixel – the readout channel to which photocharge is conveyed via transfer gate TGb in Figure 13. This alternation is repeated for each row readout to complete the pixel array scan.

[0046] Figure 15 illustrates a portion of a split-readout pixel array having four shared readout channels per pixel. In the example shown, each photodiode (PPD) in the pixel array is coupled via four transfer gates TGa, TGb, TGc and TGd to four floating diffusion nodes, respectively (i.e., FD[i,j+1], FD[i,j+2], FD[i+1,j+1] and FD[i+1,j+2] as shown at 525 for the photodiode 527 in row 'i', column 'j+1') with those floating diffusion nodes being constituents of respective readout channels a, b, c and d for photodiode 527 . Each of those floating diffusion nodes is shared by three neighboring four-readout-channel pixels with, for example, the floating diffusion node that constitutes part of readout channel 'a' for photodiode in row 'i+1' and column 'j+1' (i.e., FD[i+1,j+1]) also constituting part of readout channel b for photodiode [i+1,j], part of readout channel c for photodiode [i, j+1] and part of readout channel d for photodiode [i, j] – a readout sharing arrangement that is implemented symmetrically for all interior pixels of the pixel array (pixels at the edge of the array share two readout channels with interior neighbors). The complete shared readout channel for the four photodiodes [i, j], [i, j+1], [i+1, j] and [i+1, j+1] is depicted at 531. As shown, each of the row control signals (i.e., applied to all split-readout pixels in the same row) is asserted to control readout operations for an

adjacent pair of pixel rows (row i and row i+1 in this example). More specifically, reset signal Rst i/i+1 is asserted to reset floating diffusion node FD[i+1,j+1] prior to photocharge transfer for each of the four pixels sharing the readout channel (i.e., the two pixels in row i and the two pixels in row i+1) and select signal Sel i/i+1 is asserted to enable source-follower signal generation (via SF i/i+1) on output line Out[j,j+1] according to the floating diffusion node potential for each of the four pixels.

[0047] Figure 16 illustrates an exemplary channel multiplexing arrangement with respect to the channel a, b, c and d readouts from each of the pixels within a given row of the Figure 15 pixel array. Thus, signal TGa is pulsed to implement charge-state readout of channel 'a', with channel-select signal (CS) driven low to select the channel-a readout path, followed by pulsing of signal TGb to implement charge-state readout via channel b, with the channel-select signal driven high to select the channel-b readout path. Like operations are then carried out for channels c and d (pulsing TGc and lowering the channel-select signal, then pulsing TGd and raising the channel select signal). In embodiments having a dedicated A/D converter per column output line (i.e., one ADC for channels a and c, and another for channels b and d), channel multiplexing may be implemented downstream from A/D conversion.

[0048] The various embodiments of split-readout pixel arrays, column readout logic, readout controllers and so forth disclosed herein may be described using computer aided design tools and expressed (or represented), as data and/or instructions embodied in various computer-readable media, in terms of their behavioral, register transfer, logic component, transistor, layout geometries, and/or other characteristics. Formats of files and other objects in which such circuit expressions may be implemented include, but are not limited to, formats supporting behavioral languages such as C, Verilog, and VHDL, formats supporting register level description languages like RTL, and formats supporting geometry description languages such as GDSII, GDSIII, GDSIV, CIF, MEBES and any other suitable formats and languages. Computer-readable media in which such formatted data and/or instructions may be embodied include, but are not limited to, computer storage media in various forms (e.g., optical, magnetic or semiconductor storage media, whether independently distributed in that manner, or stored "in situ" in an operating system).

[0049] When received within a computer system via one or more computer-readable media, such data and/or instruction-based expressions of the above described circuits can be processed by a processing entity (e.g., one or more processors) within the computer system in conjunction with execution of one or more other computer programs including, without limitation, net-list generation programs, place and route programs and the like, to generate a representation or

image of a physical manifestation of such circuits. Such representation or image can thereafter be used in device fabrication, for example, by enabling generation of one or more masks that are used to form various components of the circuits in a device fabrication process.

[0050] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the disclosed embodiments. In some instances, the terminology and symbols may imply details not required to practice those embodiments. For example, any of the specific readout-channel counts, numbers of shared readout circuits, threshold levels, amplification levels, conversion gains, component counts, interconnect topologies, sensor implementations, transistor types (e.g., NMOS or PMOS) component elements and the like can be different from those described above in alternative embodiments. Signal paths depicted or described as individual signal lines may instead be implemented by multi-conductor signal buses and vice-versa and may include multiple conductors per conveyed signal (e.g., differential or pseudo-differential signaling). The term “coupled” is used herein to express a direct connection as well as a connection through one or more intervening functional components or structures. Device configuration or programming can include, for example and without limitation, loading a control value into a register or other storage circuit within an integrated circuit device in response to a host instruction (and thus controlling an operational aspect of the device and/or establishing a device configuration) or through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device (e.g., amplification factor, latching threshold, etc.). The terms “exemplary” and "embodiment" are used to express an example, not a preference or requirement. Also, the terms “may” and “can” are used interchangeably to denote optional (permissible) subject matter. The absence of either term should not be construed as meaning that a given feature or technique is required.

[0051] Various modifications and changes can be made to the embodiments presented herein without departing from the broader spirit and scope of the disclosure. For example, features or aspects of any of the embodiments can be applied in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An integrated-circuit image sensor comprising:

a photodetection element to accumulate photocharge during an exposure interval;

a first readout circuit coupled to the photodetection element and having a first floating diffusion node;

a second readout circuit coupled to the photodetection element and having a second floating diffusion node; and

readout control circuitry to (i) enable transfer of a first portion of the accumulated photocharge from the photodetection element to the first floating diffusion node and generation within the first readout circuit of a first output signal corresponding to the photocharge transferred to the first floating diffusion node and (ii) enable transfer of a second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node and generation within the second readout circuit of a second output signal corresponding to the photocharge transferred to the second floating diffusion node.

2. The integrated-circuit image sensor of claim 1 further comprising column output logic to generate a digital pixel value based at least in part on the first output signal and the second output signal.

3. The integrated-circuit image sensor of claim 2 wherein the column output logic is coupled to receive the first output signal via a first column output line and the second output signal via a second column output line.

4. The integrated-circuit image sensor of claim 2 wherein the column output logic comprises analog-to-digital (A/D) conversion circuitry to generate first and second digital values based at least in part on the first and second output signals, respectively, and merge circuitry to generate the digital pixel value based at least in part on the first and second digital values.

5. The integrated-circuit image sensor of claim 4 wherein the readout control circuitry initiates generation of the first digital value concurrently with enabling transfer of the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node.

6. The integrated-circuit image sensor of claim 1 wherein the first readout circuit comprises a

first transfer gate coupled between the first floating diffusion node and the photodetection element and the second readout circuit comprises a second transfer gate coupled between the second floating diffusion node and the photodetection element, and wherein the readout circuitry to enable transfer of the first and second portions of the accumulated photocharge to the first and second floating diffusion nodes comprises circuitry to switch on the first transfer gate during a first interval to enable transfer of the first portion of the accumulated photocharge to the first floating diffusion node and to switch on the second transfer gate during a second interval, subsequent to the first interval, to enable transfer of the second portion of the accumulated photocharge to the second floating diffusion node.

7. The integrated-circuit image sensor of claim 1 wherein:

the first readout circuit has a first conversion gain such that each constituent photocharge carrier within the first portion of the accumulated photocharge generates, upon transfer to the first floating diffusion node, a first voltage step in the first floating diffusion node;

the second readout circuit has a second conversion gain such that each constituent photocharge carrier within the second portion of the accumulated photocharge generates, upon transfer to the second floating diffusion node, a second voltage step in the second floating diffusion node, the second voltage step being smaller than the first voltage step.

8. The integrated-circuit image sensor of claim 1 wherein a photocharge capacity of the first floating diffusion node and a photocharge capacity of the second floating diffusion node collectively meet or exceed a photocharge capacity of the photodetection element.

9. The integrated-circuit image sensor of claim 8 wherein the photocharge capacity of the first floating diffusion node is constrained by a difference between minimum and maximum attainable voltages on the first and second floating diffusion nodes and proportional to a first conversion gain of the first readout circuit, and wherein the photocharge capacity of the second floating diffusion node is constrained by the difference between the minimum and maximum attainable voltages on the first and second floating diffusion nodes and proportional to a second conversion gain of the second readout circuit, and wherein the first conversion gain is higher than the second conversion gain.

10. The integrated-circuit image sensor of claim 1 wherein the first portion of the accumulated photocharge may constitute the entirety of the photocharge accumulated within the photodetection element in a low-light exposure, and wherein the readout circuitry to enable

transfer of the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node comprises circuitry to selectively enable transfer of the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node according to whether the first output signal indicates that the first portion of the accumulated photocharge constitutes the entirety of the of the photocharge accumulated within the photodetection element.

11. The integrated-circuit image sensor of claim 1 wherein the first portion of the accumulated photocharge may constitute the entirety of the photocharge accumulated within the photodetection element in a low-light exposure, the integrated-circuit image sensor further comprising column output logic to (i) generate the digital pixel value based at least in part on the first output signal and not the second output signal if the first output signal indicates that the first portion of the accumulated photocharge constitutes the entirety of the photocharge accumulated within the photodetection element, and (ii) generate the digital pixel value based at least in part on the first output signal and the second output signal if the first output signal indicates that the first portion of the accumulated photocharge may not constitute the entirety of the photocharge accumulated within the photodetection element.

12. A method of operation within an integrated-circuit image sensor, the method comprising:
accumulating photocharge within a photodetection element during an exposure interval;
transferring a first portion of the accumulated photocharge from the photodetection element to a first floating diffusion node;
generating a first output signal corresponding to the photocharge transferred to the first floating diffusion node;
transferring a second portion of the accumulated photocharge from the photodetection element to a second floating diffusion node;
generating a second output signal corresponding to the photocharge transferred to the second floating diffusion node; and
generating a digital pixel value based at least in part on the first output signal and the second output signal.

13. The method of claim 12 wherein generating the first output signal comprises generating the first output signal on a first column output line coupled to a column of pixels, including a pixel containing the photodetection element, and wherein generating the second output signal comprises generating the second output signal on a second column output line coupled to the column of pixels.

14. The method of claim 12 wherein generating the digital pixel value comprises generating first and second digital values based at least in part on the first and second output signals, respectively, and generating the digital pixel value based at least in part on the first and second digital values.

15. The method of claim 14 wherein generating the first digital value based at least in part on the first output signal comprises executing an analog-to-digital conversion of the first output signal concurrently transferring the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node.

16. The method of claim 12 wherein transferring the first and second portions of the accumulated photocharge to the first and second floating diffusion nodes comprises switching on a first transfer gate coupled between the photodetection element and the first floating diffusion node during a first interval to enable transfer of the first portion of the accumulated photocharge to the first floating diffusion node and switching on a second transfer gate coupled between the photodetection element and the second floating diffusion node during a second interval, subsequent to the first interval, to enable transfer of the second portion of the accumulated photocharge to the second floating diffusion node.

17. The method of claim 12 wherein transferring the first portion of the accumulated photocharge from the photodetection element to the first floating diffusion node comprises transferring the first portion of the accumulated photocharge from the photodetection element to the first floating diffusion node with a first conversion gain and wherein transferring the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node comprises transferring the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node with a second conversion gain, the second conversion gain being lower than the first conversion gain.

18. The method of claim 12 wherein a photocharge capacity of the first floating diffusion node and a photocharge capacity of the second floating diffusion node collectively meet or exceed a photocharge capacity of the photodetection element.

19. The method of claim 12 wherein the first portion of the accumulated photocharge may constitute the entirety of the photocharge accumulated within the photodetection element in a low-light exposure, and wherein transferring the second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node comprises selectively transferring the second portion of the accumulated photocharge from

the photodetection element to the second floating diffusion node according to whether the first output signal indicates that the first portion of the accumulated photocharge constitutes the entirety of the of the photocharge accumulated within the photodetection element.

20. The method of claim 12 wherein the first portion of the accumulated photocharge may constitute the entirety of the photocharge accumulated within the photodetection element in a low-light exposure and wherein generating the digital pixel value based at least in part on the first output signal and the second output signal comprises generating the digital pixel value based at least in part on the first output signal and the second output signal if the first output signal indicates that the first portion of the accumulated photocharge may not constitute the entirety of the photocharge accumulated within the photodetection element, the method further comprising generating the digital pixel value based at least in part on the first output signal and not the second output signal if the first output signal indicates that the first portion of the accumulated photocharge constitutes the entirety of the photocharge accumulated within the photodetection element.

21. An integrated-circuit image sensor comprising:

a photodetection element to accumulate photocharge during an exposure interval;

first and second floating diffusion nodes;

means for transferring a first portion of the accumulated photocharge from the photodetection element to the first floating diffusion node and for generating a first output signal corresponding to the photocharge transferred to the first floating diffusion node;

means transferring a second portion of the accumulated photocharge from the photodetection element to the second floating diffusion node and for generating a second output signal corresponding to the photocharge transferred to the second floating diffusion node; and

means for generating a digital pixel value based at least in part on the first output signal and the second output signal.

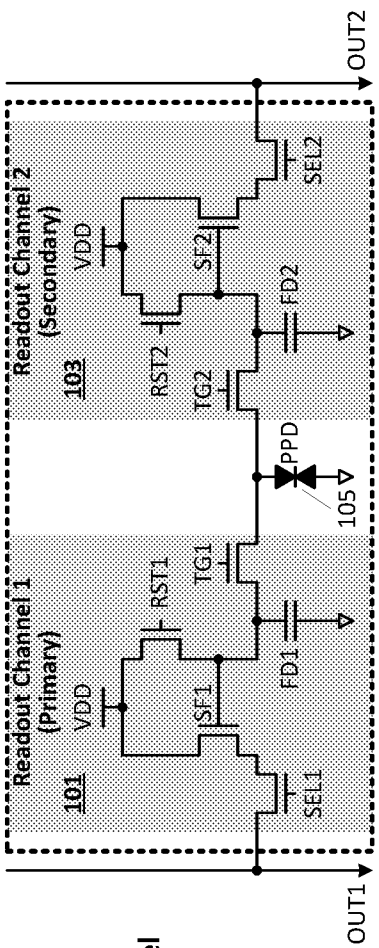


FIG. 1
Split-Readout Pixel

FIG. 2

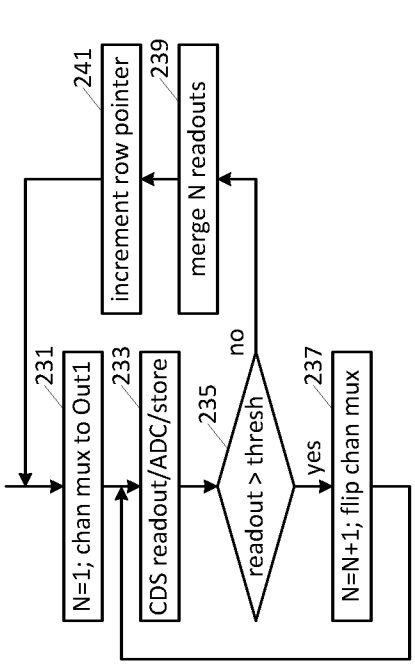


FIG. 4

One to N pixel readouts, alternating between readout channels

FIG. 5 Column-Shared ADC

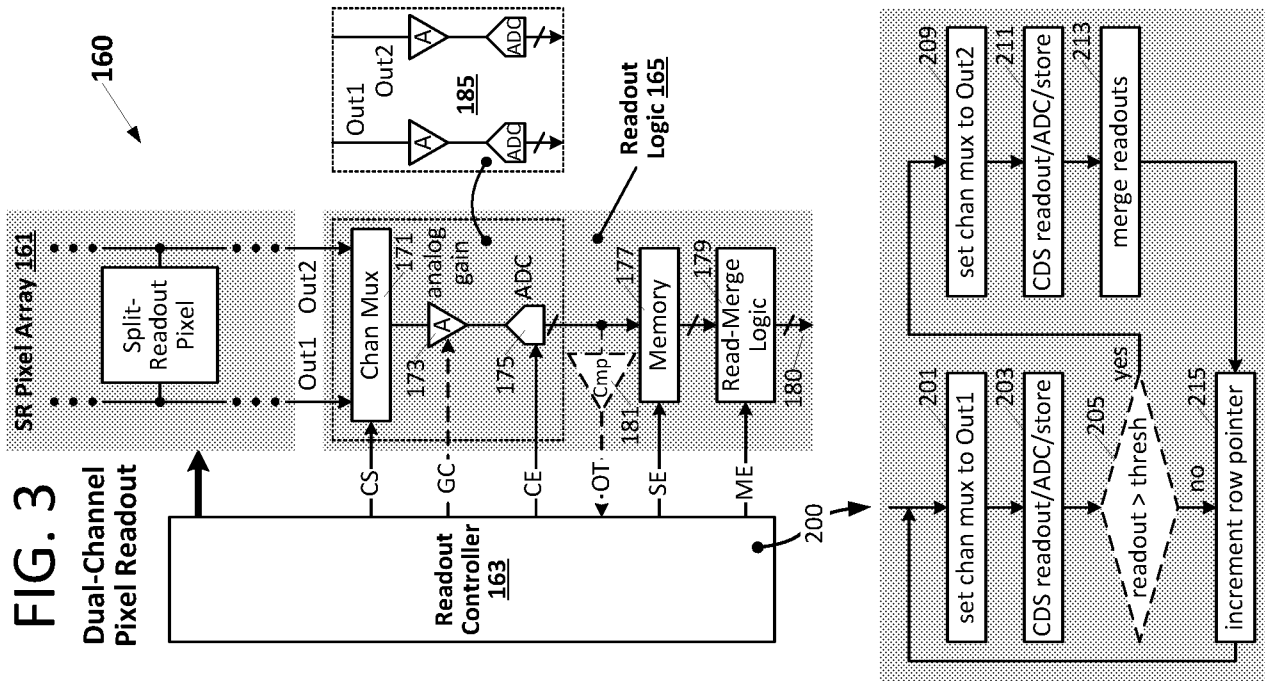


FIG. 3

Dual-Channel Pixel Readout

FIG. 6

Dual-Channel Pixel Readout with Col-Shared SSADC

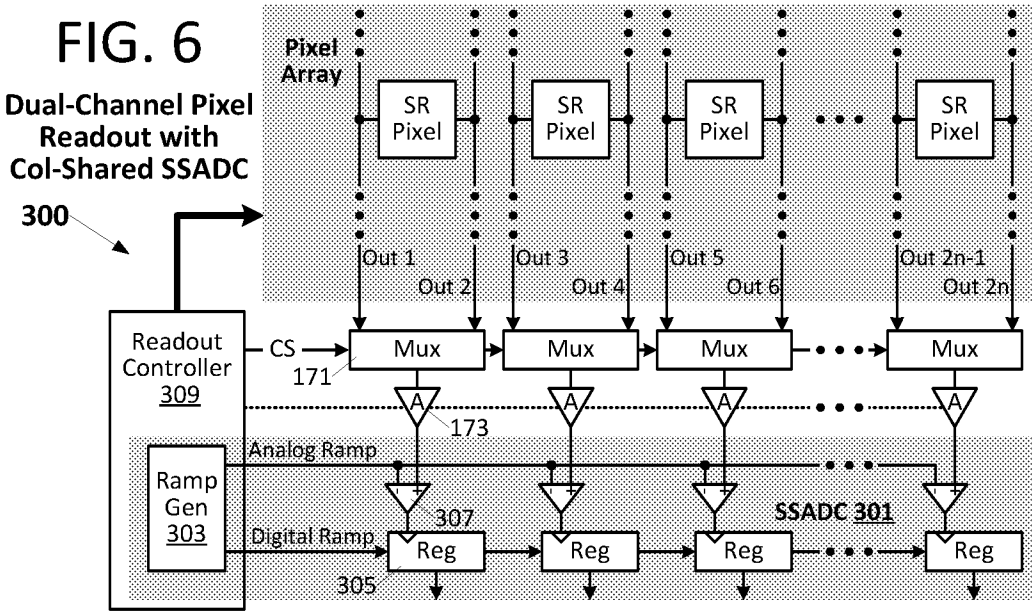


FIG. 7 Pipelined Primary/Secondary Channel Readout

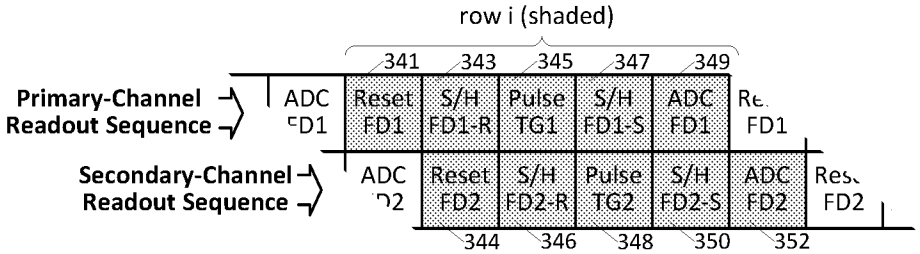


FIG. 8

Read-Merge with optional gain calibration and channel weighting

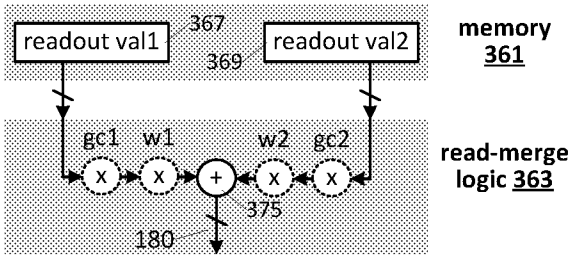


FIG. 9

Read-Merge Conditioned on Overthreshold Channel 1 Readout

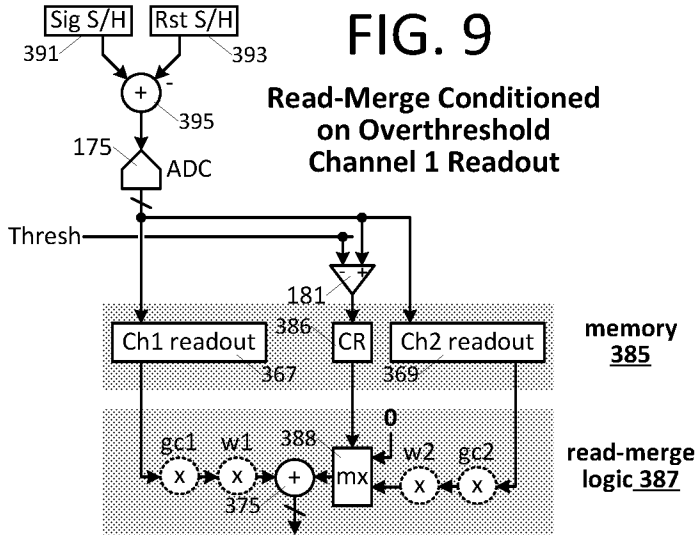


FIG. 10 Split-Readout Pixel with Non-Uniform Chan1/Chan2 Conversion Gain

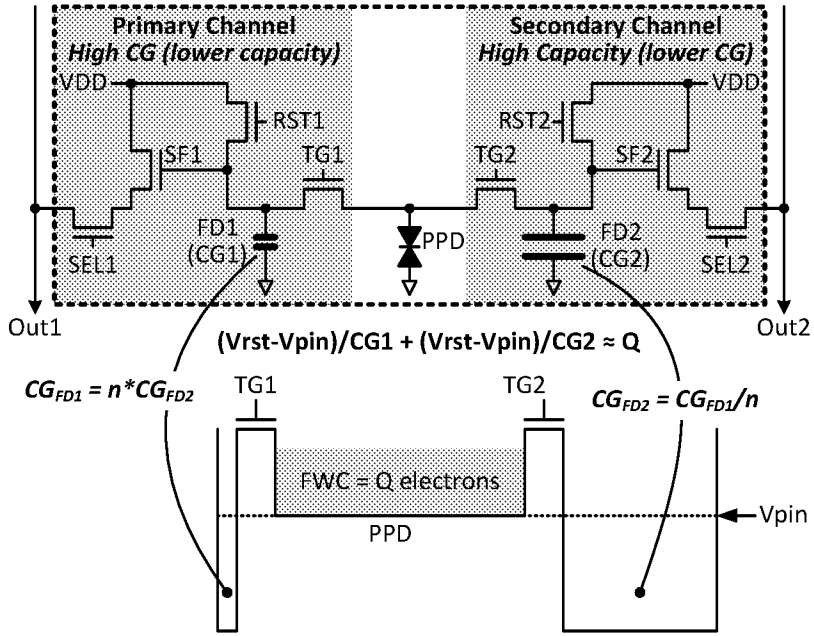


FIG. 11

Per-Pixel-Configurable Channel Read-Out Order

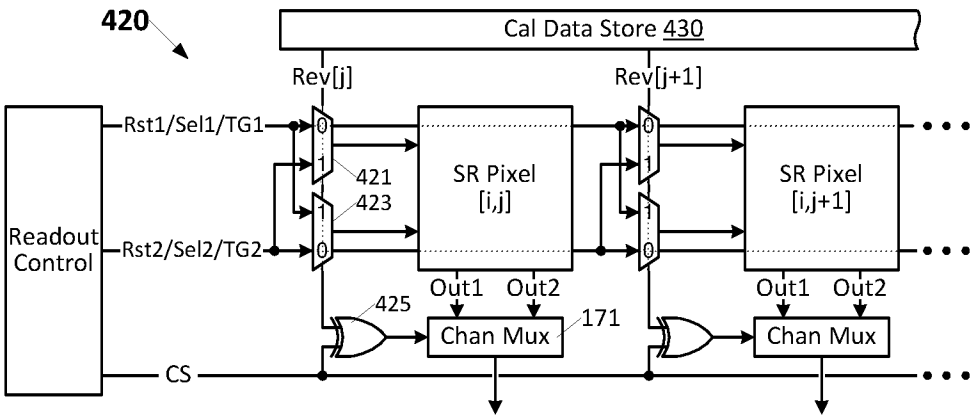


FIG. 12 Split-Readout Pixels with Shared Readout Channels

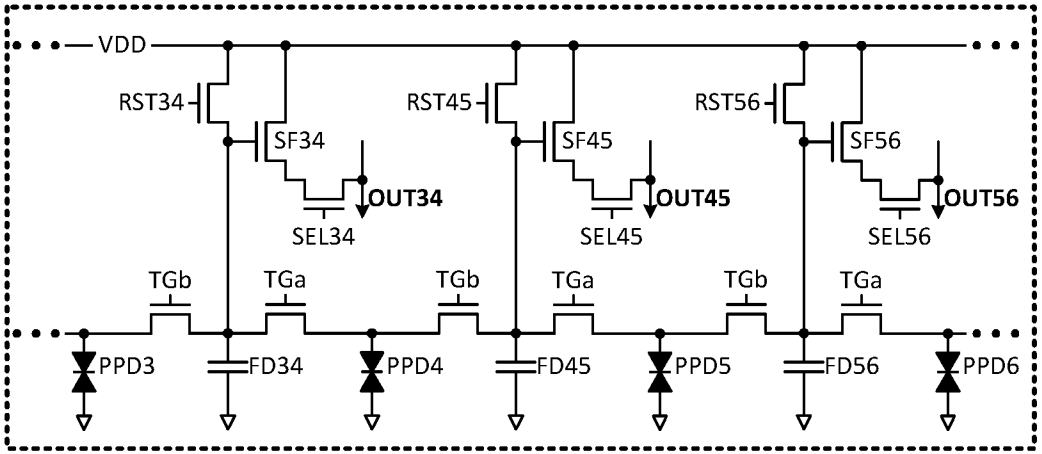


FIG. 13

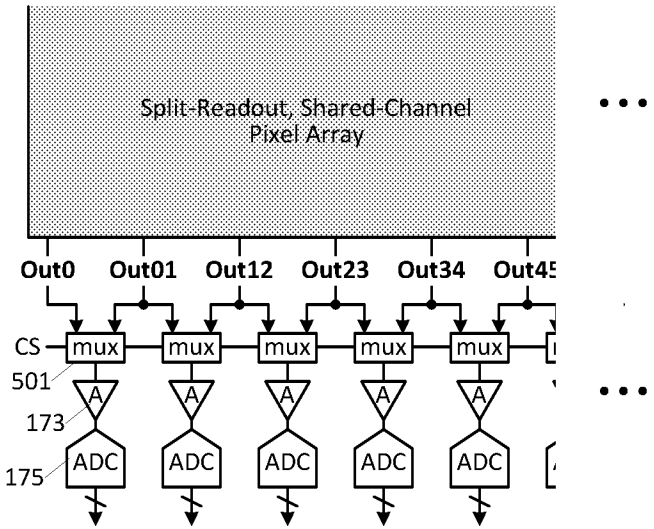


FIG. 14

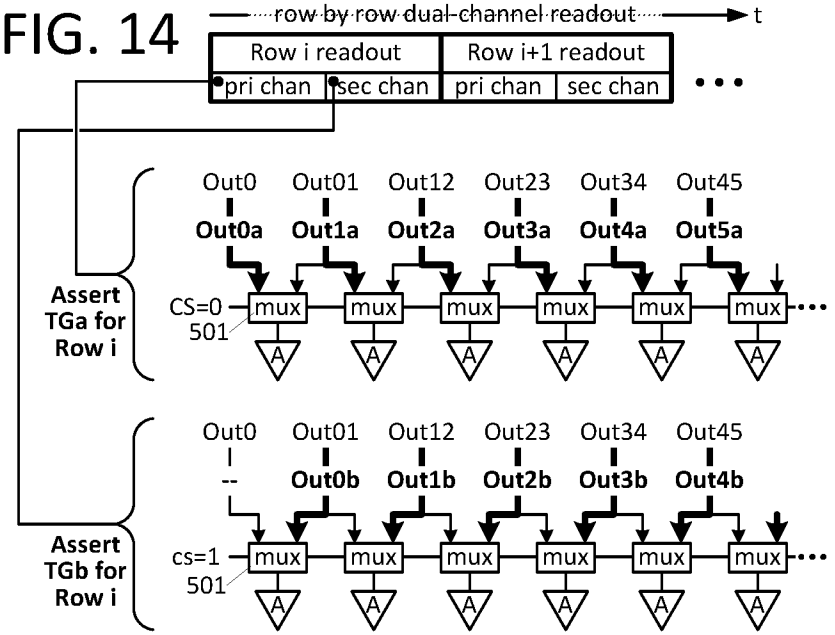


FIG. 15

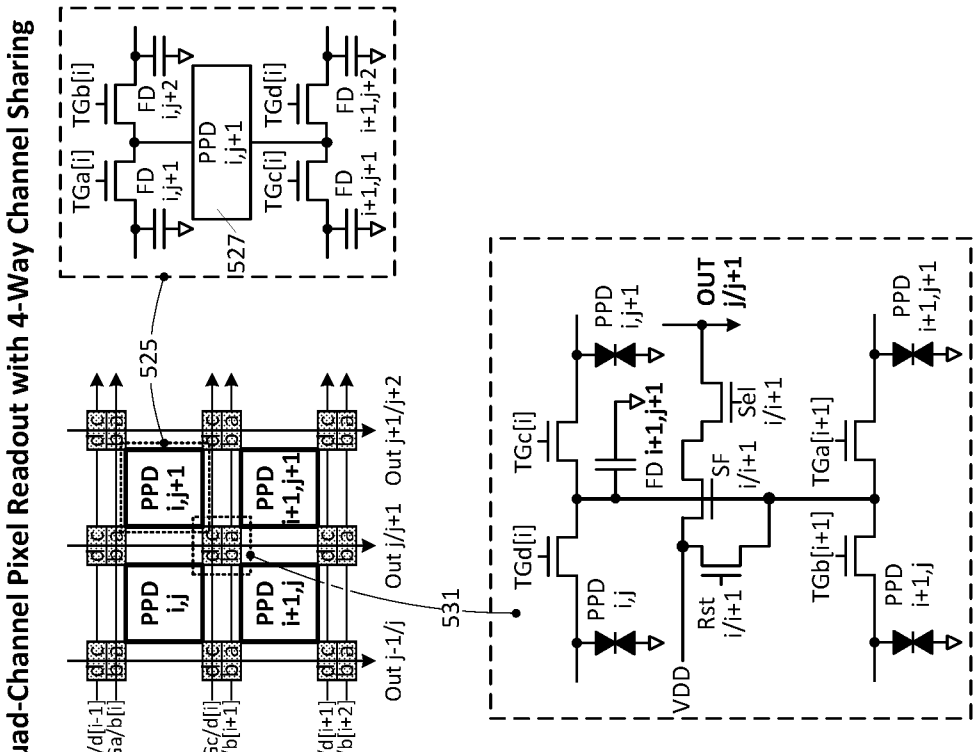
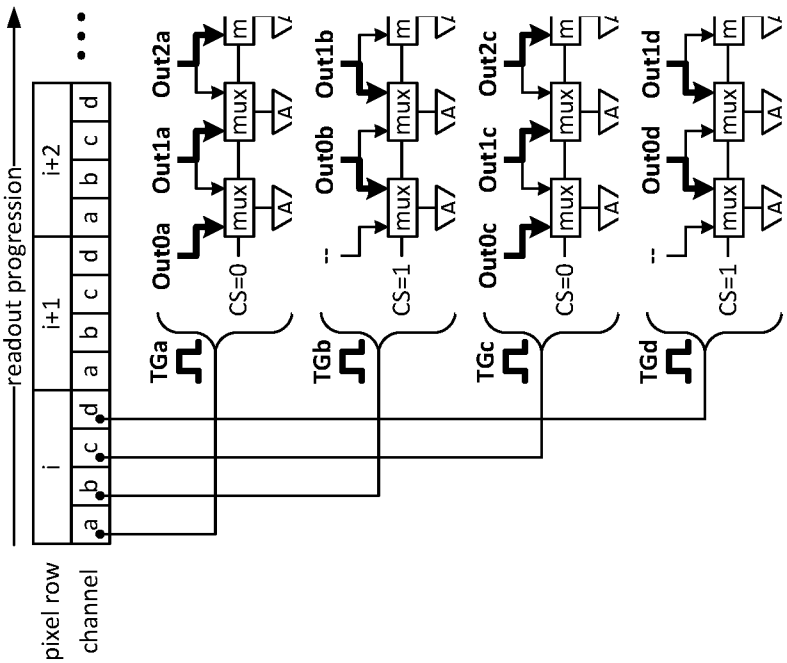

Quad-Channel Pixel Readout with 4-Way Channel Sharing
TGa[i]
TGb[i]
TGc[i]
TGd[i]
FD i,j+1
FD i,j+2
FD i+1,j+1
FD i+1,j+2
PPD i,j+1
PPD i,j
PPD i+1,j+1
PPD i+1,j
525
527
531
Out j-1/j
Out j/j+1
Out j+1/j+2
TGc/d[j-1]
TGa/b[j]
TGc/d[j]
TGa/b[j+1]
TGc/d[j+1]
TGa/b[j+2]
VDD
Rst i/i+1
SF i/i+1
Sel i/i+1
OUT i/j+1
TGa[i+1]
TGb[i+1]

FIG. 16


Quad Channel Readout
readout progression
pixel row
channel
i
i+1
i+2
TGa
TGb
TGc
TGd
Out0a
Out1a
Out2a
Out0b
Out1b
Out0c
Out1c
Out2c
Out0d
Out1d
CS=0
CS=1
mux

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/047696

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/3745 H04N5/355 H04N5/378 H01L27/146
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/073875 A2 (RECON OPTICAL INC [US]; FARRIER MICAHEL [US]) 13 July 2006 (2006-07-13) abstract figure 6 page 17, line 15 - line 27 page 19, line 8 - line 18 page 19, line 24 - line 26 page 20, line 3 - line 10 -----	1-21
X	US 9 936 153 B1 (OMNIVISION TECH INC [US]) 3 April 2018 (2018-04-03) abstract figures 2,4 page 3, line 44 - page 4, line 10 page 4, line 40 - page 5, line 18 ----- -/--	1,12,21

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 November 2019	19/11/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Lauri, Lauro

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/047696

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 2 046 022 A1 (MELEXIS NV [BE]) 8 April 2009 (2009-04-08) the whole document -----	1-21

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2019/047696

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US 9936153 B1	03-04-2018	CN 107895729 A	10-04-2018
		TW 201826513 A	16-07-2018
		US 9936153 B1	03-04-2018
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