

(51) International Patent Classification:
H04J 14/02 (2006.01)(21) International Application Number:
PCT/IB2013/002383(22) International Filing Date:
20 June 2013 (20.06.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

61/662,085	20 June 2012 (20.06.2012)	US
61/726,099	14 November 2012 (14.11.2012)	US
61/729,774	26 November 2012 (26.11.2012)	US
61/747,132	28 December 2012 (28.12.2012)	US
61/768,532	24 February 2013 (24.02.2013)	US
61/807,813	3 April 2013 (03.04.2013)	US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) Title: HIGHLY-SPECTRALLY-EFFICIENT RECEPTION USING ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING

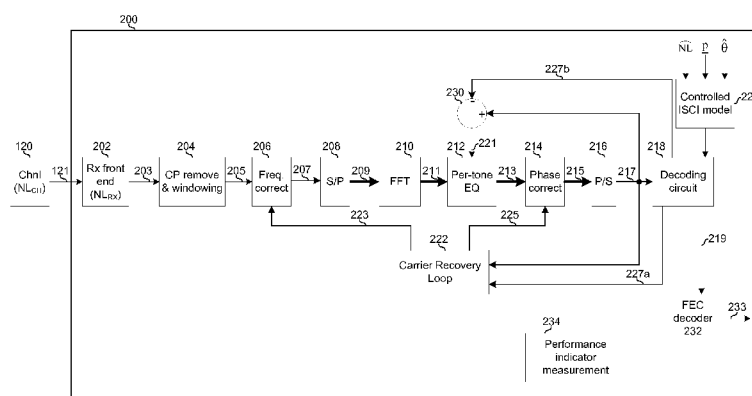


FIG. 2A

(57) Abstract: Circuitry for use in a receiver may comprise: a front-end circuit operable to receive an orthogonal frequency division multiplexing (OFDM) symbol on a first number of physical subcarriers. The circuitry may comprise a decoding circuit operable to decode the OFDM symbol using an inter-carrier interference (ICI) model, the decoding resulting in a determination of a sequence of symbols, comprising a second number of symbols, that most-likely correspond to the received OFDM symbol, where the second number is greater than the first number. The sequence of symbols may comprise N- QAM symbols, N being an integer. The ISCI model may be based, at least in part, on non-linearity experienced by the OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by the receiver. The ISCI model may be based, at least in part, on phase-noise introduced to the OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by the receiver.

HIGHLY-SPECTRALLY-EFFICIENT RECEPTION USING ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING

CLAIM OF PRIORITY

[0001] This patent application makes reference to, claims priority to and claims benefit from:

United States Provisional Patent Application Serial No. 61/662,085 entitled “Apparatus and Method for Efficient Utilization of Bandwidth” and filed on June 20, 2012;

United States Provisional Patent Application Serial No. 61/726,099 entitled “Modulation Scheme Based on Partial Response” and filed on November 14, 2012;

United States Provisional Patent Application Serial No. 61/729,774 entitled “Modulation Scheme Based on Partial Response” and filed on November 26, 2012;

United States Provisional Patent Application Serial No. 61/747,132 entitled “Modulation Scheme Based on Partial Response” and filed on December 28, 2012;

United States Provisional Patent Application Serial No. 61/768,532 entitled “High Spectral Efficiency over Non-Linear, AWGN Channels” and filed on February 24, 2013; and

United States Provisional Patent Application Serial No. 61/807,813 entitled “High Spectral Efficiency over Non-Linear, AWGN Channels” and filed on April 3, 2013.

[0002] Each of the above applications is hereby incorporated herein by reference in its entirety.

INCORPORATIONS BY REFERENCE

[0003] This patent application makes reference to:

United States Patent Application Serial No.: 13/754,964 (attorney docket no. 26150US02), titled “Low-Complexity, Highly-Spectrally-Efficient Communications,” and filed on January 31, 2013;

United States Patent Application Serial No.: 13/754,998 (attorney docket no. 26151US02), titled "Design and Optimization of Partial Response Pulse Shape Filter," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,001 (attorney docket no. 26152US02), titled "Constellation Map Optimization for Highly Spectrally Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,008 (attorney docket no. 26153US02), titled "Dynamic Filter Adjustment for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,011 (attorney docket no. 26156US02), titled "Timing Synchronization for Reception of Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,014 (attorney docket no. 26157US02), titled "Signal Reception Using Non-Linearity-Compensated, Partial Response Feedback," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,018 (attorney docket no. 26158US02), titled "Feed Forward Equalization for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,021 (attorney docket no. 26159US02), titled "Decision Feedback Equalizer for Highly Spectrally Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,025 (attorney docket no. 26160US02), titled "Decision Feedback Equalizer with Multiple Cores for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,026 (attorney docket no. 26161US02), titled "Decision Feedback Equalizer Utilizing Symbol Error Rate Biased Adaptation Function for Highly Spectrally Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,028 (attorney docket no. 26163US02), titled "Coarse Phase Estimation For Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,039 (attorney docket no. 26164US02), titled "Fine Phase Estimation for Highly Spectrally Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,972 (attorney docket no. 26165US02), titled "Multi-Mode Transmitter for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,043 (attorney docket no. 26166US02), titled "Joint Sequence Estimation of Symbol and Phase With High Tolerance Of Nonlinearity," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,050 (attorney docket no. 26168US02), titled "Adaptive Non-Linear Model for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,052 (attorney docket no. 26169US02), titled "Pilot Symbol-Aided Sequence Estimation for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,054 (attorney docket no. 26171US02), titled "Method and System for Corrupt Symbol Handling for Providing High Reliability Sequences," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,060 (attorney docket no. 26172US02), titled "Method and System for Forward Error Correction Decoding with Parity Check for Use in Low Complexity Highly-spectrally-efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,061 (attorney docket no. 26174US02), titled "Method and System for Quality of Service (QoS) Awareness in a Single Channel Communication System," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/756,079 (attorney docket no. 26467US02), titled "Pilot Symbol Generation for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,065 (attorney docket no. 26468US02), titled "Timing Pilot Generation for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/756,010 (attorney docket no. 26469US02), titled "Multi-Mode Receiver for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,068 (attorney docket no. 26470US02), titled "Forward Error Correction with Parity Check Encoding for use in Low Complexity Highly-spectrally-efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/756,469 (attorney docket no. 26480US02), titled "Highly-Spectrally-Efficient Receiver," and filed on January 31, 2013;

United States Patent Application Serial No.: _____ (attorney docket no. 26552US02), titled “Highly-Spectrally-Efficient Transmission Using Orthogonal Frequency Division Multiplexing,” and filed on the same date as this application;

United States Patent Application Serial No.: _____ (attorney docket no. 26651US02), titled “Multi-Mode Orthogonal Frequency Division Multiplexing Transmitter for Highly-Spectrally-Efficient Communications,” and filed on the same date as this application; and

United States Patent Application Serial No.: _____ (attorney docket no. 26652US02), titled “Multi-Mode Orthogonal Frequency Division Multiplexing Receiver for Highly-Spectrally-Efficient Communications,” and filed on the same date as this application.

[0004] Each of the above applications is hereby incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0005] Aspects of the present application relate to electronic communications.

BACKGROUND

[0006] Existing communications methods and systems are overly power hungry and/or spectrally inefficient. Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such approaches with some aspects of the present method and system set forth in the remainder of this disclosure with reference to the drawings.

BRIEF SUMMARY

[0007] Methods and systems are provided for highly-spectrally-efficient communications using orthogonal frequency division multiplexing, substantially as illustrated by and/or described in connection with at least one of the figures, as set forth more completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1A is a diagram of an example OFDM transmitter.

[0009] FIG. 1B depicts simulation results of an example cyclic filter for a highly-spectrally-efficient OFDM transmitter.

[0010] FIG. 1C depicts a flowchart describing operation of an example implementation of a highly-spectrally-efficient OFDM transmitter.

[0011] FIG. 2A is a diagram of an example OFDM receiver.

[0012] FIGS. 2B and 2C depict a flowchart describing operation of an example implementation of a highly-spectrally-efficient OFDM receiver.

[0013] FIG. 2D depicts a flowchart describing operation of an example decoding circuit of a highly-spectrally-efficient OFDM receiver.

[0014] FIG. 3 is a flowchart describing a process for mitigating the effects of frequency-selective fading in highly-spectrally-efficient OFDM communication system.

[0015] FIG. 4 is a flowchart depicting an example iterative sequence estimation process for highly-spectrally-efficient OFDM communications.

DETAILED DESCRIPTION

[0016] As utilized herein the terms "circuits" and "circuitry" refer to physical electronic components (i.e. hardware) and any software and/or firmware ("code") which may configure the hardware, be executed by the hardware, and or otherwise be associated with the hardware. As used herein, for example, a particular processor and memory may comprise a first "circuit" when executing a first one or more lines of code and may comprise a second "circuit" when executing a second one or more lines of code. As utilized herein, "and/or" means any one or more of the items in the list joined by "and/or". As an example, "x and/or y" means any element of the three-element set {(x), (y), (x, y)}. As another example, "x, y, and/or z" means any element of the seven-element set {(x), (y), (z), (x, y), (x, z), (y, z), (x, y, z)}. As utilized herein, the term "exemplary" means serving as a non-limiting example, instance, or illustration. As utilized herein, the terms "e.g.," and "for example" set off lists of one or more non-limiting examples, instances, or illustrations. As utilized herein, circuitry is "operable" to perform a function whenever the circuitry comprises the necessary hardware and code (if any is necessary) to perform the function, regardless of whether performance of the function is disabled, or not enabled, by some user-configurable setting.

[0017] Orthogonal Frequency Division Multiplexing (OFDM) has gained traction in recent years in high-capacity wireless and wireline communication systems such as WiFi (IEEE Std 802.11n/ac), 3GPP-LTE, and G.hn. One advantage of OFDM is that it can reduce the need for complicated equalization over frequency selective channels. It is particularly powerful in combination with multiple independent spatial streams and multiple antennas, Multiple Input Multiple Output (MIMO) systems. One advantage of OFDM is that it can reduce or eliminate the need for complicated equalization over frequency selective channels. Conventional MIMO-OFDM solutions are based on suboptimal Zero Forcing, SIC (Successive Interference Cancellation), and minimum mean square error (MMSE) receivers. These detection algorithms are significantly

inferior to maximum likelihood (ML) and near-ML receivers. Lately, in emerging standards, constellation size continues to increase (256-QAM, 1024-QAM, and so on). The associated ML state space of such solutions is N^{SS} , where N and SS stand for the constellation size and total number of MIMO spatial streams, respectively. Consequently, aspects of this disclosure pertain to reduced state/complexity ML decoders that achieve high performance.

[0018] Example implementations of the present disclosure may use relatively small constellations with partial response signaling that occupies around half the bandwidth of “ISI-free” or “full response” signaling. Thus, the ML state space is reduced significantly and cost effectiveness of reduced complexity ML detection is correspondingly improved. Additionally, aspects of this disclosure support detection in the presence of phase noise and non-linear distortion without the need of pilot symbols that reduce capacity and spectral efficiency. The spectral compression also provides multidimensional signal representation that improves performance in an AWGN environment as compared to conventional two-dimensional QAM systems. In accordance with an implementation of this disclosure, transmitter shaping filtering may be applied in the frequency domain in order to preserve the independency of the OFDM symbols.

[0019] FIG. 1A is a diagram of an example OFDM transmitter. The example transmitter 100 comprises a symbol mapper circuit 102, an inter-symbol correlation (ISC) generation circuit 104, a decimation circuit 108, a serial-to-parallel circuit 108, an inverse fast Fourier transform (IFFT) circuit 112, a parallel-to-serial circuit 114, a cyclic prefix and windowing circuit 116, and a transmit front-end circuit 118. In the example implementation shown, the transmitter transmits into a channel 120.

[0020] The symbol mapper circuit 102, may be operable to map, according to a selected modulation scheme, bits of a bitstream to be transmitted (“Tx_bitstream”) to

symbols. For example, for a quadrature amplitude modulation (QAM) scheme having a symbol alphabet of N (N-QAM), the mapper may map each $\log_2(N)$ bits of the Tx_bitstream to a single symbol represented as a complex number and/or as in-phase (I) and quadrature-phase (Q) components. Although N-QAM is used for illustration in this disclosure, aspects of this disclosure are applicable to any modulation scheme (e.g., pulse amplitude modulation (PAM), amplitude shift keying (ASK), phase shift keying (PSK), frequency shift keying (FSK), etc.). Additionally, points of the N-QAM constellation may be regularly spaced (“on-grid”) or irregularly spaced (“off-grid”). Furthermore, the symbol constellation used by the mapper 102 may be optimized for best bit-error rate (BER) performance (or adjusted to achieve a target BER) that is related to log-likelihood ratio (LLR) and to optimizing mean mutual information bit (MMIB) (or achieving a target MMIB). The Tx_bitstream may, for example, be the result of bits of data passing through a forward error correction (FEC) encoder and/or an interleaver. Additionally, or alternatively, the symbols out of the mapper 102 may pass through an interleaver.

[0021] The ISC generation circuit 104 may be operable to filter the symbols output by the mapper 102 to generate C' virtual subcarrier values (the terminology “virtual subcarrier” is explained below) having a significant, controlled amount inter-symbol correlation among symbols to be output on different subcarriers (i.e., any particular one of the C' virtual subcarrier values may be correlated with a plurality of the C' symbols output by mapper 102). In other words, the inter-symbol correlation introduced by the ISC generation circuit may be correlation between symbols to be output on different subcarriers. In an example implementation, the ISC generation circuit 104 may be a cyclic filter.

[0022] The response of the ISC generation circuit 104 may be determined by a plurality of coefficients, denoted $\underline{p}$ (where underlining indicates a vector), which may be, for example, stored in memory 124. In an example implementation, the ISC generation

circuit 104 may perform a cyclic (or, equivalently, “circular”) convolution on sets of C' symbols from the mapper 102 to generate sets of C' virtual subcarrier values conveyed as signal 105. In such an implementation, the ISC generation circuit 104 may thus be described as a circulant matrix that multiplies an input vector of C' symbols by a $C' \times C'$ matrix, where each row $i+1$ of the matrix may be a circularly shifted version of row i of the matrix, i being an integer from 1 to C' . For example, for $C'=4$ (an arbitrary value chosen for illustration only) and $\underline{p} = [p_1 \ p_2 \ p_3 \ p_4]$, the matrix may be as follows:

$$\begin{bmatrix} p_1 & p_2 & p_3 & p_4 \\ p_4 & p_1 & p_2 & p_3 \\ p_3 & p_4 & p_1 & p_2 \\ p_2 & p_3 & p_4 & p_1 \end{bmatrix}$$

In another example, the length of $\underline{p}$ may be less than C' , and zero padding may be used to fill the rows and/or columns to length C' and/or pad the rows and/or columns. For example, C' may be equal to 6 and the matrix above (with $\underline{p}$ having four elements) may be padded to create a six element vector $\underline{p}_Z = [p_1 \ p_2 \ p_3 \ p_4 \ 0 \ 0]$ and then $\underline{p}_Z$ may be used to generate a 6 by 6 matrix in the same way that $\underline{p}$ was used to generate the 4 by 4 matrix. As another example, only the rows may be padded such that the result is a $C' \times LP$ matrix, where LP is the length of $\underline{p}$ (e.g., a 4×6 matrix in the above example). As another example, only the columns may be padded such that the result is a $LP \times C'$ matrix, where LP is the length of $\underline{p}$ (e.g., a 6×4 matrix in the above example).

[0023] The decimation circuit 108 may be operable to decimate groups of C' virtual subcarrier values down to C transmitted physical subcarrier values (the term “physical subcarrier” is explained below). Accordingly, the decimation circuit 108 may be operable to perform downsampling and/or upsampling. The decimation factor may be an integer or a fraction. The output of the decimator 108 hence comprises C physical subcarrier values per OFDM symbol. The decimation may introduce significant aliasing

in case that the ISC generation circuit 104 does not confine the spectrum below the Nyquist frequency of the decimation. However, in example implementations of this disclosure, such aliasing is allowed and actually improves performance because it provides an additional degree of freedom. The C physical subcarrier values may be communicated using C of $C+\Delta$ total subcarriers of the channel 120. Δ may correspond to the number of OFDM subcarriers on the channel 120 that are not used for transmitting data. For example, data may not be transmitted a center subcarrier in order to reduce DC offset issues. As another example, one or more subcarriers may be used as pilots to support phase and frequency error corrections at the receiver. Additionally, zero subcarrier padding may be used to increase the sampling rate that separates the sampling replicas and allow the use of low complexity analog circuitry. The $C+\Delta$ subcarriers of channel 120 may be spaced at approximately (e.g., within circuit tolerances) $BW/(C+\Delta)$ (according to the Nyquist criterion) and with effective OFDM symbol duration of less than or equal to $(C+\Delta)/BW$ (according to the Nyquist criterion). Aspects of the invention may, however, enable the receiver to recover the original C' symbols from the received OFDM symbol (Thus the reason for referring to C' as the number of “virtual subcarriers”). This delivery of C' symbols using C effective subcarriers of bandwidth $BW/(C+\Delta)$, and OFDM symbol timing of less than or equal to $(C+\Delta)/BW$ thus corresponds to a bandwidth reduction of $(C'+\Delta)/(C+\Delta)$ (or, equivalently, a symbol rate increase) of C'/C over conventional OFDM systems (assuming the same number, Δ , of unused subcarriers in the conventional system).

[0024] To reduce complexity, in an example implementation, the functionalities of 104 and 108 may be merged by calculating only a subset (C_s) of the C physical subcarriers subset from C' by taking out the rows of the matrix that are related to the decimated virtual subcarriers of the ISC generating, $C' \times C'$ matrix. For example, decimation of factor of 2 may be achieved by eliminating the even column vectors of the

C'×C' matrix described in paragraph [0022] (assuming, for purposes of this example, that the information symbol vector (length of C') is a row vector that left multiplies the matrix).

[0025] Generally speaking, in an example implementation wherein the circuit 104 is a cyclic filter, methods and systems of designing the ISC generation circuit 104 may be similar to methods and systems described in U.S. Patent Application Serial No. 13/754,998 titled "Design and Optimization of Partial Response Pulse Shape Filter," which is incorporated by reference above. Similar to the design of the filter(s) in the single-carrier case described in U.S. Patent Application Serial No. 13/754,998, the design of a cyclic filter implementation of the circuit 104 may be based on using the symbol error rate (SER) union bound as a cost function and may aim to maximize the Euclidean distance associated with one or more identified error patterns. Using a shaping filter characterized by the coefficients $\underline{p}$, the distance induced by error pattern $\underline{\epsilon}$ may be expressed as:

$$\delta^2(\underline{\epsilon}, \underline{p}) = \sum_n \left| \sum_k p_{[n-k]} \epsilon_{[k]} \right|^2 = \sum_k \sum_l \epsilon_{[k]} \epsilon_{[l]}^* \sum_n p_{[n-k]} p_{[n-l]}^* \quad \text{Eq. 1A}$$

Assuming, for purposes of illustration, a spectral compression factor 2, then, after decimation by 2, EQ. 1A becomes:

$$\delta_2^2(\underline{\epsilon}, \underline{p}) = \sum_n \left| \sum_k p_{[2n-k]} \epsilon_{[k]} \right|^2 = \sum_n \left| \sum_k \epsilon_{[2n-2k]} p_{[2k]} + \sum_k \epsilon_{[2n-2k+1]} p_{[2k-1]} \right|^2 \quad \text{Eq. 1B}$$

Where the right-hand-side summation relates to odd-indexed symbols and the left-hand-side summation relates to even-indexed symbols. Eq. 1B may then be rewritten as:

$$\begin{aligned}
\delta_2^2(\underline{\epsilon}, \underline{p}) = & \sum_n \left[\sum_k \sum_m \epsilon_{[2k]} \epsilon_{[2m]}^* p_{[2n-2k]} p_{[2n-2m]}^* \right. \\
& + \sum_k \sum_m \epsilon_{[2k-1]} \epsilon_{[2m-1]}^* p_{[2n-2k+1]} p_{[2n-2m+1]}^* + 2 \\
& \cdot \text{Real} \left\{ \sum_k \sum_m \epsilon_{[2k]} \epsilon_{[2m-1]}^* p_{[2n-2k]} p_{[2n-2m+1]}^* \right\} \Big] \quad \text{Eq. 1C}
\end{aligned}$$

[0026] In Eq. 1C, the first and second summation terms are associated with the distance of the even-indexed and odd-indexed virtual subcarriers respectively. Accordingly, one goal in designing a cyclic filter implementation of ISC generation circuit 104 may be to maximize the first and second terms of Eq. 1C. The third term takes on both positive and negative values depending on the error pattern. In general, this term will reduce the minimum distance related to the most-probable error patterns. Accordingly, one goal in designing a cyclic filter implementation of ISC generation circuit 104 may be to minimize the third term of Eq. 1C (i.e., minimizing cross-correlation between even and odd virtual subcarriers). Additionally or alternatively, a cyclic filter implementation of ISC generation circuit 104 may be designed such that the first and second terms should have similar levels, which may correspond to even-indexed and odd-indexed symbol sequences have comparable distances (i.e., seeking energy balance between even-indexed and odd-indexed virtual subcarriers).

[0027] In presence of frequency-selective fading channel, the inter-subcarrier correlation created by 104 (by filtering or by matrix multiplication, for example) may be used to overcome the frequency-selective fading and to improve detection performance at the receiver. The processing of inter-subcarrier correlation may be perceived as "analog interleaving" over the frequency domain that spreads each of the C' information symbols over a plurality of frequency subcarriers. As a result of this "analog interleaving," a notch in one of the subcarriers will have a relatively low impact on detection, assuming

that rest of subcarriers that are carrying that information symbol are received with sufficiently-high SNR.

[0028] In case of frequency selective fading channel, feedback from the receiving device may be used to dynamically adapt transmission properties. An example process for such dynamic adaption is shown in FIG. 3.

[0029] In block 302 frequency selective fading is causing a significant notch that is critically impacting one or more subcarriers. For example, the notch may be reducing the received SNR of the subcarrier(s) below a certain level (e.g., a level that is predetermined and/or algorithmically controlled during run time).

[0030] In block 304, an identification of such impacted subcarrier(s) may be sent from the receiving device to the transmitting device (e.g., over a control channel).

[0031] In block 306, in response to receiving the indication sent in block 304, the transmitting device disables transmission of data over the impacted subcarrier(s). The transmitting device may disable transmission of data over the impacted subcarrier(s) by, for example, reconfiguring the mapper 102 (e.g., changing the value of C' and/or configuring the mapper 102 to insert pilot symbols between data symbols), changing p , reconfiguring the decimation circuit 108 (e.g., changing the value of C), and/or reconfiguring the mapping performed by the serial-to-parallel circuit 110.

[0032] In block 308, the receiving device may determine that data transmission on the disabled subcarriers should resume.

[0033] In block 310, the instruction to resume data transmission on the disabled subcarrier(s) may be sent (e.g., via a control channel). In an example implementation, such a determination may be made by monitoring pilot signal(s) that the transmitting device transmits on the disabled subcarrier(s). For example, the receiving device may monitor a characteristic (e.g., SNR) of the pilot signal(s) and determine to resume use of

the subcarriers(s) upon a significant and/or sustained change in the characteristic (e.g., upon SNR of the pilot signal(s) increasing above a determined threshold for a determined amount of time). In an example implementation, the determination to resume data transmission on the disabled subcarrier(s) may be based on the one or more characteristics of subcarriers adjacent to the disabled subcarrier(s). For example, while subcarrier N is disabled, the receiving device may monitor SNR of adjacent subcarriers N-1 and/or N+1, and may decide enable subcarrier N in response to a significant and/or sustained increase in the SNR of subcarrier(s) N-1 and/or N+1. The first example above for SNR estimation of disabled subcarrier(s) which is based on pilots, may be more accurate than the second example which is based on SNR estimation using adjacent subcarriers. However, the second example does not "waste" power on pilot subcarrier(s) transmission thus may provide higher power for the information (modulated) subcarriers assuming that the transmitted power is fixed. The relative increased power of the modulated subcarriers may improve decoding performance (e.g., SER, BER, packet error rate).

[0034] Similarly, feedback from the receiving device (e.g., in the form of subcarrier SNR measurements) may be used to adapt the ISC generation circuit 104 and/or decimation circuit 108. Such adaptation may, for example, give relatively-high-SNR subcarriers relatively-high coefficients and relatively-low-SNR subcarriers relatively-low coefficients. Such adaptation of coefficients may be used to optimize communication capacity (or to achieve a target communication capacity) between the transmitting device and the receiving device. The control channel latency and adaptation rate may be controlled to be fast enough to accommodate channel coherence time.

[0035] Returning to FIG. 1B, additional, or alternative, design goals for the circuit 104 may stem from a desire to reduce complexity of the sequence estimation in the receiver. As an example, one design goal may be, as described in U.S. Patent Application Serial

No. 13/754,998, maximizing the magnitude of coefficients of “early” (or low-indexed) taps of a cyclic filter implementation of circuit 104. As another example, one design goal may be, as described in U.S. Patent Application Serial No. 13/754,998, minimizing the cumulative power of the “late” (or high-indexed) taps of a cyclic filter implementation of circuit 104.

[0036] As shown by the example simulation results in FIG. 1B (compression factor = 2 used for purposes of illustration), a complex-valued shaping filter can exploit the full spectrum and make the even-indexed (“ph 1”) and odd-indexed responses (“ph 2”) substantially orthogonal by using disjoint parts of the spectrum. FIG. 1B shows an example of the frequency response of the even-indexed and odd-indexed coefficients of a cyclic filter implementation of circuit 104 that was designed in accordance with this disclosure. Also, shown in the lower portion of figure 1B is the total/combined even and odd response, which, as can be seen, is substantially flat.

[0037] Returning to FIG. 1A, the serial-to-parallel circuit 110 may be operable to convert C physical subcarrier values conveyed serially as signal 109 to C physical subcarrier values input conveyed in parallels as signals 111.

[0038] In an example implementation, the subcarrier values output by the decimation circuit 108 may be interleaved prior to being input to the circuit 112 and/or the circuit 110 may perform interleaving of the inputted subcarrier values. This interleaver may be operable to improve the tolerance to frequency selective fading caused by multipath that may impose wide notch that spans over several subcarriers. In this case the interleaver may be used to “spread” the notch over non-consecutive (interleaved) subcarriers and therefore reduce the impact of the notch on decoding performance.

[0039] Each of the signals 103, 105, 109, and 111 may be frequency-domain signals. The inverse fast Fourier transform (IFFT) circuit 112 may be operable to convert the frequency-domain samples of signals 111 to time-domain samples of signals 113.

[0040] The parallel-to-serial circuit 114 may be operable to convert the parallel signals 113 to a serial signal 115.

[0041] The circuit 116 may be operable to process the signal 115 to generate the signal 117. The processing may include, for example, insertion of a cyclic prefix. Additionally, or alternatively, the processing may include application of a windowing function to compensate for artifacts that may result when a receiver of the transmitted signal uses the FFT to recover information carried in the transmitted signal. Windowing applied in transmitter 100 may be instead of, or in addition to, windowing applied in a receiver.

[0042] The transmitter front-end 118 may be operable to convert the signal 117 to an analog representation, upconvert the resulting analog signal, and amplify the upconverted signal to generate the signal 119 that is transmitted into the channel 120. Thus, the transmitter front-end 118 may comprise, for example, a digital-to-analog converter (DAC), mixer, and/or power amplifier. The front-end 118 may introduce non-linear distortion and/or phase noise (and/or other non-idealities) to the signal 117. The non-linearity of the circuit 118 may be represented as NL_{Tx} which may be, for example, a polynomial, or an exponential (e.g., Rapp model). The non-linearity may incorporate memory (e.g., Volterra series). In an example implementation, the transmitter 100 may be operable to transmit its settings that relate to the nonlinear distortion inflicted on transmitted signals by the front-end 118. Such transmitted information may enable a receiver to select an appropriate nonlinear distortion model and associated parameters to apply (as described below).

[0043] The channel 120 may comprise a wired, wireless, and/or optical communication medium. The signal 119 may propagate through the channel 120 and arrive at a receiver such as the receiver described below with respect to FIG. 2A.

[0044] In various example embodiments, subcarrier-dependent bit-loading and time-varying bit-loading may also be used.

[0045] FIG. 1C depicts a flowchart describing operation of an example implementation of a highly-spectrally-efficient OFDM transmitter. The process begins with block 152 in which a baseband bitstream is generated (e.g., by an application running on a smartphone, tablet computer, laptop computer, or other computing device).

[0046] In block 154, the baseband bitstream is mapped according to a symbol constellation. In the example implementation depicted, C' (an integer) sets of $\log_2(N)$ bits of the baseband bitstream are mapped to C' N-QAM symbols.

[0047] In block 156, the C' symbols are cyclically convolved, using a filter designed as described above with reference to FIG. 1A, to generate C' virtual subcarrier values having a significant, controlled amount of inter-symbol correlation among symbols to be output on different subcarriers.

[0048] In block 158, the C' virtual subcarrier values output by the ISC generation circuit 104 may be decimated down to C physical subcarrier values, each of which is to be transmitted over a respective one of the $C+\Delta$ OFDM subcarriers of the channel 120. In an example implementation, the decimation may be by a factor of between approximately 1.25 and 3.

[0049] In block 160, the C physical subcarrier values are input to the IFFT and a corresponding $C+\Delta$ time-domain values are output for transmission over $C+\Delta$ subcarriers of the channel 120.

[0050] In block 162, a cyclic prefix may be appended to the C time domain samples resulting from block 160. A windowing function may also be applied to the samples after appending the cyclic prefix.

[0051] In block 164 the samples resulting from block 162 may be converted to analog, upconverted to RF, amplified, and transmitted into the channel 120 during a OFDM symbol period that is approximately (e.g., within circuit tolerances) $(C+\Delta)/BW$.

[0052] FIG. 2A is a diagram of an example OFDM receiver. The example receiver 200 comprises a front-end 202, a cyclic prefix and windowing circuit 204, a serial-to-parallel conversion circuit 208, a frequency correction circuit 206, a fast Fourier transform (FFT) circuit 210, a per-tone equalizer 212, a phase correction circuit 214, a parallel-to-serial conversion circuit 216, a decoding circuit 218, a controlled combined inter-symbol correlation (ISC) and/or inter-subcarrier interference (ICI) model (Controlled ISCI Model) circuit 220, a carrier recovery loop circuit 222, a FEC decoder circuit 232, and a performance indicator measurement circuit 234.

[0053] The receiver front-end 202 may be operable to amplify, downconvert, and/or digitize the signal 121 to generate the signal 203. Thus, the receiver front-end 202 may comprise, for example, a low-noise amplifier, a mixer, and/or an analog-to-digital converter. The front-end 202 may, for example, sample the received signal 121 at least $C+\Delta$ times per OFDM symbol period. Due to non-idealities, the receiver front-end 202 may introduce non-linear distortion and/or phase noise to the signal 203. The non-linearity of the front end 202 may be represented as NL_{Rx} which may be, for example, a polynomial, or an exponential (e.g., Rapp model). The non-linearity may incorporate memory (e.g., Volterra series).

[0054] The circuit 204 may be operable to process the signal 203 to generate the signal 205. The processing may include, for example, removal of a cyclic prefix. Additionally, or alternatively, the processing may include application of a windowing function to compensate for artifacts that may result from use of an FFT on a signal that is not periodic over the FFT window. Windowing applied in the transmitter 100 may be instead of, or in addition to, windowing applied in a receiver. The output of the circuit

204 may comprise C samples of the received signal corresponding to a particular OFDM symbol received across $C+\Delta$ subcarriers.

[0055] The frequency correction circuit 206 may be operable to adjust a frequency of signal 205 to compensate for frequency errors which may result from, for example, limited accuracy of frequency sources used for up and down conversions. The frequency correction may be based on feedback signal 223 from the carrier recovery circuit 222.

[0056] The serial-to-parallel conversion circuit 208 may be operable to convert C time-domain samples output serially as the signal 207 to C time-domain samples output in parallel as signals 209.

[0057] In an example implementation, the subcarrier values output by the decimation circuit 108 may be interleaved prior to being input to the circuit 112 and/or the circuit 110 may perform interleaving of the inputted subcarrier values. This interleaver may be operable to improve the tolerance to frequency selective fading caused by multipath that may impose wide notch that spans over several subcarriers. In this case the interleaver may be used to "spread" the notch over non-consecutive (interleaved) subcarriers and therefore reduce the impact of the notch on decoding performance.

[0058] Each of the signals 203, 205, 207, and 209 may be time-domain signals. The fast Fourier transform (FFT) circuit 210 may be operable to convert the time-domain samples conveyed as signals 209 to C physical subcarrier values conveyed as signals 211.

[0059] The per-tone equalizer 212 may be operable to perform frequency-domain equalization of each of the C physical subcarrier values to compensate for non-idealities (e.g., multipath, additive white Gaussian noise, (AWGN), etc.) experienced by a corresponding one of the C OFDM subcarriers. In an example implementation, the equalization may comprise multiplying a sample of each of signals 211 by a respective one of C complex coefficients determined by the equalization circuit 212. Such

coefficients may be adapted from OFDM symbol to OFDM symbol. Adaption of such coefficients may be based on decisions of decoding circuit 218. In an example implementation, the adaptation may be based on an error signal 221 defined as the difference, output by circuit 230, between the equalized and phase-corrected samples of signal 217 and the corresponding reconstructed signal 227b output by the decoding circuit 218. Generation of the reconstructed signal 227b may be similar to generation of the reconstructed signal 203 in the above-incorporated U.S. Patent Application No. 13/754,964 (but modified for the OFDM case, as opposed to the single-carrier case described therein) and/or as described below with reference to FIG. 2D.

[0060] The phase correction circuit 214 may be operable to adjust the phase of the received physical subcarrier values. The correction may be based on the feedback signal 225 from the carrier recovery circuit 222 and may compensate for phase errors introduced, for example, by frequency sources in the front-end of the transmitter and/or the front-end 202 of the receiver.

[0061] The parallel-to-serial conversion circuit 216 may convert the C physical subcarrier values output in parallel by circuit 214 to a serial representation. The physical subcarrier values bits may then be conveyed serially to the decoding circuit 218. Alternatively, 216 may be bypassed (or not present) and the decoding at 218 may be done iteratively over the parallel (vector) signal 215.

[0062] The controlled ISCI model circuit 220 may be operable to store tap coefficients $\underline{p}$ and/or nonlinearity model $\widehat{NL}$. The stored values may, for example, have been sent to the receiver 200 by the transmitter 100 in one or more control messages. The controlled ISCI model circuit 220 may be operable to convert a time-domain representation of a nonlinearity model to a frequency domain representation. The circuit 220 may, for example, store (e.g., into a look-up table) multiple sets of filter coefficients and/or nonlinearity models and may be operable to dynamically select (e.g., during

operation based on recent measurements) the most appropriate one(s) for the particular circumstances.

[0063] The decoding circuit 218 may be operable to process the signal 217 to recover symbols carried therein. In an example implementation, the decoding circuit 218 may be an iterative maximum likelihood or maximum a priori decoder that uses symbol slicing or other techniques that enable estimating individual symbols rather than sequences of symbols. In another example implementation, the decoding circuit 218 may be a sequence estimation circuit operable to perform sequence estimation to determine the C' symbols that were generated in the transmitter corresponding to the received OFDM symbol. Such sequence estimation may be based on maximum likelihood (ML) and/or maximum a priori (MAP) sequence estimation algorithm(s), including reduced-complexity (e.g., storing reduced channel state information) versions thereof. The decoding circuit 218 may be able to recover the C' symbols from the C physical subcarriers (where $C' > C$) as a result of the controlled inter-symbol correlation and/or aliasing that was introduced by the transmitter (e.g., as a result of processing by ISC generation 104 and/or the aliasing introduced by the decimation circuit 108). The decoding circuit 218 may receive, from circuit 220, a frequency-domain controlled ISCI model which may be based on non-linearity, phase noise, and/or other non-idealities experienced by one or more of the C physical subcarrier values arriving at the decoding circuit 218.

[0064] The decoding circuit 218 may operate iteratively to improve decoding performance (e.g., as measured by SER, BER, packet error rate, and/or another metric) by using side information such as feedback from the error correction (FEC) decoder regarding location(s) of errors within vectors output on signal 219 by the decoding circuit 218 (e.g., index of virtual subcarrier(s) for which the decoding circuit 218 output an erroneous value) and symbols reliability indication such as log-likelihood ratios (LLR)

("turbo decoding"). In the decoding circuit 218, use of the controlled ISCI model output by circuit 220 may introduce correlation between subcarriers that are relatively far from each other (e.g., a correlation between a lower-frequency subcarrier assigned an index 2 and higher-frequency subcarrier assigned an index 45). A forward sequence estimation may operate from a low-index subcarrier to a high-index subcarrier (e.g., starting at subcarrier 1 moving to 2, then 3, etc., possibly up to C).

[0065] In an example implementation, when the forward sequence estimation operates at subcarrier c ($1 \leq c \leq C$, where C is the number of data-carrying subcarriers in the OFDM symbol)), it may consider all ISCI model elements lower than c , and K elements above it (i.e., elements 1 to $c+K$), where K is an integer. In such an example implementation, K may typically be less than 10.

[0066] In an example implementation, when the sequence estimation does not use distant ISCI model elements in the first sequence estimation trial, additional iterations may be used to improve decoding performance by enabling utilization of the distant ISCI elements. For example, the first iteration may utilize close ISCI elements (e.g., elements within K elements of element c) while the distant ISCI elements (beyond K elements from element c) introduce interference. The second iteration may use the decoded sequence of the first iteration as a hypothesis for use with the distant ISCI model elements. Additional iterations (e.g., a third iteration, a fourth iteration, etc.) may be used to better utilize the distant ISCI model elements and to improve decoding performance.

[0067] It is also possible to perform a backwards sequence estimation operating in the opposite direction. The backwards sequence estimation may start from the other side of the OFDM symbol (e.g., from subcarrier having index C down to subcarrier having index 1 assuming that the forward sequence estimation is starting at subcarrier having index 1 progressing to subcarrier having index C). The forward and backward sequence estimations may operate concurrently or in series and each of the sequence estimations

may use the estimated symbols of other direction as candidates for its own estimation. Additionally, the forward and backward estimations may provide each other the contribution of the distant ISCI model elements by using each other's estimated symbols. The iterations may stopped when the total number of iterations exceeds a predefined value or upon a dynamic decoding performance indication such as SER, BER, packet error rate, MSE, and/or the like reaching a determined threshold.

[0068] The decoding circuit 218 may use the controlled ISCI model to calculate metrics similar to the manner in which a model is used to calculate metrics in above-incorporated U.S. Patent Application Serial No. 13/754,964 (but modified for the OFDM case as opposed to the single-carrier case described therein) and/or as described below with reference to FIG. 2C. The decoding circuit 218 may also use the controlled ISCI model provided by circuit 220 to generate signals 227a and 227b, as described herein. In an example implementation, the decoding circuit 218 is operable to accept at its input C equalized and phase-corrected physical subcarrier values and generate LLR values associated with the bits of the C' constellation symbols that where originally loaded over the virtual subcarriers of the WAM-OFDM transmitter. The LLRs may be generated by checking multiple hypotheses of C' constellation symbols based on the received samples. The best hypothesis may be used to generate the symbols and hard bits detection. In case of using a soft error correction code, an LLR interface that reflects the reliability of the bits (analog signal) rather than the hard bits (i.e., "0", "1") may be used. A remaining one or more of the hypotheses (the second-best, third-best, etc.) may be used to generate the LLR values. For example, assuming that a particular bit was detected as "1" according to the best hypothesis, the LLR for this bit may be provided from the distance of the best hypothesis to the second best hypothesis that estimates this particular bit as "0". The LLR values for the different virtual subcarriers may be weighted according to their respective SNR. In case of frequency-selective fading channel, each subcarrier may have

a different gain that corresponds to a different SNR per subcarrier. Because LLR value reflects the bit reliability, in an example implementation, the LLRs may be weighted according to the appropriate subcarrier gain to achieve Maximum Likelihood performance. In an example implementation, log-likelihood ratios (LLRs) determined in a receiver (e.g., in circuit 218) may have a noise variance component that varies with subcarrier. This may be because the per-subcarrier channel gain (due, for example, to the analog channel selection filter circuits and channel) may vary with frequency but the RF front-end gain at the receiver may be fixed.

[0069] For each received OFDM symbol, the circuit 220 may generate a frequency-domain controlled ISCI model of the channel over which the OFDM symbol was received. The controlled ISCI model of 220 may account for non-linear distortion experienced by the received OFDM symbol, phase noise experienced by the received OFDM symbol, and/or other non-idealities. For example, a third-order time domain distortion may be modeled in the frequency domain as:

$$\begin{aligned} y(t) &= x(t) \cdot (1 - r \cdot e^{j\varphi} \cdot |x(t)|^2) \\ &= x(t) - r \cdot e^{j\varphi} \cdot x(t) \cdot x^*(t) \cdot x(t) \end{aligned}$$

$$Y(\omega) = X(\omega) - r \cdot e^{j\varphi} \cdot X(\omega) \otimes X^*(-\omega) \otimes X(\omega),$$

where:

$x(t), X(\omega)$ - are the input signal in the time domain and frequency domain, respectively;

$y(t), Y(\omega)$ - are the distorted output signal in the time domain and frequency domain, respectively;

$r \cdot e^{j\varphi}$ - is the complex distortion coefficients;

$()^*$ - denotes complex conjugate operator; and

$\otimes$ - stands for the convolution operator.

[0070] The carrier recovery loop circuit 222 may be operable to recover phase and frequency of one or more of the C OFDM subcarriers of the channel 120. The carrier recovery loop 222 may generate a frequency error signal 223 and a phase error signal 225. The phase and/or frequency error may be determined by comparing physical subcarrier values of signal 217 to a reconstructed signal 227a. Accordingly, the frequency error and/or phase error may be updated from OFDM symbol to OFDM symbol. The reconstructed signal 227b may be generated similar to the manner in which the reconstructed signal 207 of the above-incorporated U.S. Patent Application No. 13/754,964 (but modified for the OFDM case, as opposed to the single-carrier case described therein) and/or as described below with reference to FIG. 2D.

[0071] The performance indicator measurement circuit 234 may be operable to measure, estimate, and/or otherwise determine characteristics of received signals and convey such performance measurement indications to a transmitter collocated with the receiver 200 for transmitting feedback to the remote side. Example performance indicators that the circuit 234 may determine and/or convey to a collocated transmitter for transmission of a feedback signal include: signal-to-noise ratio (SNR) per subcarrier (e.g., determined based on frequency-domain values at the output of FFT 210 and corresponding decisions at the output of the decoding circuit 218 and/or FEC decoder 232), symbol error rate (SER) (e.g., measured by decoding circuit 218 and conveyed to the circuit 234), and/or bit error rate (BER) (e.g., measured by the FEC decoder and conveyed to the circuit 234).

[0072] FIGS. 2B and 2C depict a flowchart describing operation of an example implementation of a highly-spectrally-efficient OFDM receiver. The process begins with block 242 in which an OFDM symbol arrives, as signal 121, at front-end 202 and is amplified, down-converted, and digitized to generate $C+\Delta+P$ time-domain samples of the OFDM symbol, where P is the size of the cyclic prefix.

[0073] In block 244, the cyclic prefix may be removed and a windowing function may be applied.

[0074] In block 246, frequency correction may be applied to the time-domain samples based on an error signal 223 determined by the carrier recovery circuit 222.

[0075] In block 248, the frequency-corrected time-domain samples are converted to frequency-corrected frequency-domain physical subcarrier values by the FFT circuit 210.

[0076] In block 250, the frequency-corrected physical subcarrier values output by the FFT are equalized in the frequency domain by the per-subcarrier equalizer circuit 212.

[0077] In block 252, one or more of the frequency-corrected and equalized physical subcarrier values are phase corrected based on a phase correction signal 225 generated by the carrier recovery circuit 222.

[0078] In block 254, the vector of C frequency-corrected, equalized, and phase-corrected received physical subcarrier values is input to decoding circuit 218 and sequence estimation is used to determine the best estimates of the vector of C' symbols that resulted in the vector of C frequency-corrected, equalized, and phase-corrected received physical subcarrier values. Example details of metric generation performed during the sequence estimation are described below with reference to FIG. 2C.

[0079] In block 256, the best estimate of the vector of C' symbols is determined by decoding circuit 218 and is output as signal 219 to FEC decoder 232, which outputs corrected values on signal 233. Example details of selecting the best candidate vector are described below with reference to FIG. 2C.

[0080] Referring to FIG. 2C, in block 262, the decoding circuit 218 generates a plurality of candidate vectors (each candidate vector corresponding to a possible value of

the vector of C' symbols generated by the transmitter), and generates a corresponding plurality of reconstructed physical subcarrier vectors by applying the controlled ISCI model to the candidates.

[0081] In block 264, the reconstructed physical subcarrier vectors are compared to the vector of frequency-corrected, equalized, and/or phase-corrected received physical subcarrier values to calculate metrics.

[0082] In block 266, the candidate vector corresponding to the best metric is selected as the best candidate, and the C' symbols of the best candidate are output as signal 219, to, for example, FEC decoder 232 and/or an interleaver (not shown).

[0083] FIG. 2D depicts a flowchart describing operation of an example decoding circuit of a highly-spectrally-efficient OFDM receiver. The flowchart begins with block 272 in which a vector of C received physical subcarrier values arrive at decoding circuit 218.

[0084] In block 274, the best candidate vector is determined to a first level of confidence. For example, in block 274, the best candidate vector may be determined based on a first number of iterations of a sequence estimation algorithm.

[0085] In block 276, the controlled ISCI model may be applied to the best candidate vector determined in block 274 to generate reconstructed signal 227a.

[0086] In block 278, the best candidate vector is determined to a second level of confidence. For example, the best candidate determined in block 278 may be based on a second number of iterations of the sequence estimation algorithm, where the second number of iterations is larger than the first number of iterations.

[0087] In block 280, the controlled ISCI model may be applied to the best candidate determined in block 278 to generate reconstructed signal 227b.

[0088] In block 282, coefficients used by the equalizer 212 are updated/adapted based on the reconstructed signal 227b determined in block 280.

[0089] In block 284, subsequent received physical subcarrier values are equalized based on the coefficients calculated in block 282.

[0090] Blocks 286 and 288 may occur in parallel with blocks 278–284.

[0091] In block 286, the carrier recovery loop 222 may determine frequency and/or phase error based on signal 227a calculated in block 276.

[0092] In block 288, samples received during a subsequent OFDM symbol period may be frequency corrected based on the error determined in block 286 and/or subsequent received physical subcarrier values are phase corrected based on the error determined in block 286.

[0093] FIG. 4 is a flowchart depicting an example iterative sequence estimation process for highly-spectrally-efficient OFDM communications. The sequence estimation process begins in block 402.

[0094] In block 404, an indexes i for forward sequence estimation and j for backward sequence estimation are initialized to 0 and C , respectively.

[0095] In block 406, the indexes i and j are incremented and decremented, respectively.

[0096] In block 408, if i is less than or equal to C and j is greater than or equal to zero, then in block 410, forward candidates and backward candidates are generated by the decoding circuit 218.

[0097] In block 412, the forward candidates from the most-recent execution of block 410, the backward candidates from the most-recent execution of block 410, and candidates during a most-recent execution of block 420 are merged. The merger may be

at the point where the forward and backward sequence estimations that are operating at opposite directions pass each other (e.g., $i=j$). Following that point (e.g., $i \geq j$), the sequence estimations overlap each other and symbol candidates (e.g., survivors) may be exchanged to attempt satisfaction of the sequence estimation cost function (e.g., ML, MAP, or other). Additionally, the forward candidates from the most-recent execution of block 410 may be merged with the previous symbol candidates (e.g., survivors) of the backward estimation, and the backward candidates from the most-recent execution of block 410 may be merged with the previous symbol candidates (e.g., survivors) of the forward estimation.

[0098] In an example implementation, without using the merge of candidates, only controlled ISCI model elements that are within K elements above element i (e.g., ISCI model elements having indexes from 1 to $i+K$) may be applied to the forward candidates, and only controlled ISCI model elements that are less than K elements away from element j (e.g., ISCI model elements having indexes from $j-K$ to C) may be applied to the backward candidates.

[0099] In an example implementation, when using the merged candidates, the ISCI model elements that are beyond K indices away of i, j (e.g., elements having higher index than $i+k$ and elements having lower index than $j-k$) may be used to improve the utilization of the ISCI model and to improve decoding performance. Assuming that the merge is realized between forward and backward most-recent executions, then the full ISCI model may be applied (using all the ISCI model elements) from the point that the forward and backward executions (that operate at opposite directions) are meeting each other (e.g., $i=j$) and beyond.

[00100] In block 414, in an example implementation, the controlled ISCI model is applied to the merged candidates to generate reconstructed physical subcarrier vectors.

The candidates or the survivor paths from the previous iteration for both forward and backward sequence estimation may apply the full ISCI model.

[00101] In block 416, a metric is calculated for each of the reconstructed candidates generated in block 414.

[00102] In block 418, a best one or more candidate(s) is/are selected based on the metrics generated in block 418.

[00103] Returning to block 408, if i is not less than or equal to C or j is not greater than or equal to zero, then, in block 422, it is determined whether a maximum number of iterations have been performed for the current OFDM symbol. If so, then the process ends in block 424 and the best candidate during the most-recent execution of block 418 is output. If not, then in block 420 the best candidate(s) during the most-recent execution of block 418 are saved and the process returns to block 404 for another iteration.

In an example implementation, a receiver may comprise: a front-end circuit (e.g., 202) operable to receive an orthogonal frequency division multiplexing (OFDM) symbol on a first number (e.g., C) of physical subcarriers; a decoding circuit (e.g., 218) operable to perform decoding of the OFDM symbol using an inter-symbol correlation and/or inter-subcarrier interference (ISCI) model (e.g., provided by 220), the decoding resulting in determination of a sequence of a second number (e.g., C') of symbols that most-likely corresponds to the OFDM symbol, where the second number is greater than the first number. The circuitry may receive OFDM symbols via a channel having a significant amount of nonlinearity. The significant amount of nonlinearity may be such that it degrades, relative to a perfectly linear channel, a performance metric in said receiver by less than 1dB, whereas, in a full response communication system, it would degrade, relative to a perfectly linear channel, the performance metric by 1dB or more. The sequence of symbols may comprise N-QAM symbols, N being an integer. The decoding circuit may be based on maximum likelihood (ML) or maximum a priori (MAP)

sequence estimation. The decoding may use reduced-state sequence estimation. The decoding circuit may be based on iterative decoding. The iterative decoding may use feedback from an FEC decoder (e.g., 232), the feedback may comprising one or both of: error location information and log likelihood ratios. The iterative decoding may comprises a forward sequence estimation that progresses from a first of the physical subcarriers to a second of the physical subcarriers, and may comprise a backward sequence estimation that progresses from the second of the physical subcarriers to the first of the physical subcarriers. The iterative decoding may comprise exchanging elements between a first symbol candidate or survivor and a second symbol candidate or survivor. The ISCI model is based, at least in part, on non-linearity experienced by the OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by the receiver. The ISCI model may be based, at least in part, on phase-noise introduced to the OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by the receiver.

[00104] The ISCI model may be a frequency domain model. The receiver may comprise an equalizer circuit operable to perform per-subcarrier equalization of the physical subcarriers, wherein coefficients used for the per-subcarrier equalization are adapted based on a reconstructed signal generated using the ISCI model. The decoding circuit may be operable to generate the reconstructed signal by application of the ISCI model to a sequence of symbols corresponding to a previous OFDM symbol, a number of symbols in the sequence of symbols corresponding to the previous OFDM symbol being equal to the second number. The decoding circuit may be operable to: generate a first feedback signal (e.g., 227a) to be used for phase and/or frequency correction of the physical subcarriers. The decoding circuit may be operable to generate a second feedback signal (e.g., 227b) to be used for adapting coefficients of an equalizer.

[00105] The decoding circuit may comprise a sequence estimation circuit. The sequence estimation circuit may be operable to generate the first feedback signal using the ISCI model and a best candidate vector determined from a first number of iterations of a sequence estimation algorithm. The sequence estimation circuit may be operable to generate the second feedback signal using the ISCI model and a best candidate vector determined from a second number of iterations of the sequence estimation algorithm. The first number of iterations may be less than or equal to the second number of iterations. The performance of the decoding of the OFDM symbol may comprise generating a plurality of candidate vectors, each of the candidate vectors being a possible vector corresponding to the sequence of the second number of symbols. The performance of the decoding of the OFDM symbol may comprise applying the ISCI model to the candidate vectors to generate a plurality of reconstructed subcarrier vectors. The performance of the decoding of the OFDM symbol may comprise comparing the reconstructed subcarrier vectors to a vector of equalized received subcarrier values generated from the OFMD symbol. The circuitry may be operable to measure one or more performance indicators (e.g., signal-to-noise ratio, bit error rate, symbol error rate, packet error rate, or the like) for the OFDM symbol such that the one or more performance indicators may be transmitted as feedback to a device which transmitted the OFDM symbol. The decoding may seek to achieve a target symbol error rate, target bit error rate, and/or target packet error rate in presence of additive white Gaussian noise and a dynamic frequency selective fading channel.

[00106] Other implementations may provide a non-transitory computer readable medium and/or storage medium, and/or a non-transitory machine readable medium and/or storage medium, having stored thereon, a machine code and/or a computer program having at least one code section executable by a machine and/or a computer,

thereby causing the machine and/or computer to perform the processes as described herein.

[00107] Methods and systems disclosed herein may be realized in hardware, software, or a combination of hardware and software. Methods and systems disclosed herein may be realized in a centralized fashion in at least one computing system, or in a distributed fashion where different elements are spread across several interconnected computing systems. Any kind of computing system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware and software may be a general-purpose computing system with a program or other code that, when being loaded and executed, controls the computing system such that it carries out methods described herein. Another typical implementation may comprise an application specific integrated circuit (ASIC) or chip with a program or other code that, when being loaded and executed, controls the ASIC such that it carries out methods described herein.

[00108] While methods and systems have been described herein with reference to certain implementations, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present method and/or system. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present disclosure without departing from its scope. Therefore, it is intended that the present method and/or system not be limited to the particular implementations disclosed, but that the present method and/or system will include all implementations falling within the scope of the appended claims.

CLAIMS

What is claimed is:

1. Circuitry for use in a receiver, said circuitry comprising:
 - a front-end circuit operable to receive an orthogonal frequency division multiplexing (OFDM) symbol on a first number of physical subcarriers;
 - a decoding circuit operable to perform decoding of said OFDM symbol using an inter-symbol correlation and/or inter-subcarrier interference (ISCI) model, said decoding resulting in determination of a sequence of a second number of symbols that most-likely corresponds to said OFDM symbol, where said second number is greater than said first number.
2. The method of claim 1, wherein:
 - said circuitry receives OFDM symbols via a channel having a significant amount of nonlinearity;
 - said significant amount of nonlinearity degrades a performance metric in said receiver by less than 1dB, relative to a perfectly linear channel; and
 - in a full response communication system, said significant amount of nonlinearity would degrade said performance metric by 1dB or more, relative to a perfectly linear channel.
3. The circuitry of claim 1, wherein said sequence of symbols comprises N-QAM symbols, N being an integer.
4. The circuitry of claim 1, wherein said decoding circuit is based on maximum likelihood (ML) or maximum a priori (MAP) sequence estimation.

5. The circuitry of claim 1, wherein said decoding uses reduced-state sequence estimation.

6. The circuitry of claim 1, wherein said decoding circuit is based on iterative decoding.

7. The circuitry of claim 6, wherein said iterative decoding uses feedback from an FEC decoder, said feedback comprising one or both of: error location information and log likelihood ratios.

8. The circuitry of claim 6, wherein said iterative decoding comprises exchanging elements between a first symbol candidate or survivor and a second symbol candidate or survivor.

9. The circuitry of claim 1, wherein said ISCI model is based, at least in part, on non-linearity experienced by said OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by said receiver.

10. The circuitry of claim 1, wherein said ISCI model is based, at least in part, on phase-noise introduced to said OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by said receiver.

11. The circuitry of claim 1, wherein ISCI model is a frequency domain model.

12. The circuitry of claim 1, comprising an equalizer circuit operable to perform per-subcarrier equalization of said physical subcarriers, wherein coefficients used for said

per-subcarrier equalization are adapted based on a reconstructed signal generated using said ISCI model.

13. The circuitry of claim 12, wherein said decoding circuit is operable to generate said reconstructed signal by application of said ISCI model to a sequence of symbols corresponding to a previous OFDM symbol, a number of symbols in said sequence of symbols corresponding to said previous OFDM symbol being equal to said second number.

14. The circuitry of claim 1, wherein said decoding circuit is operable to:
generate a first feedback signal to be used for phase and/or frequency correction of said physical subcarriers; and
generate a second feedback signal to be used for adapting coefficients of an equalizer.

15. The circuitry of claim 14, wherein said decoding circuit comprises a sequence estimation circuit that is operable to:
generate said first feedback signal using said ISCI model and a best candidate vector determined from a first number of iterations of a sequence estimation algorithm;
generate said second feedback signal using said ISCI model and a best candidate vector determined from a second number of iterations of said sequence estimation algorithm; and
said first number of iterations is less than or equal to said second number of iterations.

16. The circuitry of claim 1, wherein said performance of said decoding of said OFDM symbol comprises:

generating a plurality of candidate vectors, each of said candidate vectors being a possible vector corresponding to said sequence of said second number of symbols;

applying said ISCI model to said candidate vectors to generate a plurality of reconstructed subcarrier vectors; and

comparing said reconstructed subcarrier vectors to a vector of equalized received subcarrier values generated from said OFMD symbol.

17. The circuitry of claim 1, wherein said circuitry is operable to measure one or more performance indicators for said OFDM symbol such that said one or more performance indicators may be transmitted as feedback to a device which transmitted said OFDM symbol.

18. The circuitry of claim 1, wherein said decoding seeks to achieve a target symbol error rate, target bit error rate, and/or target packet error rate in presence of additive white Gaussian noise and a dynamic frequency selective fading channel.

19. A method performed in an electronic receiver, the method comprising:

receiving a first orthogonal frequency division multiplexing (OFDM) symbol on a first number of physical subcarriers of a channel;

generating an inter-carrier interference (ICI) model that accounts for non-linear distortion experienced by said first OFDM symbol and phase noise experienced by said first OFDM symbol;

subsequent to receiving said first OFDM symbol, receiving a second OFDM symbol on said physical subcarriers of said channel; and

using at least part of said ISCI model in performing decoding of said second OFDM symbol to determine a sequence of a second number of symbols that most-likely correspond to said second OFDM symbol, where said second number and is greater than said first number.

20. The method of claim 19, wherein said performing said decoding of said second OFDM symbol comprises:

generating a plurality of candidate vectors, each of said candidate vectors being a possible vector corresponding to said sequence of symbols;
applying at least part of said ISCI model to said candidate vectors to generate a corresponding plurality of reconstructed virtual subcarrier vectors; and
determining a best reconstructed subcarrier vector by comparing said reconstructed subcarrier vectors to a vector of equalized received subcarrier values generated from said second OFDM symbol.

21. The method of claim 19, comprising adapting coefficients of an equalizer of said electronic receiver based on said best reconstructed subcarrier vector.

22. The method of claim 19, comprising phase correcting and frequency correcting said physical subcarriers based on said best reconstructed subcarrier vector.

23. The method of claim 19, wherein said sequence of symbols comprises N-QAM symbols, N being an integer.

24. The method of claim 19, comprising:

measuring one or more performance indicators for said first OFDM symbol; and

processing said one or more performance indicators such that said one or more performance indicators may be transmitted as feedback to a device which transmitted said first OFDM symbol.

25. The method of claim 19, wherein said decoding seeks to achieve a target symbol error rate, target bit error rate, and/or target packet error rate in presence of additive white Gaussian noise and a dynamic frequency selective fading channel.

26. A receiver comprising:

- a front-end circuit operable to receive an orthogonal frequency division multiplexing (OFDM) symbol on a first number of physical subcarriers;
- a sequence estimation circuit operable to perform a sequence estimation process on said OFDM symbol using at least part of an inter-carrier interference (ICI) model, said sequence estimation process resulting in a determination of a sequence of quadrature amplitude modulation (QAM) symbols that most-likely correspond to said received OFDM symbol, said sequence comprising a second number of symbols and said second number being greater than said first number.

27. The receiver of claim 26, wherein said ISCI model is based, at least in part, on non-linearity experienced by said OFDM symbol during transmission by a transmitter, propagation over a channel, and/or reception by said receiver.

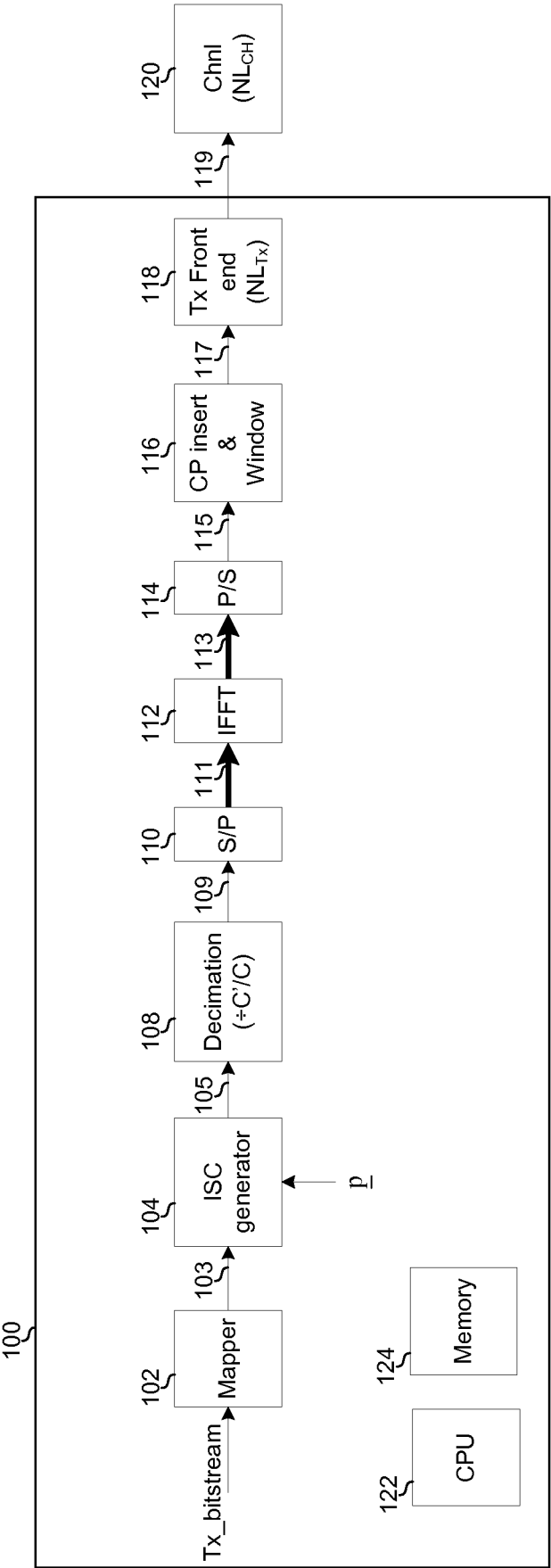


FIG. 1A

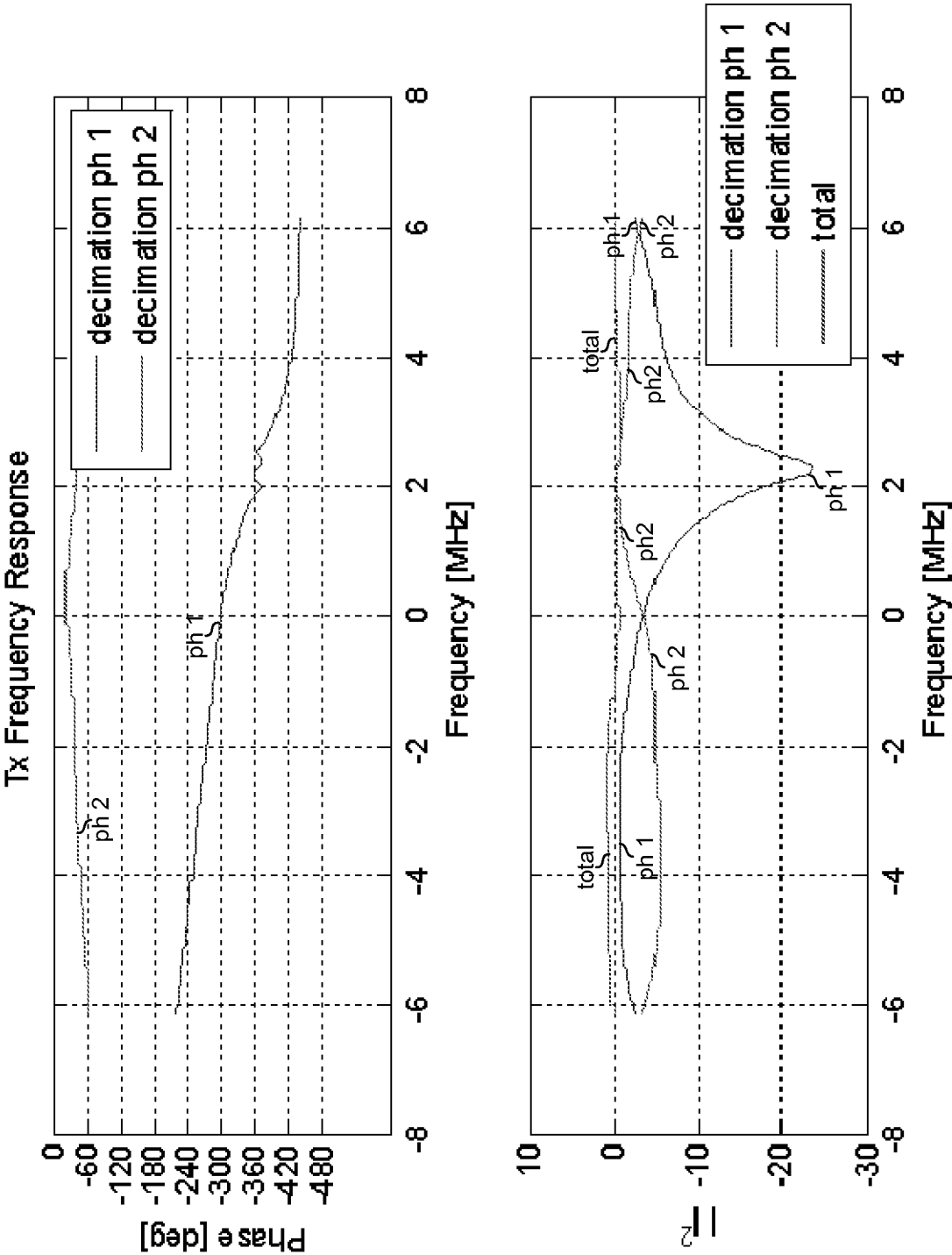


FIG. 1B

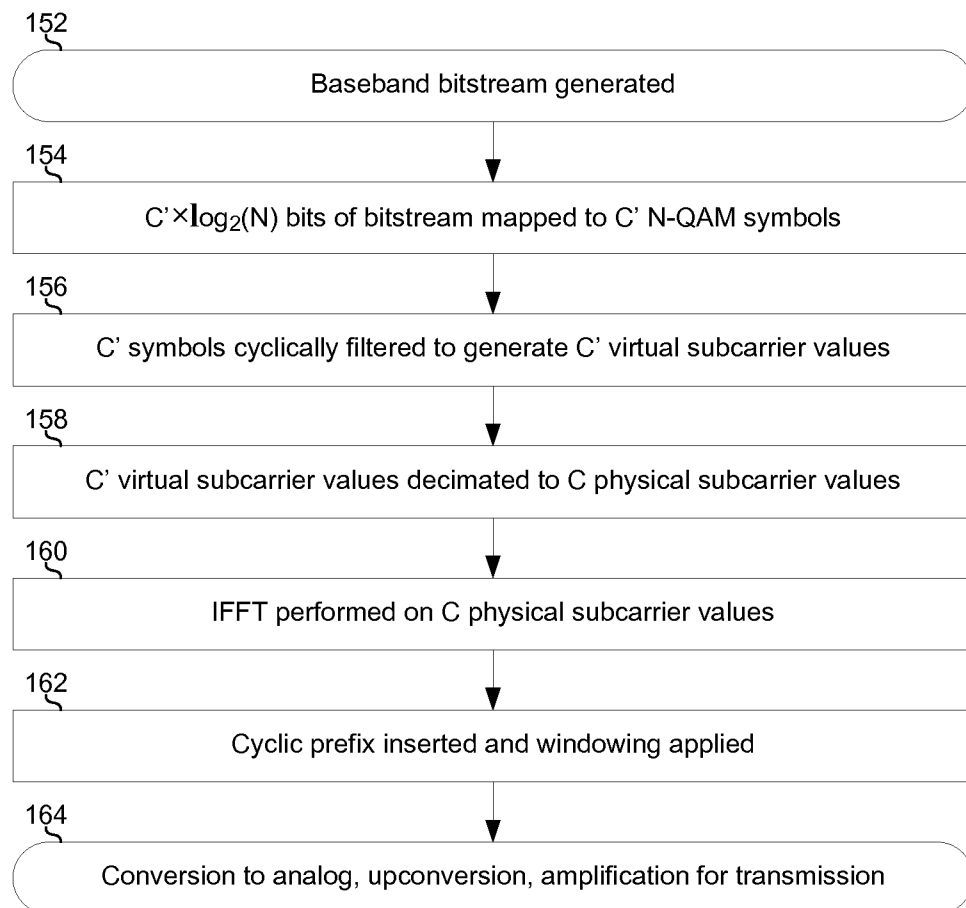


FIG. 1C

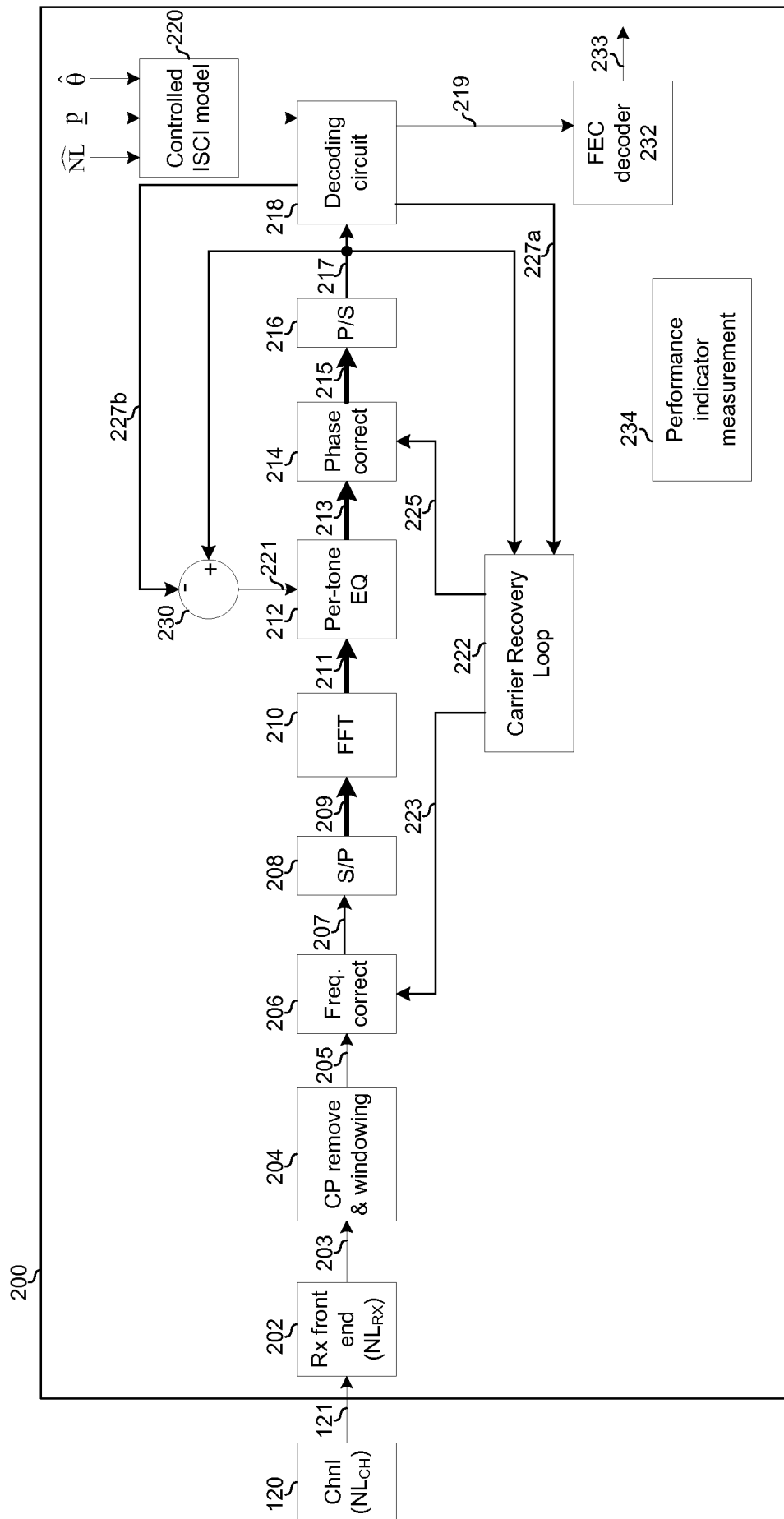


FIG. 2A

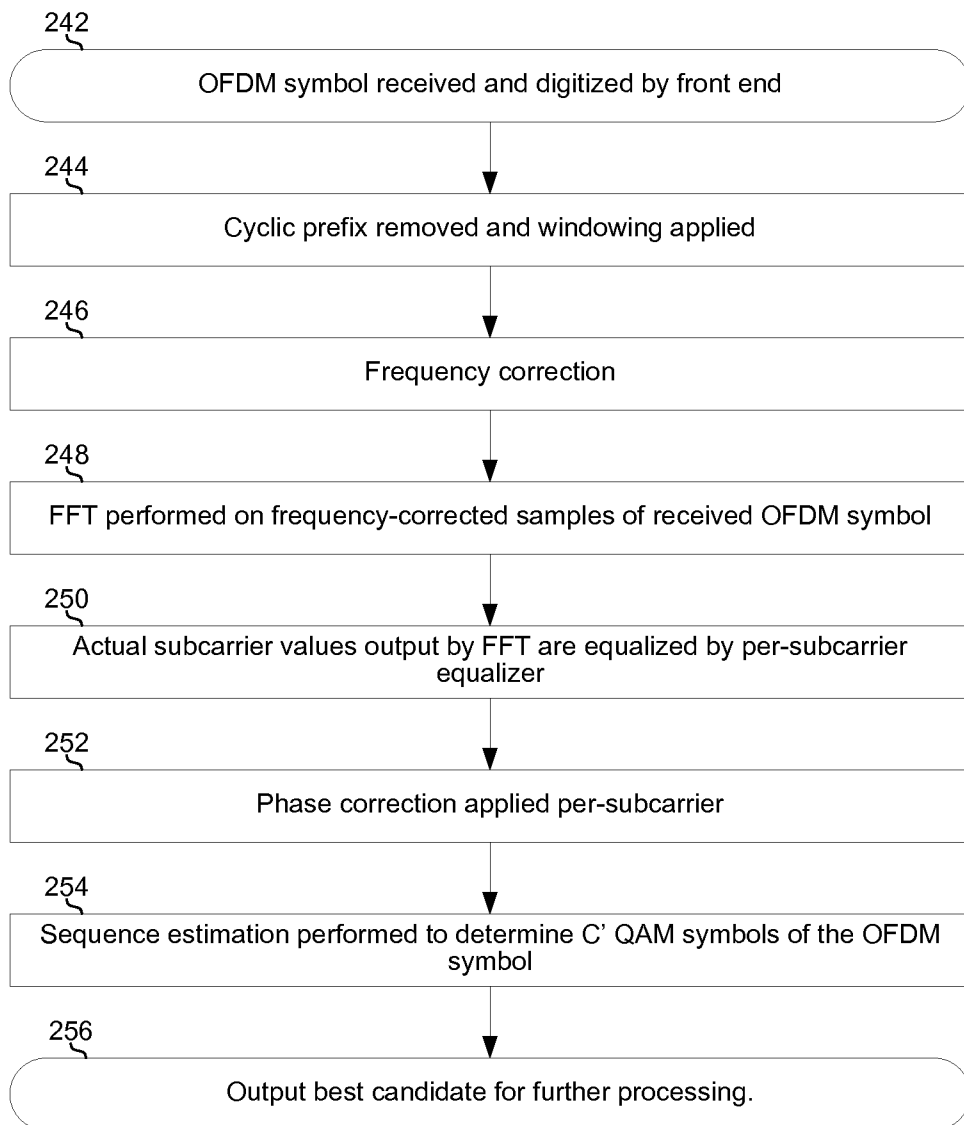
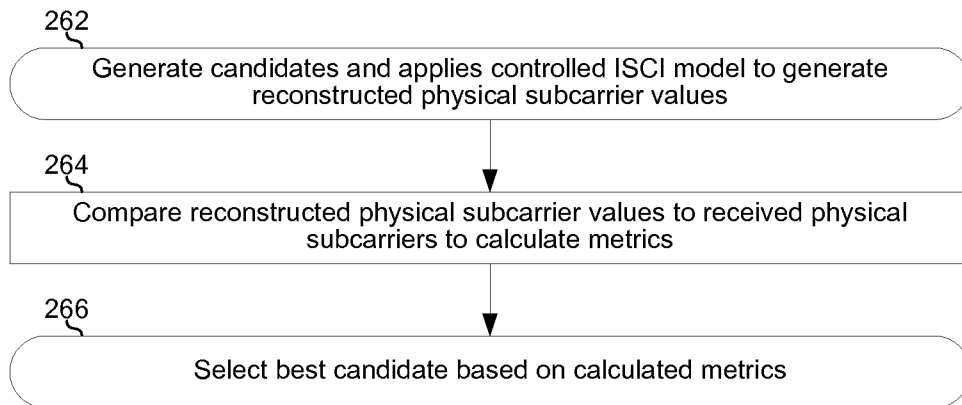


FIG. 2B

**FIG. 2C**

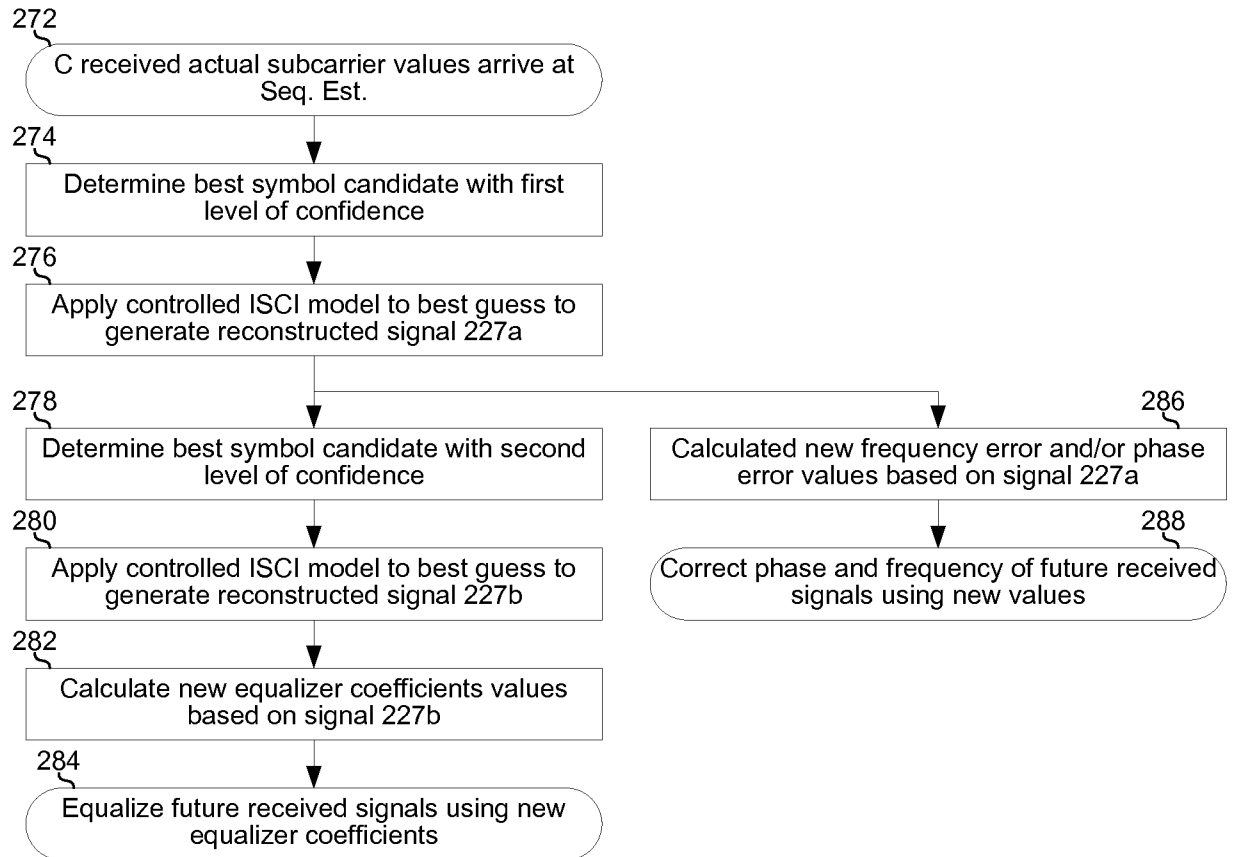
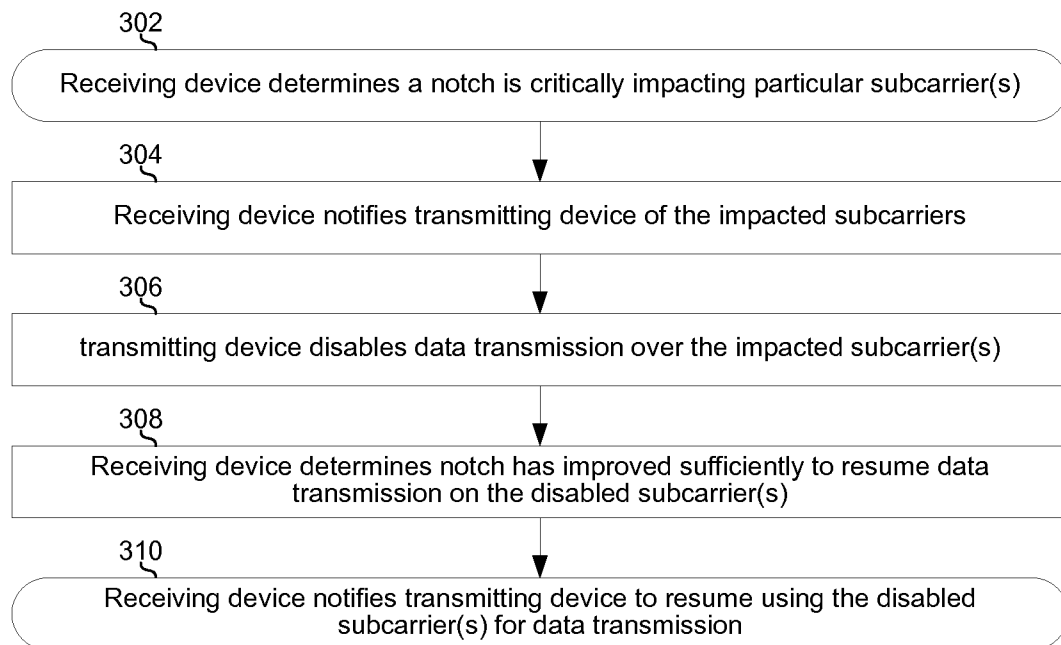


FIG. 2D

**FIG. 3**

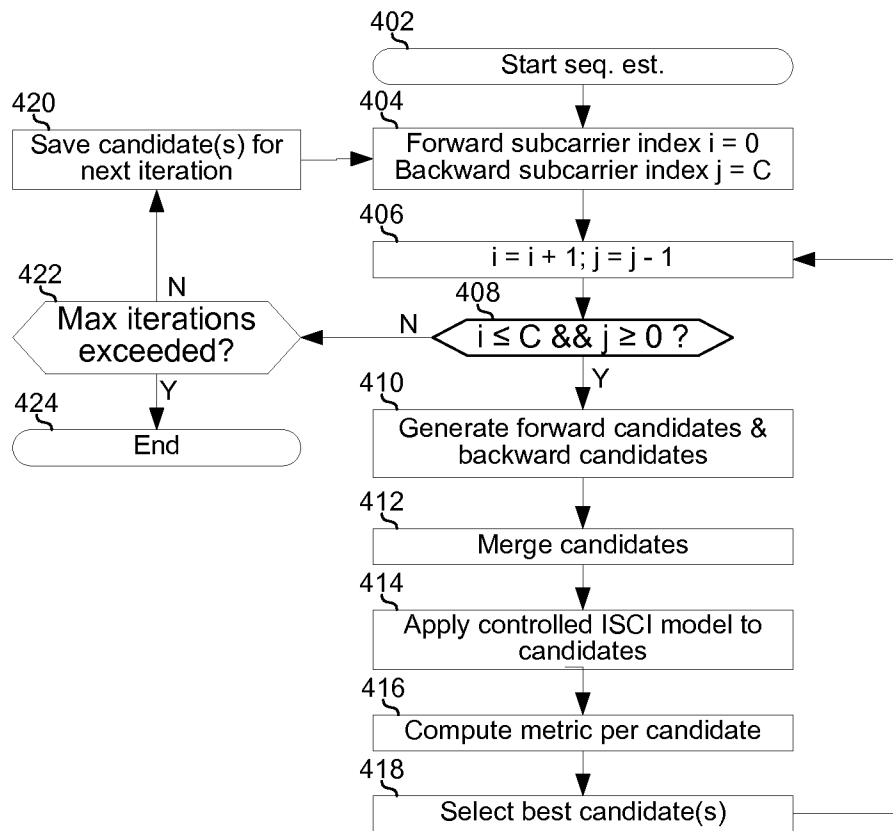


FIG. 4