



## SUBSTRATE SUPPORT FOR PLASMA ETCH OPERATIONS

### FIELD

[0001] Embodiments of the present invention generally relate to a semiconductor substrate processing.

### BACKGROUND

[0002] In processing a semiconductor substrate, the presence of contaminants on the substrate or a layer applied to a substrate can adversely affect subsequent processes or the performance of the finished semiconductor device. Contaminants can include undesirable oxides of metals applied to the substrate or residue from processes, such as mask residue from etching processes.

[0003] To remove the contaminants, substrate processing can include a non-selective etch process, for example, an etch using an ionized form of an inert gas such as argon. The etching process may take place in a chamber in which a plasma of an inert gas is formed above a substrate supported on a substrate support. In some cases the substrate support is coupled to a biasing radio frequency (RF) source to attract the argon molecules toward the substrate.

[0004] The inventors have observed that in etching procedures, non-uniformities in etch rate occur at the edge of the substrate. Under some processing conditions, the observed non-uniformities are significant and can adversely affect the substrate being processed.

[0005] Accordingly, the inventors have devised embodiments of substrate supports that may facilitate improved etch rate uniformity during plasma etching processes.

### SUMMARY

[0006] Methods and apparatus for processing substrates are disclosed herein. In some embodiments, a substrate support to support a substrate in a processing chamber comprises a dielectric insulator plate; a conductive plate supported on the dielectric insulator plate, the conductive plate comprising a top surface and a bottom surface defining a thickness between the top surface and the bottom surface, wherein an edge portion of the conductive plate tapers in a radially outward

direction; and a dielectric plate comprising a substrate support surface disposed upon the top surface of the conductor plate.

[0007] In some embodiments, a substrate processing apparatus includes a processing chamber having an internal processing volume; a radio frequency (RF) coil disposed proximate the process chamber to couple RF energy into the processing volume; a biasing RF source; and a substrate support as described in any of the embodiments disclosed herein disposed within the processing volume, wherein the conductive plate is coupled to the biasing RF source.

[0008] In some embodiments, a substrate support to support a substrate in a processing chamber includes a quartz dielectric insulator plate; a titanium conductive plate supported on the quartz dielectric insulator plate, the conductive plate comprising a top surface and a bottom surface defining a thickness between the top surface and the bottom surface, wherein the thickness tapers in a radially outward direction along an edge portion of the conductive plate; and a quartz or ceramic dielectric plate disposed upon a top surface of the conductor plate comprising a raised lip having an inner wall corresponding to a substrate support surface; wherein the quartz dielectric insulator plate includes a recess formed in a top surface thereof, the recess configured to accept the conductor plate and maintain contact with at least a portion of the bottom surface and a portion of the sidewall.

[0009] Other and further embodiments of the present invention are described below.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0010] Embodiments of the present invention, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the invention depicted in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0011] Figure 1 depicts a schematic side sectional view of a substrate support in accordance with some embodiments of the present invention.

[0012] Figure 2 depicts a schematic illustration of a substrate support within a processing chamber in accordance with some embodiments of this application.

[0013] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

### **DETAILED DESCRIPTION**

[0014] Methods and apparatus for processing substrates are disclosed herein. More specifically, embodiments of substrate supports that may beneficially affect the process uniformity proximate the edge of a substrate being etched (e.g., edge effects) are provided herein. By beneficially affecting the edge effect, embodiments of the present invention may provide a more uniform etch process across the substrate.

[0015] While not intended to be a limitation to the scope of the invention, the inventive apparatus disclosed herein may be particularly advantageous in process chambers configured to perform a plasma etch process, for example pre-clean chambers with argon sputtering capabilities. Examples of suitable plasma etch process chambers include any of the PC-XT® line of processing chambers, or the Preclean II line of preclean chambers, commercially available from Applied Materials, Inc., of Santa Clara, California. Other processing chambers from Applied Materials, Inc. or other manufactures may also benefit from the inventive apparatus disclosed herein.

[0016] Figure 1 is a schematic side sectional view of a substrate support 100 according to some embodiments of the present invention. The inventive substrate support comprises a dielectric insulator 102 (e.g., a dielectric insulator plate) which may comprise one or more process compatible materials including non-limiting examples such as quartz or ceramic.

[0017] The dielectric insulator 102 is sized to be at least as large as the substrate that will be supported on the substrate support 100 and has an top surface 106 and a bottom surface 103. In some embodiments, the dielectric insulator 102 may

include a centrally located recess 104 formed in an top surface 106 of the dielectric insulator 102. The recess 104 is configured to receive a conductive plate 108 (discussed more fully below) and to maintain contact with at least a portion of the conductive plate 108. The dielectric insulator 102 may be supported in vertical displacement or rotation, or both vertical displacement and rotation, on a support shaft 140.

[0018] The conductive plate 108 has a top surface 110 with a top edge 112 and a bottom surface 114 with a bottom edge 116 defining a thickness T between the top surface 110 and the bottom surface 114. The conductive plate 108 may have a tapered edge portion, that is, the thickness T decreases in a radially outward direction along a portion of the radius proximate the edge of the conductive plate 108. In the non-limiting embodiment illustrated in Figure 1, at the edge portion of the conductive plate 108, a generally upwardly sloped sidewall 118 connects the top edge 112 and bottom edge 116, with one or more straight or curved segments. The tapered edge may be a continuous or partially continuous transition, as illustrated in Figure 1, or it may be a stepped transition from the bottom edge 116 to the top edge 112 comprising one or more steps. In embodiments including curved segments, the curvature of the segments may be either concave or convex, and may be a combination of concave and convex segments.

[0019] In the non-limiting embodiment illustrated in Figure 1, the sidewall 118 includes two segments. A first sidewall segment 118a is inclined from the bottom edge 116 toward the top edge 112 at an angle of about 15 degrees to about 75 degrees, for example about 45 degrees. A second sidewall segment 118b connects the end of first sidewall segment 118a opposite the bottom edge 116 with the top edge 112. The second sidewall segment 118b, and additional segments if used (not shown), may extend at the same angle as the first sidewall segment 118a, or may extend at a different angle as illustrated. For example, in some embodiments, the second sidewall segment 118b, or the final sidewall segment adjacent the top surface 110, may extend substantially perpendicularly to the top surface 110.

[0020] In some embodiments, the recess 104 formed in the top surface 106 of the dielectric insulator 102 is configured to correspond with (e.g., to mate with) the

bottom surface 114 of the conductive plate 108. In the non-limiting embodiment illustrated in Figure 1, the recess 104 is configured to coaxially receive the conductive plate 108 such that the top surface 110 is coplanar with, substantially coplanar with, a portion of the top surface 106 of the dielectric insulator 102. In other embodiments, the top surface 110 may be disposed above or below the top surface 106.

[0021] The conductive plate 108 may be formed from materials conductive to at least RF energy, including non-limiting examples such as metallic materials such as, titanium or aluminum, or a doped ceramic. In some embodiments, the conductive plate 108 may be coupled to an RF biasing source (e.g., power source 109) through an RF conduit 111.

[0022] In some embodiments, a dielectric plate 120 is disposed on the top surface 110 of the conductive plate 108. The dielectric plate 120 may be fabricated of similar materials as the dielectric insulator 102. The outer periphery of the dielectric plate 120 may extend beyond the periphery of the conductive plate 108 and rest on a portion of the top surface 106 of the dielectric insulator 102. In some embodiments, the dielectric plate 120 may extend beyond the radial bounds, e.g., the outermost edge 122, of the dielectric insulator 102.

[0023] According to some embodiments, the dielectric plate 120 includes a raised lip 124 having an inner wall 126 defining a substrate support surface 128. The substrate support surface is configured to support a substrate, for example a 200mm, 300mm, or 450mm diameter semiconductor substrate, within the inner wall 126. In some embodiments, when the dielectric plate is disposed on the top surface 110 of the conductive plate 108, the tapered edge portion of the conductive plate 108 extends beyond the substrate support surface 128.

[0024] The dielectric plate 120 may include a first locating hole 130 aligned coaxially with a second locating hole 132 formed at least partially through the conductive plate 108. A first locating device, for example a first locating pin 136, may pass through the dielectric plate 120 such that the pin rests within the dielectric plate, at or below the substrate support surface 128, and the first locating pin 136 partially passes through the conductive plate 108 to position the dielectric plate 120

at least angularly with respect to the conductive plate 108. A third locating hole 134 may be formed at least partially through the dielectric plate 120 aligned coaxially with the first locating hole 130. A second locating device, for example a second locating pin 137, may pass through the dielectric insulator 102 and extend partially into the second locating hole 132 to at least angularly position the conductive plate 108 with respect to the dielectric insulator 102.

[0025] The first, second, and third locating holes 130, 132, and 134 need not be coaxially aligned in order to position the components of the substrate support. For alignment, adjacent elements, for example the dielectric plate 120 and the conductive plate 108, may have one or more axially aligned holes to accept a first locating pin 136. Similarly, the conductive plate 108 and the dielectric insulator 102 may have one or more axially aligned holes to accept a second locating pin 137. When used together, the locating holes and locating pins may provide at least radial alignment for the dielectric insulator 102, the conductive plate 108, and the dielectric plate 120.

[0026] The inventors have observed that a dielectric plate configured and positioned on the top surface of the conductive plate 108 as described above advantageously affects the formation of the plasma and has a beneficial effect on the etch rate uniformity at the edge of the substrate. The inventors have observed that a conductive plate 108 with a tapered edge that extends beyond the substrate support surface 128 may reduce the significance of the edge effects. Without being bound by theory, the inventors believe that the dielectric plate 120 improves uniformity of the plasma through diffusion or spreading of the electric field away from the edges of the conductive plate 108 below.

[0027] The substrate support may include a heater 150 to heat a substrate, when disposed on the substrate support 100, to a desired temperature. The heater 150 may be any type of heater suitable to provide control over the substrate temperature. For example, the heater 150 may be a resistive heater. In such embodiments, the heater 150 may be coupled to a power source 152 configured to provide the heater 150 with power to facilitate operating the heater 150. In some embodiments, the heater 150 may be embedded within one or more of the dielectric

insulator 102, the conductive plate 108, and the dielectric plate 120 of the substrate support 100. The heater 150 may also be located in the interface of the dielectric insulator 102 and the conductive plate 108, or at the interface of the conductive plate 108 and the dielectric plate 120. Alternatively, or in combination, in some embodiments, the heater 150 may be disposed above or proximate to the surface of the substrate support 100. The number and arrangement of the heater 150 may be varied to provide additional control over the temperature of the substrate 216 (Figure 2). For example, in embodiments where more than one heater is utilized, the heaters may be arranged in a plurality of zones to facilitate control over the temperature across the substrate 216, thus providing increased temperature control.

[0028] The inventors have observed that the edge effects typical of some current substrate supports adversely affect the substrate processing at the substrate edge. In general, during preclean processes or other etch or sputter-etch processes, the edge effects have been observed to cause a non-uniformity in the etch rate in which the substrate edge is more aggressively etched than other portions of the substrate.

[0029] Under some process conditions, and for some substrates, the increased etch rate at the edge of the substrate is insufficient to cause manufacturing concerns. However, in some processes, for example processes using a biasing radio frequency (RF) energy source, the non-uniformity cannot be tolerated and current techniques cannot adequately correct the condition. In some processes, such as high bias processes using certain hardware configurations in which the conductive plate is supplied with about 500W to about 1kW of biasing RF power, the edge effect at the substrate edge is sufficient to cause manufacturing concerns with process non-uniformity. In other situations on other hardware configurations, a high bias condition can exist when the biasing power exceeds about 50% of the system capability. In other embodiments, high bias may have different characteristics, but in all cases, as the bias power applied to the substrate support increases to a level desirable for other processing considerations, the non-uniformity at the substrate edge becomes problematic.

[0030] In cases of high bias, an undesirable non-uniformity condition exists at the edge in an amount sufficient to affect the yield of semiconductors produced from the

substrate. The non-uniformity cannot be tolerated in commercialized and cannot be adequately controlled to an acceptable level using current equipment.

[0031] The inventive substrate support disclosed herein can favorably modify the higher etch rate at the edge of the substrate noted on typical substrate supports. Test results have shown that the present substrate support may reduce the etch nonuniformity caused by the edge effect to an acceptable level, even under high bias conditions. Results in some etch uniformity tests showed improvements in uniformity of material removed or etched when compared to substrates processed under similar conditions using current substrate supports.

[0032] The inventors noted in some tests that the inventive substrate support produced a uniform, but lower etch rate. That is, the etch rate was more uniform across the substrate with a lesser amount of material removed in a timed period than similar substrates processed under similar conditions using current substrate supports. The etch rate observed using the present substrate support was uniform, or substantially uniform, across the substrate. The lower etch rate has been shown to beneficially improve the controllability of the etch process.

[0033] Figure 2 depicts a substrate processing system in accordance with some embodiments of the present invention. Other process chambers of other configurations may also be modified in accordance with the teachings provided herein.

[0034] Generally, a substrate processing system 200 comprises a process chamber 202 having a first volume 203 and a second volume 205. The first volume 203 may include a portion of the process chamber 202 where a plasma 207 is to be received (e.g., introduced or formed). The second volume 205 may include a portion of the process chamber 202 where a substrate is to be processed with reactants from the plasma 207. For example, a substrate support 100 may be disposed within the second volume 205 of the process chamber 202.

[0035] The substrate processing system 200 may include a gas inlet 206 coupled to the process chamber to provide one or more processes gases that may be utilized to form a plasma 207 in the first volume. A gas exhaust 208 may be coupled to the process chamber 202, for example in a lower portion of the process

chamber 202 including the second volume 205. In some embodiments, an RF power source 210 may be coupled to an inductive coil 212 to generate the plasma 207 within the process chamber 202. Alternatively, (not shown), the plasma may be generated remotely, for example, by a remote plasma source or the like, and flowed into the first volume 203 of the process chamber. In some embodiments, a power source 109 may be coupled to the substrate support 100 to control ion flux to a substrate 216 when present on a surface of the substrate support 100. The substrate processing system 200 may include a controller 220, for example, to control one or more components of the substrate processing system 200 to perform operations on the substrate 216. Other and further components and substrate processing system 200 are discussed below.

**[0036]** The process chamber 202 includes walls 230, a bottom 232 and a top 234. A dielectric lid 236 may be disposed under the top 234 and above a process kit 228, the process kit 228 coupled to the process chamber 202. The dielectric lid 236 may be dome-shaped as illustrated in Figure 2. The dielectric lid 236 may be made from dielectric materials such as glass or quartz, and is typically a replaceable part that may be replaced after a certain number of substrates have been processed in the substrate processing system 200. The inductive coil 212 may be disposed about the dielectric lid 236 and coupled to an RF power source 210 to inductively couple RF power to the first volume 203 to form the plasma 207 in the first volume 203. Alternatively to or in combination with the inductive coil 212, a remote plasma source (not shown) may be used to form the plasma 207 in the first volume 203 or to provide the plasma 207 to the first volume 203.

**[0037]** The process kit 228 may include a ring 238, such as a flange, having an outer edge 240 configured to rest on the wall 230 of the process chamber 202. For example, as shown in Figure 2, the outer edge 240 of the ring 238 may rest on the wall 230 and have the dielectric lid 236 and the top 234 rest upon the ring 238. However, the embodiments illustrated in Figure 2 are merely exemplary, and other embodiments are possible. For example, the ring 238 may be configured to rest on an internal feature of the chamber (not shown), such as a lip extending inward from the wall 230 or the like. The ring 238 may further include an inner edge 242.

[0038] The process kit 228 may include a body 244 extending downward from the inner edge 242 of the ring 238. The body 244 may include sidewalls 246 which define an opening 248 above the substrate support 100. For example, as illustrated in Figure 2, the diameter of the opening 248 may exceed the diameter of the substrate support 100. For example, a gap 250 formed between the substrate support 100 and the sidewalls 246 of the body 244 may be utilized as a flow path for process gases, byproducts, and other materials to be exhausted to the gas exhaust 208.

[0039] The process kit 228 may comprise any suitable materials compatible with processes being run in the substrate processing system 200. The components of the process kit 228 may contribute to defining the first and second volumes 203, 205. For example, the first volume 203 may be defined by at least the ring 238 and the dielectric lid 236. For example, in some embodiments, such as illustrated in Figure 2, the first volume 203 may be further defined by the sidewalls 246 of the body 244. For example, the second volume 205 may be defined by the body 244 and the substrate support 100.

[0040] The gas inlet 206 is connected to a processing gas supply 218 and introduces the processing gas into the substrate processing system 200 during processing. As illustrated, the gas inlet 206 is coupled to the first volume 203 via the dielectric lid 236. However, the gas inlet 206 may be coupled into the first volume 203 at any suitable location. The gas exhaust 208 may comprises a servo control throttle valve 252 and a vacuum pump 254. The vacuum pump 254 evacuates the substrate processing system 200 prior to processing. During processing, the vacuum pump 254 and the servo control throttle valve 252 maintain the desired pressure within the substrate processing system 200. Heater 256 is provided to heat the substrate 216 to a desired temperature. The heater 256 is coupled to a power source 264 configured to provide the heater 256 with power to facilitate operating the heater 256.

[0041] The controller 220 comprises a central processing unit (CPU) 222, a memory 224, and support circuits 226 for the CPU 222 and facilitates control of the components of the substrate processing system 200 and, as such, methods of

processing a substrate in the substrate processing system 200. The controller 220 may be one of any form of general-purpose computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The memory, or computer-readable medium, 224 of the CPU 222 may be one or more of readily available memory such as random access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote. The support circuits 226 are coupled to the CPU 222 for supporting the processor in a conventional manner. These circuits include cache, power supplies, clock circuits, input/output circuitry and subsystems, and the like. The memory 224 stores software (source or object code) that may be executed or invoked to control the operation of the substrate processing system 200 in the manner described herein. The software routine may also be stored and/or executed by a second CPU (not shown) that is remotely located from the hardware being controlled by the CPU 222.

[0042] In an example of operation, the substrate 216 is positioned on the substrate support surface 128 of the substrate support 100. The substrate processing system 200 may be evacuated to provide a vacuum processing environment. A processing gas is introduced through the gas inlet 206 into the first volume 203. To activate the reaction, a plasma of the processing gas is generated in the processing region through inductive coupling and/or capacitive coupling. The plasma 207 may be generated by applying power to the inductive coil 212 sufficient to sustain a plasma in the processing region. It is contemplated that the plasma within the processing region may be excited and sustained during processing by inductive coupling only, capacitive coupling only or combinations of both inductive and capacitive coupling.

[0043] In a non-limiting embodiment, the disclosed substrate support may be advantageously used in a preclean chamber used to clean a substrate prior to a deposition process or as a cleaning step between process steps. In such cases, an inert gas such as argon may be used for the processing gas. The inductive coil creates an ionized species of argon molecules, the plasma 207, in the process chamber 202.

**[0044]** In order to direct the ionized molecules in a desired direction, for example towards the substrate 216, in some embodiments a bias, or a high bias, RF power is coupled to the substrate support 100, for example via power source 109. In the present invention, the RF is applied to the conductive plate 108. The inventors have observed that the tapered thickness of the conductive plate 108 in the radially outward direction as illustrated at least in Figure 1 beneficially minimizes edge effects at the substrate edge and produces a more even etch across the substrate.

**[0045]** Thus, an improved apparatus for processing substrates has been provided herein. Embodiments of the inventive apparatus have been described with regard to an argon sputter etch process as an illustration and not as a limitation. Other plasma etch processes may advantageously employ the present substrate support to reduce edge effects during processing of a substrate disposed thereon.

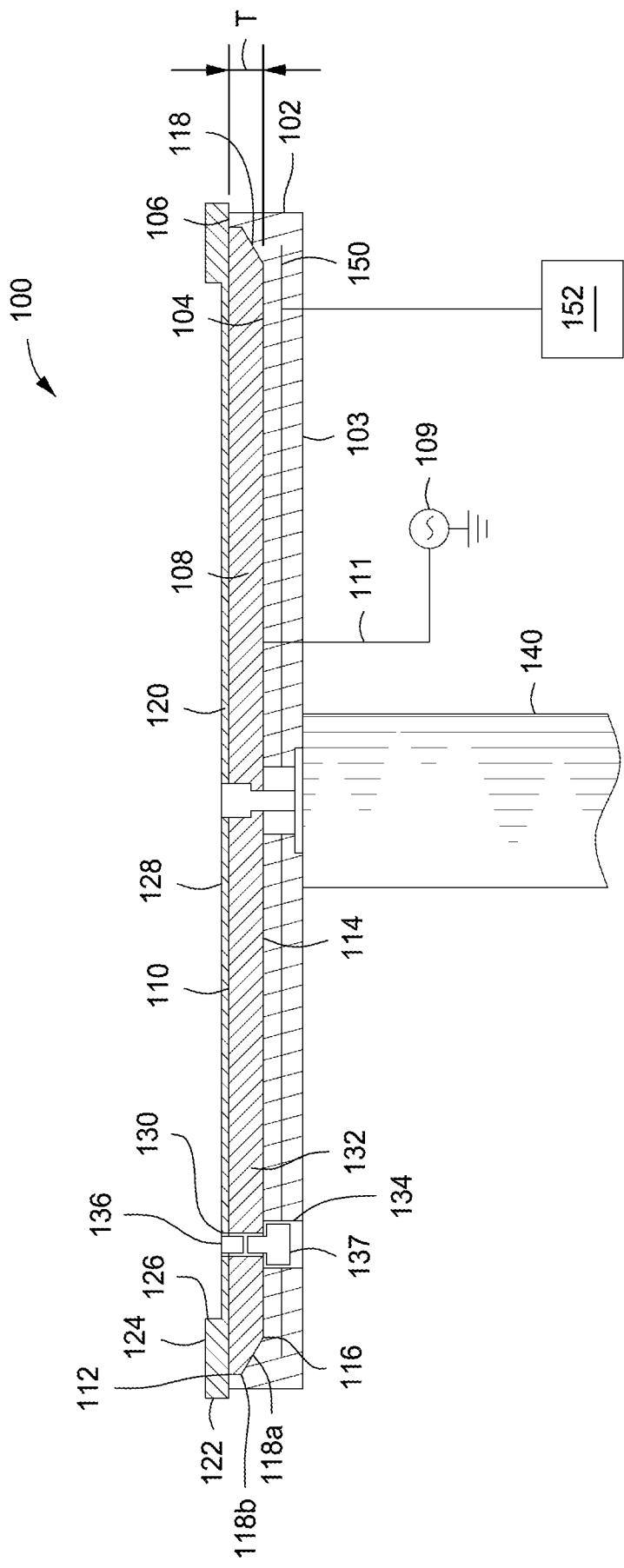
**[0046]** While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof.

**Claims:**

1. A substrate support to support a substrate in a processing chamber, comprising:
  - a dielectric insulator plate;
  - a conductive plate supported on the dielectric insulator plate, the conductive plate comprising a top surface and a bottom surface defining a thickness between the top surface and the bottom surface, wherein an edge portion of the conductive plate tapers in a radially outward direction; and
  - a dielectric plate comprising a substrate support surface disposed upon the top surface of the conductive plate.
2. The substrate support of claim 1, wherein at least a portion of the bottom surface tapers upwardly.
3. The substrate support of claim 2, wherein the tapered portion comprises a sidewall connecting the top surface and the bottom surface, wherein the sidewall is inclined at an angle of about 15 degrees to about 75 degrees from horizontal.
4. The substrate support of claim 2, wherein the tapered portion comprises a sidewall connecting the top surface and the bottom surface, wherein the sidewall comprises one or more straight or curved segments.
5. The substrate support of any of claims 1 to 4, wherein the tapered portion of the conductive plate extends radially beyond the substrate support surface.
6. The substrate support of any of claims 1 to 4, wherein the dielectric insulator plate includes a recess formed in a top surface thereof, the recess configured to accept at least a portion of the conductive plate and maintain contact with at least a portion of the bottom surface.

7. The substrate support of claim 6, wherein the recess is configured such that the top surface of the conductive plate is coplanar with a portion of the top surface of the dielectric insulator plate.
8. The substrate support of any of claims 1 to 4, wherein the dielectric insulator plate is formed from quartz.
9. The substrate support of any of claims 1 to 4, wherein the conductive plate is formed from a metallic material.
10. The substrate support of claim 9, wherein the conductive plate is formed from titanium.
11. The substrate support of any of claims 1 to 4, wherein the conductive plate is formed from a doped ceramic.
12. The substrate support of any of claims 1 to 4, wherein the dielectric plate comprises a raised lip having an inner wall corresponding to the substrate support surface.
13. The substrate support of any of claims 1 to 4, wherein the dielectric plate comprises at least one of quartz or ceramic.
14. The substrate support of any of claims 1 to 4, wherein the conductive plate is adapted to connect to an RF biasing source.
15. The substrate support of any of claims 1 to 4, further comprising:
  - a first locating hole in the dielectric plate;
  - a second locating hole in the conductive plate coaxial with the first locating hole; and
  - a locating device disposed partially through the first locating hole and partially within the conductive plate.

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FIG.

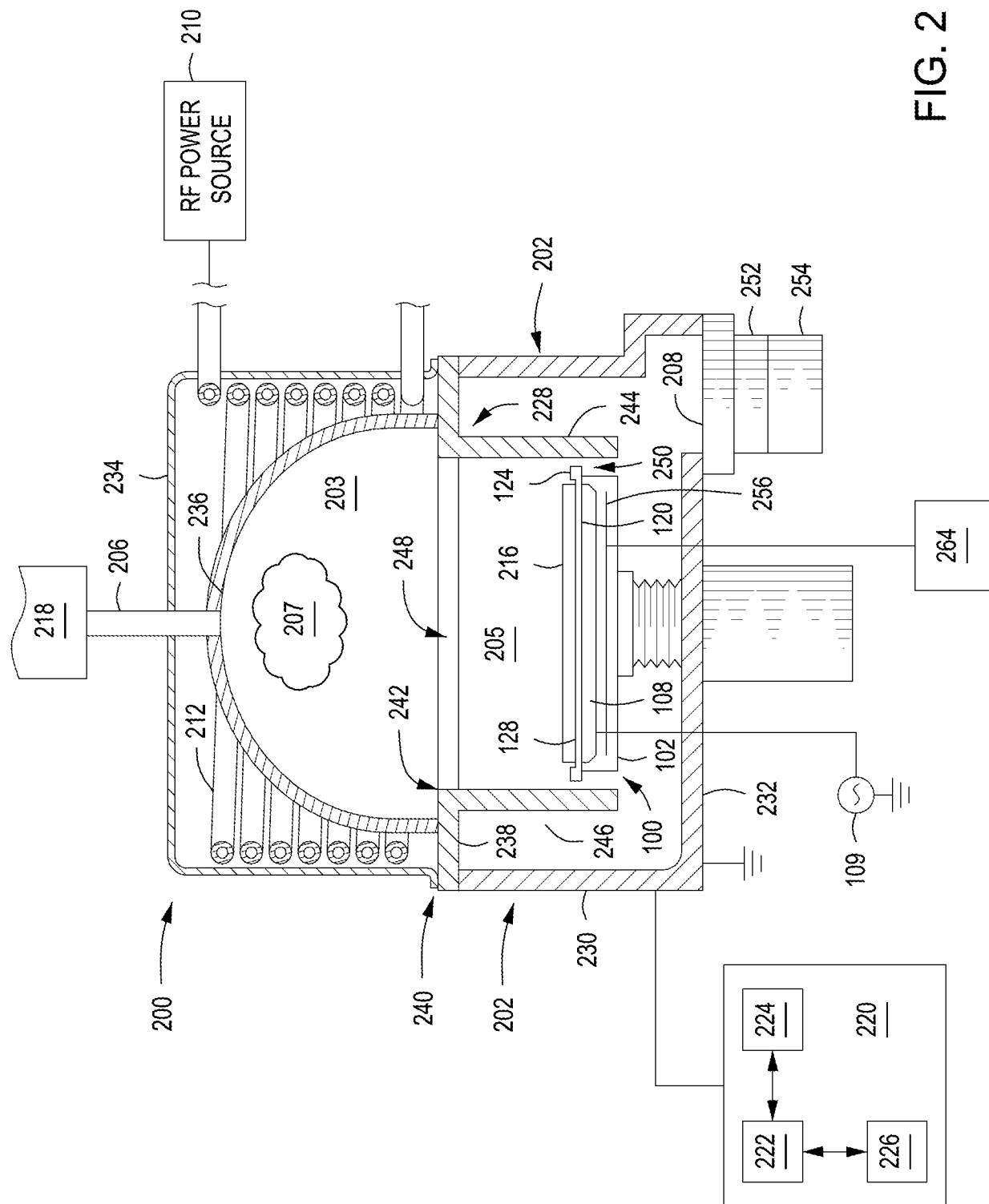


FIG. 2

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2014/016719

## A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/3065; G01R 31/26; H01L 21/302; H01L 21/306; C23F 1/00; C23C 16/44; C23F 1/08; C23C 16/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
Korean utility models and applications for utility models  
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
eKOMPASS(KIPO internal) & Keywords: substrate support, conductive plate, dielectric insulator plate, dielectric plate, tapered

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0194234 A1 (KENICHIRO ARAI et al.) 06 August 2009 See abstract; paragraphs [0046]–[0063], [0091]–[0096] and figures 1–2B, 6A–6B.	1–15
A	US 2009-0308537 A1 (YOHSUKE SHIBUYA et al.) 17 December 2009 See abstract; paragraphs [0028]–[0042]; claims 1–12 and figure 1.	1–15
A	US 2002-0075027 A1 (KENNETH HOLLMAN et al.) 20 June 2002 See abstract; paragraphs [0067]–[0083]; claims 1–13 and figures 1–10A.	1–15
A	US 2002-0162630 A1 (KIYOSHI SATOH et al.) 07 November 2002 See abstract; paragraphs [0030]–[0039], [0043]–[0045] and figures 1–2.	1–15
A	KR 10-2004-0049907 A (SAMSUNG ELECTRONICS CO., LTD.) 14 June 2004 See abstract; page 2; claims 1–3 and figures 1–2.	1–15

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 19 June 2014 (19.06.2014)	Date of mailing of the international search report <b>20 June 2014 (20.06.2014)</b>
Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer CHOI, Sang Won Telephone No. +82-42-481-8291

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2014/016719**

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