(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 June 2016 (23.06.2016)

WIPO | PCT

(10) International Publication Number
WO 2016/100805 A1

(51) International Patent Classification:
H01L 29/78 (2006.01)

(21) International Application Number:
PCT/US2015/066650

(22) International Filing Date:
18 December 2015 (18.12.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/576,310 19 December 2014 (19.12.2014) US
14/576,303 19 December 2014 (19.12.2014) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

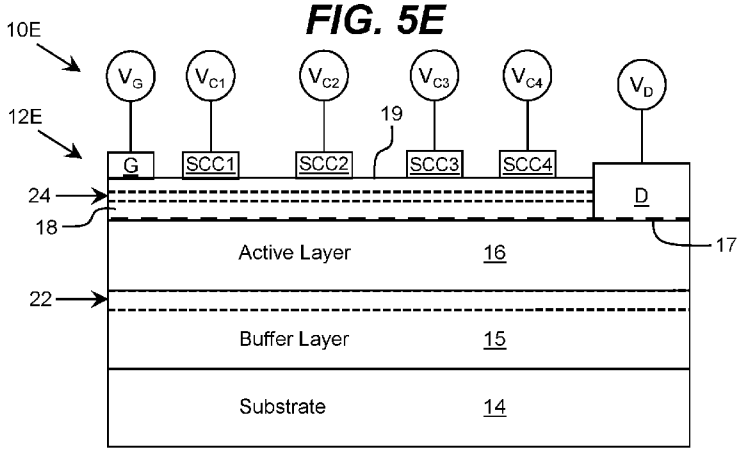
Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: SEMICONDUCTOR DEVICE WITH MULTIPLE SPACE-CHARGE CONTROL ELECTRODES

FIG. 5E



(57) Abstract: A circuit including a semiconductor device having a set of space-charge control electrodes is provided. The set of space-charge control electrodes is located between a first terminal, such as a gate or a cathode, and a second terminal, such as a drain or an anode, of the device. The circuit includes a biasing network, which supplies an individual bias voltage to each of the set of space-charge control electrodes. The bias voltage for each space-charge control electrode can be: selected based on the bias voltages of each of the terminals and a location of the space-charge control electrode relative to the terminals and/or configured to deplete a region of the channel under the corresponding space-charge control electrode at an operating voltage applied to the second terminal.

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Semiconductor Device with Multiple Space-Charge Control Electrodes

REFERENCE TO RELATED APPLICATIONS

[0001] The current application claims the benefit of U.S. Application No. 14/576,303, which was filed on 19 December 2014 and U.S. Application No. 14/576,310, which was filed on 19 December 2014, both of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The disclosure relates generally to semiconductor devices, and more particularly, to a semiconductor device with multiple space-charge control electrodes.

BACKGROUND ART

[0003] In power semiconductor devices, achieving the highest breakdown voltage simultaneously with minimal on-resistance is one of the most important performance characteristics. Lateral geometry devices, such as field-effect transistors (FETs), including metal oxide semiconductor FETs (MOSFETs), metal semiconductor FETs (MESFETs), high electron mobility transistors (HEMTs), etc., have a channel aligned along the semiconductor surface, and which is often located close to the semiconductor surface. If the space-charge (depletion) region occupies only a portion of the gate-drain spacing, the electric field in that spacing is strongly non-uniform and can result in premature breakdown, which limits the device performance. Due to a high carrier concentration in the channel and the close vicinity of the channel to the semiconductor surface, efficient control over the space charge distribution in the gate-drain spacing is extremely challenging.

[0004] FIG. 1 shows a conventional heterostructure FET (HFET) 2 according to the prior art, and FIG. 2 shows an illustrative electric field distribution chart according to the prior art. As illustrated in FIG. 2, the electric field profile in the gate-drain spacing having a distance, L_{GD}, shown in FIG. 1 exhibits a strong peak near the gate edge when the HFET 2 is operated as a switch (without field plate). The peak width is defined by the carrier concentration in the channel. To this extent, a breakdown voltage for the HFET 2 does not increase when the gate-drain spacing distance L_{GD} is increased.

[0005] One approach to lower the peak electric field near the gate edge is the use of one or more field-modulating plates (FPs), which can be connected to either the gate, source, or drain electrode. FIG. 2 illustrates an illustrative field plate connected to a gate and the resulting electric field distribution. A multistep field plate structure is shown in FIG. 3, and a gradual

field plate structure is shown in FIG. 4. In each case, the field plate structure decreases the peak field near the gate electrode edge by splitting it into two or more peaks, thereby increasing the breakdown voltage for the device. However, even multiple field plate structures cannot achieve a uniform electric field in the device channel.

[0006] Additionally, optimal configuration of multiple field plates is difficult to achieve. For example, the optimal configuration requires precisely controlled field plate length and dielectric thickness variation along the channel. In addition, prior art field plates have either source or gate potential applied to them, and therefore significant voltage exists between the field plate and the drain electrode. As a result, a device including field plate(s) can suffer from premature breakdown between the field plate(s) and the drain electrode. Furthermore, the field plate(s) increases the inter-electrode and electrode-semiconductor capacitances and therefore decreases the device maximum operating frequency.

[0007] As a result of the above limitations, current high-voltage FET switches (i) do not achieve the breakdown voltages predicted by fundamental material properties and (ii) exhibit breakdown voltage – gate-drain spacing dependence saturating at high voltages, typically four hundred volts and above, which imposes serious limitations on device design for kilovolt switching applications.

SUMMARY OF THE INVENTION

[0008] Aspects of the invention provide a circuit including a semiconductor device having a set of space-charge control electrodes. The set of space-charge control electrodes is located between a first terminal, such as a gate or a cathode, and a second terminal, such as a drain or an anode, of the device. The circuit includes a biasing network, which supplies an individual bias voltage to each of the set of space-charge control electrodes. The bias voltage for each space-charge control electrode can be: selected based on the bias voltages of each of the terminals and a location of the space-charge control electrode relative to the terminals and/or configured to deplete a region of the channel under the corresponding space-charge control electrode at an operating voltage applied to the second terminal.

[0009] A first aspect of the invention provides a circuit comprising: a semiconductor device including: a semiconductor structure including a channel; a first terminal and a second terminal to the channel; and a set of space-charge control electrodes located between the first terminal and the second terminal on a surface of the semiconductor structure; and a biasing network supplying an individual bias voltage to each of the set of space-charge control electrodes, wherein the bias voltage for each of the set of space-charge control electrodes is selected based

on a bias voltage of the first terminal, a bias voltage of the second terminal, and a location of the space-charge control electrode relative to the first terminal and the second terminal.

[0010] A second aspect of the invention provides a circuit comprising: a semiconductor device including: a semiconductor structure including a channel; a first terminal and a second terminal to the channel; and a set of space-charge control electrodes located between the first terminal and the second terminal on a surface of the semiconductor structure; and a biasing network supplying an individual bias voltage to each of the set of space-charge control electrodes, wherein the bias voltage for each of the set of space-charge control electrodes is configured to deplete a region of the channel under the corresponding space-charge control electrode at an operating voltage applied to the second terminal.

[0011] A third aspect of the invention provides a circuit comprising: a transistor including: a semiconductor structure including a channel; a gate and a drain; and a set of space-charge control electrodes located between the gate and the drain on a surface of the semiconductor structure; and a biasing network supplying an individual bias voltage to each of the set of space-charge control electrodes, wherein the bias voltage for each of the set of space-charge control electrodes is selected based on a bias voltage of the gate, a bias voltage of the drain, and a location of the space-charge control electrode relative to the gate and the drain.

[0012] The illustrative aspects of the invention are designed to solve one or more of the problems herein described and/or one or more other problems not discussed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and other features of the disclosure will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various aspects of the invention.

[0014] FIG. 1 shows a conventional heterostructure field effect transistor according to the prior art.

[0015] FIG. 2 shows an illustrative electric field distribution chart according to the prior art.

[0016] FIG. 3 shows a schematic structure of a multistep field plate according to the prior art.

[0017] FIG. 4 shows a schematic structure of a gradual field plate according to the prior art.

[0018] FIGS. 5A-5G show schematic structures of gate-drain regions of illustrative devices connected in circuits according to embodiments.

[0019] FIG. 6 shows an illustrative schematic voltage biasing diagram according to an embodiment.

[0020] FIG. 7 shows an illustrative comparison of qualitative electric field profiles according to an embodiment.

[0021] FIG. 8 shows a schematic structure of an illustrative diode connected in a circuit according to an embodiment.

[0022] FIGS. 9A-9D show illustrative biasing networks according to embodiments.

[0023] FIG. 10 shows an illustrative flow diagram for fabricating a circuit according to an embodiment.

[0024] FIGS. 11A and 11B show top and side views, respectively, of an illustrative space-charge control electrode according to an embodiment.

[0025] It is noted that the drawings may not be to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0026] As indicated above, aspects of the invention provide a circuit including a semiconductor device having a set of space-charge control electrodes. The set of space-charge control electrodes is located between a first terminal, such as a gate or a cathode, and a second terminal, such as a drain or an anode, of the device. The circuit includes a biasing network, which supplies an individual bias voltage to each of the set of space-charge control electrodes. The bias voltage for each space-charge control electrode can be: selected based on the bias voltages of each of the terminals and a location of the space-charge control electrode relative to the terminals and/or configured to deplete a region of the channel under the corresponding space-charge control electrode at an operating voltage applied to the second terminal. Aspects of the invention can provide a solution for increasing an operating voltage and/or a maximum power of the semiconductor device within the circuit. As used herein, unless otherwise noted, the term "set" means one or more (i.e., at least one) and the phrase "any solution" means any now known or later developed solution.

[0027] Turning to the drawings, FIGS. 5A-5G show schematic structures of gate-drain regions of illustrative devices 12A-12G connected in circuits 10A-10F according to embodiments. Each device 12A-12G is shown including a substrate 14, an active layer 16, a barrier layer 18, a gate G, and a drain D. A channel is formed at a junction of the active layer 16 and the barrier layer 18. While not shown in all of the figures for clarity, it is understood that a device 12A-12G can include various additional contacts (e.g., a source contact S (FIG. 5F, 5G)) and/or layers (e.g., an

initiation layer 13 (FIG. 5F, 5G) and/or a buffer layer 15 (FIGS. 5E-5G) located between the substrate 14 and the active layer 16). Each device 12A-12G, and components thereof, can be manufactured and fabricated using any solution. In an embodiment, the substrate 14 is formed of silicon carbide (SiC), the active layer 16 is formed of gallium nitride (GaN), the barrier layer 18 is formed of aluminum gallium nitride (AlGaN), and the gate G and drain D are formed of metal.

[0028] However, it is understood that this is only illustrative of various possible devices. To this extent, the substrate 14 can be formed of any of various types of compound semiconductor or dielectric materials, including for example, sapphire, diamond, germanium (Ge), gallium nitride (GaN), silicon, SiC, gallium arsenic (GaAs), and/or the like. Furthermore, the substrate 14 can comprise a conducting and/or semiconducting substrate. Similarly, layers 13, 15, 16, 18 can be formed of any combination of various types of group III nitride materials comprising one or more group III elements (e.g., boron (B), aluminum (Al), gallium (Ga), and indium (In)) and nitrogen (N), such that $B_WAl_XGa_YIn_ZN$, where $0 \leq W, X, Y, Z \leq 1$, and $W+X+Y+Z = 1$. Illustrative group III nitride materials include AlN, GaN, InN, BN, AlGaN, AlInN, AlBN, InGaN, AlGaInN, AlGaBN, AlInBN, and AlGaInBN with any molar fraction of group III elements. Furthermore, it is understood that the device 12A-12G can be formed from other types of semiconductor materials, including other types of group III-V materials, such as such as GaAs, GaAlAs, InGaAs, indium phosphorus (InP), and/or the like. Regardless, one or more of the layers in a heterostructure described herein can include one or more attributes to alleviate strain. For example, a layer can be formed of a superlattice structure.

[0029] Additionally, each device 12A-12F is shown including a set of space-charge control electrodes SCC1-SCC4 located on a surface of the semiconductor device 12A-12F between the gate G and the drain D. It is understood that while each device 12A-12F is shown including three or four electrodes SCC1-SCC4, a device can include any number of one or more electrodes SCC1-SCC4. When multiple electrodes SCC1-SCC4 are included, the electrodes SCC1-SCC4 can be spaced uniformly or non-uniformly within the region between the gate G and the drain D. Regardless, each electrode SCC1-SCC4 can be fabricated using any solution and can be formed of any type of material, such as a metal. Furthermore, although a set of space-charge control electrodes SCC1-SCC4 is not shown in FIG. 5G, it is understood that the device 12G can include any number of space-charge control electrodes (e.g., between the source S and the gate G or the gate G and the drain D).

[0030] The gate G and/or one or more of the electrodes SCC1-SCC4 can form any type of contact to the surface of the semiconductor, such as a Schottky contact (shown in FIGS. 5A and

5E), a metal-oxide-semiconductor (MOS) contact, a metal-insulator-semiconductor (MIS) contact, and/or the like, to the semiconductor surface. To this extent, the devices 12B-12D, 12F, 12G of FIGS. 5B-5D, 5F and 5G are shown including insulating layers 20B-20D, 20F, 20G located between the barrier layer 18 and the gate G (and the electrodes SCC1-SCC4 in FIGS. 5B-5D and 5F). The insulating layers 20B-20D, 20F, 20G can reduce an amount of leakage current associated with the gate G (and the electrodes SCC1-SCC4 in FIGS. 5B-5D and 5F). The insulating layers 20B-20D, 20F, 20G can be formed of any type of insulating material, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and/or the like. While each insulating layer 20B-20D, 20F, 20G is shown extending across the entire region from under the gate G to the drain D, it is understood that a device can include an insulating layer that only extends under any combination of one or more of the gate G and/or the electrodes SCC1-SCC4.

[0031] Furthermore, a device can include one or more field plates. To this extent, the devices 12C, 12D are shown including a pair of field plates FP1, FP2. Field plate FP1 is connected to the gate G and extends toward the drain D, while field plate FP2 is connected to the drain D and extends toward the gate G. It is understood that the field plates FP1, FP2 are only illustrative. To this extent, a device can include any number of zero or more field plates connected to the source, the drain D, and/or the gate G. Furthermore, it is understood that one or more of the electrodes SCC1-SCC4 can be a Schottky electrode.

[0032] As illustrated, the insulating layer 20C of the device 12C can have a different thickness in the regions on which the field plates FP1, FP2 are located. Similarly, as shown in conjunction with the device 12D, the insulating layer 20 can have a varying thickness for each of the electrodes SCC1-SCC3 and/or the gate G. In this case, a voltage applied to an electrode on a thicker portion of the insulating layer 20, such as the electrode SCC3, will have less effect on the electric field at the channel than a similar voltage applied to an electrode on a thinner portion of the insulating layer 20, such as the electrode SCC1. While the insulating layer 20 is shown having an increasing thickness going in a gate G to drain D direction, it is understood that this is only illustrative and any configuration of varying thicknesses of an insulating layer for the gate and/or electrodes located thereon can be utilized. For example, a thickness of the insulating layer 20 can decrease in thickness going in a gate G to drain D direction.

[0033] A device described herein can include one or more additional features, which are configured to improve one or more aspects of operation of the device. For example, as illustrated in conjunction with the devices 12E-12G shown in FIGS. 5E-5G, a device can include a buffer layer 15 located between the substrate 14 and the active layer 16. Additionally, as

shown in conjunction with the devices 12F and 12G, a device can include an initiation layer 13 located between the substrate 14 and the buffer layer 15. The substrate 14, initiation layer 13 (when included), and/or the buffer layer 15 (when included) can be formed of a semiconducting material. For a group III nitride device 12E-12G, illustrative materials for the substrate 14 include silicon, silicon carbide, gallium nitride, and/or the like, and illustrative materials for the initiation layer 13 and buffer layer 15 include aluminum nitride, gallium nitride, aluminum gallium nitride, a superlattice of these materials, and/or the like. However, it is understood that any materials can be selected based on the corresponding semiconductor materials used to fabricate the device.

[0034] In an embodiment, the substrate 14, the initiation layer 13, and/or the buffer layer 15 can have a conductivity type (n-type or p-type) opposite that of the conductivity type of the active channel 17. In this configuration, a peak electric field in the channel 17 and a channel surface 19 can be lowered. In a more particular illustrative embodiment, the active channel 17 is an n-type channel and the initiation layer 13, the buffer layer 15, and/or the substrate 14 are p-type. For example, a p-type doping of the buffer layer 15 can be adjusted to achieve a maximum field lowering effect, which corresponds to a full layer depletion at a maximum operating voltage of the devices 12E-12G.

[0035] In an embodiment, the buffer layer 15 includes a low-conducting layer 22 located therein. Similarly, the barrier layer 18 can include a low-conducting layer 24 located therein. While both of the buffer layer 15 and the barrier layer 18 are shown including a low-conducting layer 22, 24, respectively, in FIGS. 5E and 5G, it is understood that embodiments can include low-conducting layer(s) located in only one of the buffer layer 15 or the barrier layer 18. As illustrated, the low-conducting layers 22, 24 can extend across substantially all of the active region. However, it is understood that embodiments of each of the low-conducting layers 22, 24 can extend across only a portion of the active region. Similarly, the buffer layer 15 and/or the barrier layer 18 can include any combination of multiple low-conducting layers, each of which extends across only a portion of the active region.

[0036] Furthermore, as shown in FIG. 5F, the active layer 16A, 16B can include a low-conducting layer 26. The buried low-conducting layer 26 is located below the active region (e.g., a device channel formed at an interface of the active layer 16B and the barrier layer 18) within the device epitaxial structure in a vicinity of the device channel. As illustrated, the buried low-conducting layer 26 can extend under all of the active region. However, it is understood that the buried low-conducting layer 26 also can only extend under a portion of the active region. Similarly, an active layer 16A, 16B can include any combination of multiple buried

low-conducting layers, each of which is located under a portion of the active region. The buried low-conducting layer 26 can be electrically connected and/or capacitively coupled to one or more of the device contacts (e.g., source S, drain D, and/or the like).

[0037] Additionally, as shown in conjunction with the devices 12F, 12G shown in FIGS. 5F and 5G, a device described herein can include a set of surface low-conducting layers (e.g., field-controlling elements) 28. As illustrated, the surface low-conducting layer 28 can be located in the surface region between the source contact S and the gate G (gate-source region) and/or the surface region between the gate G and the drain D (gate-drain region). It is understood that a device described herein can include one or more surface low-conducting layers 28 located in any combination of one or more of: the gate-source region; the gate-drain region; the source-drain region; and/or the like. For example, in FIG. 5G, the device 12G includes a first surface low-conducting layer 28A located in a gate-source region and a second surface low-conducting layer 28B located in a gate-drain region. Furthermore, a device described herein can include a low-conducting layer that forms an additional contact or passivation layer. To this extent, a low-conducting layer with low surface conductivity as described herein can be used in addition to or instead of regular metal electrodes (e.g., for the gate G, one or more of the electrodes SCC1-SCC4, and/or the like).

[0038] As illustrated in FIGS. 5F and 5G, the surface low-conducting layer(s) 28 can be located on a gate insulating layer 20F, 20G, when included. Furthermore, the gate G also can be insulated from the low-conducting layer(s) 28. For example, the device 12F is shown including a gate insulating wall 29, which isolates the gate G from the corresponding low-conducting layer 28. In another example, when the device 12G includes a first surface low-conducting layer 28A and a second surface low-conducting layer 28B, the device 12G can include a first gate insulating wall 29A between the first surface low-conducting layer 28A and the gate G and a second gate insulating wall 29B between the gate G and the second surface low-conducting layer 28B. The insulating wall 29 can be formed of any type of insulating material, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and/or the like.

[0039] A low-conducting layer 22, 24, 26, 28 can be formed of a low-conducting material using any solution. In an embodiment, a low-conducting layer 22, 24, 26, 28 is formed of a semiconductor, dielectric, metal, polycrystalline material, and/or the like, or a compound thereof. The low-conducting material can have a surface resistance that is significantly higher than that of metal electrodes, but is also much lower than that of a dielectric material. Similarly, the low-conducting material can have a surface conductivity that is significantly lower than that

of metal electrodes, but is also much higher than that of a dielectric material. As a result, the associated characteristic charging-recharging time of the low-conducting layer 22, 24, 26, 28 is much higher than that of metal electrodes. To this extent, during operation of a device 12E-12G at DC or low frequencies (e.g., below 10 megahertz (MHz)), typically used for pulse or sinusoidal modulation, the low-conducting layer(s) 22, 24, 26, 28 will behave similar to metal electrodes. However, during operation of the device 12E-12F at high (signal) frequencies, (e.g., typically exceeding 100 MHz) the low-conducting layer(s) 22, 24, 26, 28 will behave similar to an insulator, thereby not deteriorating the device frequency performance.

[0040] Illustrative low-conducting materials include, for example: GaN, InGaN, or another semiconductor; a low-conducting dielectric single crystal; a textured, poly-crystalline or amorphous material; a semi-metal material; oxides of nickel and other metals; composite materials, such as aluminum oxide with embedded platinum; and/or the like. The low-conducting layer 22, 24, 26, 28 can be configured to provide a discharge current path for the corresponding trapped charge. For example, the low-conducting layer(s) 22, 26 can remove trapped charges from the buffer layer 15, while the low-conducting layer(s) 24, 28 can remove surface trapped charges. In an embodiment, one or more of the discharge current paths provided by a low-conducting layer 22, 24, 26, 28 terminates at the drain contact D. Alternatively, the device 12E-12G can include an additional contact to terminate a discharge path. For example, the device 12E can include an additional contact to terminate the discharge current path provided by the low conducting layer 22.

[0041] As described herein, in an embodiment, it is desired for each low-conducting layer 22, 24, 26, 28 to act as a conductor (e.g., electrode) when the corresponding device 12E-12G is operating at low frequencies. The low frequencies can correspond to, for example, an inverse of the characteristic carrier trapping/de-trapping times, a frequency at which interfering (e.g., noise, interference, and/or the like) signals occur, a highest frequency at which the interfering signals should be suppressed, and/or the like. However, within a target device operating frequency range, which includes much higher frequencies (e.g., at least ten times higher) than the low frequencies, each low-conducting layer 22, 24, 26,28 can act as a dielectric, thereby making only a minor increase in the total electrode area and, as a result, in the device capacitance.

[0042] In an embodiment, the design and configuration of a low-conducting layer 22, 24, 26, 28 accounts for the characteristic charging-discharging time of the low-conducting layer 22, 24, 26, 28. For example, contrary to other approaches, the design and configuration of a low-conducting layer 22, 24, 26, 28 can identify a range of acceptable lateral and/or sheet resistances/conductances and/or a target lateral and/or sheet resistance/conductance for a set of

low-conducting layers 22, 24, 26, 28 included in a device 12E-12G based on a target operating frequency (e.g., a minimal operating frequency), a characteristic charge-discharge time of a trapped charge targeted for removal with the low-conducting layer 22, 24, 26, 28, a frequency targeted for suppression (e.g., interfering frequency), and/or the like. In a more particular example, a low-conducting layer 22, 24, 26, 28 is configured to have a sheet conductivity such that an associated characteristic charging-discharging time of the low-conducting layer 22, 24, 26, 28 is much (e.g., at least ten times) higher than an inverse of the minimal target operating frequency and much (e.g., at least ten times) lower than a characteristic charge-discharge time of the trapped charge targeted for removal using the low-conducting layer 22, 24, 26, 28 and/or an inverse of the maximum interfering frequency targeted for suppression. When a low-conducting layer 22, 24, 26, 28 is configured in such a manner, the low-conducting layer 22, 24, 26, 28 can normally behave as a conducting layer at direct current or low frequencies, but as an insulator within a target device operating frequency range, therefore not deteriorating the device frequency performance.

[0043] One or more aspects of a semiconductor device described herein can be designed using any solution. For example, the materials, dimensions, layer structure, and/or the like, can be selected and configured according to a target set of device operating properties using any solution. As part of designing the semiconductor device, one or more low-conducting layers 22, 24, 26, 28 can be designed as described herein. For example, a low-conducting layer 22, 24, 26, 28 can have a material with a target lateral resistance, which can be selected based on a minimum target operating frequency for the device 12E, 12F. In an embodiment, the material is selected such that a product of the target lateral resistance and a capacitance between the low-conducting layer 22, 24, 26, 28 and the device channel 17 is larger than an inverse of the minimum target operating frequency of the device 12E-12G and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer 22, 24, 26, 28 or an inverse of a maximum interfering frequency targeted for suppression using the low-conducting layer 22, 24, 26, 28. The low-conducting layer 22, 24, 26, 28 can then be designed based on the corresponding target lateral resistance, e.g., a material for the low-conducting layer 22, 24, 26, 28 can be selected to provide a lateral resistance approximately equal to the target lateral resistance.

[0044] In an embodiment, a resistivity of the buried low-conducting layer 22, 24, 26 can be designed such that a characteristic time constant of the buried low-conducting layer 22, 24, 26 is lower than that of a trapped charge, but much higher than a period of a signal corresponding to a lowest target operating frequency for the device 12E-12G. In this manner, the buried low-

conducting layer 22, 24, 26 can have a minimal effect on the operating frequency of the device, while being capable of removing the corresponding trapped charge. In another embodiment, the material forming the low conducting layer 22, 24, 26 has a sheet resistance between approximately $1x10^3$ (approximately $1x10^5$ in in a still more particular embodiment) Ohms per square and approximately $1x10^7$ Ohms per square. Each low-conducting layer 22, 24, 26 can be located any distance from the active channel 17. In an embodiment, one or more of the low-conducting layers 22, 24, 26 are located within a channel space-charge region (generally within a distance of ten nanometers to one micrometer from the device active region). In an embodiment, a low-conducting layer 22, 24, 26 can be located outside of a vicinity of the active channel 17, e.g., outside of a channel space-charge region (e.g., generally greater than ten nanometers to one micrometer from the active channel 17).

[0045] The following discussion provides a theoretical basis for determining an illustrative set of attributes of the device 12E-12G and the low-conducting layer(s) 22, 24, 26, 28 as currently understood by the inventors. As discussed herein, depending on a target function, the low-conducting layer 22, 24, 26, 28 can be located in the gate-source, gate-drain, or source-drain spacing, form an additional contact or passivation layer, be formed on a surface of the heterostructure or buried within the heterostructure, and/or the like. The following description uses a low-conducting layer located in the source-drain region of a group III-nitride based HFET as an illustrative example.

[0046] In order for the low-conducting layer to not significantly affect a radio frequency (RF) performance (e.g., impedance) of the device, a corresponding time constant for the low-conducting layer, τ_{LC}, must be much larger than $1/(2\pi f)$, where f is the target operating frequency for the device. The time constant for the low-conducting layer can be expressed as $\tau_{LC} = R_{LC}C_{LC}$, where R_{LC} is the lateral resistance of the low-conducting layer measured in a direction of the current flow in the device along the surface of the low-conducting layer and C_{LC} is the total capacitance between the low-conducting layer and the device channel. This yields the following condition:

$$\tau_{LC} = R_{LC}C_{LC} >> 1/(2\pi f) \quad (1)$$

Assuming τ_{LC} is at least approximately six times (2□ times) greater than $1/(2\pi f)$, the condition (1) can be rewritten as:

$$\tau_{LC} = R_{LC}C_{LC} > 1/f \quad (2)$$

As used herein, the lateral resistance of the low-conducting layer, R_{LC}, is related to the low-conducting layer sheet resistance, R_{LCSH}, as:

$$R_{LC} = R_{LCSH} * L/W \quad (2a)$$

where L and W are the length and width, respectively, of the low-conducting layer with respect to a direction of the current flow in the device.

[0047] Furthermore, the low-conducting layer should be sufficiently fast to allow for de-trapping of trapped carriers and/or screening interfering signals. Assuming a maximum de-trapping or interfering frequency, f_C, and following the derivation that led to condition (2) above, the required τ_{LC} also should meet the following condition:

$$\tau_{LC} < 1/ f_C \quad (3)$$

As an example, for practical purposes and material selection, in order to meet both conditions (2) and (3), the value of the τ_{LC} can be selected as follows:

$$\tau_{LC} = 1/(f \times f_C)^{1/2} \quad (4)$$

[0048] As an illustrative example, assume a field effect transistor has the following attributes: a source to drain distance, L = 5 μm; a gate-channel separation (also equal to the surface low-conducting layer-channel separation), d = 20 nm; a channel width, W = 1 mm; a relative dielectric permittivity of the material between the low-conducting layer and the channel, $\varepsilon_r = 9$; a target operating frequency, f = 1 GHz; a characteristic carrier trapping time $\tau_{TR} = 0.16$ μs; and a corresponding de-trapping frequency $f_C = 1$ MHz. The low-conducting layer-channel capacitance can be calculated as, $C_{LC} = \varepsilon_0 \varepsilon_r L*W/d \approx 20$ pF, where ε_0 is vacuum permittivity. From equation (2), the low-conducting layer resistance $R_{LC} = \tau_{LC}/C_{LC}$.

[0049] Using the above-described attributes and equations, values for R_{LC} which provide the corresponding desired time constant for the low-conducting layer, τ_{LC}, can be derived. For example, τ_{LC} can be configured to be greater than an inverse of the target operating frequency, e.g., greater than 1/1 GHz and less than an inverse of the de-trapping frequency, e.g., less than 1/1 MHz. Solving for R_{LC}, the R_{LC} can be between $R_{LCMIN} = 1.6$ kΩ/sq and $R_{LCMAX} = 1.6$ MΩ/sq. As discussed herein, the τ_{LC} can be much larger than the inverse of the target operating frequency of the device and much smaller than the inverse of the de-trapping frequency. A target value of R_{LC} between the R_{LCMIN} and R_{LCMAX} values can be selected based on the application of the corresponding device. In an embodiment, a target (e.g., optimal) value for

R_{LC}, $R_{LC\,OPT}$, can be calculated using the formula: $R_{LC\ OPT} = \sqrt{R_{LC\,MIN} \cdot R_{LC\,MAX}}$. In this case, using the R_{LCMIN} and R_{LCMAX} calculated above, the target value for R_{LC} in the device described herein is approximately 50.6 kΩ/sq.

[0050] Inclusion of one or more low-conducting layers described herein can provide one or more improvements to the operation of the device. For example, inclusion of a low-conducting layer in the gate-drain spacing on the surface of a device can remove surface trapped charges within that spacing. Furthermore, inclusion of a set of low-conducting layer 28 over substantially an entire source-drain spacing on the surface of the device 12F can remove the surface trapped charges as well as screen the active region from surface potential modulation caused by interfering sources. Additionally, inclusion of a buried low-conducting layer 26 can remove the bulk trapped charges in the corresponding region (e.g., across substantially an entire length of the channel) of the device 12F. As a result, a device 12E-12G including one or more of the low-conducting layers 22, 24, 26, 28 described herein can have an increased operating frequency, power, and/or efficiency over existing devices that do not include any low-conducting layers. Similarly, a device 12E-12G including one or more of the low-conducting layers 22, 24, 26, 28 described herein can be more resistant to interfering signals, the impact of which can be reduced due to the presence of one or more of the low-conducting layers 22, 24, 26, 28 described herein.

[0051] One or more aspects of a semiconductor device described herein can be designed using any solution. For example, the materials, dimensions, layer structure, and/or the like, can be selected and configured according to a target set of device operating properties using any solution. As part of designing the semiconductor device, one or more low-conducting layers 22, 24, 26, 28 can be designed as described herein. For example, a minimum target operating frequency for the semiconductor device can be determined. Subsequently, a target lateral resistance for the low-conducting layer 22, 24, 26, 28 can be determined such that a product of the target lateral resistance and a capacitance between the low-conducting layer 22, 24, 26, 28 and the device channel is larger than an inverse of the minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer 22, 24, 26, 28 or an inverse of a maximum interfering frequency targeted for suppression using the low-conducting layer 22, 24, 26, 28. The low-conducting layer 22, 24, 26, 28 can then be designed based on the corresponding target lateral resistance, e.g., a material for the low-conducting layer can be selected to provide a lateral resistance approximately equal to the target lateral resistance.

[0052] When a device 12A-12F (and the device 12G if the electrodes SCC1-SCC4 are included) is implemented in a circuit 10A-10F (and the circuit 10G), the circuit 10A-10F (and circuit 10G) can include components that apply an individual voltage bias V_{C1}-V_{C4} to each of the electrodes SCC1-SCC4, respectively. In this case, individually biased electrodes SCC1-SCC4 can provide independent control of a potential difference between a corresponding portion of the channel located under the electrode SCC1-SCC4 and the drain D. In an embodiment, the voltage V_{C1}-V_{C4} applied to each electrode SCC1-SCC4 is sufficiently high to deplete the portion of the channel located below the corresponding electrode SCC1-SCC4. Furthermore, the voltage V_{C1}-V_{C4} applied to each electrode SCC1-SCC4 is significantly below (e.g., by at least 30%) a breakdown voltage between the electrode SCC1-SCC4, the gate G, the drain D, and the other electrodes SCC1-SCC4. In this case, the electrodes SCC1-SCC4 can reduce premature breakdown, which can occur between the field plate(s) and the drain electrode of prior art devices, since the voltages between the electrodes SCC1-SCC4 and the other electrodes are much lower than the breakdown voltage.

[0053] During operation of the device 12A-12F (and the device 12G if electrodes SCC1-SCC4 are included) within the circuit 10A-10F (and circuit 10G), the voltages V_{C1}-V_{C4} applied to each electrode SCC1-SCC4 can be configured to provide any target space-charge (electric field) profile in the spacing between the gate G and the drain D. Furthermore, the electrodes SCC1-SCC4 can be used to achieve any target (e.g., required) degree of depletion and/or space-charge region extension within the spacing between the gate G and the drain D. In an embodiment, the space-charge profile is configured to provide an increased (e.g., maximal) breakdown voltage for the device 12A-12F (and the device 12G) over other approaches.

[0054] The voltage V_{C1}-V_{C4} applied to each electrode SCC1-SCC4 can be selected based on a location of the electrode SCC1-SCC4 relative to the gate G and the drain D, the gate voltage bias V_G, and/or the drain voltage V_D. For example, FIG. 6 shows an illustrative schematic voltage biasing diagram according to an embodiment. In this case, a linear function 30 can be calculated using a linear interpolation between two points in a plot of a distance between adjacent edges of the gate G and the drain D versus a difference between the gate voltage bias V_G and the drain voltage V_D. Each voltage V_{C1}-V_{C4} can be calculated using the linear function and a location of the corresponding electrode SCC1-SCC4 (e.g., a gate-side edge of the electrode) from a drain-side edge of the gate G. Alternatively, it is understood that a target location of an electrode SCC1-SCC4 can be calculated using the linear function and a corresponding voltage V_{C1}-V_{C4} to be applied to the electrode SCC1-SCC4. Furthermore, it is understood that each voltage V_{C1}-V_{C4} also can be calculated based on one or more additional

factors. For example, when a device includes an insulating layer having a varying thickness, such as the insulating layer 20D (FIG. 5D), the corresponding voltage V_{C1}-V_{C4} to be applied to each electrode SCC1-SCC3 (FIG. 5D) can be further based on the corresponding thickness of the insulating layer 20D. To this extent, the varying thickness of an insulating layer can be used to adjust (e.g., reduce) a difference in the voltages applied to the corresponding electrodes from that which would be otherwise required to have a desired effect on the electric field, such as those voltages calculated using the linear function 30.

[0055] As described herein, the electrodes SCC1-SCC4 can be operated to provide improved control over the electric field within the spacing between the gate G and the drain D of a device 12A-12F (and device 12G if included). To this extent, FIG. 7 shows an illustrative comparison of qualitative electric field profiles according to an embodiment. As illustrated for a FET, such as FET 2A (FIG. 1), the electric field exhibits a strong peak near the gate edge. Using a field plate, the electric field peak near the gate can be reduced by splitting the electric field into two or more peaks. However, using the electrodes SCC1-SCC4 and corresponding circuit described herein, the electric field distribution can be substantially uniform between the gate G and the drain D.

[0056] It is understood that the various device configurations shown herein are only illustrative of numerous device configurations possible. To this extent, a device can include more or fewer layers having any of various configurations. For example, a device can include an isolation layer and/or a passivation layer over some or all of the surface of the structure. Additionally, it is understood that the space-charge control electrodes SCC1-SCC4 described herein can be implemented in various types of field-effect transistors, including, for example, a field-effect transistor, a heterostructure field-effect transistor, an insulated gate field-effect transistor, an insulated gate heterostructure field-effect transistor, a multiple heterostructure field-effect transistor, a multiple heterostructure insulated gate field-effect transistor, an inverted field-effect transistor, an inverted heterostructure field-effect transistor, an inverted insulated gate field-effect transistor, an inverted insulated gate heterostructure field-effect transistor, an inverted multiple heterostructure field-effect transistor, an inverted insulated gate multiple heterostructure field-effect transistor, and/or the like.

[0057] Furthermore, the space-charge control electrodes can be implemented in other types of semiconductor devices, including for example, a diode of any type, a semiconductor resistor, a semiconductor sensor, a light emitting diode, a laser, an integrated element, and/or the like. To this extent, FIG. 8 shows a schematic structure of an illustrative diode 12H connected in a circuit 10H according to an embodiment. As illustrated, the diode 12H includes three electrodes SCC1-

SCC3 located in the spacing between the cathode and the anode. During operation of the diode 12H in the circuit 10H, the circuit 10H can include components to bias the electrodes SCC1-SCC3 as described herein.

[0058] An embodiment of a space-charge control electrode described herein can have a non-rectangular shape. For example, a space-charge control electrode can include a set of openings located along a lateral width of the electrode. To this extent, FIGS. 11A and 11B show top and side views, respectively, of an illustrative space-charge control electrode SCC located on a barrier layer 18 according to an embodiment. While the space-charge control electrode SCC is shown located on the barrier layer 18, it is understood that the space-charge control electrode SCC can be formed on any layer, which may be located between the space-charge control electrode SCC and the barrier layer 18.

[0059] Regardless, as illustrated, the space-charge control electrode SCC includes a plurality of stripes of conducting material (e.g., metal) MS1-MS4 aligned in a substantially parallel fashion along a direction of current flow through the device channel, which are physically separated from one another by openings. While four stripes of conducting material MS1-MS4 are shown in FIGS. 11A and 11B, it is understood that embodiments of the space-charge control electrode SCC can include any number of two or more stripes of conducting material. Furthermore, the stripes of conducting material MS1-MS4 are shown physically connected by a stripe of conducting material (e.g., metal) CM substantially perpendicular to the other stripes of conducting material MS1-MS4. However, it is understood that this is only illustrative of various configurations that can be utilized to electrically connect the stripes of conducting material MS1-MS4 of the space-charge control electrode SCC.

[0060] The stripes of conducting material MS1-MS4 (and corresponding openings) of the space-charge control electrode SCC can have any of various dimensions. For example, an embodiment of the space-charge control electrode SCC has multiple stripes of conducting material MS1-MS4 covering a total channel width CW (indicated in FIG. 11A). In an illustrative embodiment, within the total channel width CW, a ratio of the channel width covered by the stripes of conducting material MS1-MS4 to the channel width not covered by the stripes of conducting material MS1-MS4 is in a range of 1:1 to 10:1. A target ratio can be selected using any solution. For example, the target ratio can be selected based on an intended application (e.g., operating frequency, operating voltage, and/or the like) for the corresponding device/circuit. In particular, a space-charge control electrode SCC having a larger width CW can provide better control of the electric field over the entire device width. However, an increased width CW can result in an increased capacitance. Similarly, the stripes of conducting

material MS1-MS4 can have the widths and/or spacing selected to provide a target amount of control of the electric field while having a capacitance below an acceptable level for the corresponding application.

[0061] As discussed herein, a circuit can include components that individually bias each of the space-charge control electrodes. To this extent, FIGS. 9A-9D show illustrative biasing networks 30A-30D according to embodiments. In FIG. 9A, the biases are provided using a resistive divider type of biasing network 30A with the divider connected between the source, V_S, and drain, V_D, electrodes. In this case, a resistive component is located between each of the source voltage V_S, the voltage sources for each of the electrodes SCC1-SCC4, and the drain voltage V_D, thereby providing a unique voltage to each of the electrodes SCC1-SCC4.

[0062] The resistance values can be selected to ensure the source-drain leakage current does not exceed a maximum allowed value. For example, for a maximum off-state current, I_{OFFMAX}, and a maximum drain bias, V_{DMAX}, a total resistance of the biasing network 30A, R_{DIV}, should meet the condition $R_{DIV} > V_{DMAX} / I_{OFFMAX}$. An individual resistance value for each of the resistive components in the biasing network 30A can be selected based on the corresponding locations of the electrodes, e.g., using the linear function shown in FIG. 6.

[0063] Alternatively, the biasing network can be formed using nonlinear elements, such as transistors of any type, diodes, or the like. For example, FIG. 9B shows a biasing network 30B formed by an active voltage controlled voltage divider using a series of transistors, e.g., field effect transistors or bipolar junction transistors. In this case, each of the transistors can be controlled using a unique voltage control, VC1-VC5, thereby providing individual control over the biases provided to the space-charge control electrodes. In FIG. 9C, the biasing network 30C is formed using a capacitive divider. In this configuration, an amount of additional leakage current associated with the biasing network 30C can be reduced. In FIG. 9D, the biasing network 30D is formed by a parallel connection of biasing elements or any other type of circuitry delivering individual and independent biases to the space-charge control electrodes. In this case, the voltage bias for each space-charge control electrode (SCC1-SCC4) is provided using a pair of individually controlled transistors. It is understood that the biasing networks 30A-30D are only illustrative of various analog or digital electronic circuits that can be utilized to provide the target biasing to each space-charge control electrode.

[0064] It is understood that the various semiconductor devices described herein can be manufactured using any solution. For example, a device heterostructure can be formed using any solution, e.g., by obtaining (e.g., forming, preparing, acquiring, and/or the like) a substrate 14, forming (e.g., growing, depositing, adhering, and/or the like) an initiation layer and/or a

buffer layer thereon, forming an active layer 16 thereon, and forming a barrier layer 18 on the active layer 16. Additionally, metal electrode(s), dielectric layer(s), and/or the like, can be formed on the device heterostructure using any solution. Furthermore, as described herein, the manufacture of the device can include the formation of one or more space-charge control electrodes and/or one or more low-conducting layers using any solution. It is understood that the manufacture of a device described herein can include additional processing, including for example: the deposition and removal of a temporary layer, such as mask layer; the patterning one or more layers; the formation of one or more additional layers/contacts not shown; application to a submount (e.g., via contact pads); and/or the like.

[0065] Similarly, it is understood that the various circuits described herein can be manufactured using any solution. For example, one or more of the space-charge control electrodes of a device can include connectors for applying an external bias or other signal to the corresponding space-charge control electrode(s). Furthermore, the biasing network can comprise a built-in biasing network. The circuit also can be formed of a series of discrete components, a monolithic integrated circuit, or a hybrid circuit. Additionally, while each space-charge control electrode is shown and described as being individually controlled, it is understood that the circuit can provide a required bias to a group of two or more space-charge control electrodes that are connected to each other.

[0066] While shown and described herein as a method of designing and/or fabricating a semiconductor device and/or circuit, it is understood that aspects of the invention further provide various alternative embodiments. For example, in one embodiment, the invention provides a method of designing and/or fabricating a circuit that includes one or more of the semiconductor devices designed and fabricated as described herein.

[0067] To this extent, FIG. 10 shows an illustrative flow diagram for fabricating a circuit 126 according to an embodiment. Initially, a user can utilize a device design system 110 to generate a device design 112 for a semiconductor device as described herein. The device design 112 can comprise program code, which can be used by a device fabrication system 114 to generate a set of physical devices 116 according to the features defined by the device design 112. Similarly, the device design 112 can be provided to a circuit design system 120 (e.g., as an available component for use in circuits), which a user can utilize to generate a circuit design 122 (e.g., by connecting one or more inputs and outputs to various devices included in a circuit). The circuit design 122 can comprise program code that includes a device designed as described herein. In any event, the circuit design 122 and/or one or more physical devices 116 can be provided to a circuit fabrication system 124, which can generate a physical circuit 126 according to the circuit

design 122. The physical circuit 126 can include one or more devices 116 designed as described herein.

[0068] In another embodiment, the invention provides a device design system 110 for designing and/or a device fabrication system 114 for fabricating a semiconductor device 116 as described herein. In this case, the system 110, 114 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the semiconductor device 116 as described herein. Similarly, an embodiment of the invention provides a circuit design system 120 for designing and/or a circuit fabrication system 124 for fabricating a circuit 126 that includes at least one device 116 designed and/or fabricated as described herein. In this case, the system 120, 124 can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the circuit 126 including at least one semiconductor device 116 as described herein.

[0069] In still another embodiment, the invention provides a computer program fixed in at least one computer-readable medium, which when executed, enables a computer system to implement a method of designing and/or fabricating a semiconductor device as described herein. For example, the computer program can enable the device design system 110 to generate the device design 112 as described herein. To this extent, the computer-readable medium includes program code, which implements some or all of a process described herein when executed by the computer system. It is understood that the term "computer-readable medium" comprises one or more of any type of tangible medium of expression, now known or later developed, from which a stored copy of the program code can be perceived, reproduced, or otherwise communicated by a computing device.

[0070] In another embodiment, the invention provides a method of providing a copy of program code, which implements some or all of a process described herein when executed by a computer system. In this case, a computer system can process a copy of the program code to generate and transmit, for reception at a second, distinct location, a set of data signals that has one or more of its characteristics set and/or changed in such a manner as to encode a copy of the program code in the set of data signals. Similarly, an embodiment of the invention provides a method of acquiring a copy of program code that implements some or all of a process described herein, which includes a computer system receiving the set of data signals described herein, and translating the set of data signals into a copy of the computer program fixed in at least one computer-readable medium. In either case, the set of data signals can be transmitted/received using any type of communications link.

[0071] In still another embodiment, the invention provides a method of generating a device design system 110 for designing and/or a device fabrication system 114 for fabricating a semiconductor device as described herein. In this case, a computer system can be obtained (e.g., created, maintained, made available, etc.) and one or more components for performing a process described herein can be obtained (e.g., created, purchased, used, modified, etc.) and deployed to the computer system. To this extent, the deployment can comprise one or more of: (1) installing program code on a computing device; (2) adding one or more computing and/or I/O devices to the computer system; (3) incorporating and/or modifying the computer system to enable it to perform a process described herein; and/or the like.

[0072] The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to an individual in the art are included within the scope of the invention as defined by the accompanying claims.

CLAIMS

What is claimed is:

1. A circuit comprising:

a semiconductor device including:

a semiconductor structure including: a substrate; a barrier layer; an active layer located between the substrate and the barrier layer; and a channel formed at a junction of the active layer and the barrier layer;

a first terminal and a second terminal to the channel, wherein the first terminal and the second terminal are both located on a first side of the active layer; and

a plurality of space-charge control electrodes spaced entirely between the first terminal and the second terminal on a surface of the semiconductor structure, wherein an individual bias voltage is supplied to each of the plurality of space-charge control electrodes, wherein the bias voltage for each of the plurality of space-charge control electrodes is selected based on a bias voltage of the first terminal, a bias voltage of the second terminal, and a location of the space-charge control electrode relative to the first terminal and the second terminal, wherein at least one of the plurality of space-charge control electrodes includes a set of openings located along a lateral width of the electrode.

2. The circuit of claim 1, wherein the bias voltage for each of the plurality of space-charge control electrodes is calculated using a linear function derived from the bias voltage of the first terminal, the bias voltage of the second terminal, and the distance between the first terminal and the second terminal.

3. The circuit of claim 1, wherein the semiconductor structure further includes a buffer layer located between the substrate and the active layer, wherein a conductivity type of the buffer layer is opposite a conductivity type of the channel.

4. The circuit of claim 1, wherein the semiconductor structure further includes a buffer layer located between the substrate and the active layer, wherein at least one of: the active layer, the buffer layer, or the barrier layer includes a low-conducting layer having a sheet resistance between approximately $1x10^3$ Ohms per square and approximately $1x10^7$ Ohms per square.

5. The circuit of claim 1, further comprising a surface low-conducting layer located on a surface of the semiconductor device between the first terminal and a gate, wherein the surface low-conducting layer is isolated from the gate by a gate insulating layer.

6. The circuit of claim 1, wherein the semiconductor device further includes an insulating layer located between at least one of the plurality of space-charge control electrodes and the semiconductor structure, and the insulating layer has a different thickness for each of the plurality of space-charge control electrodes.

7. The circuit of claim 1, wherein the semiconductor device further includes at least one field plate connected to one of: the first terminal or the second terminal, and wherein the plurality of space-charge control electrodes are spaced entirely between the at least one field plate and the other of: the first terminal or the second terminal.

8. The circuit of claim 1, wherein the substrate is one of: a conducting substrate or a semiconducting substrate, and wherein a conductivity type of the substrate is opposite a conductivity type of the channel.

9. The circuit of claim 1, wherein the at least one of the plurality of space-charge control electrodes includes a plurality of stripes of conducting material aligned in a substantially parallel orientation along a direction of current flow through the semiconductor device, wherein the plurality of stripes of conducting material are separated by the set of openings.

10. The circuit of claim 9, further comprising a center stripe of conducting material substantially perpendicular to the plurality of stripes of conducting material, wherein the center stripe of conducting material electrically connects the plurality of stripes of conducting material.

11. A circuit comprising:

a semiconductor device including:

a semiconductor structure including: a substrate; a barrier layer; an active layer located between the substrate and the barrier layer; and a channel formed at a junction of the active layer and the barrier layer;

a first terminal and a second terminal to the channel, wherein the first terminal and the second terminal are both located on a first side of the active layer; and

a plurality of space-charge control electrodes spaced entirely between the first terminal and the second terminal on a surface of the semiconductor structure, wherein an individual bias voltage is applied to each of the plurality of space-charge control electrodes, wherein the bias voltage for each of the plurality of space-charge control electrodes is configured to deplete a region of the channel under the corresponding space-charge control electrode at an operating voltage applied to the second terminal, wherein at least one of the plurality of space-charge control electrodes includes a set of openings located along a lateral width of the electrode.

12. The circuit of claim 11, wherein the bias voltage for each of the plurality of space-charge control electrodes is calculated using a linear function derived from the bias voltage of the first terminal, the bias voltage of the second terminal, and the distance between the first terminal and the second terminal.

13. The circuit of claim 11, wherein the semiconductor structure further includes a buffer layer located between the substrate and the active layer, wherein a conductivity type of the buffer layer is opposite a conductivity type of the channel.

14. The circuit of claim 11, wherein the semiconductor structure further includes a buffer layer located between the substrate and the active layer, wherein at least one of: the active layer, the buffer layer, or the barrier layer includes a low-conducting layer having a sheet resistance between approximately $1x10^3$ Ohms per square and approximately $1x10^7$ Ohms per square.

15. The circuit of claim 11, wherein the semiconductor device further includes an insulating layer located between at least one of the plurality of space-charge control electrodes and the semiconductor structure, and the insulating layer has a different thickness for each of the plurality of space-charge control electrodes

16. The circuit of claim 11, wherein the substrate is one of: a conducting substrate or a semiconducting substrate, and wherein a conductivity type of the substrate is opposite a conductivity type of the channel.

17. The circuit of claim 11, wherein the at least one of the plurality of space-charge control electrodes includes a plurality of stripes of conducting material aligned in a substantially parallel

orientation along a direction of current flow through the semiconductor device, wherein the plurality of stripes of conducting material are separated by the set of openings.

18. The circuit of claim 17, further comprising a center stripe of conducting material substantially perpendicular to the plurality of stripes of conducting material, wherein the center stripe of conducting material electrically connects the plurality of stripes of conducting material.

19. A circuit comprising:

a group III nitride-based transistor including:

a semiconductor structure including: a substrate; a barrier layer; an active layer located between the substrate and the barrier layer; a buffer layer located between the active layer and the substrate; and a channel formed at a junction of the active layer and the barrier layer;

a gate and a drain, wherein the gate and the drain are both located on a first side of the active layer; and

a plurality of space-charge control electrodes spaced entirely between the gate and the drain on a surface of the semiconductor structure, wherein an individual bias voltage is applied to each of the plurality of space-charge control electrodes, wherein the bias voltage for each of the plurality of space-charge control electrodes is selected based on a bias voltage of the gate, a bias voltage of the drain, and a location of the space-charge control electrode relative to the gate and the drain, wherein at least one of the plurality of space-charge control electrodes includes a set of openings located along a lateral width of the electrode.

20. The circuit of claim 19, wherein a conductivity type of at least one of: the buffer layer or the substrate, is opposite a conductivity type of the channel.

21. The circuit of claim 19, wherein at least one of: the active layer, the buffer layer or the barrier layer, includes a low-conducting layer having a sheet resistance between approximately $1x10^3$ Ohms per square and approximately $1x10^7$ Ohms per square.

FIG. 1
Prior Art

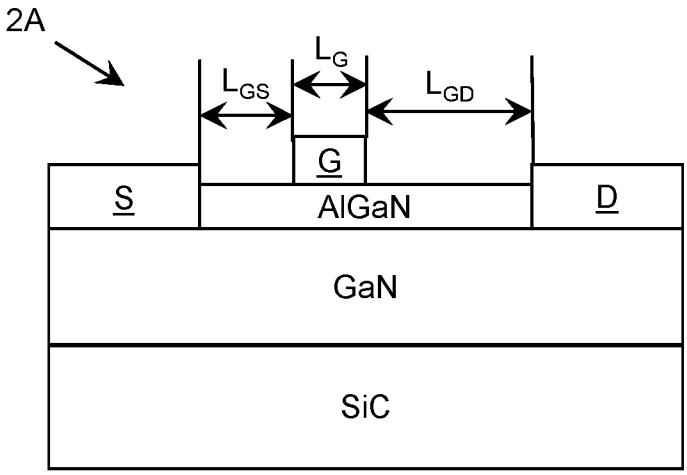


FIG. 2
Prior Art

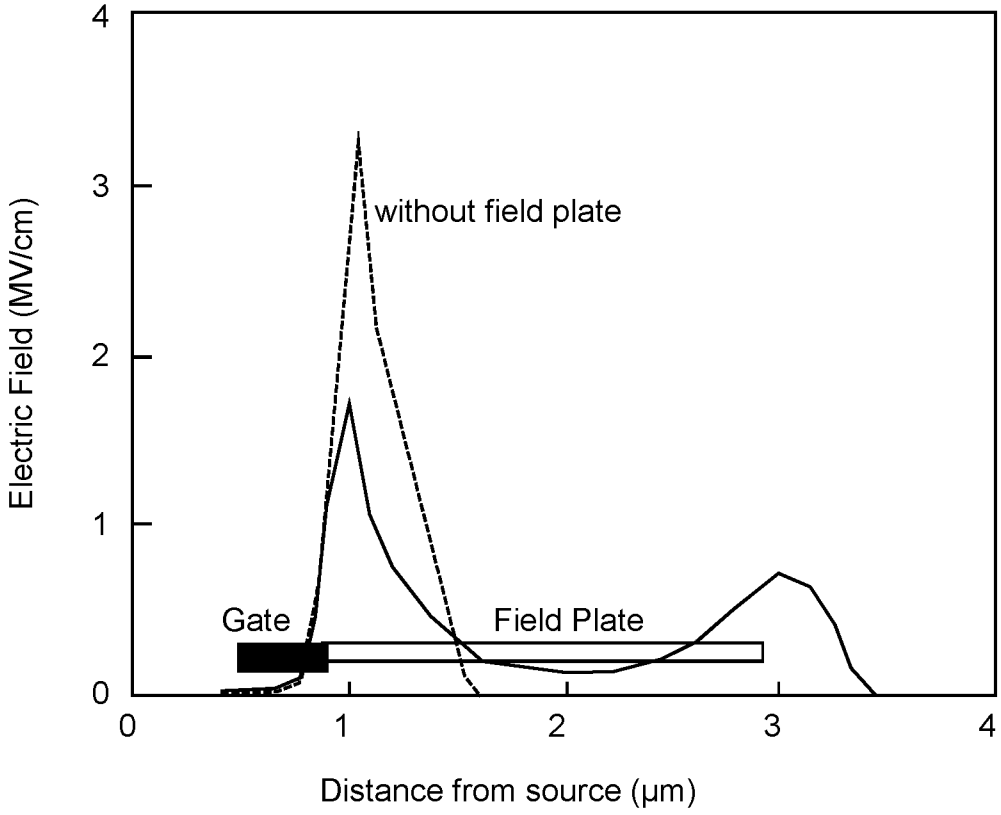


FIG. 3

Prior Art

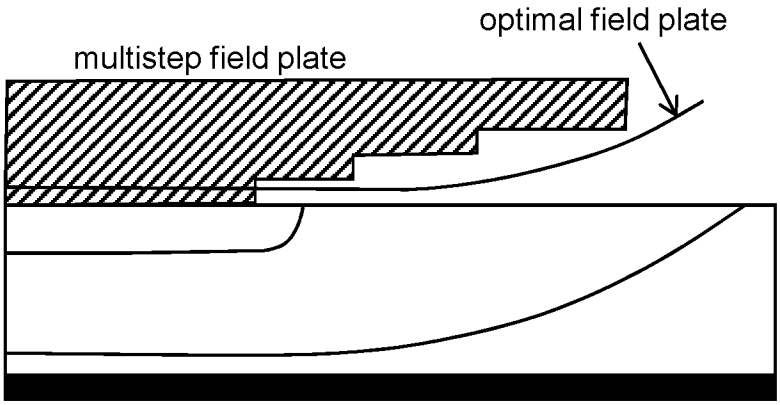


FIG. 4

Prior Art

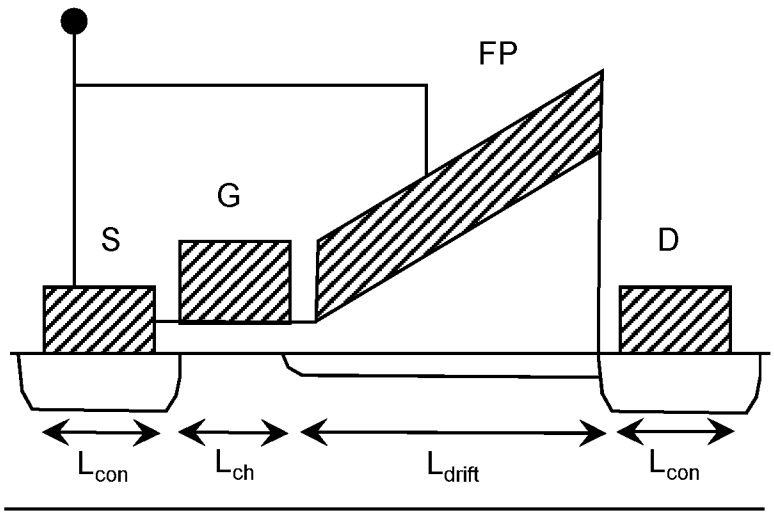


FIG. 5A

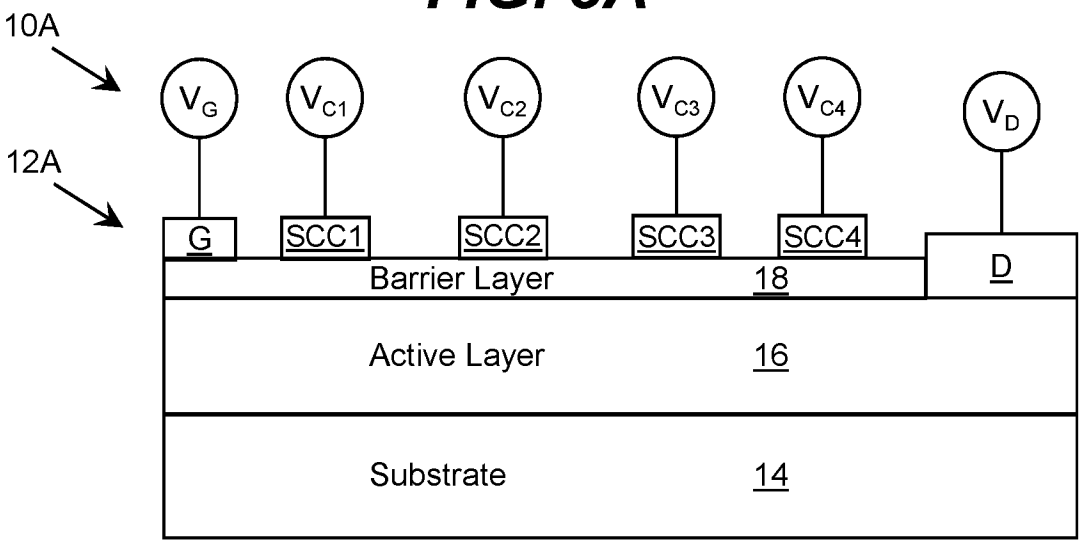

10A
12A
V_G
V_{C1}
V_{C2}
V_{C3}
V_{C4}
V_D
G
SCC1
SCC2
SCC3
SCC4
D
Barrier Layer
18
Active Layer
16
Substrate
14

FIG. 5B

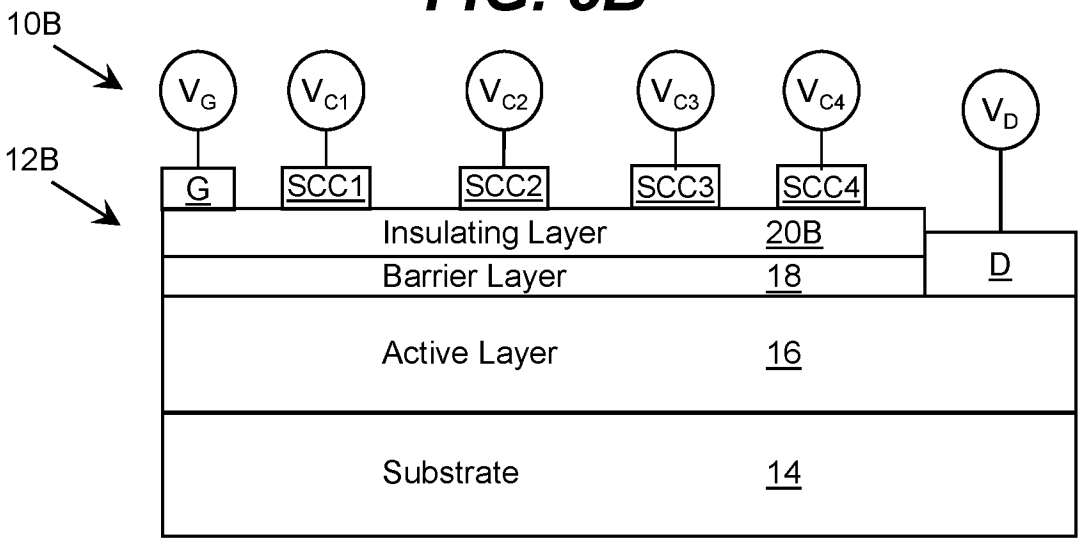

10B
12B
V_G
V_{C1}
V_{C2}
V_{C3}
V_{C4}
V_D
G
SCC1
SCC2
SCC3
SCC4
D
Insulating Layer
20B
Barrier Layer
18
Active Layer
16
Substrate
14

FIG. 5C

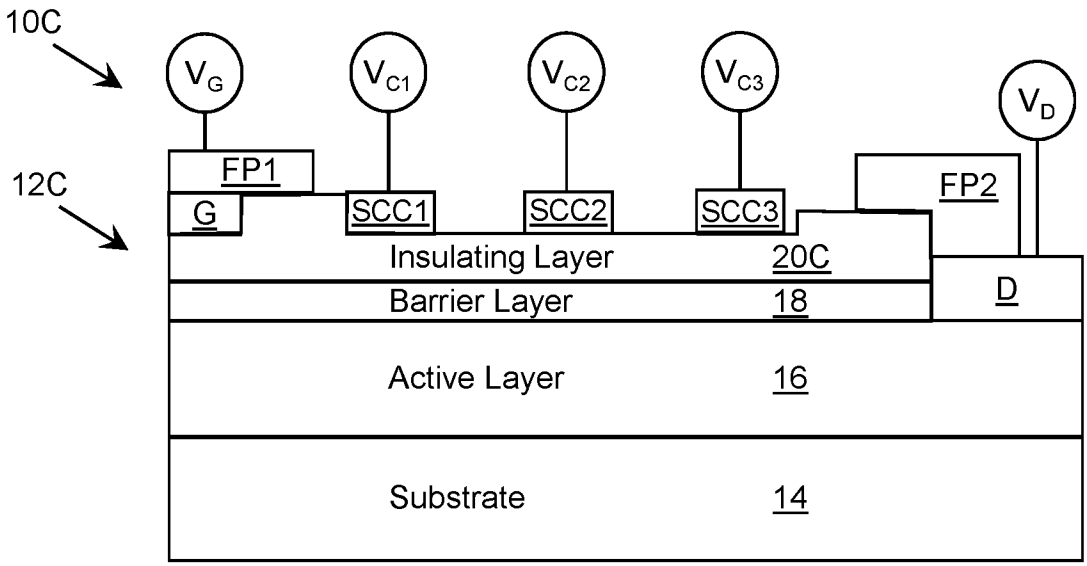

10C
12C
V_G
V_{C1}
V_{C2}
V_{C3}
V_D
FP1
G
SCC1
SCC2
SCC3
FP2
Insulating Layer
20C
D
Barrier Layer
18
Active Layer
16
Substrate
14

FIG. 5D

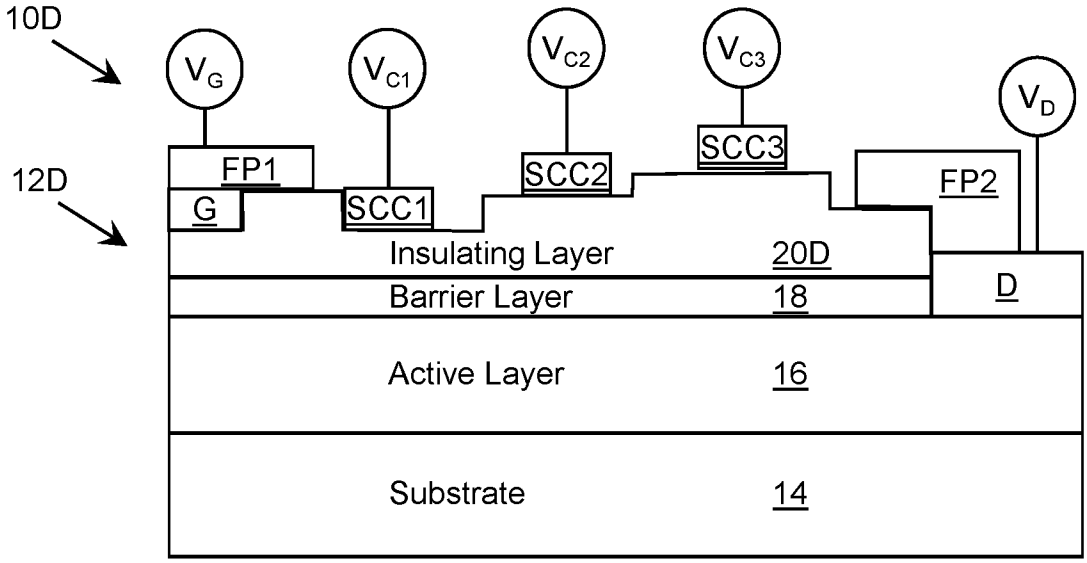

10D
12D
V_G
V_{C1}
V_{C2}
V_{C3}
V_D
FP1
G
SCC1
SCC2
SCC3
FP2
Insulating Layer
20D
D
Barrier Layer
18
Active Layer
16
Substrate
14

FIG. 5E

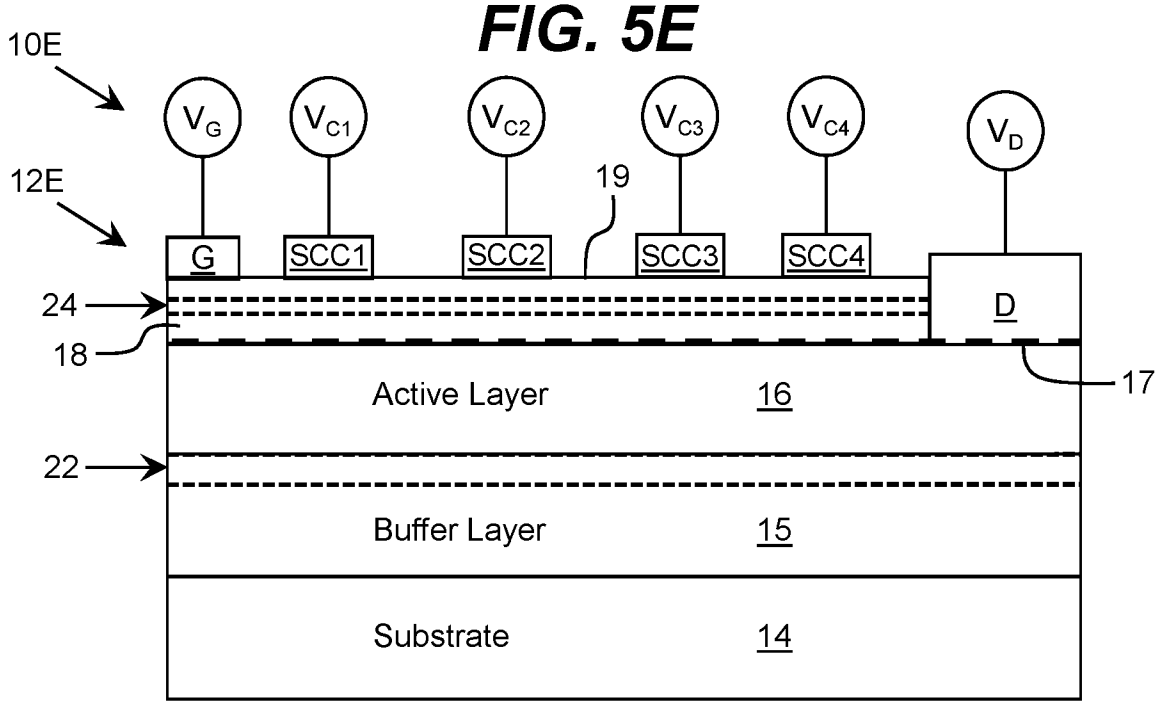

10E
12E
V_G
V_{C1}
V_{C2}
V_{C3}
V_{C4}
V_D
19
G
SCC1
SCC2
SCC3
SCC4
D
24
18
17
Active Layer 16
22
Buffer Layer 15
Substrate 14

FIG. 5F

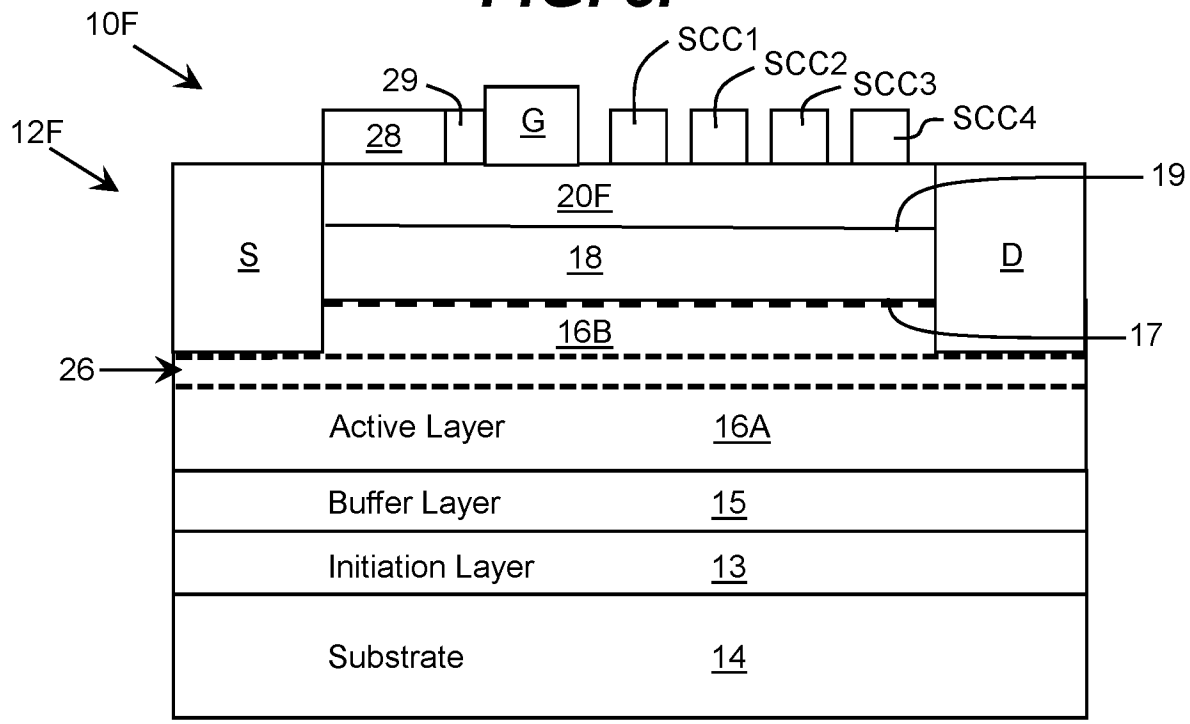

10F
12F
29
28
G
SCC1
SCC2
SCC3
SCC4
19
20F
S
18
D
16B
17
26
Active Layer 16A
Buffer Layer 15
Initiation Layer 13
Substrate 14

FIG. 5G

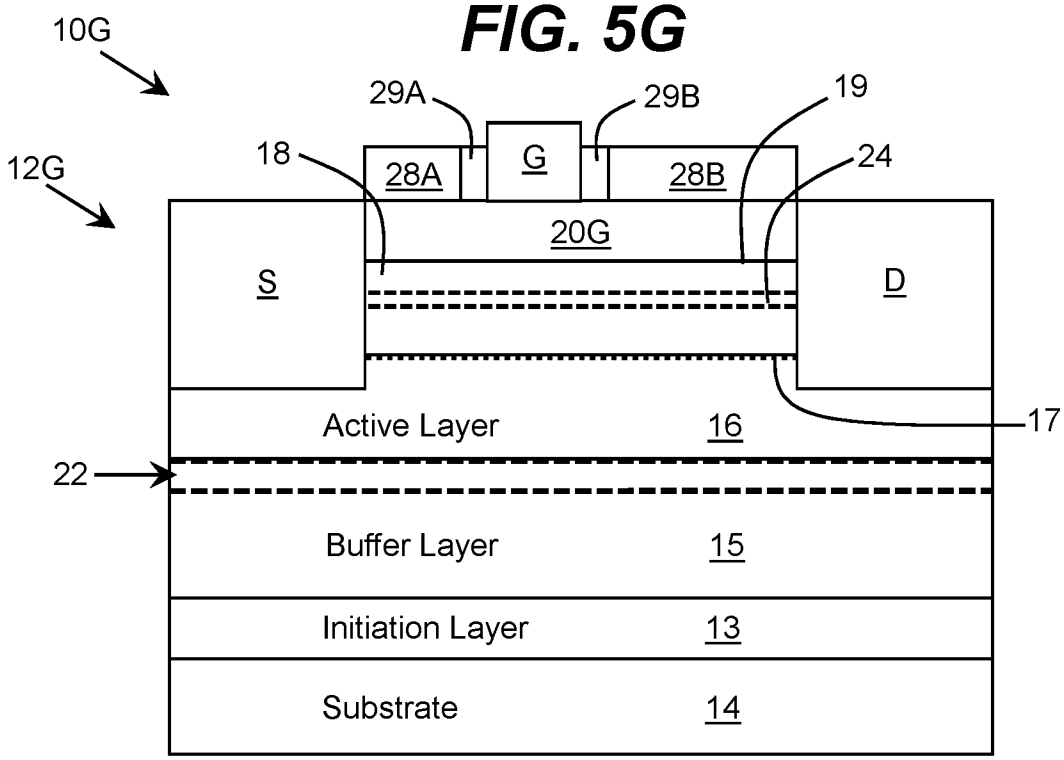

10G
12G
29A
29B
19
18
24
28A
G
28B
20G
S
D
17
Active Layer
16
22
Buffer Layer
15
Initiation Layer
13
Substrate
14

FIG. 6

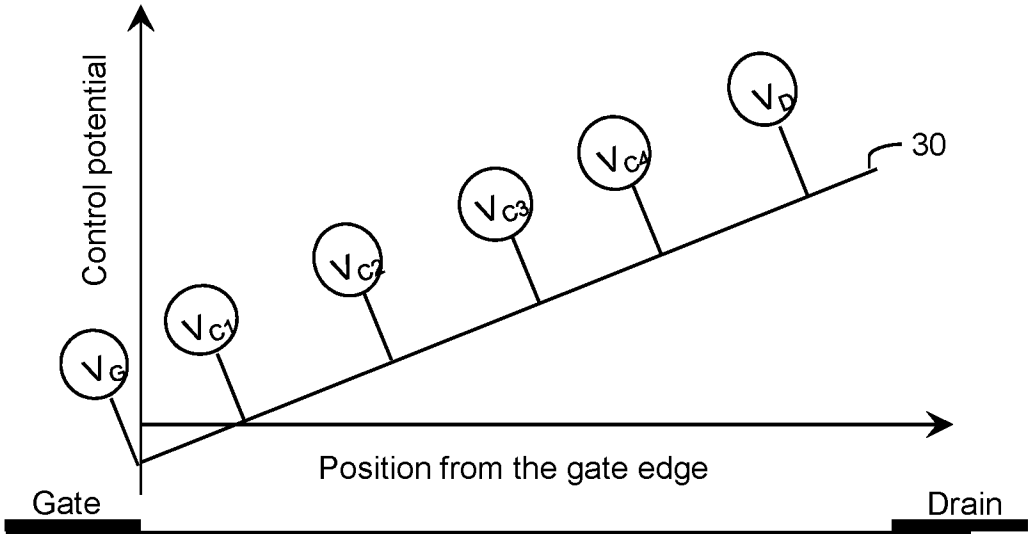

Control potential
V_G
V_{C1}
V_{C2}
V_{C3}
V_{C4}
V_D
30
Position from the gate edge
Gate
Drain

FIG. 7

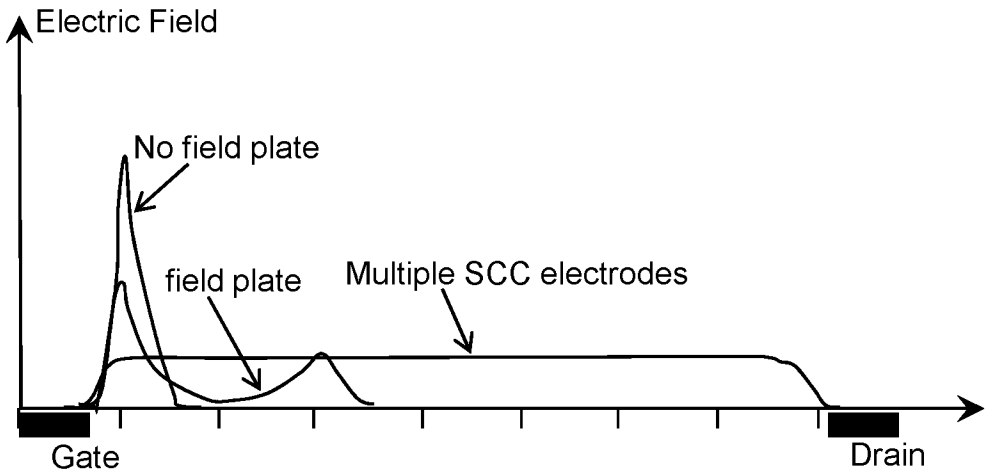

Electric Field
No field plate
field plate
Multiple SCC electrodes
Gate
Drain

FIG. 8

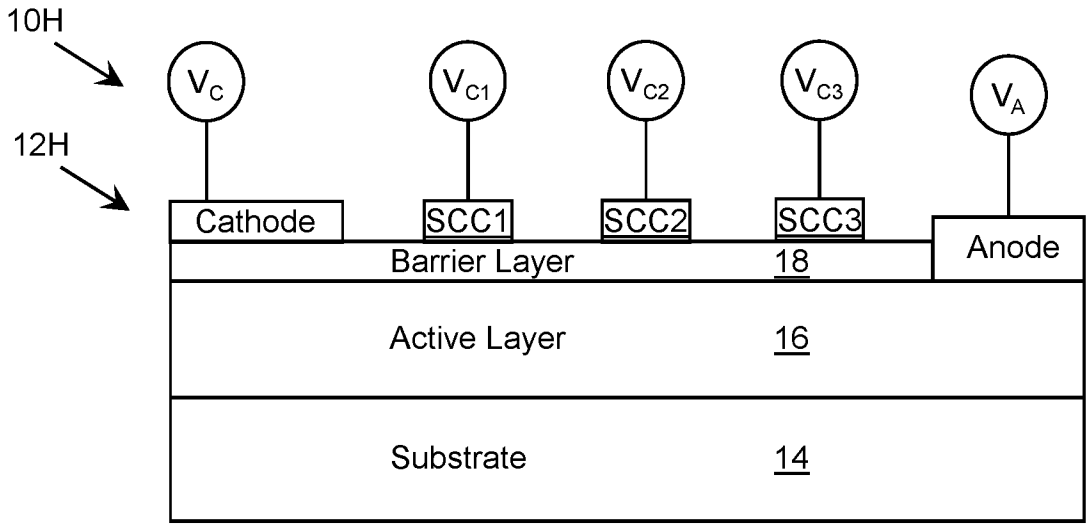


FIG. 11A

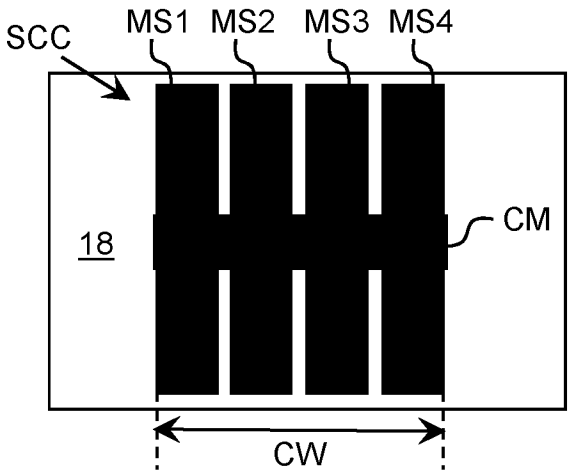


FIG. 11B

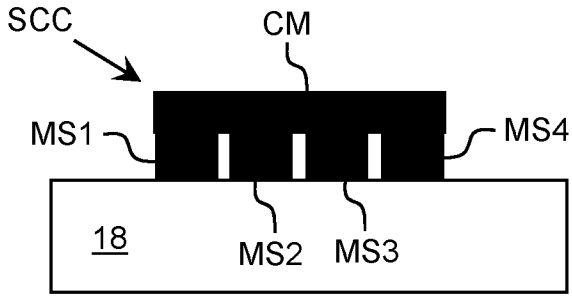


FIG. 9A

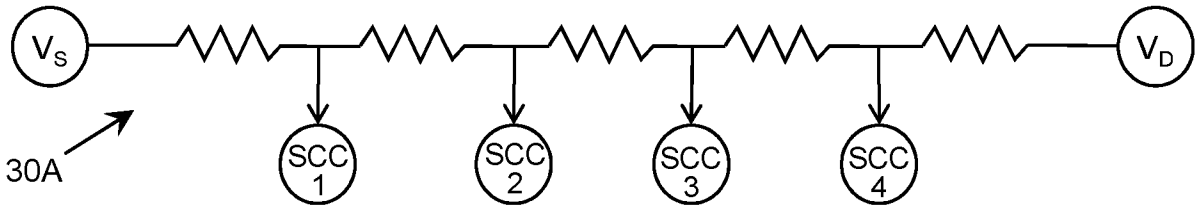


FIG. 9B

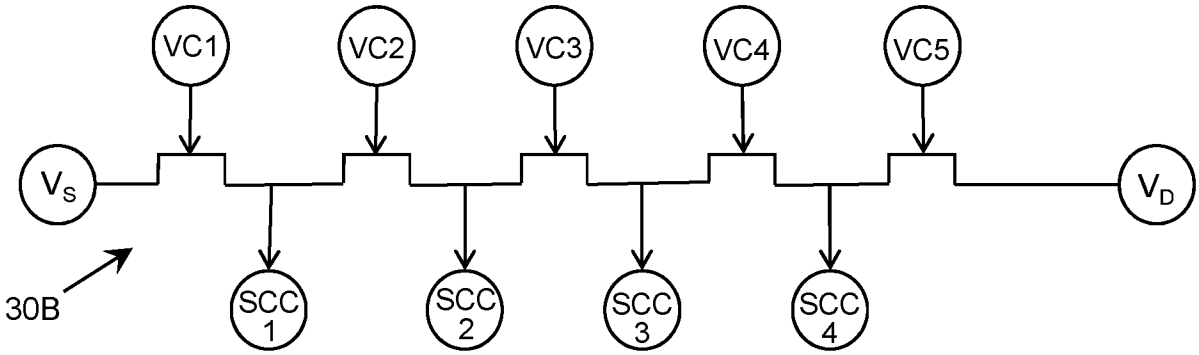


FIG. 9C

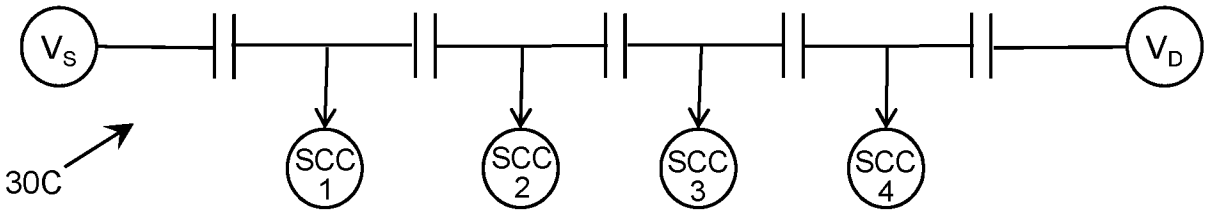


FIG. 9D

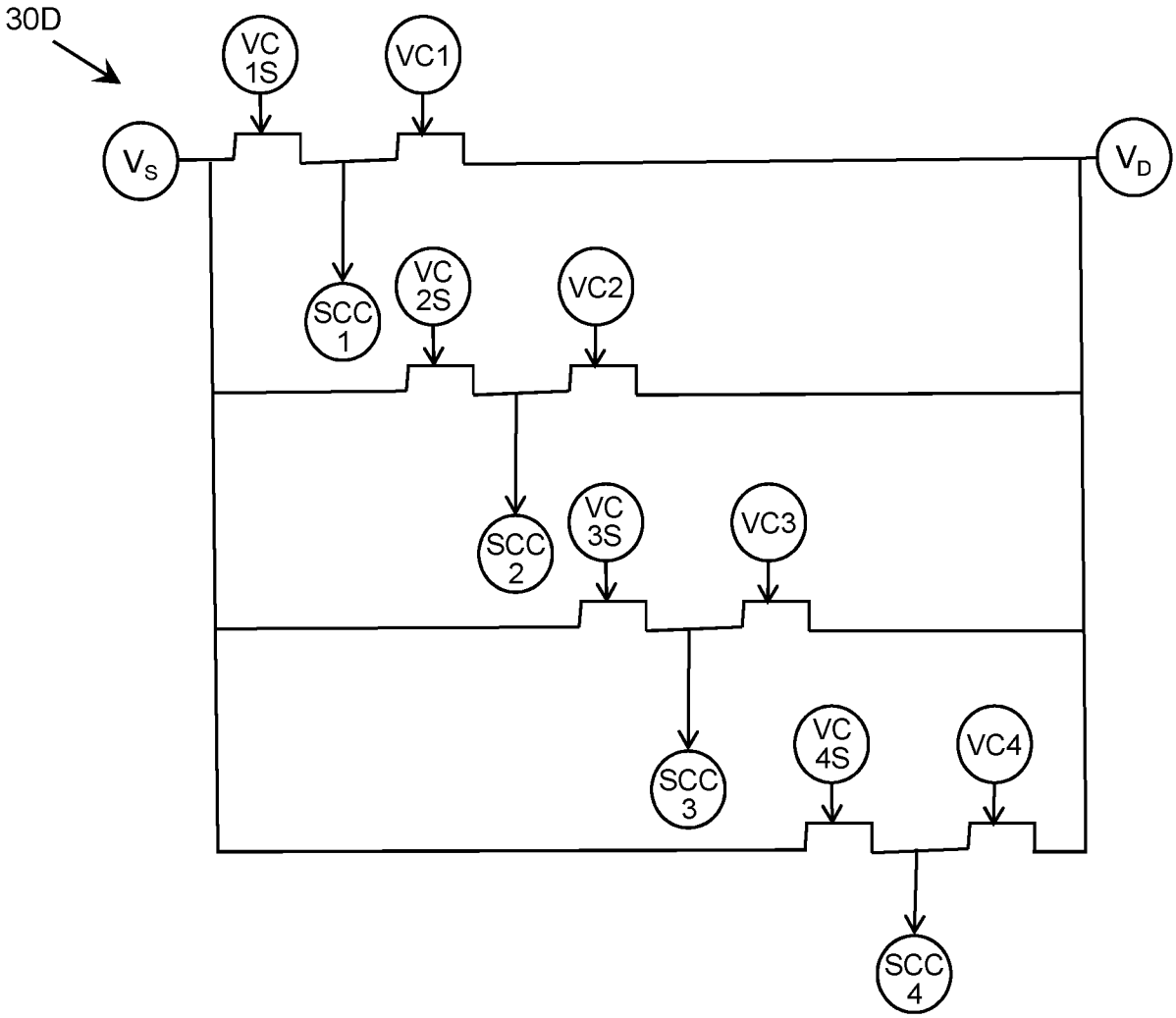
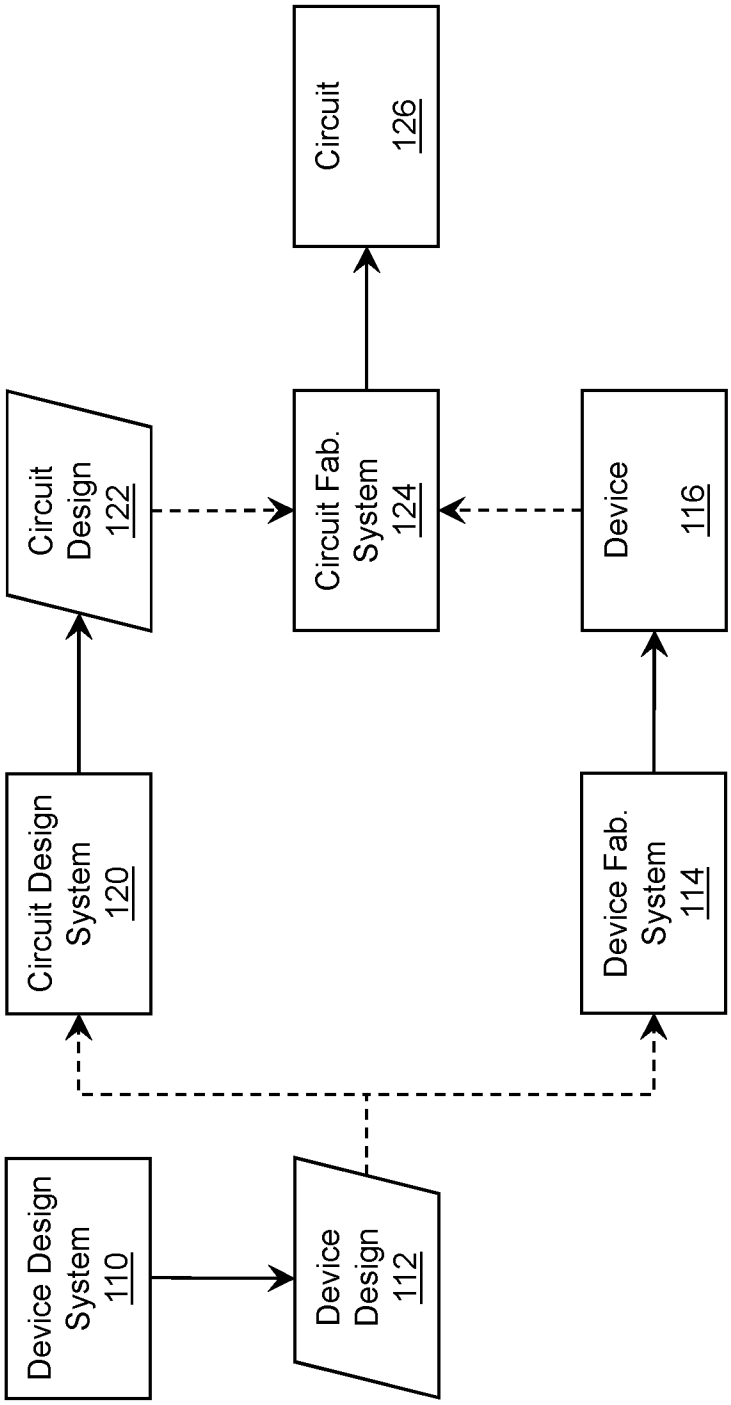

30D
VC 1S
VC1
V_S
V_D
SCC 1
VC 2S
VC2
SCC 2
VC 3S
VC3
SCC 3
VC 4S
VC4
SCC 4

FIG. 10


Device Design System 110
Device Design 112
Circuit Design System 120
Circuit Design 122
Circuit Fab. System 124
Device Fab. System 114
Device 116
Circuit 126

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/066650

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 29/778; H01L 21/336; H01L 29/739; H01L 29/06; H01L 21/335; H01L 31/00; H01L 21/76

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: gate, drain, bias voltage, space-charge control electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0062693 A1 (MASAYASU TANAKA) 14 March 2013 See abstract, paragraphs [0034]-[0056] and figures 1-7.	1-2,9,11-12,17,19
Y		6-8,15-16,20
A		3-5,10,13-14,18,21
Y	US 2008-0073670 A1 (KYOUNGHOON YANG et al.) 27 March 2008 See abstract, paragraphs [0033]-[0042], claims 1, 4 and figure 2.	6-7,15
Y	US 2014-0353723 A1 (INTERNATIONAL RECTIFIER CORPORATION) 04 December 2014 See abstract, paragraph [0027] and figure 2.	8,16,20
A	US 2011-0221011 A1 (ELDAT BAHAT-TREIDEL et al.) 15 September 2011 See abstract, paragraphs [0033]-[0040] and figures 1-3.	1-21
A	KR 10-2014-0115585 A (SEOUL SEMICONDUCTOR CO., LTD.) 01 October 2014 See abstract, paragraphs [0043]-[0089] and figures 4-10.	1-21
A	US 2009-0159925 A1 (OSAMU MACHIDA) 25 June 2009 See abstract, paragraphs [0034]-[0073] and figures 3-4.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2016 (29.04.2016)	**29 April 2016 (29.04.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/066650

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