



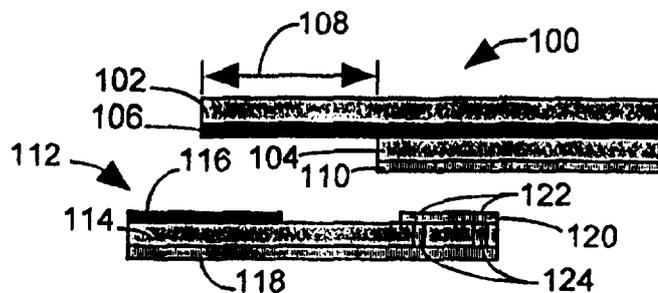
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(54) Title: PRINTED CIRCUIT BOARD LAYERING CONFIGURATION FOR VERY HIGH BANDWIDTH INTERCONNECT

## (57) Abstract

A ground plane interconnection is provided on first and second substrates (100, 112), the first and second substrates (100, 112) having respective first and second ground layers (110, 118) disposed on a first surface of each of the first and second substrates (100, 112). A ground conductor strip (120) is disposed on a second surface of the second substrate (112), wherein the ground conductor strip (120) includes a plurality of electrically conductive members (124) which pass through the second substrate (112) to electrically couple the ground conductor strip (120) and the second ground layer (118). The first substrate (100) is positioned with respect to the second substrate (112) such that when the first substrate (100) is placed proximate the second substrate (112), the ground conductor strip (120) electrically couples the first and second ground layers (110, 118) to form a continuous ground plane. A method of forming a reduced-inductance continuous ground plane is also provided.



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-1-

## **PRINTED CIRCUIT BOARD LAYERING CONFIGURATION FOR VERY HIGH BANDWIDTH INTERCONNECT**

### **Field Of The Invention**

5           The present invention relates generally to  
conductor interconnections. More particularly, the  
present invention relates to a conductor strip and  
substrate interconnect configuration exhibiting low  
inductance and high bandwidth characteristics.

### **Background Of The Invention**

10           Printed circuit board (PCB) substrates  
carrying high frequency signals (upwards of or greater  
than 1 gigahertz) often include microstrip or stripline  
conductor configurations for providing shielding and  
15           controlled impedance for the high frequency signals.  
For purposes of signal integrity, it is often necessary  
or desirable to interconnect these substrates to form  
one continuous substrate. In most cases this type of  
interconnect is accomplished with coaxial type  
20           connectors because of their high frequency capabilities  
- in the tens of gigahertz range. A limitation of  
coaxial type connectors is their large size, and their  
interconnect density is low relative to elastomeric,  
flex circuit, or standard pin and socket-type  
25           connectors.

A flex circuit provides a method of  
interconnecting such substrates. One such flex circuit

-2-

is described in U.S. Patent No. 5,261,826 entitled "Device for Contacting Shielded Conductors," issued November 16, 1993 to Leeb et al. The Leeb et al. device contacts two shielded conductors, each one of which is embedded in or located on a dielectric sheet or laminate. In the Leeb et al. device the ground plan is used as a shield to completely surround a signal trace. The contact for a ground is made from the surface layer of one of the substrates to the surface layer of the other substrate. A via or plated through-hole is used to connect the signal from the surface layer to an internal layer and the signal is further propagated through the substrate. The via is a location in the signal path where a discontinuity in the impedance of the transmission path will occur. These impedance discontinuities result in a reduction of the bandwidth of the signal transmission path.

A need exists for a flex circuit interconnection that has a low inductance, continuous ground plane between the interconnecting substrates. At the same time, unlike the signal traces of Leeb et al., this flex circuit interconnection should provide a tightly controlled impedance with low discontinuity between signal traces.

The present invention provides a solution to these and other problems, and offers other advantages over the prior art.

### **Summary Of The Invention**

The present invention relates to a ground plane interconnection including a ground conductor strip

-3-

having a plurality of conductive members which allows a continuous ground plane to be formed between the ground planes of interconnecting substrates, thereby reducing inductive effects. The present invention also relates to an interconnection which has a signal conductor geometry that can be configured to provide a constant transmission line impedance from one substrate to the other (i.e., low discontinuity between signal traces).

In accordance with one embodiment of the invention, a ground plane interconnection is provided on first and second substrates, the first and second substrates having respective first and second ground layers disposed on a first surface of each of the first and second substrates. A ground conductor strip is disposed on a second surface of the second substrate, wherein the ground conductor strip includes a plurality of electrically conductive members which pass through the second substrate to electrically couple the ground conductor strip and the second ground layer. The first substrate is positioned with respect to the second substrate such that when the first substrate is placed proximate the second substrate, the ground conductor strip electrically couples the first and second ground layers to form a continuous ground plane. A method of forming a continuous ground plane is also provided in which the ground planes in adjacent circuit boards are coupled to form a reduced inductance, continuous ground plane.

In accordance with another embodiment of the invention, a circuit interconnection is provided which includes at least a first and a second substrate, where each substrate has a first ground layer with an exposed

-4-

bottom side and a top side positioned proximate a first dielectric layer. Each substrate has at least one signal trace positioned between the first dielectric layer and a second dielectric layer, where the signal trace and the second dielectric layer extend beyond the end of the first ground layer and the first dielectric layer. Each substrate further has a second ground layer positioned between the second dielectric layer and a third dielectric layer, where the second ground layer and the third dielectric layer extend beyond the end of the signal trace and the second dielectric layer. The first and second substrates are formed such that when one substrate is rotated 180 degrees with respect to the other substrate into a mating position, the first ground layers, the signal trace, and the second ground layers of the first and the second substrates are each electrically coupled to one another to form a mated circuit interconnection.

These and various other features as well as advantages which characterize the present invention will be apparent upon reading of the following detailed description and review of the associated drawings.

### **Brief Description Of The Drawings**

FIG. 1 is a diagram of a printed circuit board substrate.

FIG. 2 is a diagram of a printed circuit board substrate having a ground conductor strip.

FIG. 3 is a cross-sectional view of the ground conductor strip.

-5-

FIG. 4 illustrates the positioning of two substrates which allows for connection of their signal traces and ground layers.

FIG. 5 is a diagram of two substrates electrically coupled to form a continuous ground plane, and to form continuous signal traces.

FIG. 6 illustrates the contact location of the ground conductor strip and the ground layer of a connecting substrate.

FIG. 7 illustrates the positioning of two stripline substrates which forms two continuous ground planes.

FIG. 8 illustrates another embodiment of two microstrip substrates which form one continuous ground planes.

FIG. 9 illustrates another embodiment of two stripline substrates which form two continuous ground planes.

### **Detailed Description**

Referring now to FIG. 1, a printed circuit board (PCB) substrate 100 is shown. The substrate is the physical supporting material upon which an electronic circuit is fabricated. The substrate 100 of the preferred embodiment is made of flexible materials so that the substrate 100 as a whole is flexible. Substrate 100 has a first dielectric layer 102, and second dielectric layer 104. Disposed between

-6-

dielectric layers 102 and 104 are signal traces 106 that carry electronic signals through the substrate 100. Dielectric 102 extends a distance 108 beyond dielectric 104, thereby exposing a portion of signal trace 106. 5 The exposed portions of the signal traces may be coupled to signal traces of another substrate to form a complete signal path, as will be described more fully below.

The signal traces 106 of the preferred embodiment can be a part of either a stripline transmission system or a microstrip transmission system. 10 Stripline is a type of transmission line used in a circuit consisting of a narrow, flat conductor sandwiched between, and insulated from, wider flat grounded conductors. Microstrip is a transmission 15 system in which a signal conductor is supported above a ground plane. Substrate 100 of Fig. 1 represents a microstrip substrate having ground plane 110, dielectric layers 102 and 104, and signal traces 106.

Referring now to Fig. 2, substrate 112 20 represents a second substrate that can be connected to substrate 100 to form a continuous interconnection of the substrates. The portion of substrate 112 shown in Fig. 2 includes dielectric material 114 and signal traces 116. A ground layer 118 is formed on the 25 dielectric layer 114 opposite the signal traces 116. Also, coupled to dielectric layer 114 is a conductor strip 120 which engages the dielectric layer 114 beyond the end of signal traces 116. The conductor strip 120 of the preferred embodiment is photographically 30 generated on the surface of the dielectric layer 114. Alternatively, other types of strip deposit techniques

-7-

can be used, such as chemical, vapor, electrical, vacuum, or other processes.

As will be appreciated by those skilled in the art, very high bandwidth signals require tightly controlled impedance signal transmission paths in order to avoid reflecting power that is intended to be transmitted. Discontinuities in the geometry of the signal path or the ground path result in variations in the distributed inductance and capacitance of the transmission path. Since the impedance of the transmission path is indicated by the ratio of these distributed parameters, and the amount of the signal that is reflected is determined by the variation in the transmission line impedance, avoiding ground plane and signal trace discontinuities is of the utmost importance. The large number of conducting through-holes reduces the inductance and allows the impedance of the ground interconnect to match that of the ground plane on the substrate.

The conductor strip 120 of Fig. 2 includes a plurality of openings 122 which extend from the conductor strip 120 through the dielectric layer 114, to the ground layer 118. Conductive members are formed in openings 122 to electrically connect conductor strip 120 to ground layer 118. These conductive members allow ground layer 110 of substrate 100 to be directly coupled to a ground layer that contacts the conductor strip 120.

Fig. 3 shows a cross-sectional view of the conductor strip 120 having openings 122, ground layer 118, and conductive members 124. Openings 122 can be formed by boring through conductive strip 120 and the

-8-

dielectric layer 114 below conductive strip 120. The  
conductive members 124 can be solid conductors,  
conductive through-holes or vias, or other conductive  
members. Solid conductors can be positioned between  
5 conductive strip 120 and ground layer 118 through  
openings 122. Similarly, conductive through-holes can  
be formed onto the inner walls of openings 122 to  
provide an electrical connection between conductive  
strip 120 and ground layer 118. It is also conceivable  
10 to provide a conductive strip 120 having fixed  
conductive members 124 further being fixed to ground  
layer 118, and forming the dielectric layer 114 around  
conductive members 124. A relatively large number of  
conductive members 124 connecting the conductive strip  
15 120 to ground layer 118 are used to maintain a high  
conductivity and low inductance at a connection point  
between a ground layer of another substrate and the  
conductive strip 120.

As an alternative (or in addition) to the  
20 conductive members 124, a flex conductor 125 can be  
electrically coupled between conductive strip 120 and  
ground layer 118. One or more flex conductors 125 can  
be used similarly to the conductive members 124, by  
providing a low impedance current path between the  
25 conductive strip 120 and ground layer 118. This is  
particularly beneficial for use with substrates in which  
openings 122 have not been provided.

Referring now to Fig. 4, substrate 100 can be  
oriented in a manner to allow connection of its signal  
30 traces 106 and ground layer 110 to the signal traces 116  
and conductive strip 120 of substrate 112. Substrate  
100 is placed so that the signal traces 106 are facing

-9-

signal traces 116 of substrate 112. The extension 108 of dielectric 102 and signal traces 106 beyond that of dielectric 104 and ground layer 110, allows signal traces 106 to be coupled to signal traces 116 of substrate 112. Substrate 112 also includes a second dielectric layer (not shown) above signal traces 116, that provides an exposed portion of the signal traces 116, which is the portion of the signal traces 116 seen in Fig. 4.

The orientation of substrates 100 and 112 in Fig. 4 also depicts the manner in which ground layer 110 is electrically coupled to ground layer 118. In connecting substrate 100 to substrate 112, the parallel plane of ground layer 110 will make contact with conductor strip 120, thereby connecting ground layer 110 to ground layer 118 through conductive members 124. This is described more fully in connection with the description of Fig. 5 below.

Referring now to Fig. 5, the interconnection of substrate 100 and substrate 112 of the preferred embodiment is shown. As previously described, ground layer 110 of substrate 100 makes contact with conductor strip 120 when substrate 100 is moved into contact with substrate 112. This interconnection provides a direct electrical contact from ground layer 110, through conductor strip 120, conductive members 124, to ground layer 118. Electrical currents can therefore flow directly from ground layer 110 to ground layer 118, and vice-versa, as shown by arrow 126. This mechanical configuration allows the ground layers 110 and 118 to mate in such a way that an extremely low inductance current path is produced.

-10-

The area where conductor strip 120 of substrate 112 contacts the ground layer 110 of substrate 100 can be seen in Fig. 6. The conductor strip 120 contacts the ground layer 110 over the entire surface of conductor strip 120. This can be seen by the dashed area 128, which depicts the location of the contact point of conductor strip 120 when the substrates 100 and 112 are interconnected.

Again referring to Fig. 5, substrate 100 of the preferred embodiment has a flexible dielectric 102 and signal traces 106 to allow the signal traces 106 to be coupled to the signal traces 116 of substrate 112. This can be seen by referring to flex area 130, which shows a non-planar portion of substrate 100. The "flexing" of substrate 100 in the flex area 130 occurs as a result of applying a pressure to dielectric 102 and signal traces 106 in the direction of arrow 132. The curvature in flex area 130 allows an electrical contact to be made between signal traces 106 and signal traces 116 on substrate 100 and 112 respectively.

Signal traces 106 and 116 can be reduced in width in situations where maintaining a constant signal trace impedance is critical. Because there is an overlap of signal traces 106 and 116 where the electrical contact is made, the impedance is reduced due to the additional current-carrying capacity. By reducing the width of the signal traces at the contact location, the impedance can be restored to more closely match that of the remaining portions of the signal traces.

-11-

Referring now to Fig. 7, the principles described above may also be applied to stripline having conductive layers on both sides of the dielectric encompassing the signal traces. Fig. 7 shows a first  
5 stripline substrate 150 having signal traces 152 disposed between two dielectric layers 154 and 156. A portion of signal traces 152 are not totally encompassed by dielectric layers 154 and 156, as can be seen by the signal trace portion formed on dielectric layer 154 over  
10 the distance 158. A first ground layer 160 and a second ground layer 162 comprise the two ground planes in the stripline transmission substrate 150.

The conductor strip 164 is used similarly to conductor strip 120 of the microstrip substrate 112 described above. Conductor strip 164 includes multiple  
15 openings 166 for providing access to conductive members 168. Conductive members 168 provide an electrical connection between conductor strip 164 and the first ground layer 160.

Fig. 7 also shows a second stripline substrate 170 having signal traces 172 disposed between two dielectric layers 174 and 176. A portion of signal traces 172 are also exposed over a distance 178 from the truncated edge of dielectric layer 176. A first ground  
20 layer 180 and a second ground layer 182 comprise the two ground planes in the stripline transmission substrate 170. Conductor strip 184 includes multiple openings 186 for providing access to conductive members 188. Conductive members 188 provide an electrical connection  
25 between conductor strip 184 and the first ground layer 180. Again, the conductive members 168 and 188 can be  
30

-12-

solid conductors, conductive through-holes or vias, or other conductive members.

Substrate 150 can be oriented in a manner to allow connection of its signal traces 152 and second ground layer 162 to the signal traces 172 and conductive strip 184 of substrate 170 respectively. Likewise, second ground layer 182 is oriented to allow planar contact with conductive strip 164 of substrate 150. Substrates 150 and 170 are oriented so that the extended portions of signal traces 152 are facing the extended portions of signal traces 172. The extended portions of signal traces 152 and 172, along dielectric layers 154 and 174 respectively, allow signal traces 152 and 172 to be coupled to together when the substrates are moved into contact with each other.

In one embodiment of the invention, such striplines are used, and the associated substrates are made of a pliable material so that one or both of the substrates 150 and 170 are flexible. This flexibility allows an interconnection of the signal traces of substrates 150 and 170 to be made by applying a pressure on substrate 150 in the direction of arrow 190, or by applying a pressure on substrate 170 in the direction of arrow 192, or both. The substrates will flex in the area of the exposed signal traces 152 and 172, so that these signal traces contact each other.

Referring now to Fig. 8, the principles described for the interconnection of Fig. 7 may also be applied to microstrip substrates 200 and 202 of Fig. 8. Substrate 200 has one or more signal traces 204 disposed between two dielectric layers 206 and 208. A portion of

-13-

the signal traces 204 are not totally encompassed by dielectric layers 206 and 208. This can be seen by the signal trace portion formed on dielectric layer 206 over the distance 210. A first ground layer 212 is disposed  
5 on dielectric layer 208.

Substrate 202 similarly has one or more signal traces 214 disposed on dielectric layer 216. A ground layer 218 is disposed between dielectric layer 216 and another dielectric layer 220. A portion of the ground  
10 layer 218 is not totally encompassed by dielectric layers 216 and 220, as can be seen by the ground layer portion formed on dielectric layer 220 over the distance 222.

Substrates 200 and 202 can be interconnected  
15 by aligning the substrates in such a way that signal traces 204 are aligned with signal traces 214, and ground layer 212 is aligned with ground layer 218. By moving the substrates 200 and 202 towards each other, as represented by arrow 224, the signal and ground layer of  
20 the two substrates are electrically coupled.

Referring now to Fig. 9, the principles described for the interconnection of Figs. 7 and 8 may also be applied to stripline substrates 230 and 232 of Fig. 9. Substrate 230 has one or more signal traces 234  
25 disposed between two dielectric layers 236 and 238. A portion of the signal traces 234 are not totally encompassed by dielectric layers 236 and 238. This can be seen by the signal trace portion formed on dielectric layer 236 over the distance 240. A first ground layer  
30 242 is disposed on dielectric layer 238, and a second ground layer 244 is disposed between the dielectric

-14-

layer 236 and another dielectric layer 246. A portion of the ground layer 244 is not totally encompassed by dielectric layers 236 and 246, as can be seen by the ground layer portion formed on dielectric layer 246 over the distance 248.

Substrate 232 similarly has one or more signal traces 250 disposed between two dielectric layers 252 and 254. A portion of the signal traces 250 are remain exposed, as can be seen by the portion of the signal traces 250 over the distance 256. A first ground layer 258 is disposed on dielectric layer 254, and a second ground layer 260 is disposed between dielectric layer 252 and another dielectric layer 262. A portion of the ground layer 260 is not totally encompassed by dielectric layers 252 and 262, as can be seen by the ground layer portion formed on dielectric layer 262 over the distance 264.

Substrates 230 and 232 can be interconnected by aligning the substrates in such a way that the ground layer 244 is aligned with ground layer 258, signal traces 234 are aligned with signal traces 250, and ground layer 242 is aligned with ground layer 260. By moving the substrates 230 and 232 towards each other, as represented by arrow 266, the signal and ground layers of the two substrates are electrically coupled.

The embodiments of Figs. 8 and 9 represent embodiments where continuous ground planes are formed without the need for the conductive members between ground planes, which allows continuous ground planes to be formed between the ground planes of interconnecting substrates. The embodiments of Figs. 8 and 9 do,

-15-

however, require the use of an additional dielectric layer on each substrate over those shown in the other figures which use through-holes or solid conductors between substrate layers. The additional layers may  
5 cause the substrate to have a more rigid structure, which may or may not be beneficial in a particular implementation. The circuit interconnection of Fig. 9 provides low inductance, continuous ground planes on both sides of the signal traces on the interconnecting  
10 substrates which may provide some beneficial shielding properties.

It is to be understood that even though numerous characteristics and advantages of various embodiments of the present invention have been set forth  
15 in the foregoing description, together with details of the structure and function of various embodiments of the invention, this disclosure is illustrative only, and changes may be made in detail, especially in matters of structure and arrangement of parts within the principles  
20 of the present invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

-16-

**Claims****What Is Claimed Is:**

1. A circuit interconnection, comprising:
  - 5 (a) first and second substrates, each having a top surface and a bottom surface, wherein the first substrate is positioned above the second substrate;
  - 10 (b) first and second ground layers disposed on the bottom surfaces of the first and second substrates, respectively; and
  - 15 (c) a ground conductor strip disposed on the top surface of the second substrate, wherein the ground conductor strip comprises a plurality of electrically conductive members which pass through the second substrate to electrically couple the ground conductor strip and the second ground layer such that when the first substrate is placed proximate the second substrate, the ground conductor strip electrically couples the first and second ground layers to form a continuous ground plane.
- 20 2. The circuit interconnection of Claim 1 wherein each of the first and second substrates further comprise  
25 signal traces embodied in a dielectric medium.
3. The circuit interconnection of Claim 2 wherein a portion of the signal traces on each of the first and second substrates are exposed, the exposed

-17-

portions being electrically coupled when the first substrate is placed proximate the second substrate.

4. The circuit interconnection of Claim 3 wherein the exposed portions of the signal traces of each of the substrates are volumetrically reduced to maintain a constant signal trade impedance over a total length of the signal traces.
5. The circuit interconnection of Claim 2 wherein the first and second substrates are selected from the group comprising microstrip transmission components, and stripline transmission components.
6. The circuit interconnection of Claim 1 wherein at least the first substrate is flexible.
7. The circuit interconnection of Claim 6 wherein each of the first and second substrates further comprise signal traces embedded in a dielectric medium, wherein a portion of the signal traces on each of the first and second substrates are exposed, the exposed portions being electrically coupled when the first substrate is placed proximate the second substrate.
8. The circuit interconnection of Claim 1 wherein the conductive members are selected from the group comprising solid conductive columns, and conductive through-holes passing through the second substrate from the ground conductor strip to the second ground layer.

-18-

9. A method of forming a continuous ground plane when two circuit boards are placed adjacent one another, each circuit board comprising a substrate having at least one signal conductor embodied in a dielectric layer where a portion of the signal conductor is exposed proximate the substrate edge, each substrate further including a ground layer disposed on the dielectric layer, the method comprising steps of:
- 5
- 10 (a) forming a conductor strip on the dielectric layer of a first substrate substantially parallel to and opposite the ground layer of the first substrate;
- 15 (b) electrically coupling a plurality of conductive members between the conductor strip and the ground layer of the first substrate; and
- 20 (c) aligning the first substrate and a second substrate wherein the exposed portions of the signal conductors in each of the first and second substrates are electrically coupled, and wherein the conductor strip of the first substrate electrically couples the ground layer of the second substrate to form a
- 25 continuous ground plane.
10. The method of Claim 9 wherein the electrically coupling step comprises passing the plurality of conductive members through the dielectric layer of the first substrate.
- 30 11. The method of Claim 9 wherein the electrically coupling step comprises passing at least one of the

-19-

plurality of conductive members external to the dielectric layer of the first substrate.

- 5 12. The method of Claim 9 wherein the forming step comprises photographically generating the conductor strip on the dielectric layer of the first substrate.
- 10 13. The method of Claim 9 further comprising reducing a width of the exposed portions of the signal conductors that are electrically coupled to maintain a constant signal conductor impedance.
14. The method of Claim 9 wherein the coupling step comprises steps of:
- 15 (i) boring a plurality of passages through the dielectric layer of the first substrate between the conductor strip and the ground layer of the first substrate;
  - (ii) inserting the plurality of conductive members in the plurality of passages; and
  - 20 (iii) electrically connecting each of the plurality of conductive members to the conductor strip and the ground layer of the first substrate.
- 25 15. The method of Claim 14 wherein the inserting step of the coupling step comprises an operation selected from the group consisting of forming the plurality of conductive members as conductive through-holes within the plurality of passages and

-20-

forming the conductive members as solid conductors within the plurality of passages.

- 5 16. The method of Claim 9 wherein the aligning step further comprises flexing an edge of the substrate of at least one of the first and second substrates in order to electrically couple the exposed portions of the signal conductors in each of the first and second substrates.
- 10 17. The method of Claim 16 wherein the step of flexing comprises flexing the substrate edge of the second substrate in order to mate the exposed portion of the signal conductor in the second substrate with the exposed portion of the signal conductor in the first substrate.
- 15 18. The method of Claim 9 further comprising a step of applying pressure to at least one of the first and second substrates to reduce a contact resistance between the conductor strip and the ground layer of the second substrate.
- 20 19. A circuit interconnection for electrically coupling the signals of two communications devices, the circuit interconnection comprising:  
25 (a) first and second substrates, each comprising a signal conductor disposed on an inner surface between first and second dielectric layers, the first dielectric layer covering only a portion of the signal conductor and the second dielectric layer such that the signal conductor has an exposed portion, the signal  
30 conductor in the exposed portion having a

-21-

- proximal end adjacent the first dielectric layer and a distal end;
- 5 (b) a first ground layer disposed on an outer surface of the first dielectric layer of the first substrate;
- (c) a second ground layer disposed on an outer surface of the second dielectric layer of the second substrate;
- 10 (d) a ground conductor strip disposed on the inner surface of the second dielectric layer of the second substrate which extends beyond the distal end of the signal conductor of the second substrate; and
- 15 (e) a plurality of electrically conductive members which pass through the second dielectric layer of the second substrate to electrically couple the ground conductor strip and the second ground layer such that when the first substrate is placed proximate to the second
- 20 substrate, the exposed portion of the signal conductor of each substrate are electrically coupled and the ground conductor strip electrically couples the first and second ground layers to form a continuous ground
- 25 plane.
20. The circuit interconnection of Claim 19 further comprising:
- 30 (a) a third ground layer disposed on an outer surface of the second dielectric layer of the first substrate;
- (b) a fourth ground layer disposed on an outer surface of the first dielectric layer of the second substrate;

-22-

- 5 (c) a second ground conductor strip disposed on the inner surface of the second dielectric layer of the first substrate which extends beyond the distal end of the signal conductor of the first substrate; and
- 10 (d) a second plurality of electrically conductive members which pass through the second dielectric layer of the first substrate to electrically couple the second ground conductor strip and the third ground layer such that when the first substrate is placed proximate to the second substrate, the second ground conductor strip electrically couples the third and fourth ground layers to form a
- 15 second continuous ground plane.
21. A circuit interconnection including at least a first and a second substrate, each substrate comprising:
- 20 (a) a first ground layer having an exposed bottom side, and having a top side positioned proximate a first dielectric layer; and
- 25 (b) at least one signal trace positioned between the first dielectric layer and a second dielectric layer, the at least one signal trace and the second dielectric layer extending beyond an end of the first ground layer and the first dielectric layer, the first and the second substrates being formed
- 30 such that, when one substrate is rotated 180 degrees with respect to the other substrate into a mating position, the first ground layers and the at least one signal trace of the first and the second substrates are each

-23-

electrically coupled to one another to form a mated circuit interconnection.

22. The circuit interconnection of Claim 21 wherein each substrate further comprises a second ground layer positioned between the second dielectric layer and a third dielectric layer, the second ground layer and the third dielectric layer extending beyond an end of the at least one signal trace and the second dielectric layer, the first and the second substrates being formed such that, when one substrate is rotated 180 degrees with respect to the other substrate into a mating position, the second ground layers of the first and the second substrates are each electrically coupled to one another to form a mated circuit interconnection.
23. The circuit interconnection of Claim 21 wherein the first ground layers and that at least one signal trace are electrically coupled to one another by flexing the first substrate to contact the second substrate.
24. The circuit interconnection of Claim 22 wherein the electrical coupling of the first ground layers forms a first continuous ground plane, and the electrical coupling of the second ground layers forms a second continuous ground layer.

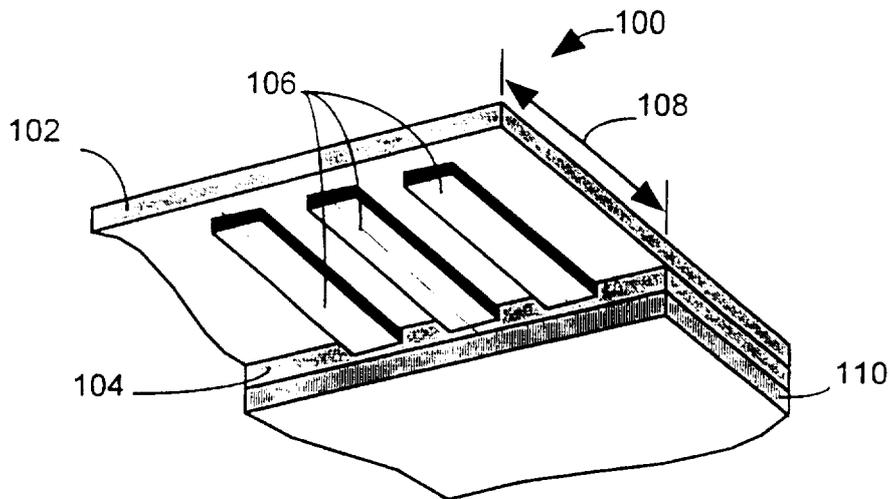


FIG. 1

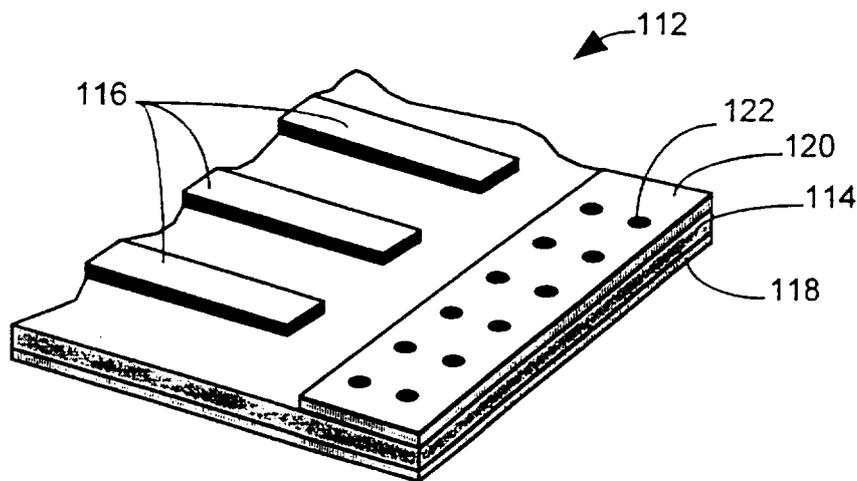


FIG. 2

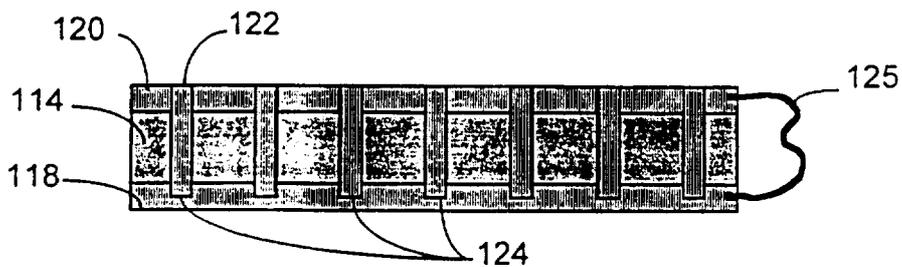


FIG. 3

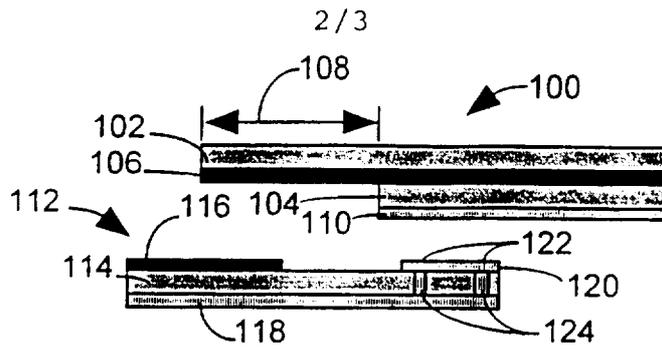


FIG. 4

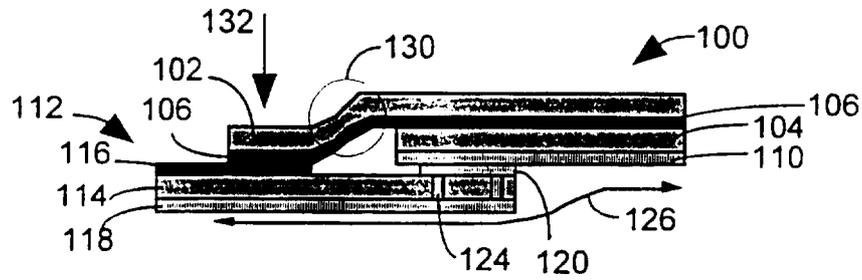


FIG. 5

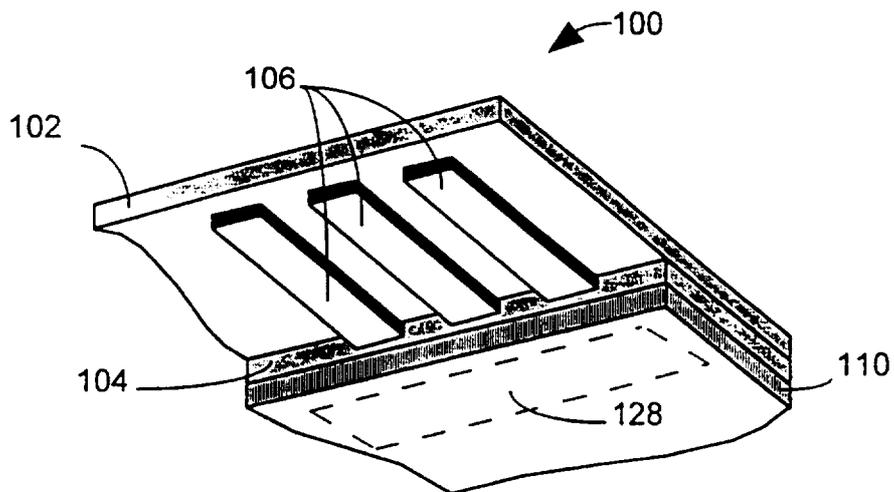


FIG. 6

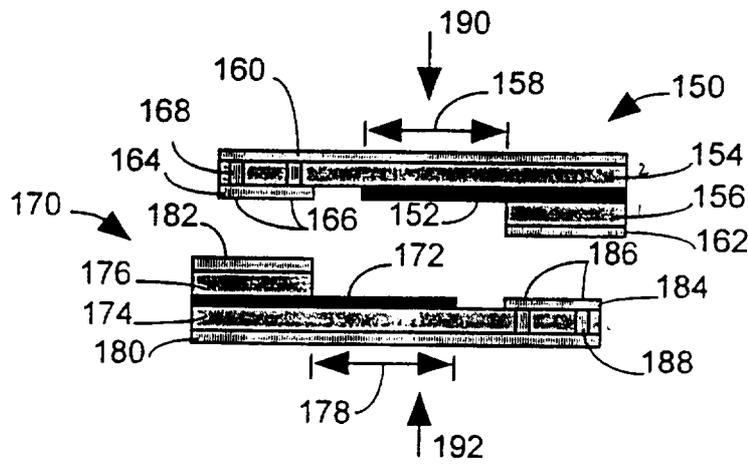


FIG. 7

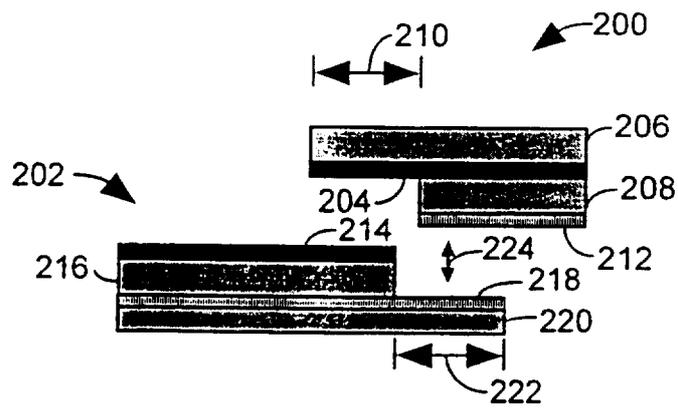


FIG. 8

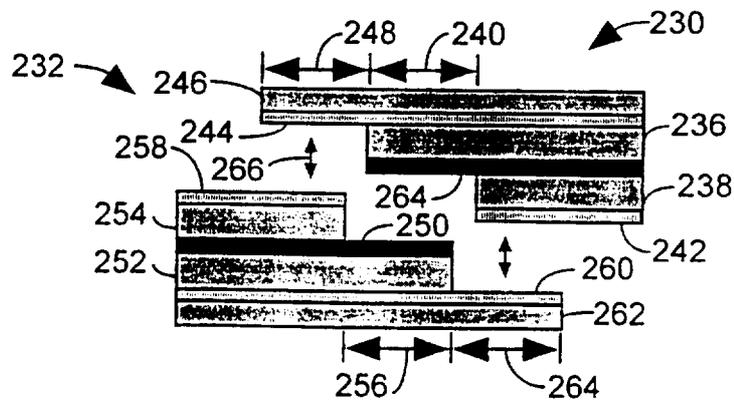


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US97/11925

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) : H01P 3/08, 5/02  
US CL : 333/246, 260

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 333/238, 246, 260

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

search terms: substrate (w) connect?, and strip or stripline or microstrip, and ground, and through hole# or via or interconnect.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,980,659 A (ALLARD) 25 December 1990 (25-12-90), see entire document, especially Fig. 2A and col. 3, lns. 30-65.	21
Y	US 5,261,826 A (LEEB ET AL) 16 November 1993 (16-11-93), entire document, especially Figs. 1, 2 and 3, col. 2, lns. 25-61, and col. 3, lns. 28-29.	1-18
Y	US 4,513,266 A (ISHIHARA) 23 April 1985 (23-04-85), see especially Fig. 4 and col. 2, lns. 36-46.	1-18
Y	US 4,543,544 A (ZIEGNER) 24 September 1985 (24-09-85), see especially Fig. 1 and the abstract lns. 6-9.	4 and 13

Further documents are listed in the continuation of Box C.  See patent family annex.

* Special categories of cited documents:	*T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*A* document defining the general state of the art which is not considered to be of particular relevance	*X*	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*E* earlier document published on or after the international filing date	*Y*	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Z*	document member of the same patent family
*O* document referring to an oral disclosure, use, exhibition or other means		
*P* document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 15 AUGUST 1997	Date of mailing of the international search report 29 AUG 1997
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Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer BARBARA SUMMONS Telephone No. (703) 308-4947
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## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US97/11925

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 3,218,584 A (AYER) 16 November 1965 (16-11-65), see especially Fig. 3.	
A	US 5,469,130 A (OKADA ET AL) 21 November 1995 (21-11-95), see especially Figs. 2a, 2b, and 7.	