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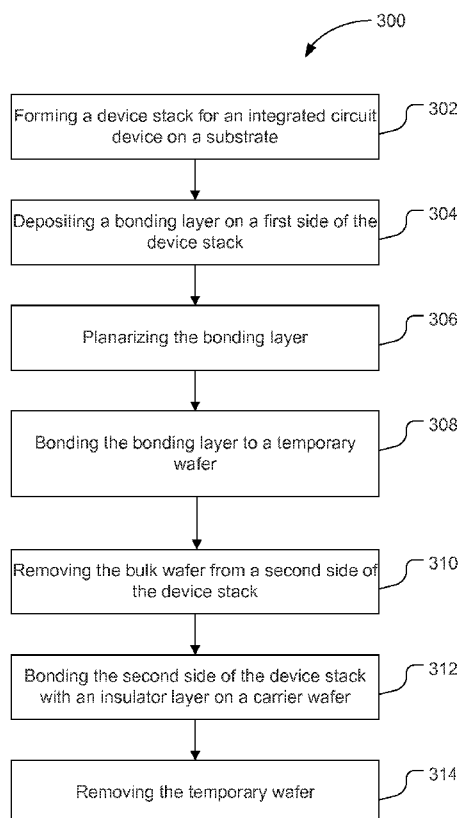
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(54) **Title:** TECHNIQUES FOR SOI DEVICE FORMATION ON A VIRTUAL SUBSTRATE, AND ASSOCIATED CONFIGURATIONS



(57) **Abstract:** Embodiments of the present disclosure describe techniques for silicon-on-insulator (SOI) device formation in an integrated circuit (IC) device, and associated configurations. A method of fabricating an SOI structure may include forming a device stack for an IC device on a bulk wafer, removing the bulk wafer from a first side of the device stack, and bonding the first side of the device stack with an insulator layer on a carrier wafer. Other embodiments may be described and/or claimed.

FIG. 3



PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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TECHNIQUES FOR SOI DEVICE FORMATION ON A VIRTUAL SUBSTRATE, AND ASSOCIATED CONFIGURATIONS

Field

5 Embodiments of the present disclosure generally relate to the field of integrated circuits, and more particularly, to techniques for silicon-on-insulator (SOI) device formation in an integrated circuit device and associated configurations.

Background

10 For some applications, a SOI structure provides advantages over traditional devices made from bulk silicon such as reduced under-device leakage. Current SOI structures are typically made from a SOI wafer. In advanced semiconductor fabrication facilities, processing conditions are very sensitive to incoming materials. To process SOI wafers, dedicated SOI flow processes must
15 be developed and used which are different than bulk wafer flows. Since not all applications necessitate a SOI structure, this may result in a duplicated process development for SOI structure and bulk structure, adding development time and cost.

Brief Description of the Drawings

20 Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

25 **FIG. 1** schematically illustrates a top view of an example die in wafer form and in singulated form, in accordance with some embodiments.

FIG. 2 schematically illustrates a cross-section side view of an integrated circuit (IC) assembly, in accordance with some embodiments.

FIG. 3 is a flow diagram that illustrates a process for fabricating a
30 silicon-on-insulator (SOI) structure of an IC device, in accordance with some embodiments.

FIGS. 4A-4F schematically illustrate a cross-section side view of an IC device during various stages of fabricating the SOI structure of FIG. 3, in accordance with some embodiments.

FIG. 5 is a flow diagram that illustrates a process for fabricating a SOI structure of an IC device with a template substrate that includes a thin film epitaxial material layer, in accordance with some embodiments.

FIGS. 6A-6F schematically illustrate a cross-section side view of an IC device during various stages of fabricating the SOI structure of FIG. 5, in accordance with some embodiments.

FIG. 7 schematically illustrates an example system that may include an IC device as described herein, in accordance with some embodiments.

Detailed Description

Embodiments of the present disclosure describe techniques for SOI device formation on a virtual substrate and associated configurations. A method of fabricating an SOI structure may include forming a device stack for an IC device on a bulk wafer, removing the bulk wafer from a first side of the device stack, and bonding the first side of the device stack with an insulator layer on a carrier wafer.

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments in which the subject matter of the present disclosure may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments is defined by the appended claims and their equivalents.

For the purposes of the present disclosure, the phrase “A and/or B” means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

The description may use perspective-based descriptions such as top/bottom, side, over/under, and the like. Such descriptions are merely used to facilitate the discussion and are not intended to restrict the application of embodiments described herein to any particular orientation.

The description may use the phrases “in an embodiment,” or “in embodiments,” which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the

like, as used with respect to embodiments of the present disclosure, are synonymous.

The term “coupled with,” along with its derivatives, may be used herein. “Coupled” may mean one or more of the following. “Coupled” may mean
5 that two or more elements are in direct physical or electrical contact. However, “coupled” may also mean that two or more elements indirectly contact each other, but yet still cooperate or interact with each other, and may mean that one or more other elements are coupled or connected between the elements that are said to be coupled with each other. The term “directly coupled” may mean that two or
10 more elements are in direct contact.

In various embodiments, the phrase “a first feature formed, deposited, or otherwise disposed on a second feature” may mean that the first feature is formed, deposited, or disposed over the second feature, and at least a part of the first feature may be in direct contact (e.g., direct physical and/or
15 electrical contact) or indirect contact (e.g., having one or more other features between the first feature and the second feature) with at least a part of the second feature.

As used herein, the term “module” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor
20 (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

FIG. 1 schematically illustrates a top view of an example die 102 in wafer form 10 and in singulated form 100, in accordance with some embodiments.
25 In some embodiments, the die 102 may be one of a plurality of dies (e.g., dies 102, 103a, 103b) of a wafer 11 composed of semiconductor material such as, for example, silicon or other suitable material. The plurality of dies may be formed on a surface of the wafer 11. Each of the dies may be a repeating unit of a semiconductor product that includes one or more IC devices that may include
30 circuit structure 400 described with respect to FIGS. 4A-4F and/or circuit structure 600 described with respect to FIGS. 6A-6F.

For example, the die 102 may include circuitry having transistor structures 104 such as, for example, one or more channel bodies (e.g., fin structures, nanowires, planar bodies, etc.) that provide a channel pathway for

mobile charge carriers of one or more transistor devices or source/drain regions. Electrical interconnect structures such as, for example, transistor electrode assemblies (e.g., terminal contacts) may be formed on and coupled with the one or more transistor structures 104 to route electrical energy to or from the transistor structures 104. For example, terminal contacts may be electrically coupled with a channel body to provide a gate electrode for delivery of a threshold voltage and/or a source/drain current to provide mobile charge carriers for operation of a transistor device. Although the transistor structures 104 are depicted in rows that traverse a substantial portion of the die 102 in FIG. 1 for the sake of simplicity, it is to be understood that the transistor structures 104 may be configured in any of a wide variety of other suitable arrangements on the die 102 in other embodiments, including, for example, vertical and horizontal features having much smaller dimensions than depicted.

After a fabrication process of the semiconductor product embodied in the dies is complete, the wafer 11 may undergo a singulation process in which each of the dies (e.g., die 102) is separated from one another to provide discrete “chips” of the semiconductor product. The wafer 11 may be any of a variety of sizes. In some embodiments, the wafer 11 may have a diameter ranging from about 25.4 mm to about 450 mm. The wafer 11 may include other sizes and/or other shapes in other embodiments. According to various embodiments, the transistor structures 104 may be disposed on a semiconductor substrate in wafer form 10 or singulated form 100. The transistor structures 104 described herein may be incorporated in a die 102 for logic or memory, or combinations thereof. In some embodiments, the transistor structures 104 may be part of a system-on-chip (SoC) assembly.

FIG. 2 schematically illustrates an example cross-section side view of an IC package assembly 200, in accordance with some embodiments. The IC package assembly 200 represents one example configuration of a die 202, according to various embodiments. The die 202 may correspond to the die 102 of FIG. 1.

In various embodiments, the die 202 may include a first side S1 and a second side S2 opposite the first side S1. In some embodiments, the second side S2 may be referred to as a “front side” of the die 202, and the first side S1 may be referred to as a “backside” of the die 202, although in other embodiments

the second side S2 may be the backside and the first side S1 may be the front side. The backside of the die 202 may be the side of the die 202 on which an insulator layer on a semiconductor carrier substrate is disposed during fabrication of the die 202.

5 In some embodiments, the die 202 may generally include one or more device layers (hereinafter “device layer 204b”), one or more interconnect layers (hereinafter “interconnect layer 204a”) disposed on the second side S2 of the die 202, and a carrier substrate layer 204c disposed on the first side S1 of the die 202. An insulator layer 204d may be disposed between the carrier substrate
10 layer 204c and the device layer 204b. The device layer 204b may represent a region where active devices such as transistor devices are formed on the semiconductor substrate. The device layer 204b may include, for example, transistor structures such as channel bodies and/or source/drain regions of transistor devices. The interconnect layer 204a may include interconnect
15 structures (e.g., electrode terminals) that are configured to route electrical signals to or from the active devices in the device layer 204b. For example, the interconnect layer 204a may include horizontal lines (e.g., trenches) and/or vertical plugs (e.g., vias) or other suitable features to provide electrical routing and/or contacts. The interconnect layer 204a may additionally or alternatively
20 include one or more through vias (sometimes referred to as through-silicon vias (TSVs) in devices that include a silicon substrate) that extend from the second side S2 to the first side S1 of the die 202 to route signals between another die (not shown) that may be present in some configurations such as a stacked die configuration, and the package substrate 210.

25 The die 202 may represent a discrete product made from a semiconductor material (e.g., silicon) using semiconductor fabrication techniques such as thin film deposition, lithography, etching and the like used in connection with forming complementary metal-oxide-semiconductor (CMOS) devices. In some embodiments, the die 202 may be, include, or be a part of a processor,
30 memory, system-on-chip (SoC) or application-specific IC (ASIC). In some embodiments, an electrically insulative material such as, for example, molding compound or underfill material (not shown) may encapsulate at least a portion of the die 202 and/or a plurality of die-level interconnect structures 206.

In some embodiments, the die 202 may include a processor or memory. The die 202 may be configured to perform other functions in other embodiments. For example, in some embodiments, the die 202 may be configured to function as memory, an application specific integrated circuit (ASIC),
5 processor, or combinations thereof.

In the depicted configuration, the die 202 is coupled with the package substrate 210 in a flip-chip configuration. The IC package assembly 200 is not limited to the configuration depicted in FIG. 2 and may include a wide variety of other suitable configurations in other embodiments. For example, in
10 some embodiments additional dies may be stacked on the die 202 and/or the die 202 may be coupled with a component other than the package substrate 210. The IC package assembly 200 may include, for example, combinations of flip-chip and wire-bonding techniques, interposers, multi-chip package configurations including SoC and/or package-on-package (PoP) configurations to route electrical signals in
15 some embodiments.

In some embodiments, the IC package assembly 200 may include package interconnects 212 configured to route electrical signals between the die 202 and other electrical components external to the IC package assembly 200 including, for example, a circuit board such as a motherboard (e.g., motherboard
20 702 of FIG. 7). According to various embodiments, the package substrate 210 may be composed of a polymer, ceramic, glass, or semiconductor material having electrical routing features formed therein to electrically couple the die-level interconnects 206 and the package interconnects 212. The electrical routing features may include, for example, pads or traces (not shown) disposed on one or
25 more surfaces of the package substrate 210 and/or internal routing features (not shown) such as, for example, trenches, vias or other interconnect structures to route electrical signals through the package substrate 210. For example, in some embodiments, the package substrate 210 may include electrical routing features such as pads (not shown) configured to receive the respective die-level
30 interconnects 206 of the die 202.

The interconnects 206, 212 may include any of a wide variety of suitable structures and/or materials including, for example, bumps, pillars or balls formed using metals, alloys, solderable material, or combinations thereof. The interconnects 206, 212 may include other suitable structures and/or materials in

other embodiments. The interconnects 206 may be electrically coupled with the interconnect layer 204a to route electrical signals between the die 202 and other electrical devices (e.g., via the package substrate 210). The electrical signals may include, for example, input/output (I/O) signals and/or power/ground signals that
5 are used in connection with operation of the die 202.

FIG. 3 is an illustrative flow diagram of a process 300 for fabricating a SOI structure of an IC device, in accordance with various embodiments. In some embodiments, some or all of the process 300 may be performed on a semiconductor wafer that includes a plurality of IC devices disposed thereon.

10 **FIGS. 4A, 4B, 4C, 4D, 4E, and 4F** schematically illustrate a cross-sectional side view of a circuit structure 400 at various stages of the process 300, in accordance with various embodiments. Accordingly, the process 300 will be described below with reference to FIGS. 4A-4F. The circuit structure 400 may correspond to an IC device on a die such as the die 202, with other circuit
15 structures, IC devices and/or dies that may be also be formed on a wafer along with the circuit structure 400 not shown for clarity.

Referring to FIG. 4A, the circuit structure 400 may include a device stack 402 that is formed on a substrate 404. The device stack 402 may include a first side coupled with the substrate 404. The substrate 404 may be a
20 semiconductor substrate that may be a wafer in various embodiments. The substrate 404 may be a bulk semiconductor material such as, for example, silicon in some embodiments. Alternatively, or additionally, the substrate 404 may be composed of other materials. The device stack 402 may include a device layer 406 that corresponds to a region where active devices such as transistor
25 structures 408 are formed on the substrate 404. The device layer 406 may include, for example, transistor structures such as channel bodies and/or gate/source/drain regions of transistor devices. Alternatively, or additionally, the device layer 406 may include other components in various embodiments. At a block 302, the process 300 may include forming a device stack such as the device
30 stack 402, for an IC device that may include a circuit structure having a plurality of transistors, on a bulk substrate such as the bulk substrate 404. Forming the device stack may include forming the device layer, forming routing layers, forming dielectric layers, forming vias, forming metal layers, and/or forming any other suitable layers.

At a block 304, the process 300 may include depositing a bonding layer on a second side of the device stack opposite the first side of the device stack. This is illustrated in FIG. 4B, where a bonding layer 410 is shown deposited on a second side of the device stack 402. In various embodiments, the bonding layer 410 may be formed of silicon oxide or a polymer material. The bonding layer 410 may be formed of other materials in some embodiments. At a block 306, the bonding layer may be planarized such that it will be smooth enough to bond to another temporary layer. The entire stack, including the device stack 402, the bonding layer 410, and the substrate 404 may then be flipped. At a block 308, the process 300 may include bonding the bonding layer to a temporary wafer.

FIG. 4C illustrates the circuit structure 400 after the bonding layer 410 has been bonded with a temporary carrier wafer 412. In various embodiments, the bonding layer 410 may be bonded with the temporary carrier wafer 412 by oxide fusion bonding, metallic bonding, adhesive bonding, or another bonding method. The temporary carrier wafer 412 may be any suitable material, such as silicon, glass, and/or another material. At a block 310, the process 300 may include removing the bulk wafer from the first side (e.g., backside) of the device stack. FIG. 4D illustrates the circuit structure 400 after the substrate 404 has been at least partially removed. In various embodiments, the substrate 404 may be completely removed to expose the first side of the device stack. Removing the substrate 404 may include thinning the substrate 404 by a mix of micromachining processes such as dry etch, wet etch, wafer grinding, and chemical-mechanical planarization (CMP) in various embodiments. In some embodiments, the thinning process may proceed all the way down to a shallow trench isolation (STI) level of the device stack 402 to isolate individual devices and/or may proceed to sufficiently thin the substrate 404 such that the device channel is sufficiently thinned to fully deplete the channel of charge carriers. In various embodiments, the thinning may include planarization of the thinned surface to prepare for bonding to an insulator layer on a carrier wafer. In various embodiments, the circuit structure 400 may be flipped before bonding to the insulator layer on the carrier wafer.

At a block 312, the process 300 may include bonding the first side of the device stack with an insulator layer on a carrier wafer. Oxide fusion bonding and/or another suitable bonding method may be used to bond the first side of the

device stack with the insulator layer in various embodiments. In some
embodiments, a bonding layer may be deposited on the first side of the device
stack before bonding to the insulator layer on the carrier wafer. In various
embodiments, the carrier wafer may itself be an insulator such that a separate
5 insulator layer on the carrier wafer may not be present.

FIG. 4E illustrates the circuit structure 400 after the first side of the
device stack 402 has been bonded with an insulator layer 414 on a carrier wafer
416. In various embodiments, the transistor structures 408 may be fully depleted
devices that are sitting on the insulator layer 414. In various embodiments, the
10 insulator layer 414 may be silicon dioxide. In some embodiments, the insulator
layer 414 may be formed of another material such as sapphire. In various
embodiments, the carrier wafer 416 may be formed of a material such as silicon,
quartz, glass, or sapphire. In some embodiments, the carrier wafer 416 may be
formed of another material such as a ceramic that may be porous, or a relatively
15 low temperature material that cannot withstand typical device fabrication
temperatures such as a plastic polymer material, metal, or glass. The insulator
layer 414 may be structured as a buried oxide (BOX) layer in various
embodiments.

At a block 314, the process 300 may include removing the
20 temporary wafer. FIG. 4F illustrates the circuit structure 400 after the temporary
carrier wafer 412 has been removed. In some embodiments, the temporary carrier
wafer 412 may be removed by a mix of micromachining processes such as dry
etch, wet etch, wafer grinding, and CMP. The temporary carrier wafer 412 may be
removed by another method, such as peeling, in other embodiments. After
25 removal of the temporary carrier wafer 412, the circuit structure 400 may be a
SOI-like structure. In various embodiments, the device layer 406 may correspond
to the device layer 204b, the carrier wafer 416 may correspond to the carrier
substrate layer 204c, and/or the insulator layer 414 may correspond to the
insulator layer 214d of FIG. 2.

30 **FIG. 5** is an illustrative flow diagram of a process 500 for fabricating
a SOI structure of an IC device with a template substrate that includes a thin film
epitaxial material layer, in accordance with various embodiments. In some
embodiments, some or all of the process 500 may be performed on a
semiconductor wafer that includes a plurality of IC devices disposed thereon.

FIGS. 6A, 6B, 6C, 6D, 6E, and 6F schematically illustrate a cross-sectional side view of a circuit structure 600 at various stages of the process 500, in accordance with various embodiments. Accordingly, the process 500 will be described below with reference to FIGS. 6A-6F. The circuit structure 600 may correspond to an IC device on a die such as the die 202, with other circuit structures, IC devices and/or dies that may be also be formed on a wafer along with the circuit structure 600 not shown for clarity.

Referring to FIG. 6A, the circuit structure 600 may include a device stack 602 that is completed on a template substrate 604 having an epitaxial thin film material layer 605. The device stack 602 may include a first side coupled with the epitaxial thin film material layer 605. In various embodiments, the epitaxial thin film material layer 605 may be any suitable material, such as a group III-V semiconductor, a group III-nitride semiconductor, germanium (Ge), or silicon carbide (SiC). The epitaxial thin film material layer 605 may have a thickness of a few hundreds of nanometers (e.g., about 200 nanometers to about 600 nanometers) in various embodiments. The epitaxial thin film material layer 605 may be thicker or thinner in some embodiments. The epitaxial thin film material layer 605 may include a buffer and/or transition layer associated with an epitaxial process in some embodiments. The template substrate 604 may be a semiconductor substrate that may be a wafer in various embodiments. The template substrate 604 may be a bulk semiconductor material such as, for example, silicon in some embodiments. The template substrate 604 may be composed of other materials in various embodiments.

The device stack 602 may include a device layer 606 that corresponds to a region where active devices such as transistor structures 608 are formed at least in part by the epitaxial thin film material layer 605. The device layer 606 may correspond to a region where active devices such as transistor devices are formed on the epitaxial thin film material layer 605. The device layer 606 may include, for example, transistor structures such as channel bodies and/or gate/source/drain regions of transistor devices. Alternatively, or additionally, the device layer 606 may include other components in various embodiments. At a block 502, the process 500 may include forming a device stack such as the device stack 502, for an IC device that may include a circuit structure having a plurality of transistors, on a wafer having a template substrate layer and an epitaxial thin film

material layer such as the template substrate 604 and the epitaxial thin film material layer 605. Forming the device stack may include forming the device layer, forming routing layers, forming dielectric layers, forming vias, forming metal layers, and/or forming any other suitable layers.

5 At a block 504, the process 500 may include depositing a bonding layer on a second side of the device stack opposite the first side of the device stack. This is illustrated in FIG. 6B, where a bonding layer 610 is shown deposited on a second side of the device stack 602. In various embodiments, the bonding layer 610 may be formed of silicon oxide or a polymer material. The bonding layer
10 610 may be formed of other materials in some embodiments. At a block 506, the bonding layer may be planarized such that it will be smooth enough to bond to another temporary layer (e.g., a temporary carrier wafer, as further described below). The entire stack, including the device stack 602, the bonding layer 610, the template substrate 604, and the epitaxial thin film material layer 605 may then
15 be flipped.

 At a block 508, the process 500 may include bonding the bonding layer to a temporary wafer. FIG. 6C illustrates the circuit structure 600 after the bonding layer 610 has been bonded with a temporary carrier wafer 612. In various embodiments, the bonding layer 610 may be bonded with the temporary carrier
20 wafer 612 by oxide fusion bonding, metallic bonding, adhesive bonding, or another bonding method. The temporary carrier wafer 612 may be silicon or glass in various embodiments. The temporary carrier wafer 612 may be formed of another material in some embodiments.

 At a block 510, the process 500 may include removing the template
25 substrate layer and at least a portion of the epitaxial thin film material layer to reveal a first surface of the epitaxial thin film material layer or device stack. FIG. 6D illustrates the circuit structure 600 after the template substrate 604 and at least a portion of the epitaxial thin film material layer 605 have been removed to reveal a first surface 613 of the device stack 602. In some embodiments, a portion of the
30 epitaxial thin film material layer 605 may remain (not shown) such that the first surface 613 may be a surface of the epitaxial thin film material layer 605. In some embodiments, the transistor structures 608 are formed at least in part from the epitaxial thin film material layer 605, and the transistor structures 608 remain after the epitaxial thin film material layer 605 has been partially or completely removed.

In various embodiments, the epitaxial thin film material layer 605 may be completely removed.

Removing the template substrate 604 and at least a portion of the epitaxial thin film material layer 605 may include thinning the template substrate 604 and the epitaxial thin film material layer 605 by a mix of micromachining processes such as dry etch, wet etch, wafer grinding, and chemical-mechanical planarization (CMP) in various embodiments. In some embodiments, the thinning process may proceed all the way down to a shallow trench isolation (STI) level to isolate individual devices and/or may proceed to sufficiently thin the epitaxial thin film material layer 605 such that the device channel is fully depleted. In various embodiments, a final step of the thinning may be planarization of the thinned surface to prepare for bonding to an insulator layer on a carrier wafer. In various embodiments, the circuit structure 600 may be flipped before bonding to the insulator layer on the carrier wafer.

At a block 512, the process 500 may include bonding the first surface with an insulator layer on a carrier wafer. Oxide fusion bonding may be used to bond the first surface with the insulator layer in various embodiments. In some embodiments a different bonding method may be used. In some embodiments, a bonding layer may be deposited on the first surface before bonding to the insulator layer on the carrier wafer. In various embodiments, the carrier wafer may itself be an insulator such that a separate insulator layer on the carrier wafer may not be present. FIG. 6E illustrates the circuit structure 600 after the first surface 613 has been bonded with an insulator layer 614 on a carrier wafer 616. In various embodiments, the transistor structures 608 may be fully depleted devices that are sitting on the insulator layer 614. In various embodiments, the insulator layer 614 may be silicon dioxide. In some embodiments, the insulator layer 614 may be formed of another material such as sapphire. In various embodiments, the carrier wafer 616 may be formed of a material such as silicon, quartz, glass, or sapphire. In some embodiments, the carrier wafer 616 may be formed of another material such as a ceramic that may be porous, or a relatively low temperature material that cannot withstand typical device fabrication temperatures such as a plastic polymer material, metal, or glass. The insulator layer 614 may be structured as a BOX layer in various embodiments.

At a block 514, the process 500 may include removing the temporary wafer from the circuit structure. FIG. 6F illustrates the circuit structure 600 after the temporary carrier wafer 612 has been removed. In some embodiments, the temporary carrier wafer 612 may be removed by a mix of micromachining processes such as dry etch, wet etch, wafer grinding, and CMP. The temporary carrier wafer 612 may be removed by another method, such as peeling, in other embodiments. After removal of the temporary carrier wafer 612, the circuit structure 600 may be a SOI-like structure. In various embodiments, the circuit structure 600 may include materials such as group III-V semiconductors or group III-nitride semiconductors that are not commercially available for use in a standard SOI device fabrication process or are difficult to prepare for use in a standard SOI device fabrication process. In various embodiments, the device layer 606 may correspond to the device layer 204b, the carrier wafer 616 may correspond to the carrier substrate layer 204c, and/or the insulator layer 614 may correspond to the insulator layer 214d of FIG. 2.

In various embodiments, an IC device that may include a die such as the die 202 and/or the circuit structure 400 or the circuit structure 600 may include one or more fins, one or more transistor structures, and/or an isolation oxide. The IC device may be a radio frequency (RF) or an analog device on a high resistivity carrier, a high performance device on a flexible carrier, or another type of device in various embodiments. The isolation oxide may be any suitable oxide, such as silicon oxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_xN_y), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium aluminum oxide (HfAl_xO_y), hafnium silicon oxide (HfSi_xO_y), zirconium oxide (ZrO_2), zirconium silicon oxide (ZrSi_xO_y), lanthanum oxide (La_2O_3), yttrium oxide (Y_2O_3), lanthanum aluminum oxide (LaAl_xO_y), tantalum oxide (Ta_2O_5), titanium oxide (TiO_2), barium strontium titanium oxide ($\text{BaSrTi}_x\text{O}_y$), barium titanium oxide (BaTi_xO_y), strontium titanium oxide (SrTi_xO_y), lead scandium tantalum oxide ($\text{PbSc}_x\text{Ta}_y\text{O}_z$), or lead zinc niobate ($\text{PbZn}_x\text{Nb}_y\text{O}_z$), carbon doped oxide (CDO), or combinations thereof, where x, y, and z represent suitable quantities of the respective elements.

The transistor structures may include a plurality of transistor layers that form one or more transistors with the fins. For example, the fins may form a channel region of the transistors, and the transistor structures may form another portion of the channel region and/or gate/source/drain regions of the transistors. It

will be appreciated that the transistor structures may include any suitable material layers to form the transistors with the fins. For example, the transistor structures may include one or more semiconductor layers, oxide layers, dielectric layers, insulator layers, and/or metal layers. In some embodiments, the isolation oxide
5 may substantially surround the transistor structures. One or more vias may be disposed in the isolation oxide to electrically connect one or more of the transistor structures to other components. In some embodiments, one or more interconnect layers may be formed on the IC device.

Various operations are described as multiple discrete operations in
10 turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. Embodiments of the present disclosure may be implemented into a system using any suitable hardware and/or software to configure as desired.

15 **FIG. 7** schematically illustrates an example system (e.g., computing device 700) that may include an IC device (e.g., an IC device including the die 202, the circuit structure 400 and/or the circuit structure 600) as described herein, in accordance with some embodiments. Components of the computing device 700 may be housed in an enclosure (e.g., housing 708). A motherboard 702 may
20 include a number of components, including but not limited to a processor 704 and at least one communication chip 706. The processor 704 may be physically and electrically coupled to the motherboard 702. In some implementations, the at least one communication chip 706 may also be physically and electrically coupled to the motherboard 702. In further implementations, the communication chip 606
25 may be part of the processor 704.

Depending on its applications, computing device 700 may include other components that may or may not be physically and electrically coupled to the motherboard 702. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a
30 graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, a Geiger counter, an accelerometer, a gyroscope, a speaker,

a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 706 may enable wireless communications for the transfer of data to and from the computing device 700. The term “wireless”
5 and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 706 may
10 implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile
15 broadband (UMB) project (also referred to as “3GPP2”), etc.). IEEE 802.16 compatible broadband wireless access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip
20 606 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 606 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM
25 EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 706 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), derivatives thereof, as well as any
30 other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 706 may operate in accordance with other wireless protocols in other embodiments.

The computing device 700 may include a plurality of communication chips 706. For instance, a first communication chip 706 may be dedicated to

shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 706 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, and others.

5 The processor 704 of the computing device 700 may include a die (e.g., die 102 of FIG. 1 or the die 202 of FIG. 2) having an IC device (e.g., an IC device that includes the circuit structure 400 or the circuit structure 600) as described herein. For example, the die 202 of FIG. 2 may be mounted in a package assembly (e.g., package assembly 200) that is mounted on a circuit
10 board such as the motherboard 702. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

 The communication chip 706 may also include a die (e.g., die 102 of
15 FIG. 1 or the die 202 of FIG. 2) having an IC device (e.g., an IC device including the circuit structure 400 or the circuit structure 600) as described herein. In further implementations, another component (e.g., memory device or other integrated circuit device) housed within the computing device 700 may contain a die (e.g., die 102 of FIG. 1 or the die 202 of FIG. 2) having an IC device (e.g., an IC device
20 including the die 202, the circuit structure 400 and/or the circuit structure 600) as described herein.

 In various implementations, the computing device 700 may be a mobile computing device, a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a
25 mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 700 may be any other electronic device that processes data.

 Some non-limiting Examples are provided below.

30 Example 1 may include a method of fabricating a silicon-on-insulator (SOI) structure comprising: forming a device stack for an integrated circuit device on a bulk wafer; removing the bulk wafer from a first side of the device stack; and bonding the first side of the device stack with an insulator layer on a carrier wafer.

Example 2 may include the subject matter of Example 1, wherein the insulator layer is formed of silicon dioxide or sapphire.

Example 3 may include the subject matter of Example 1, further comprising bonding the device stack with a temporary wafer before removing the
5 bulk wafer.

Example 4 may include the subject matter of Example 3, wherein bonding the device stack with the temporary wafer includes depositing a bonding layer on a second side of the device stack, planarizing the bonding layer, and bonding the bonding layer to the temporary wafer.

10 Example 5 may include the subject matter of Example 3, further comprising removing the temporary wafer after bonding the first side of the device stack with the insulator layer.

Example 6 may include the subject matter of any one of Examples 1-5, wherein removing the bulk wafer includes thinning the bulk wafer to a shallow
15 trench isolation of the device stack.

Example 7 may include the subject matter of any one of Examples 1-5, wherein removing the bulk wafer includes performing a micromachining process.

Example 8 may include the subject matter of any one of Examples
20 1-5, wherein the bulk wafer is a silicon wafer.

Example 9 may include the subject matter of any one of Examples 1-5, wherein the carrier wafer is formed of silicon.

Example 10 may include the subject matter of any one of Examples 1-5, wherein the carrier wafer is formed of glass.

25 Example 11 may include the subject matter of any one of Examples 1-5, wherein the carrier wafer is formed of ceramic, metal, or a polymer material.

Example 12 may include a method of fabricating a silicon-on-insulator (SOI) structure comprising: forming a device stack for an integrated circuit device on a wafer, the wafer having a template substrate layer and an
30 epitaxial thin film material layer, and the device stack having a first side coupled to the epitaxial thin film material layer; removing the template substrate layer and at least a portion of the epitaxial thin film material layer to reveal a first surface of the epitaxial thin film material layer or device stack; and bonding the first surface with an insulator layer that is disposed on a carrier wafer.

Example 13 may include the subject matter of Example 12, wherein the epitaxial thin film material layer is formed of Germanium (Ge), Silicon Carbide (SiC), a group III-V semiconductor, or a III-nitride compound semiconductor.

5 Example 14 may include the subject matter of Example 12, further comprising bonding the device stack with a temporary wafer before removing the template substrate layer and at least a portion of the epitaxial thin film material layer.

10 Example 15 may include the subject matter of Example 14, wherein bonding the device stack with the temporary wafer includes depositing a bonding layer to a second side of the device stack opposite the first side, planarizing the bonding layer, and bonding the bonding layer to the temporary wafer.

Example 16 may include the subject matter of Example 14, further comprising removing the temporary wafer after bonding the first surface with the insulator layer.

15 Example 17 may include the subject matter of any one of Examples 12-16, wherein the removing the template substrate layer and at least a portion of the epitaxial thin film material layer leaves a portion of the epitaxial thin film material layer coupled to the device stack to form a transistor with the device stack.

20 Example 18 may include the subject matter of any one of Examples 12-16, wherein the insulator layer is formed of silicon dioxide or sapphire.

Example 19 may include the subject matter of Example 18, wherein the carrier wafer is formed of silicon or glass.

25 Example 20 may include the subject matter of any one of Examples 12-16, wherein the carrier wafer is formed of ceramic, metal, or a polymer material.

30 Example 21 may include an integrated circuit device comprising: a device stack having a transistor including a group III-V semiconductor or a group III-nitride compound semiconductor material disposed on a first side of the device stack; a carrier substrate; and an insulator layer disposed on the carrier substrate and bonded to the transistor on the first side of the device stack.

Example 22 may include the subject matter of Example 21, wherein the insulator layer is formed of silicon dioxide or sapphire.

Example 23 may include the subject matter of any one of Examples 21-22, wherein the carrier substrate is formed of silicon.

Example 24 may include the subject matter of any one of Examples 21-22, wherein the carrier substrate is formed of glass.

5 Example 25 may include the subject matter of any one of Examples 21-22, wherein the carrier substrate is formed of ceramic, metal, or a polymer material.

Various embodiments may include any suitable combination of the above-described embodiments including alternative (or) embodiments of
10 embodiments that are described in conjunctive form (and) above (e.g., the “and” may be “and/or”). Furthermore, some embodiments may include one or more articles of manufacture (e.g., non-transitory computer-readable media) having instructions, stored thereon, that when executed result in actions of any of the above-described embodiments. Moreover, some embodiments may include
15 apparatuses or systems having any suitable means for carrying out the various operations of the above-described embodiments.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the embodiments of the present disclosure to the precise forms disclosed. While
20 specific implementations and examples are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the present disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to embodiments of the present disclosure in light of the above detailed description. The terms used in the
25 following claims should not be construed to limit various embodiments of the present disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

30

Claims

What is claimed is:

1. A method of fabricating a silicon-on-insulator (SOI) structure comprising:
forming a device stack for an integrated circuit device on a bulk wafer;
5 removing the bulk wafer from a first side of the device stack; and
bonding the first side of the device stack with an insulator layer on a carrier wafer.
2. The method of claim 1, wherein the insulator layer is formed of silicon dioxide or sapphire.
- 10 3. The method of claim 1, further comprising bonding the device stack with a temporary wafer before removing the bulk wafer.
4. The method of claim 3, wherein bonding the device stack with the temporary wafer includes depositing a bonding layer on a second side of the device stack, planarizing the bonding layer, and bonding the bonding layer to the
15 temporary wafer.
5. The method of claim 3, further comprising removing the temporary wafer after bonding the first side of the device stack with the insulator layer.
6. The method of any one of claims 1-5, wherein removing the bulk wafer includes thinning the bulk wafer to a shallow trench isolation of the device stack.
- 20 7. The method of any one of claims 1-5, wherein removing the bulk wafer includes performing a micromachining process.
8. The method of any one of claims 1-5, wherein the bulk wafer is a silicon wafer.
9. The method of any one of claims 1-5, wherein the carrier wafer is formed of
25 silicon.
10. The method of any one of claims 1-5, wherein the carrier wafer is formed of glass.
11. The method of any one of claims 1-5, wherein the carrier wafer is formed of ceramic, metal, or a polymer material.
- 30 12. A method of fabricating a silicon-on-insulator (SOI) structure comprising:
forming a device stack for an integrated circuit device on a wafer, the wafer having a template substrate layer and an epitaxial thin film material layer, and the device stack having a first side coupled to the epitaxial thin film material layer;

removing the template substrate layer and at least a portion of the epitaxial thin film material layer to reveal a first surface of the epitaxial thin film material layer or device stack; and

5 bonding the first surface with an insulator layer that is disposed on a carrier wafer.

13. The method of claim 12, wherein the epitaxial thin film material layer is formed of Germanium (Ge), Silicon Carbide (SiC), a group III-V semiconductor, or a III-nitride compound semiconductor.

10 14. The method of claim 12, further comprising bonding the device stack with a temporary wafer before removing the template substrate layer and at least a portion of the epitaxial thin film material layer.

15 15. The method of claim 14, wherein bonding the device stack with the temporary wafer includes depositing a bonding layer to a second side of the device stack opposite the first side, planarizing the bonding layer, and bonding the bonding layer to the temporary wafer.

16. The method of claim 14, further comprising removing the temporary wafer after bonding the first surface with the insulator layer.

20 17. The method of any one of claims 12-16, wherein the removing the template substrate layer and at least a portion of the epitaxial thin film material layer leaves a portion of the epitaxial thin film material layer coupled to the device stack to form a transistor with the device stack.

18. The method of any one of claims 12-16, wherein the insulator layer is formed of silicon dioxide or sapphire.

25 19. The method of claim 18, wherein the carrier wafer is formed of silicon or glass.

20. The method of any one of claims 12-16, wherein the carrier wafer is formed of ceramic, metal, or a polymer material.

30 21. An integrated circuit device comprising:
a device stack having a transistor including a group III-V semiconductor or a group III-nitride compound semiconductor material disposed on a first side of the device stack;

a carrier substrate; and

an insulator layer disposed on the carrier substrate and bonded to the transistor on the first side of the device stack.

22. The integrated circuit device of claim 21, wherein the insulator layer is formed of silicon dioxide or sapphire.
23. The integrated circuit device of any one of claims 21-22, wherein the carrier substrate is formed of silicon.
- 5 24. The integrated circuit device of any one of claims 21-22, wherein the carrier substrate is formed of glass.
25. The integrated circuit device of any one of claims 21-22, wherein the carrier substrate is formed of ceramic, metal, or a polymer material.

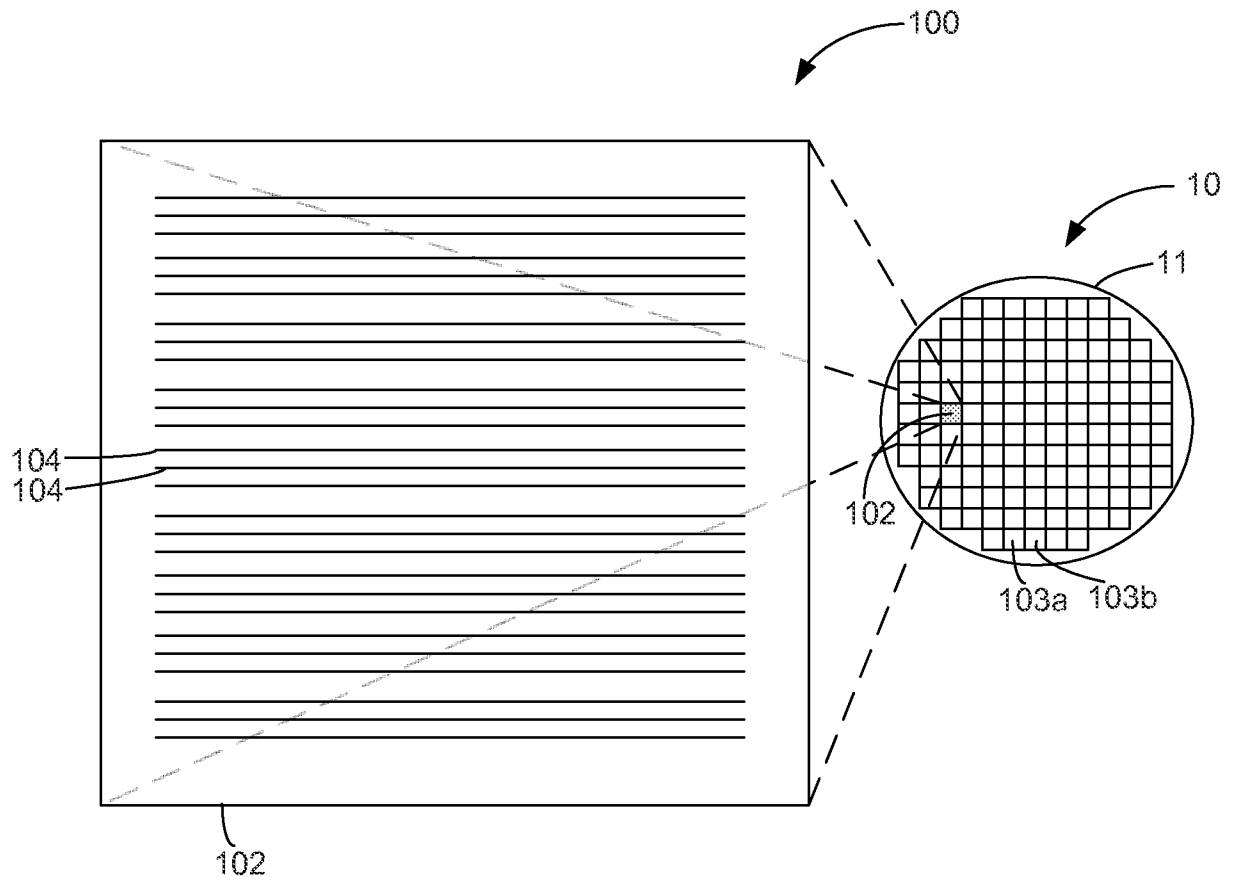


FIG. 1

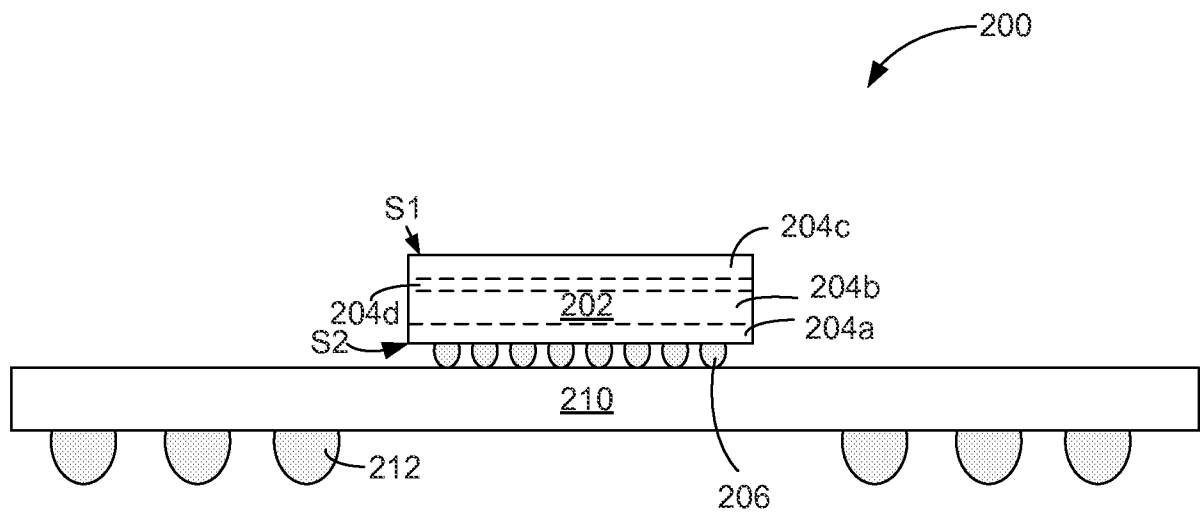


FIG. 2

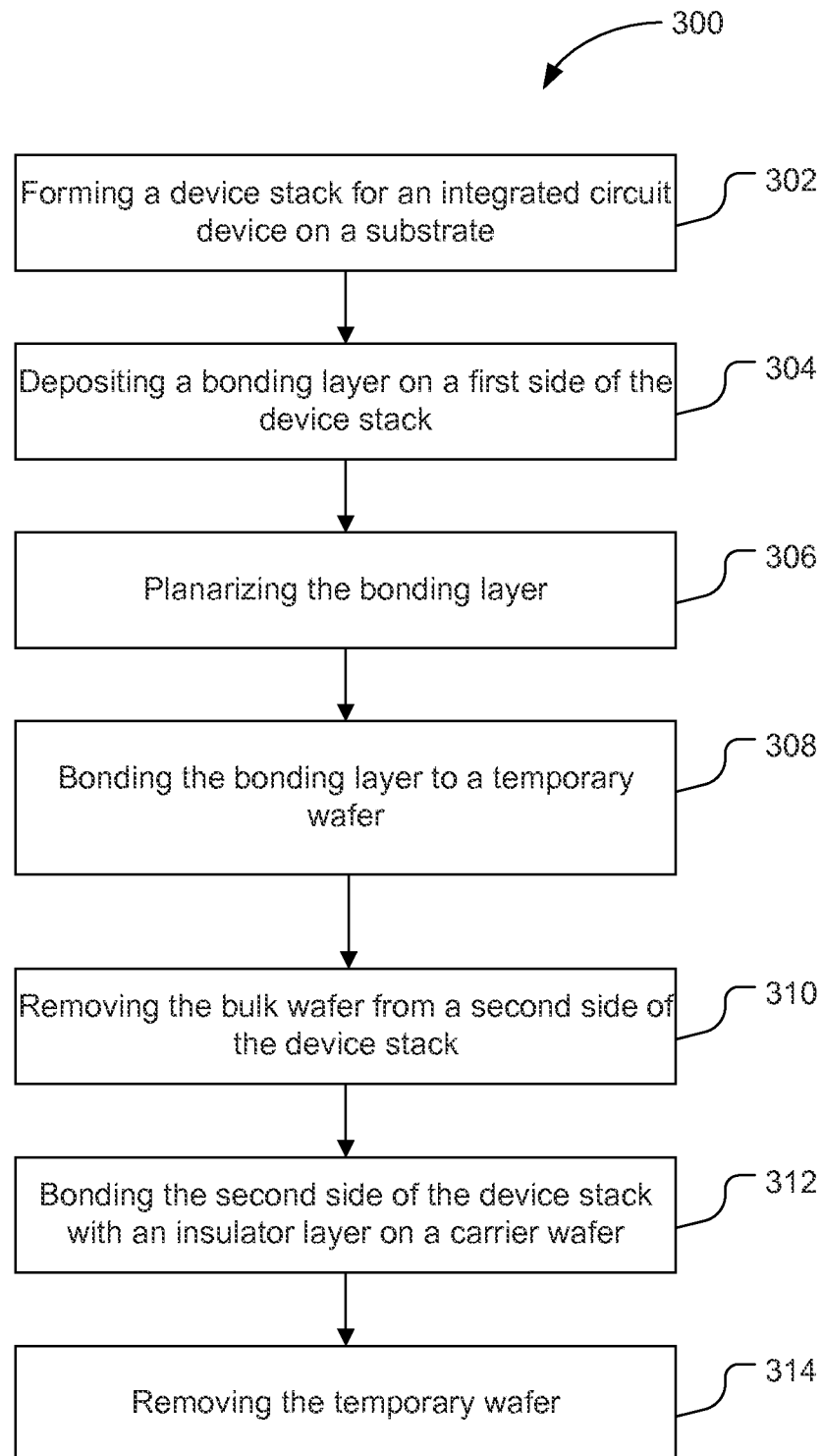


FIG. 3

3/8

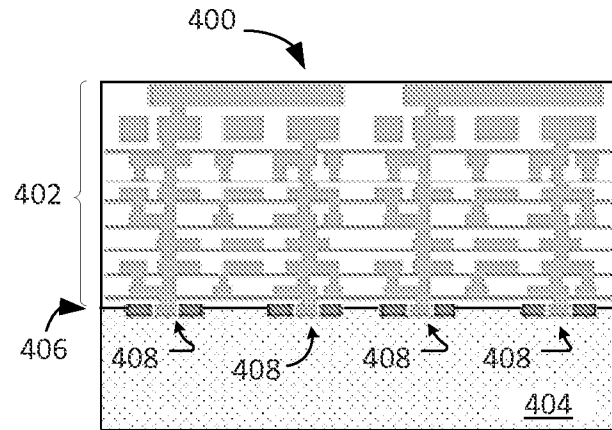


FIG. 4A

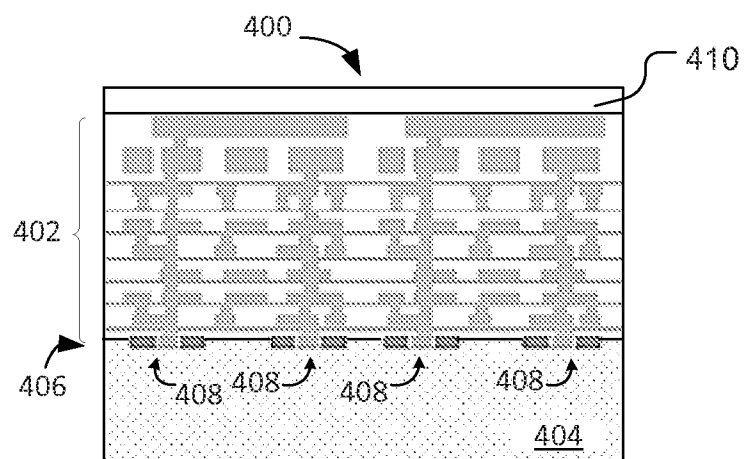


FIG. 4B

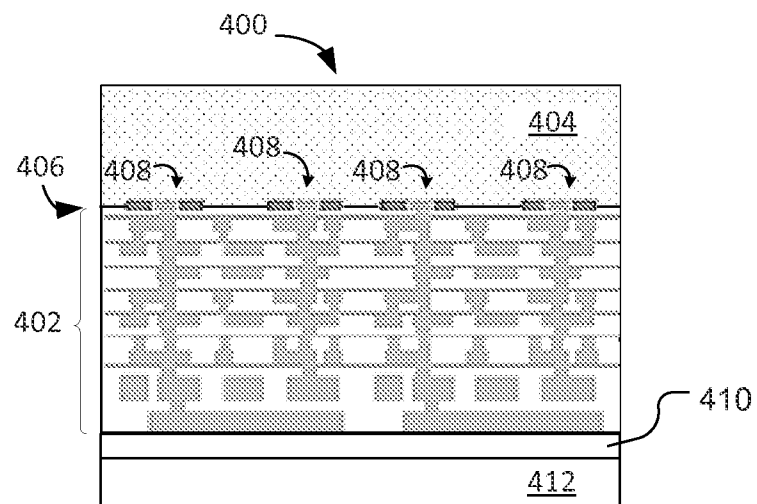


FIG. 4C

4/8

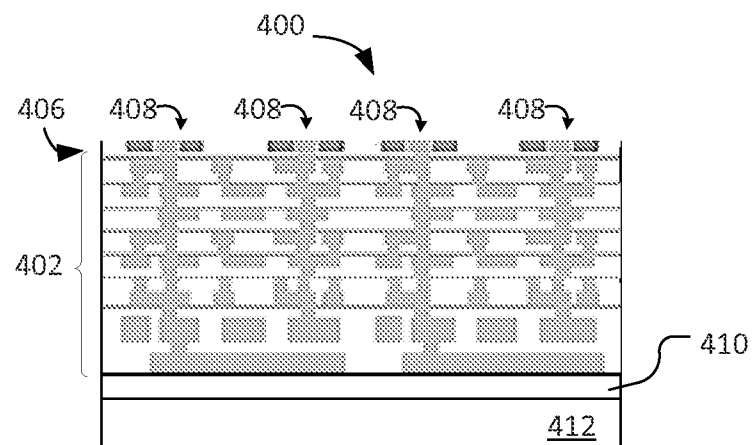


FIG. 4D

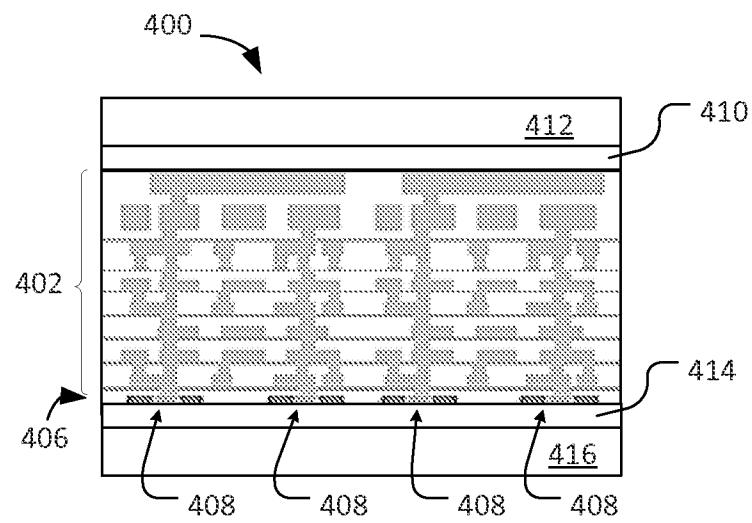


FIG. 4E

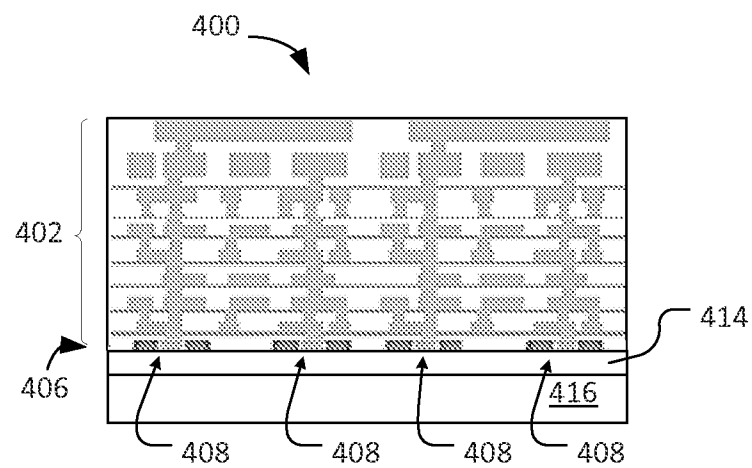


FIG. 4F

5/8

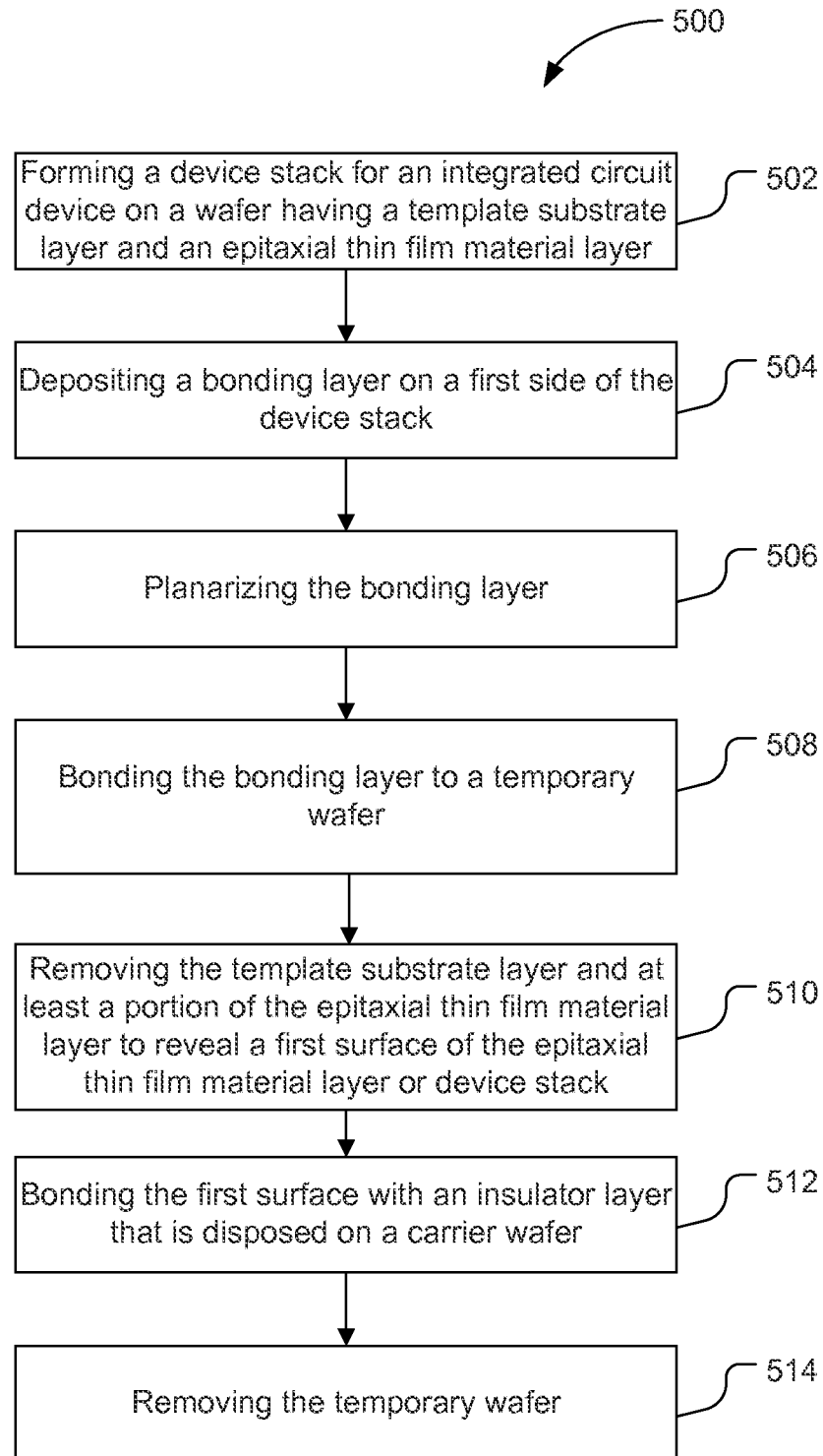


FIG. 5

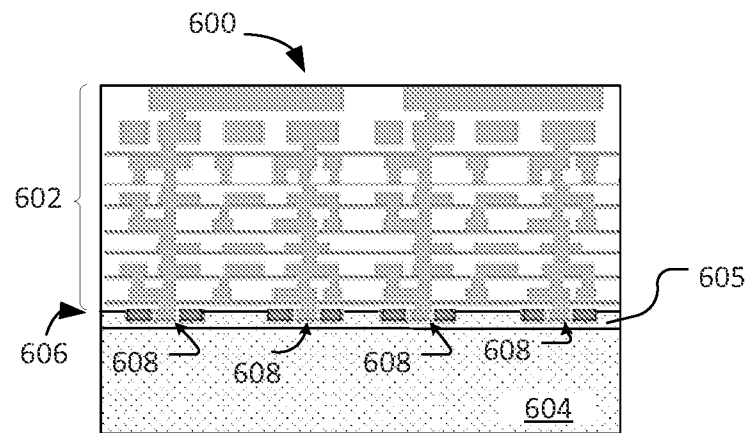


FIG. 6A

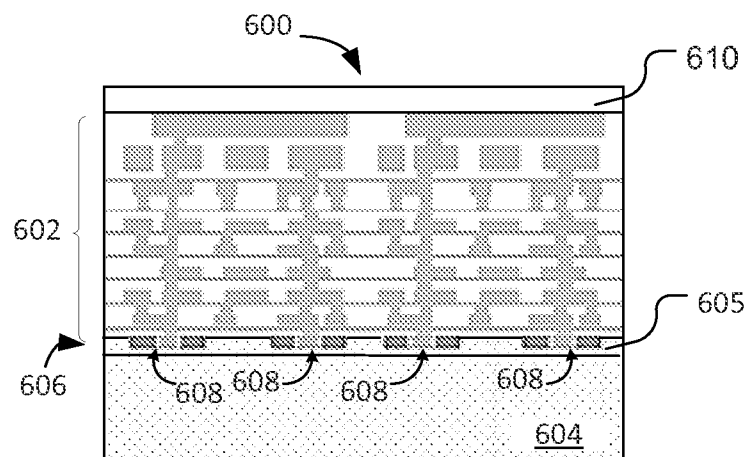


FIG. 6B

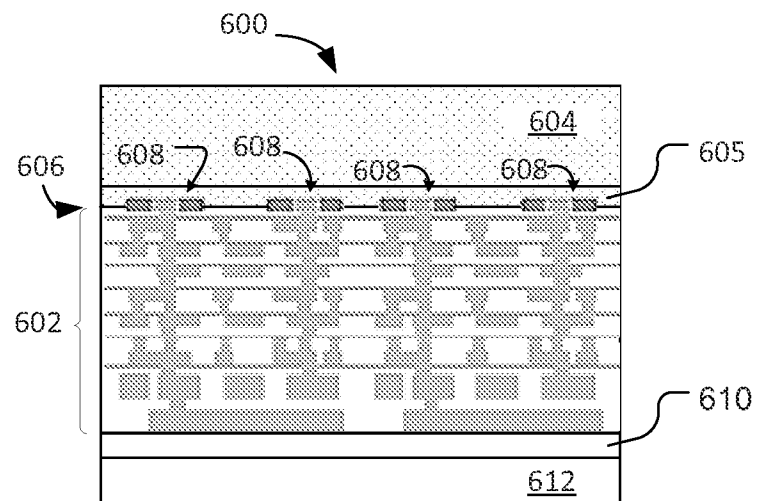


FIG. 6C

7/8

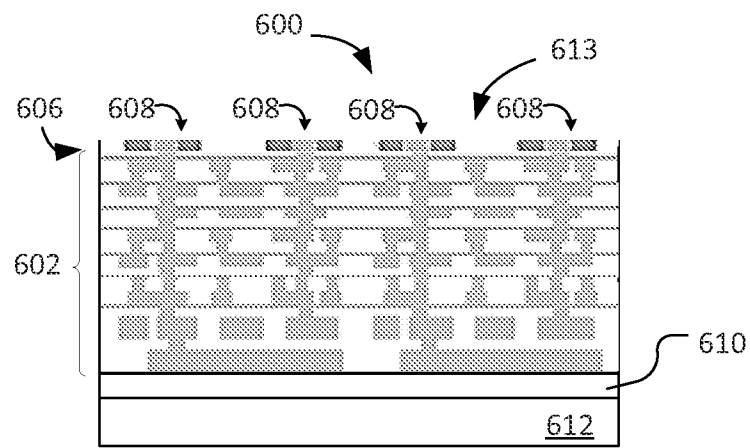


FIG. 6D

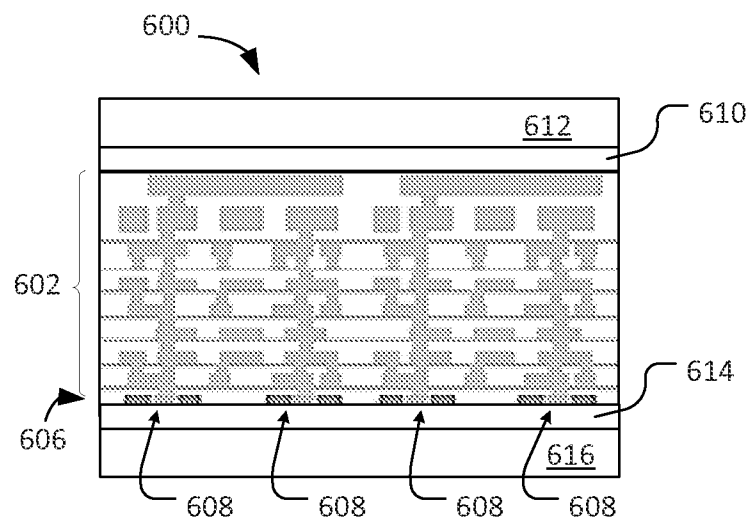


FIG. 6E

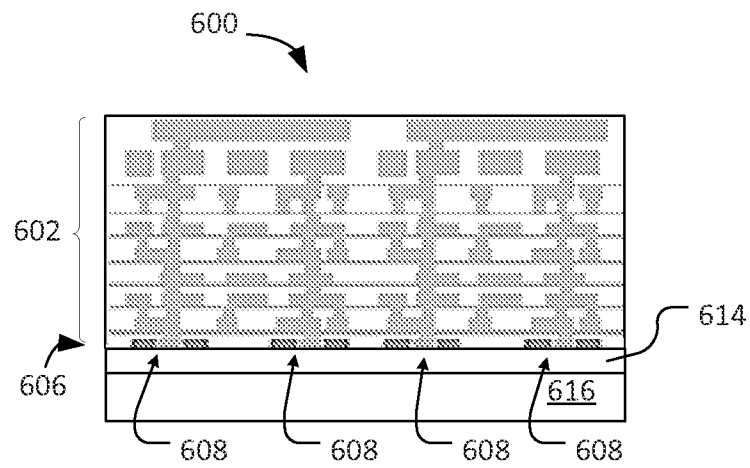


FIG. 6F

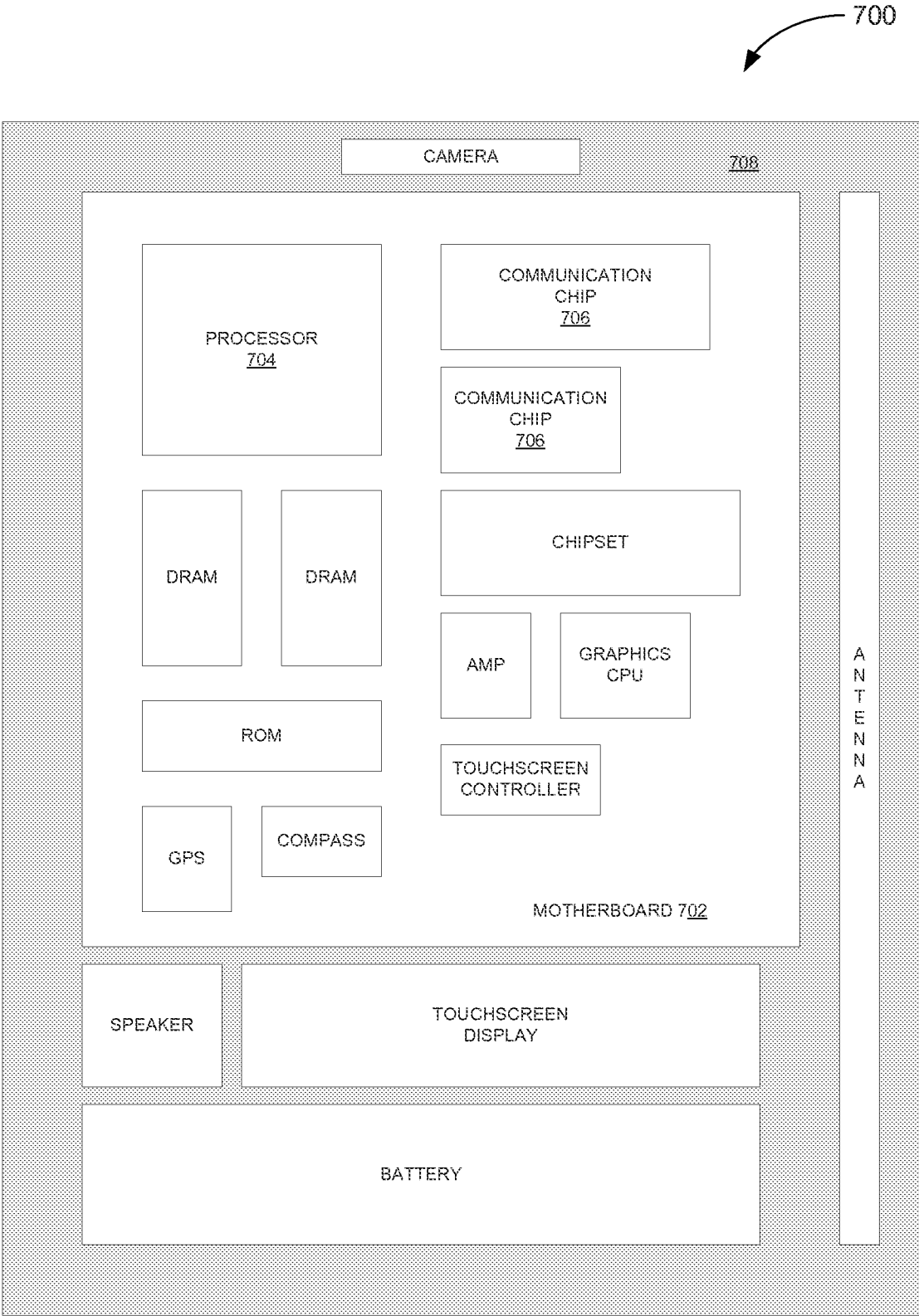


FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/12; H01L 21/324; H01L 21/8249; H01L 27/06; H01L 21/762; H01L 27/15; H01L 21/265; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: SOI, wafer, bond, remove, transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-0257068 B1 (HYUNDAI MICRO ELECTRONICS CO.,LTD.) 15 May 2000 See abstract, page 3 and figures 3-5k.	1-25
A	US 2013-0210214 A1 (SKORPIOS TECHNOLOGIES INC.) 15 August 2013 See abstract, paragraphs [0040]-[0087] and figures 1-9E.	1-25
A	US 5580802 A (DONALD C. MAYER et al.) 03 December 1996 See abstract, column 4, line 55 - column 7, line 44 and figures 1-4C.	1-25
A	JP 2000-077548 A (TOSHIBA CORP.) 14 March 2000 See abstract, paragraphs [0009]-[0024] and figures 2-10.	1-25
A	US 2005-0280011 A1 (JOHAN HENDRIK KLOOTWIJK et al.) 22 December 2005 See abstract, paragraphs [0029]-[0042] and figures 1-6.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 June 2016 (13.06.2016)

Date of mailing of the international search report

13 June 2016 (13.06.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/051994

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