(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 August 2009 (06.08.2009)

PCT

(10) International Publication Number
WO 2009/095349 A1

(51) International Patent Classification:
H03M 1/36 (2006.01) *H03M 1/42* (2006.01)

(21) International Application Number:
PCT/EP2009/050723

(22) International Filing Date: 22 January 2009 (22.01.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/024,952 31 January 2008 (31.01.2008) US
08075253.8 31 March 2008 (31.03.2008) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) Title: COMPARATOR BASED ASYNCHRONOUS BINARY SEARCH A/D CONVERTER

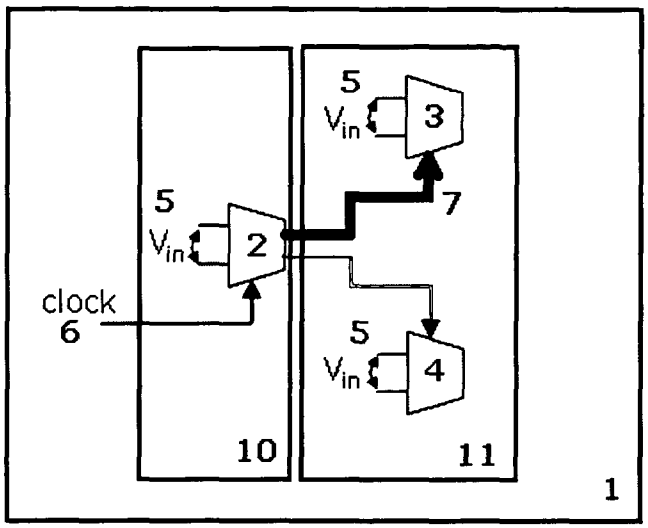


Fig.1

(57) Abstract: The present invention is related to an analog-to-digital converter circuit (1) wherein a comparator based asynchronous binary search is used. The architecture comprises a self-clocked (asynchronous) hierarchical binary tree of comparators, each arranged for being provided with a predetermined threshold. The input signal is applied in parallel to all comparators as is the case with flash converters, but the clock is applied to (at least) one comparator (2) only, preferably to the first or root comparator. The at least one comparator (2) is further arranged for controlling at least one other comparator (3) of the plurality of comparators (2, 3, 4).

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COMPARATOR BASED ASYNCHRONOUS BINARY SEARCH A/D CONVERTER

Field of the Invention

[0001] The present invention relates to an analog-to-digital converter architecture, wherein a comparator based asynchronous binary search is used.

Background of the Invention

[0002] In recent years significant progress is made in lowering the power consumption in medium- to high-speed (tens of MS/s to a few GS/s) and medium- to low-resolution (4 bit to 9 bit) A/D converters. Current state-of-the-art Figure of Merit (FoM) is 65fJ. The FoM is determined as

$$FoM = \frac{P}{2^{ENOB} \cdot F_{sample}}$$

and represents the energy needed per conversion step. P denotes power in W, F_{sample} sample rate in 1/s and ENOB stands for the Effective Number of Bits. These efficiency improvements are primarily driven by mobile, wireless applications and sensor networks.

[0003] Flash architectures, as in WO2008/006751, are often chosen because they offer the largest speed. However, area and power depend exponentially on the resolution since the comparators are often the largest contributor to the overall power consumption. The bits are determined via a parallel search. On the other hand, a low-power SAR-based architecture is presented in patent application WO2007/088175.

[0004] Another possible approach to reduce the power consumption and increase the speed of a converter is by splitting the conversion process into two steps. A 1-bit folding front-end can for example be used in combination with a flash ADC as presented in patent document US6369726, reducing the number of comparators.

[0005] In patent document EP1079528-A1 a current-mode ADC is proposed that uses an asynchronous search algorithm in which each comparator in a set is triggered by its neighbour in a non-hierarchical way (i.e. all comparators have the same weight or importance), and a current is used to alter the input current. The

architecture relies on current mode to realize low-voltage operation and hence to save on power.

[0006] In the paper "A current boosting full-flash A/D converter" (*Jungwook Yang et al., Proc.Int'l Symp. On Circuits and Systems, San Diego, vol.2, 3 May 1992, pp.609-612*) the number of activated comparators in a flash converter is reduced by selecting a relevant set. The range finder circuit introduced by the authors are clocked synchronously (all at the same time) and based on their outputs only a part of the comparators of the flash converter are deactivated by reducing their biasing current and hence reducing power consumption.

Summary of the Invention

[0007] An analog to digital conversion circuit is presented comprising a plurality of comparing means each being provided with a predetermined threshold and arranged for being fed with a version of a same input voltage signal and whereby at least one comparing means is arranged for being fed with a clock signal. The at least one comparing means is further arranged for controlling or triggering at least one other comparing means of the plurality of comparing means. In a preferred embodiment this plurality of comparing means is structured in at least two hierarchical levels, meaning that the layers form a hierarchical tree wherein each layer determines the value of the input signal to a smaller degree than the preceding layer. It is checked if the signal is smaller or bigger than half of the range and then inside half a range smaller or bigger than a quarter of the range etc... A comparing means at the highest hierarchical layer is arranged for being fed with the clock signal.

[0008] A Comparator based Asynchronous Binary Search (CABS) architecture is presented to minimize power consumption. The only active circuits needed are dynamic comparing means to which a predetermined threshold can be applied. An example of comparing means can be comparators with embedded thresholds. The architecture offers a power consumption that is proportional to the sampling frequency. The architecture comprises a self-clocked (asynchronous) binary tree of comparing means (comparators). The input voltage signal is applied in parallel to all comparators as is the case with flash converters, but the clock is applied to the first or root comparator only. The architecture of the present invention combines a fast flash architecture with a classical SAR-approach. Typically, in a flash converter, the bits are determined via a parallel search, requiring a lot of power consuming

comparators. By using (preferably) a binary search instead of a parallel one, the number of active comparators is reduced and therefore the power consumption.

[0009] In an alternative embodiment the architecture further comprises a delay circuit and a digital-to-analog converter (DAC) between two subsequent hierarchical layers. Based on the decision of a comparing means, this DAC outputs a signal that either adds or subtracts from the sampled input voltage a value depending on the weight of the decision. The input voltage signal is thus updated. Again, a self-clocked chain of comparators (with threshold at zero), with inserted delay circuits, controls this DAC. By using that DAC, a successive approximation process or binary search algorithm may be implemented. In this embodiment the comparators at lower hierarchical layers are fed with an input signal being a combination of the input voltage signal and the updating signal output by the DAC.

[0010] In a preferred embodiment an analog-to-digital conversion circuit is presented for converting an analog signal into a digital representation with n bits. In a first block, m bits are determined via an architecture comprising a self-clocked chain of comparators with delay blocks controlling a DAC implementing the successive approximation process. In a second block, n-m bits are determined via the CABS architecture.

[0011] In an alternative embodiment a method is presented for converting an analog signal into a digital representation of this analog signal. The method comprises the steps of: applying this signal to each comparing means (e.g. a comparator) of an analog-to-digital conversion circuit, comparing this input signal with the predetermined threshold of an at least one comparator and controlling (triggering) a second comparator based on the comparison in the previous step. The analog-to-digital converter comprises a plurality of comparators each configured to have a predetermined threshold and whereby at least one comparator of this plurality is fed with a clock signal.

[0012] In a preferred embodiment the plurality of comparing means is structured in at least two hierarchical layers and the at least one comparing means to which the clock signal is fed, is at higher hierarchical layer then the second comparator.

[0013] In an embodiment the step of comparing yields a binary output signal. An unsigned binary code is obtained by taking an OR of all '>' output pins of the activated comparators on each layer of the binary tree. For an *n*-bit ADC, this

architecture contains 2^n-1 comparators, similar to a flash ADC, but of which, only *n* comparators are activated during quantization, with *n* OR encoder functions to determine the outputs. This drastically lowers the power consumption.

[0014] In another embodiment the step of comparing yields an output signal that is fed to a DAC, implementing a successive approximation process. A binary code is determined.

[0015] The CABS can be read out by taking an OR of all '>' (greater than) output pins of the activated comparators on each layer. This has a beneficial effect on the power consumption.

Brief Description of the Drawings

[0016] Preferred embodiments are described below in conjunction with the appended drawing figures, wherein like reference numerals refer to like elements in the various figures.

[0017] Fig. 1 represents a block diagram of the present invention.

[0018] Fig. 2 illustrates the proposed CABS hierarchical binary tree architecture.

[0019] Fig. 3 illustrates the proposed comparator chain architecture.

[0020] Fig. 4 illustrates the architecture of the 2-step 7 bit ADC, 1 bit coarse A/D and D/A followed by a 6 bit CABS ADC.

[0021] Fig. 5 illustrates schematically the clocking.

[0022] Fig. 6 shows the comparator-based asynchronous binary-search operating principle of the 6 bit converter.

[0023] Fig. 7 shows schematically the circuit of the comparator and the encoder.

[0024] Fig. 8 plots the INL/DNL of ADC after calibration.

[0025] Fig. 9 plots the SNDR versus the clock frequency for a low frequency and Nyquist input frequency at different clock rates and the SNDR versus the signal frequency.

[0026] Fig. 10 plots the low frequency and the Nyquist power spectra.

Detailed Description of Embodiment(s)

[0027] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the scope is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0028] An analog to digital conversion circuit (1) is presented as shown in Fig.1, comprising a plurality of comparing means (2, 3, 4) like comparators, preferably structured in layers (10,11). In the higher up layer (10) more important decisions with a bigger impact are taken than in lower layer (11). In this way an hierarchical tree is created by the various layers. Each comparing means has a predetermined threshold, which may have been fed to the comparing means. Each comparator (or other comparing means) is arranged for being fed with a same input signal (5). At least one comparator (2) is arranged for being fed with a clock signal (6), thereby controlling or triggering (7) at least one other comparator (3) of said plurality of comparators (2, 3, 4). By controlling is meant that a comparing means is arranged for selecting a path in the structure formed by the plurality of comparing means. The clock signal (6) is preferably applied to the comparator (2) of the highest hierarchical layer (10).

[0029] In a preferred embodiment the architecture of the present invention is based on combining a fast flash architecture with a classical SAR-approach. Typically, in a flash converter the bits are determined via a parallel search, requiring a lot of power consuming comparators. By using (preferably) a binary search instead of a parallel one, the number of active comparators and therefore the power consumption is reduced. The proposed architecture leverages the advantages of both techniques. In other words, an analog-to-digital converter is presented that uses a Comparator based Asynchronous Binary Search (CABS) architecture to minimize power consumption. The only active circuits needed are dynamic comparators with embedded threshold. The architecture offers a power consumption that is proportional to the sampling frequency.

[0030] The operation of the proposed CABS architecture is exemplified in Fig. 2. The example is illustrated for V_{in}=0.3 and n=3 (number of hierarchical levels and hence also the number of bits). The black bold line gives the binary search sequence. In a first step the sign of the input is determined (> or < 0). In a second step the input is compared to half the range and in a third step to ¼ of the range.

Only 3 (or n) comparators need to be activated, instead of 7 (or 2^n-1). The clock signal is only applied to the root comparator. A comparator of a second level is triggered or controlled by the comparator of the first comparison step. In other words, the various levels in the structure are hierarchically ordered. This hierarchical order is also reflected in the range covered by a comparator : the comparator at the highest level covers the full scale range, the two comparators at the level below each cover only half of the range etc...

[0031] In an alternative embodiment the architecture comprises a self-clocked chain of comparators (with threshold at zero) with inserted delay blocks controlling a DAC implementing the successive approximation process or binary search. The DAC (40) converts the decision of the previous comparator into an analogue voltage (41) that must be added to/subtracted from the input voltage signal. The delay circuit (17) can be implemented using inverters with limited drive strength. The presence of the delay block provides the DAC some time to adapt the input signal of the next comparator in the chain (15). The settling of the DAC occurs faster than the logic delay time τ. Fig. 3 shows the proposed comparator chain for two bits. Again, the clock signal is only applied to the comparator of the highest hierarchical level and a comparator of a second level is triggered by the first comparison step. In this embodiment a SAR controller is implemented. The output of the first comparison is applied to a DAC (40). The example is illustrated for V_{in} = 0.3 and n=2. In every step, the input is compared to zero. In the first step, the DAC subtracts 1/2 of the full-scale range in charge from one of the input nodes (0.3 > 0). In a second step, the DAC adds ¼ (-0.2 < 0) to the input. Note that in this embodiment the SAR approach has been used for reading out the binary code. The SAR register is hence formed by the comparator outputs at each layer (to be more precise, by the positive output).

[0032] Both embodiments can be combined. This results in an analog-to-digital conversion circuit, converting an analog signal into a digital representation with n bits. In a first block, m bits are determined via an architecture comprising a self-clocked chain of comparators with delay blocks controlling a DAC implementing the successive approximation process. In a second block, n-m bits are determined via the CABS architecture.

[0033] This combination is illustrated for a 7 bit ADC. The present invention is illustrated in Fig.4 and provides a 2-step 7 bit ADC comprising a track and hold (T/H) circuit (21), followed by a 1 bit comparison and D/A conversion (22), and a 6 bit

comparator-based asynchronous binary-search (CABS) conversion (23), whereby the different blocks are steered by a clock generator (24). The 7b ADC operates as follows: the passive T/H circuit (21) samples the input signal (25) on a capacitance (26), the 1 bit comparator (27) determines the sign of the input (MSB, B[6]) and steers a capacitive DAC (28). The DAC subtracts ¼ of the full-scale range in charge from one of the input nodes, changing simultaneously differential signal and common-mode level to be in range of the 6 bit CABS converter (23). The clock buffer (24) generates the 1 bit coarse A/D clock signal (29) and starts (30) the 6 bit fine conversion after the 1 bit D/A conversion has finished (31). This clocking is graphically represented in Fig.5.

[0034] The 6 bit CABS converter comprises a self-clocked (asynchronous) binary tree of comparators with embedded threshold. A conceptual block diagram is shown in Fig. 6(a) (for the two MSBs only). The input signal is applied in parallel to all comparators as is the case with flash converters, but the clock (30) is applied to the root comparator only. This comparator determines if the sampled signal is above or below 0 and outputs this on either its '<' (lower than) or '>' (greater than) pin. One of the comparators (3,4) in the next layer of the binary tree is then triggered asynchronously, i.e. either the ½ or the -½ scale comparator (waveforms shown in Fig. 6(b)). An unsigned binary code is obtained by taking an OR of all '>' output pins of the activated comparators on each layer. For an *n*-bit ADC, this architecture contains 2^n-1 comparators, similar to a flash ADC, but of which, only *n* comparators are activated during quantization, with *n* OR encoder functions to determine the outputs. This drastically lowers the power consumption. A clock signal starts and resets the level-triggered quantization process. Note that in contrast to standard asynchronous SAR implementations, in this architecture a comparator is not reset immediately. Only when the whole quantization process is finished, the *n* activated comparators are reset from the root comparator following the same path as during quantization. This reset phase overlaps with the tracking phase of the T/H circuit.

[0035] The comparator is implemented using a dynamic latch (see Fig. 7), as described for example in "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture" (*T. Kobayashi et al., IEEE J. Solid-State Circuits, vol. 28, no. 4, pp. 523-527, Apr. 1993*) or in "Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier" (*B. Wicht et al., IEEE J. Solid-State Circuits, vol. 39, no. 7, pp. 1148-1158, Jul. 2004*). When the 'Comp' pin is low,

the comparator is reset and both outputs are low. In contrast to the implementation of the Wicht paper, there is an additional NMOS device (indicated on Fig. 7) pulling down node 'M', to drive the PMOS input pair in accumulation. This is done to reduce the non-linearity of the input capacitance of the comparators since the input signal is sampled on this capacitance. A rising edge on 'Comp' turns on the PMOS input pair (which contains an intentional imbalance to set its threshold level) and the cross-coupled regenerative latch amplifies the input signal to a full logic level. This comparator circuit is sized as small as possible, thermal noise being the limiting performance metric. To compensate for the increased mismatch, calibration capacitances are added on all internal nodes of the comparator. The inverter stages at both outputs have a high input threshold to avoid causing a trigger event on both outputs. They also buffer the signal to drive the next comparator in the binary tree and the encoder transistors. The OR encoder function is implemented by driving the bitline B[*i*] (of the *ith* layer) by a pull-up transistor if the comparator decides 'greater than', and a pull-down transistor if the comparator decides 'lower than'. The non-activated comparators on each layer have a high-impedance output. When the comparator is reset, the outputs remain on the bit lines, so the output of the ADC is available after the quantization has finished and the comparators are reset.

[0036] The converter is implemented in a 1V 90nm digital CMOS using low- and regular-V_T devices only. The ADC is calibrated as follows : for each comparator the desired threshold is applied at the input and the digital calibration code is found with a binary search where the ADC output toggles 50% between the two codes. The capacitive DAC is calibrated similarly, by applying two thresholds and using a comparator to determine when the step is exactly ¼ of full scale. Both feedback capacitances $C_{in\text{-}DA}$ (coarse steps) as well as C_{in} (fine steps) are calibrated in this way (Fig. 3). Once calibrated, the ADC is characterized for different clock frequencies. A maximum INL (integral non-linearity) and DNL (differential non-linearity) of 0.48 and 0.93LSB are obtained (Fig. 8) where the LSB size is 6mV. At clock frequencies up to 150MS/s, the ADC achieves 40dB SNDR over the whole Nyquist band, the Effective Resolution Bandwidth (ERBW) is 270MHz (Fig. 9). Because of the fully dynamic implementation, the power consumption scales linearly with the sampling rate and is equal to 0.89µW per MHz of clock rate. This gives a FOM of 10fJ/conversion-step. For comparison, the FOM of the ADC above 100MS/s and for 6 bits and more has been improved from 220fJ to 10fJ/Conversion step. The

power spectra of a full-scale low-frequency and Nyquist input signal at 150MS/s are shown in Fig. 10, the Spurious Free Dynamic Range (SFDR) is 55.4dB for a low-frequency.

[0037] Although the present invention has been illustrated by reference to specific embodiments, it will be apparent to those skilled in the art that the invention is not limited to the details of the foregoing illustrative embodiments, and that the present invention may be embodied with various changes and modifications without departing from the spirit and scope thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein. In other words, it is contemplated to cover any and all modifications, variations or equivalents that fall within the spirit and scope of the basic underlying principles and whose essential attributes are claimed in this patent application. It will furthermore be understood by the reader of this patent application that the words "comprising" or "comprise" do not exclude other elements or steps, that the words "a" or "an" do not exclude a plurality, and that a single element, such as a computer system, a processor, or another integrated unit may fulfil the functions of several means recited in the claims. Any reference signs in the claims shall not be construed as limiting the respective claims concerned. The terms "first", "second", third", "a", "b", "c", and the like, when used in the description or in the claims are introduced to distinguish between similar elements or steps and are not necessarily describing a sequential or chronological order. Similarly, the terms "top", "bottom", "over", "under", and the like are introduced for descriptive purposes and not necessarily to denote relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and embodiments of the invention are capable of operating according to the present invention in other sequences, or in orientations different from the one(s) described or illustrated above.

CLAIMS

1. An analog to digital conversion circuit (1) comprising a plurality of comparing means (2, 3, 4) each arranged for being fed with a same input voltage signal (5) and each arranged for being provided with a predetermined threshold to compare said input voltage with, and whereby at least one comparing means (2) of said plurality is arranged for being fed with a clock signal (6) characterised in that said at least one comparing means (2) is further arranged for controlling at least one other comparing means (3) of said plurality of comparing means (2, 3, 4).

2. An analog to digital conversion circuit (1) as in claim 1 wherein said plurality of comparing means (2, 3, 4) is configured to form a hierarchical tree structure comprising a plurality of hierarchical levels (10, 11).

3. An analog to digital conversion circuit (1) as in claim 2, wherein a comparing means (2) of said plurality being at the top level (10) of said structure is arranged for being fed with said clock signal (6).

4. An analog to digital conversion circuit as in any of claims 2 or 3 further comprising between two subsequent levels (10, 11) of said structure a delay circuit (17) and a DAC (40) arranged for outputting a signal (41) for updating said input voltage signal (5), said DAC arranged for being controlled by the comparing means at the highest level of said two subsequent levels .

5. An analog to digital conversion circuit as in claim 4 wherein said at least one comparator (2) is further arranged for controlling said delay circuit and said DAC.

6. An analog to digital converter for converting an analog signal into a digital representation of said analog signal with n bits comprising a first analog to digital conversion circuit as in claim 4 or 5 and a second analog to digital conversion circuit as in any of claims 1 to 3 whereby the first analog to digital conversion circuit is arranged for determining m bits of said digital representation and the second analog to digital conversion circuit is arranged for determining n-m bits of said digital representation.

7. A method for converting an analog signal into a digital representation of said analog signal comprising the steps of

- applying said signal to each comparing means of an analog-to-digital conversion circuit comprising a plurality of comparing means each being provided with a predetermined threshold; and whereby at least one comparing means of said plurality is fed with a clock signal;
- comparing said input signal with the predetermined threshold of said at least one comparing means
- controlling a second comparing means of said plurality of comparing means based on the comparison in the previous step.

8. A method as in claim 7 whereby said plurality of comparing means is structured in at least two hierarchical layers and whereby the at least one comparing means to which the clock signal is fed, is at higher hierarchical layer than said second comparing means.

9. A method as in any if claims 7 or 8 whereby the step of comparing yields a binary output signal.

10. A method as in any of claims 7 or 8 whereby the step of comparing yields an output signal that is fed to a DAC.

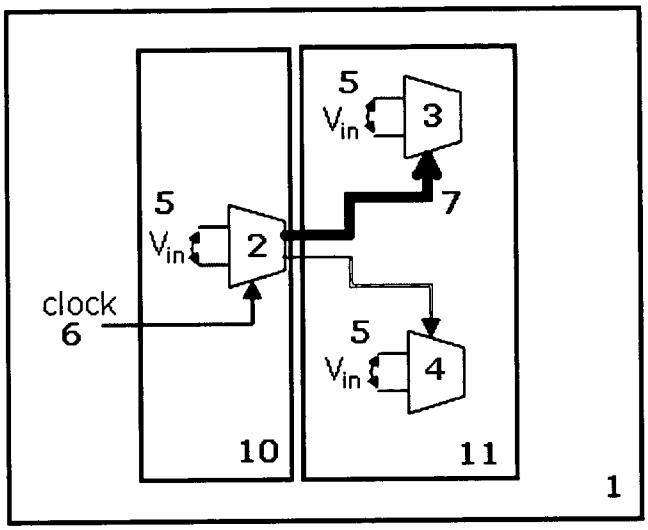

5
Vin
3
7
5
Vin
2
clock
6
5
Vin
4
10
11
1

Fig.1

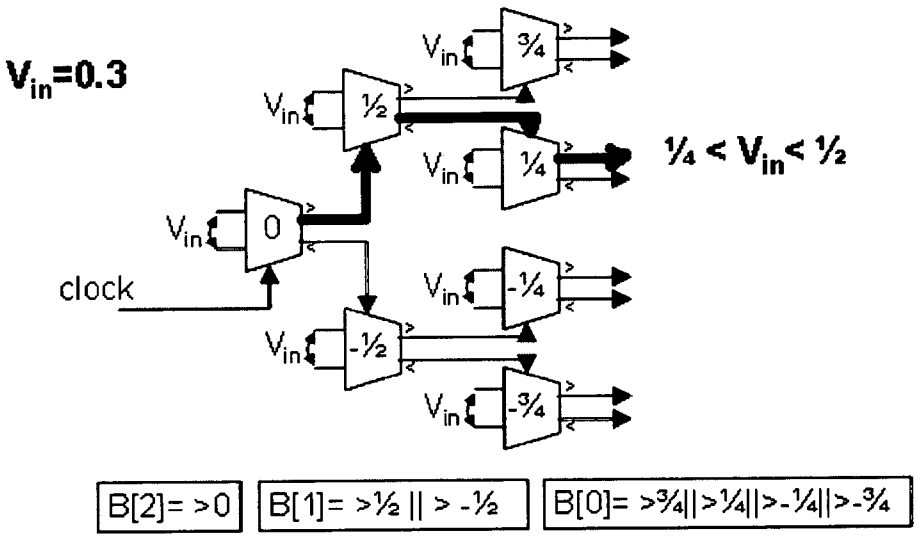

Vin=0.3
Vin
¾
Vin
½
Vin
¼
¼ < Vin < ½
Vin
0
clock
Vin
-¼
Vin
-½
Vin
-¾
B[2]= >0
B[1]= >½ || > -½
B[0]= >¾||>¼||>-¼||>-¾

Fig.2

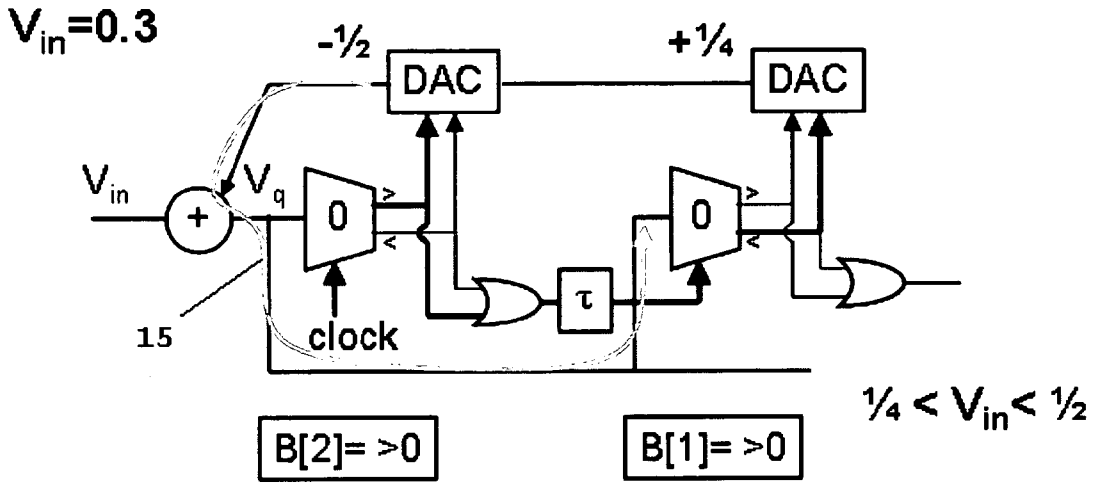

Vin=0.3
-½
DAC
+¼
DAC
Vin
Vq
+
0
0
τ
15
clock
¼ < Vin < ½
B[2]= >0
B[1]= >0

Fig.3

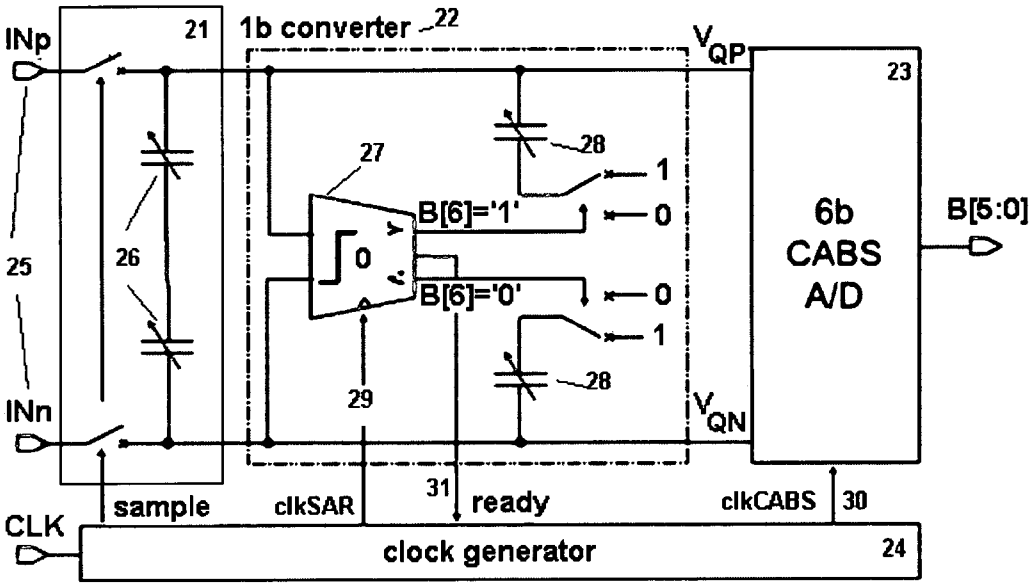

INp
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1b converter
22
VQP
23
27
28
1
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0
6b
CABS
A/D
B[5:0]
25
26
0
B[6]='0'
0
1
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INn
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VQN
CLK
sample
clkSAR
31
ready
clkCABS
30
clock generator
24

Fig.4

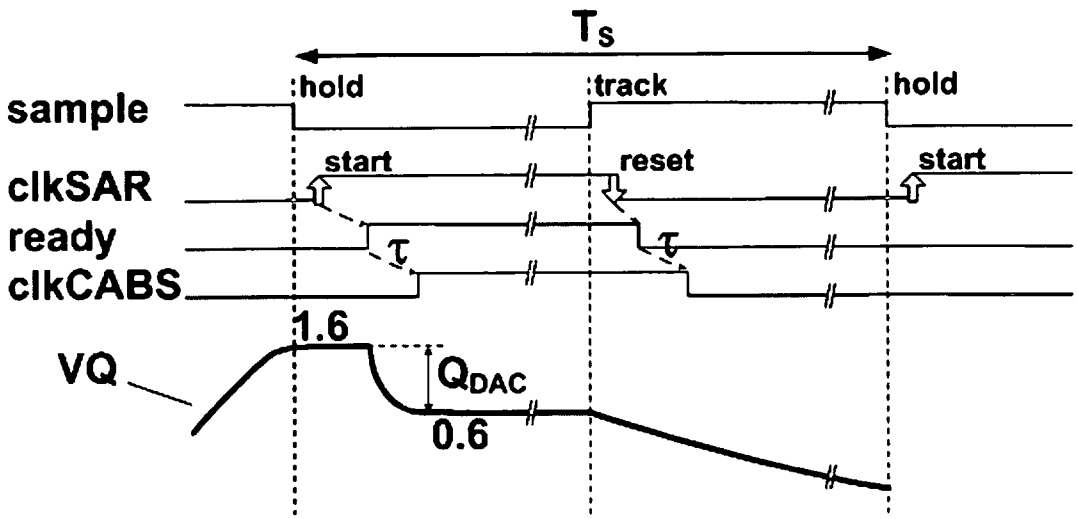

Ts
hold
track
hold
sample
start
reset
start
clkSAR
ready
clkCABS
τ
τ
1.6
VQ
QDAC
0.6

Fig.5

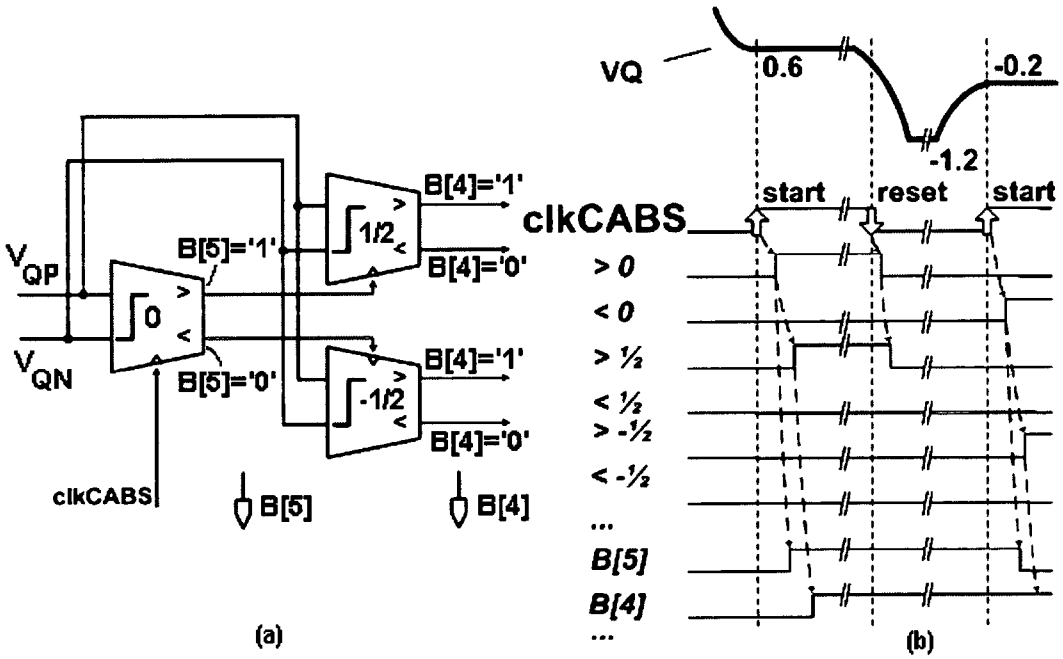

VQP
VQN
0
B[5]='1'
B[5]='0'
1/2
-1/2
B[4]='1'
B[4]='0'
B[4]='1'
B[4]='0'
clkCABS
B[5]
B[4]
(a)
VQ
0.6
-0.2
-1.2
start
reset
start
clkCABS
> 0
< 0
> ½
< ½
> -½
< -½
...
B[5]
B[4]
...
(b)

Fig.6

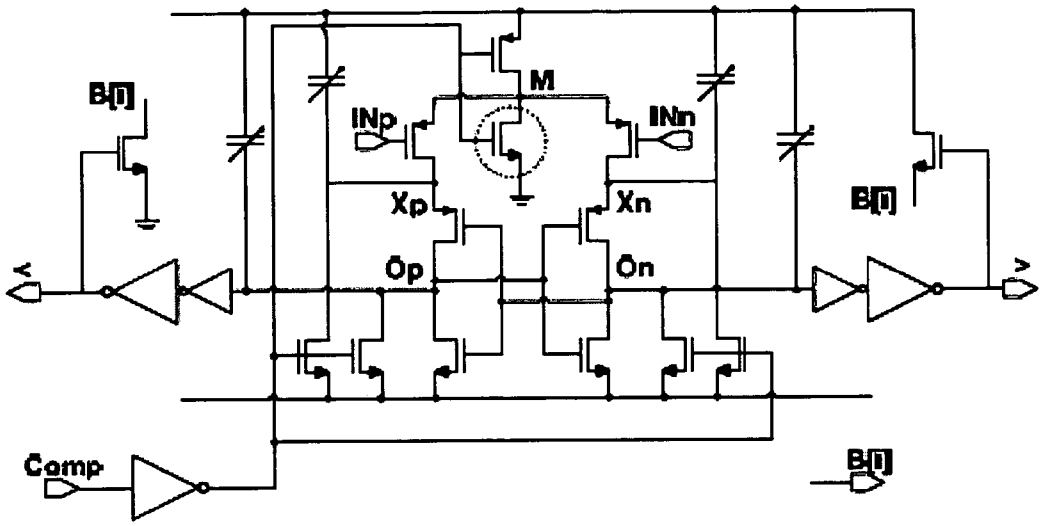

B[i]
M
INp
INn
Xp
Xn
Op
On
B[i]
Comp
B[i]

Fig.7

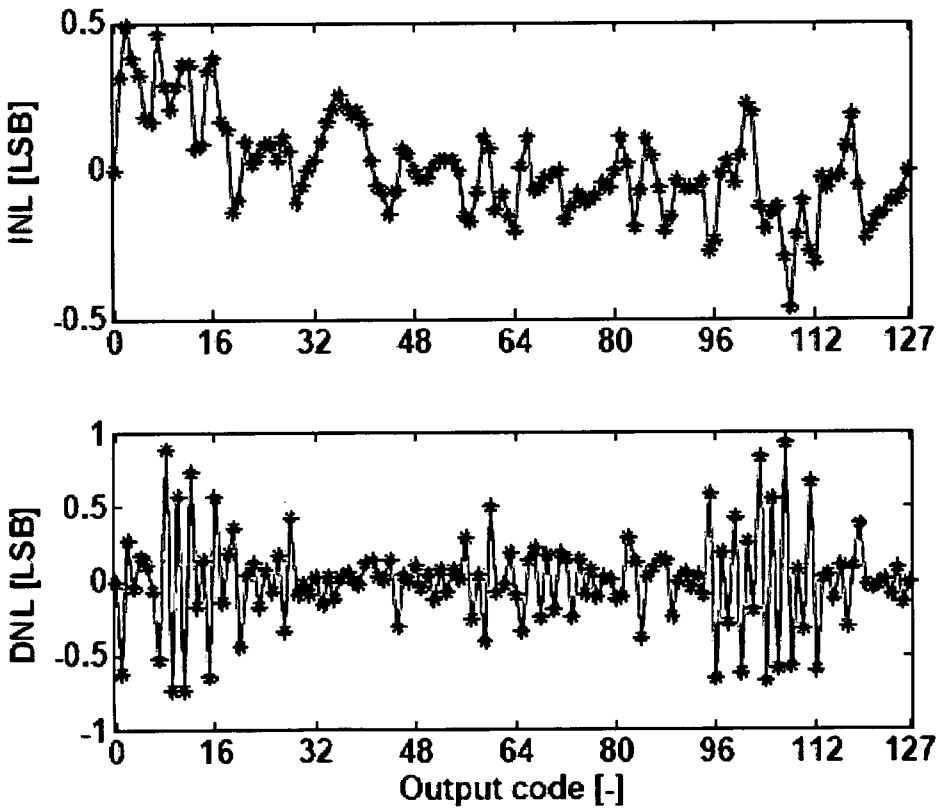

INL [LSB]
0.5
0
-0.5
0
16
32
48
64
80
96
112
127
DNL [LSB]
1
0.5
0
-0.5
-1
0
16
32
48
64
80
96
112
127
Output code [-]

Fig.8

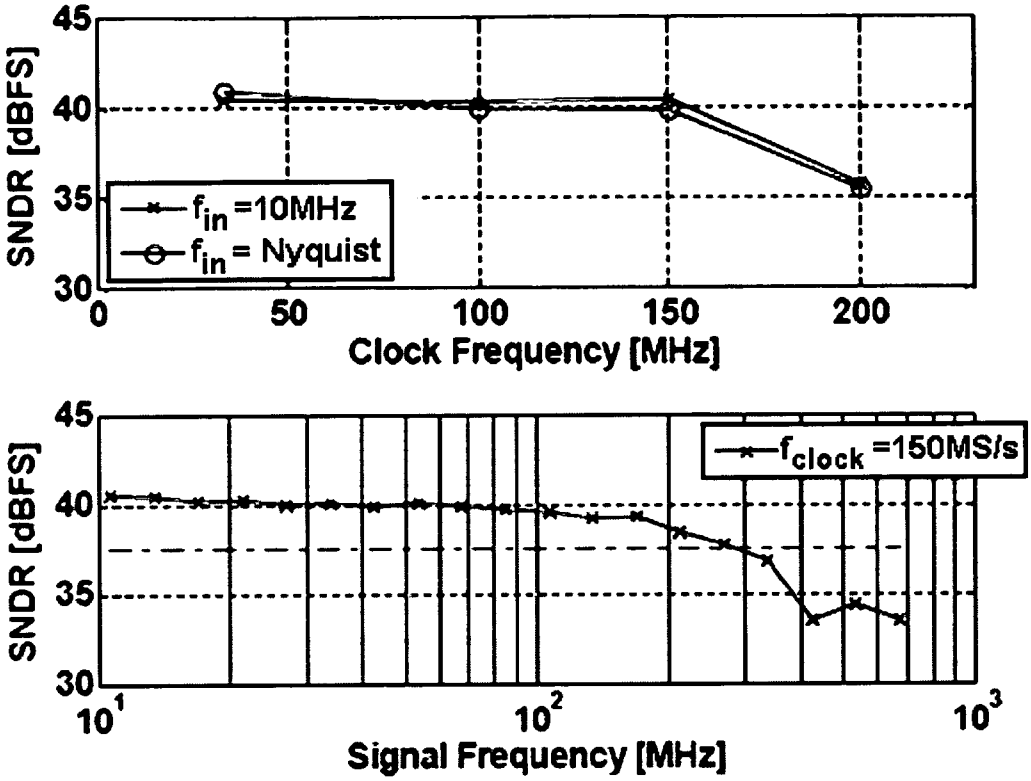

SNDR [dBFS]
45
40
35
30
0
50
100
150
200
Clock Frequency [MHz]
f_{in} =10MHz
f_{in} = Nyquist
SNDR [dBFS]
45
40
35
30
10^1
10^2
10^3
Signal Frequency [MHz]
f_{clock} =150MS/s

Fig.9

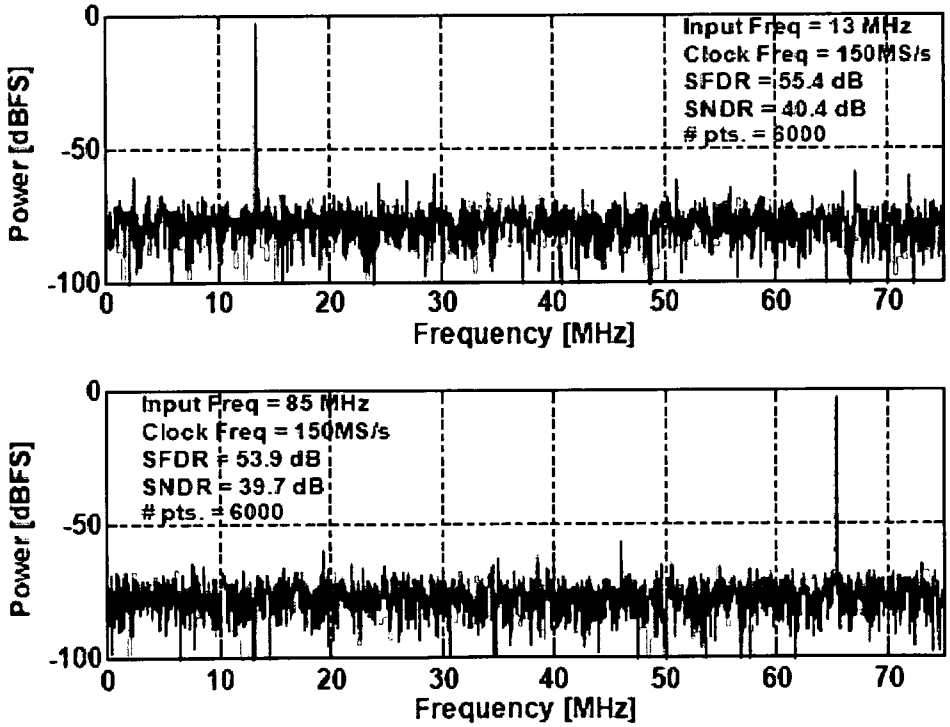

Power [dBFS]
0
-50
-100
0
10
20
30
40
50
60
70
Frequency [MHz]
Input Freq = 13 MHz
Clock Freq = 150MS/s
SFDR = 55.4 dB
SNDR = 40.4 dB
# pts. = 6000
Power [dBFS]
0
-50
-100
0
10
20
30
40
50
60
70
Frequency [MHz]
Input Freq = 85 MHz
Clock Freq = 150MS/s
SFDR = 53.9 dB
SNDR = 39.7 dB
# pts. = 6000

Fig.10

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/050723

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/36 H03M1/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 079 528 A (CIT ALCATEL [FR]) 28 February 2001 (2001-02-28) paragraphs [0019], [0024] - [0028], [0033] - [0037]	1-10
X	JUNGWOOK YANG ET AL: "A current boosting full-flash A/D converter" PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. SAN DIEGO, MAY 10 - 13, 1992; [PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCAS)], NEW YORK, IEEE, US, vol. 2, 3 May 1992 (1992-05-03), pages 609-612, XP010061262 ISBN: 978-0-7803-0593-9 pages 609-610; figures 1,2	1-3,5-7

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search	Date of mailing of the international search report
6 May 2009	18/05/2009

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/050723

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

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