(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 May 2013 (23.05.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/075007 A1

(51) International Patent Classification:
H01L 27/06 (2006.01)

(21) International Application Number:
PCT/US2012/065644

(22) International Filing Date:
16 November 2012 (16.11.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/560,471 16 November 2011 (16.11.2011) US
13/356,717 24 January 2012 (24.01.2012) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: STACKED CHIPSET HAVING AN INSULATING LAYER AND A SECONDARY LAYER AND METHOD OF FORMING SAME

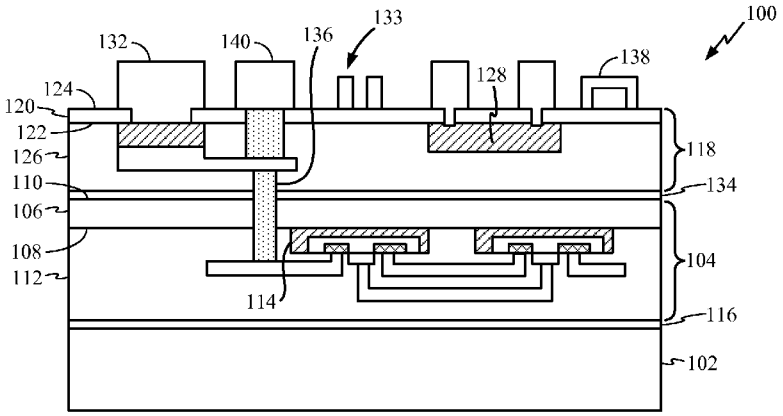

FIG. 1

(57) Abstract: A chipset (100) includes a sheet (102) of glass, quartz or sapphire and a first wafer (104) having at least one first circuit layer (112) on a first side (108) of a first substrate layer (106). The first wafer (104) is connected to the sheet (102) such that the at least one first circuit layer (112) is located between the first substrate layer (106) and the sheet (102). A second wafer (126) having at least one second circuit layer (126) on a first side (122) of a second substrate layer (120) is connected to the first substrate layer (106) such that the at least one second circuit layer (126) is located between the second substrate layer (120) and the first substrate layer (106). A method of forming a chipset is also disclosed.

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STACKED CHIPSET HAVING AN INSULATING LAYER AND A SECONDARY LAYER AND METHOD OF FORMING SAME

Claim of Priority under 35 U.S.C. §119

[0001] The present Application for Patent claims priority to U.S. Provisional Application No. 61/560,471, entitled "STACKED CMOS CHIPSET HAVING AN INSULATING LAYER AND A SECONDARY LAYER AND METHOD OF FORMING SAME", filed November 16, 2011, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

Field of Disclosure

[0002] The present application for patent is directed toward a chipset having a complementary metal oxide semiconductor (CMOS) layer bonded to an insulator and a second layer stacked on the CMOS layer, and toward a method of forming same, and, more specifically, toward a chipset including a CMOS layer bonded to an insulator and a second layer having passive elements, radio frequency (RF) circuitry or microelectromechanical system (MEMS) elements and toward a method of forming same.

Background

[0003] As cellular wireless systems evolve from 2G to 4G, there is increasing demand for radio frequency (RF) chipsets to support larger numbers of bands. Providing the chipsets with the ability to handle these additional bands may require adding additional transceivers, filters, power amplifiers, passive components and switches to the chipset front end, and this increases the cost and complexity of the chipsets. The RF system of a cellphone mainly consists of two parts: the transceiver, which is often a single complementary metal oxide semiconductor (CMOS) chip, and the RF front-end (including various on-board components: filters, duplexers, RF switches, power amplifiers and passives). While the CMOS transceiver can be designed to be shared by different bands or modes, generally called a multi-mode/multi-band transceiver design, the front-end part, especially the filters

and duplexers, cannot be shared between different bands, simply because they operate in different frequency range. The presence of these additional elements to support more bands/modes may cause the front end to become a limiting factor when attempting to increase performance and reduce size and cost.

[0004] Conventional multi-band and/or multi-mode RF chipset front ends may include devices such as RF switches, power amplifiers, acoustic filters and passives, e.g., inductors and capacitors. While the CMOS chip elements generally may scale continuously, resulting in lower cost and smaller size with new technological advances, the front end does not always scale as readily. One approach to this situation has been to integrate multiple chips, e.g., GaAs antenna switches, GaAs power amplifiers, CMOS controllers, surface acoustic wave (SAW) filters, integrated passive devices, etc. onto a single laminate or ceramic substrate. This approach may be referred to as a "system-in-package" solution for front-end integration. There is also interest in addressing the multi-band complexity problem at a system architecture level by introducing a tunable front end. To realize a low-loss multi-band tunable system, a way must be found to implement high-Q tunable passives, such as semiconductor varactors and MEMS-based tunable capacitors, and high-performance RF switches into a single arrangement. Front end integration may also be useful for reducing the overall size and cost of multiband and/or multi-mode RF transceiver chipsets. It would therefore be desirable to provide a chipset that integrates CMOS components with other front end components in a space- and cost-effective manner.

SUMMARY

[0005] An exemplary embodiment includes a chipset comprising a sheet of glass, quartz or sapphire, and a first wafer having at least one first circuit layer on a first side of a first substrate layer. The first wafer is connected to the sheet such that the at least one first circuit layer is located between the first substrate layer and the sheet. The chipset also includes a second wafer having at least one second circuit layer on a first side of a second substrate layer, and the second wafer is connected to the first substrate layer such that the at least one second circuit layer is located between the second substrate layer and the first substrate layer.

[0006] Another embodiment is a method of forming a chipset that includes providing a first wafer comprising a first silicon substrate and at least one first circuit layer on the first silicon substrate, connecting the at least one first circuit layer to a sheet of glass, quartz or sapphire and then removing a portion of the first silicon substrate. The method also includes providing a second wafer comprising a second silicon substrate and at least one second circuit layer on the second substrate, connecting the at least one second circuit layer to the first silicon substrate and then removing a portion of the second silicon substrate.

[0007] A further embodiment includes a chipset having insulator sheet means for supporting a wafer and a first wafer comprising at least one first circuit means for processing signals on a first side of a first substrate layer, where the first wafer is connected to the insulator sheet means such that the at least one first circuit means is located between the first substrate layer and the insulator sheet means. The chipset further includes a second wafer comprising at least one second circuit means for processing signals on a first side of a second substrate layer, and where the second wafer is connected to the first substrate layer such that the at least one second circuit layer is located between the second substrate layer and the first substrate layer.

[0008] Another embodiment is a method of forming a chipset that includes steps for providing a first wafer comprising a first silicon substrate and at least one first circuit layer on the first silicon substrate, steps for connecting the at least one first circuit layer to a sheet of glass, quartz or sapphire, steps for then removing a portion of the first silicon substrate, steps for providing a second wafer comprising a second silicon substrate and at least one second circuit layer on the second substrate, steps for connecting the at least one second circuit layer to the first silicon substrate and steps for then removing a portion of the second silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings are presented to aid in the description of embodiments of the invention and are provided solely for illustration of the embodiments and not limitation thereof.

[0010] FIG. 1 is a schematic side elevational view of a chipset according to an

embodiment.

[0011] FIGS. 2-7 are schematic side elevational views of stock material and components of the chipset of FIG. 1 showing assembly stages of a method for producing the chipset of FIG. 1.

[0012] FIG. 8 is a schematic side elevational view of a chipset according to another embodiment.

DETAILED DESCRIPTION

[0013] Aspects of the invention are disclosed in the following description and related drawings directed to specific embodiments of the invention. Alternate embodiments may be devised without departing from the scope of the invention. Additionally, well-known elements of the invention will not be described in detail or will be omitted so as not to obscure the relevant details of the invention.

[0014] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments. Likewise, the term “embodiments of the invention” does not require that all embodiments of the invention include the discussed feature, advantage or mode of operation.

[0015] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of embodiments of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises", "comprising,", "includes" and/or "including", when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0016] Further, many embodiments are described in terms of sequences of actions to be performed by, for example, elements of a computing device. It will be recognized that various actions described herein can be performed by specific circuits (e.g., application specific integrated circuits (ASICs)), by program instructions being executed by one or

more processors, or by a combination of both. Additionally, these sequence of actions described herein can be considered to be embodied entirely within any form of computer readable storage medium having stored therein a corresponding set of computer instructions that upon execution would cause an associated processor to perform the functionality described herein. Thus, the various aspects of the invention may be embodied in a number of different forms, all of which have been contemplated to be within the scope of the claimed subject matter. In addition, for each of the embodiments described herein, the corresponding form of any such embodiments may be described herein as, for example, "logic configured to" perform the described action.

[0017] Figure 1 illustrates a chipset 100 according to an embodiment. The chipset 100 includes a sheet 102 formed from an insulator such as glass, quartz or sapphire to which a first silicon-on-insulator (SOI) wafer 104 is bonded. The first SOI wafer 104 includes a first substrate layer or first insulating layer 106 having a first side 108 facing the sheet 102 and a second side 110, and the first SOI wafer 104 also includes a first circuit layer 112, which first circuit layer 112 includes a plurality of CMOS transistors 114 on the first side 108 of the first insulating layer 106 and associated wiring. These CMOS transistors 114 and other circuit elements (not illustrated) may comprise circuitry for digital signal processing, application or graphics processors, and/or circuitry for handing baseband signals. The first SOI wafer 104 is bonded to the sheet 102 using a first adhesive layer 116 or other conventional wafer bonding techniques such that the first circuit layer 112 is located between the first side 108 of the first insulating layer 106 of the first SOI wafer 104 and the sheet 102.

[0018] A second SOI wafer 118 is connected to the first SOI wafer 104. The second SOI wafer 118 includes a second substrate layer or second insulating layer 120 having a first side 122 facing the second side 110 of the first insulating layer 106 and a second side 124. The second SOI wafer 118 also includes a second circuit layer 126, which second circuit layer 126 includes passive elements or "passives" such as a resistor 128 and a capacitor 132 located partially or entirely within the second circuit layer 126 and an inductor 133 and a MEMS device or sensor 138 located on the second side 124 of the second insulating layer 120. A single resistor 128, capacitor 132, inductor 133 and MEMS device 138 are

illustrated in Figure 1; however, the second SOI wafer 118 may, in some cases, only include one or two of these component types and/or include multiple ones of these individual components (including active circuitry like CMOS transistors). The second SOI wafer 118 is bonded to the second side 110 of the first insulating layer 106 using a second adhesive layer 134 such that the second circuit layer 126 is located between the first side 122 of the second insulating layer 120 and the second side 110 of the first insulating layer 106. Vias 136 electrically connect elements of the second circuit layer 126 to elements of the first circuit layer 112, and suitable metal contacts 140 may be connected at the second side 124 of the second insulating layer 120 to electrically connect elements in or on the second circuit layer 126 and/or the first circuit layer 112 to devices outside the chipset 100.

[0019] If a similar chipset were constructed on a high-resistivity Silicon (Si) substrate with buried oxide (as the case in SOI CMOS technology) instead of on the sheet 102 formed from a pure insulator like sapphire, quartz or glass, nonlinear parasitic capacitances would be produced at the interface between the high-resistivity Si and buried SiO_2 in the SOI substrate at RF frequencies. These parasitic capacitances result in nonlinearities and power handling issues for RF switches and power amplifiers. The use of the sheet 102 as described herein substantially eliminates the nonlinear-parasitic-capacitance problem and allows CMOS elements such as the CMOS transistors 114 and the passives, which may comprise high-Q passives, to be used together in the same chipset 100 with much better performance than on SOI wafers.

[0020] Various manufacturing stages of the chipset 100 are illustrated in Figures 2-7, and elements present in the chipset 100 and discussed in Figure 1 are identified by the same reference numerals in Figures 2-7. Figure 2 illustrates a first stock SOI wafer 202 that includes a first silicon substrate or handle layer 204 on which the first insulating layer 106 and the first circuit layer 112 are formed. The first stock SOI wafer 202 may comprise a conventional bulk Silicon CMOS wafer to help reduce costs, and in this case, the first substrate layer 106 would not comprise an insulator but instead would be the portion of the bulk Silicon located immediately beneath the elements of the first circuit layer 112.

[0021] Figure 3 shows the first stock SOI wafer 202 inverted and bonded to the sheet 102 by the first adhesive layer 116 with the first side 108 of the first insulating layer 106 facing

the sheet 102, and Figure 4 shows a first component 302 formed by the removal of the first silicon handle layer 204, for example, by chemical mechanical polishing (CMP) or other suitable process for selectively removing a desired amount of the first silicon handle layer 204. Figure 5 illustrates a second stock SOI wafer 502 that comprises a second silicon substrate or handle layer 504 on which the second insulating layer 120 and the second circuit layer 126 are formed. Figure 6 shows the second stock SOI wafer 502 inverted and attached to the first component 302 with the second circuit layer 126 of the second stock SOI wafer 502 bonded to the first insulating layer 106 by the second adhesive layer 134. Figure 7 shows a second component 702 comprising the combination of the second stock SOI wafer 502 and the first component 302 with the second silicon handle layer 504 of the second stock SOI wafer 502 removed by CMP or other suitable process. The vias 136 are also formed in the second component 702, and the addition of the metal contacts 140 and other Back-End-of-the-Line (BEOL) components (including passives, MEMS, sensors and other) results in the chipset 100 of Figure 1.

[0022] Figure 8 illustrates another embodiment in which elements common to the first embodiment are identified with like reference numerals. Figure 8 illustrates a second chipset 800 that includes the sheet 102, the first SOI wafer 104 and the second SOI wafer 118 with the first SOI wafer 104 and the second SOI wafer 118 spaced apart by a third SOI wafer 802. The third SOI wafer 802 comprises a third substrate layer or insulating layer 804 having a first side 806 and a second side 808, and a third circuit layer 810 comprising a plurality of circuit element on the first side 806 of the third insulating layer 804, which circuit elements may include analog circuitry 814 and/or RF components 816. The third SOI wafer 802 is attached to the second side 110 of the first SOI wafer 104 with a second adhesive layer 818 so that the first side 806 of the third SOI wafer 802 faces the second side 110 of the first SOI wafer 104. The second SOI wafer 118 is attached to the second side 808 of the third SOI wafer 802 by a third adhesive layer 820 such that the first side of the second SOI wafer 118 faces the second side 808 of the third SOI wafer 802. All three of the first SOI wafer 104, the second SOI wafer 118 and the third SOI wafer 802 have substantially the same surface areas. Vias 822 connect circuit components of the first circuit layer 112, the second circuit layer 126 and the third circuit layer 810, and metal

contacts 140 provides connections to elements outside the second chipset 800. This arrangement allows for the analog circuitry 814 and/or the RF components 816 to be included in the same chipset as the digital circuit elements 114 and the passives, such as capacitor 132 and provides a vertically integrated chipset that performs many conventional functions in a compact package.

[0023] While the sheet 102 has been described as comprising glass, sapphire or quartz, the use of glass for the sheet 102 may be particularly beneficial in some situations. First, it generally has a lower cost than sapphire or quartz. Next, it also has a much lower dielectric constant than sapphire, which significantly reduces the parasitic capacitance from the substrate. Finally, the wafer/panel size of glass can be much larger than sapphire and quartz, and this may allow for larger scale mass production and lower unit cost.

[0024] The chipsets of the disclosed embodiments may be integrated into one or more semiconductor dies or integrated into a device such as a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer.

[0025] The methods, sequences and/or algorithms described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor.

[0026] While the foregoing disclosure shows illustrative embodiments of the invention, it should be noted that various changes and modifications could be made herein without departing from the scope of the invention as defined by the appended claims. The functions, steps and/or actions of the method claims in accordance with the embodiments of the invention described herein need not be performed in any particular order. Furthermore, although elements of the invention may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

CLAIMS

What is claimed is:

1. A chipset comprising:

a sheet of glass, quartz or sapphire;

a first wafer comprising at least one first circuit layer on a first side of a first substrate layer, the first wafer being connected to the sheet such that the at least one first circuit layer is located between the first substrate layer and the sheet; and

a second wafer comprising at least one second circuit layer on a first side of a second substrate layer, the second wafer being connected to the first substrate layer such that the at least one second circuit layer is located between the second substrate layer and the first substrate layer.

2. The chipset of claim 1, wherein the first substrate layer comprises a first insulating layer and wherein the second substrate layer comprises a second insulating layer.

3. The chipset of claim 2 wherein the first wafer and the second wafer each comprise a silicon-on-insulator (SOI) wafer.

4. The chipset of claim 3, wherein the at least one first circuit layer comprises a plurality of CMOS transistors.

5. The chipset of claim 3, wherein the at least one second circuit layer comprises or supports at least one passive circuit element.

6. The chipset of claim 3, wherein the at least one second circuit layer comprises or supports at least one microelectromechanical (MEMS) element.

7. The chipset of claim 3, wherein the at least one second circuit layer comprises or supports at least one sensor.

8. The chipset of claim 3, wherein the first SOI wafer is bonded directly to the sheet.

9. The chipset of claim 3, wherein the second SOI wafer is bonded directly to the first SOI wafer.

10. The chipset of claim 3 integrated into at least one semiconductor die.

11. The chipset of claim 3 integrated into a device selected from the group consisting of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer.

12. The chipset of claim 3,

wherein the at least one first circuit layer comprises a plurality of CMOS transistors,

wherein the at least one second circuit layer comprises or supports at least one passive component or at least one MEMS element,

wherein the first SOI wafer is bonded directly to the sheet, and

wherein the second SOI wafer is bonded directly to the first insulating layer.

13. The chipset of claim 3, including a third wafer comprising SOI and having at least one third circuit layer on a first side of a third insulating layer, the third wafer being connected to the first wafer such that the at least one third circuit layer is located between the first insulating layer and the second insulating layer.

14. The chipset of claim 13, wherein the at least one third circuit layer comprises CMOS transistors.

15. The chipset of claim 13, wherein the second wafer is bonded directly to the

third wafer such that the at least one second circuit layer is located between the second insulating layer and the third insulating layer.

16. The chipset of claim 13, wherein the at least one first circuit layer includes a digital circuit and the at least one third circuit layer includes an analog circuit.

17. The chipset of claim 13, wherein the at least one first circuit layer includes a digital circuit, the at least one second circuit layer includes or supports a passive device or a MEMS element and the at least one third circuit layer includes an analog or RF circuit.

18. The chipset of claim 13, wherein a surface area of the first substrate layer is substantially equal to a surface area of the second substrate layer, and the surface area of the second substrate layer is substantially equal to a surface area of the third substrate layer.

19. A method of forming a chipset comprising:

providing a first wafer comprising a first silicon substrate and at least one first circuit layer on the first silicon substrate;

connecting the at least one first circuit layer to a sheet of glass, quartz or sapphire and then removing a portion of the first silicon substrate;

providing a second wafer comprising a second silicon substrate and at least one second circuit layer on the second silicon substrate; and

connecting the at least one second circuit layer to the first silicon substrate and then removing a portion of the second silicon substrate.

20. The method of claim 19, including providing an insulating layer between the first silicon substrate and the second silicon substrate.

21. The method of claim 20, wherein connecting the at least one second circuit layer to the first silicon substrate comprises bonding the at least one second circuit layer directly to the insulating layer.

22. The method of claim 19, wherein the first silicon substrate includes a first insulating layer, a first body of silicon is located on a first side of the first insulating layer and the at least one first circuit layer is located on a second side of the first insulating layer and removing a portion of the first silicon substrate comprises removing the first body of silicon, and

wherein the second silicon substrate includes a second insulating layer, a second body of silicon is located on a first side of the second insulating layer and the at least one second circuit layer is located on a second side of the second insulating layer and removing a portion of the second silicon substrate comprises removing the second body of silicon.

23. The method of claim 19, including providing a first insulating layer between the first silicon substrate and the second silicon substrate, wherein the second silicon substrate include a second insulating layer, wherein a body of silicon is located on a first side of the second insulating layer and the at least one second circuit layer is located on a second side of the second insulating layer and wherein removing a portion of the second silicon substrate comprises removing the body of silicon.

24. The method of claim 23, including forming a via extending through the first insulating layer and electrically connecting a portion of the at least one first circuit layer to a portion of the at least one second circuit layer.

25. The method of claim 23, wherein the at least one first circuit layer comprises a plurality of CMOS transistors.

26. The method of claim 23, wherein the at least one second circuit layer comprises at least one passive component.

27. The method of claim 23, wherein the at least one second circuit layer comprises at least one analog/RF component.

28. The method of claim 23, wherein the at least one second circuit layer comprises at least one microelectromechanical (MEMS) or sensor component.

29. The method of claim 23, wherein connecting the at least one first circuit layer to a sheet of glass, quartz or sapphire comprises bonding the at least one first circuit layer directly to the sheet of glass, quartz or sapphire.

30. The method of claim 19, including providing a third wafer comprising a third silicon substrate and at least one third circuit layer on the third silicon substrate, connecting the at least one third circuit layer to the second silicon substrate and then removing a portion of the third silicon substrate.

31. The method of claim 30 wherein the first silicon substrate includes a first insulating layer, a first body of silicon is located on a first side of the first insulating layer and the at least one first circuit layer is located on a second side of the first insulating layer and removing a portion of the first silicon substrate comprises removing the first body of silicon,

wherein the second silicon substrate includes a second insulating layer, a second body of silicon is located on a first side of the second insulating layer and the at least one second circuit layer is located on a second side of the second insulating layer and removing a portion of the second silicon substrate comprises removing the second body of silicon, and

wherein the third silicon substrate includes a third insulating layer, a third body of silicon is located on a first side of the third insulating layer and the at least one third circuit layer is located on a second side of the third insulating layer and removing a portion of the third silicon substrate comprises removing the third body of silicon.

32. The method of claim 31,

wherein connecting the at least one third circuit layer to the second insulating layer

comprises bonding the at least one third circuit layer directly to the second insulating layer.

33. The method of claim 31,

wherein the at least one first circuit layer comprises a plurality of CMOS transistors for a digital circuit,

wherein the at least one second circuit layer comprises a plurality of CMOS transistors for an analog or RF circuit, and

wherein the at least one third circuit layer comprises or supports at least one passive component or at least one MEMS or sensor element.

34. The method of claim 31, wherein a surface area of the first insulating layer is substantially equal to a surface area of the second insulating layer, and the surface area of the second insulating layer is substantially equal to a surface area of the third insulating layer.

35. The method of claim 19 including integrating the first wafer and the second wafer into at least one semiconductor die.

36. The method of claim 19 including integrating first wafer and the second wafer into a device selected from the group consisting of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer.

37. A chipset comprising:

insulator sheet means for supporting a wafer;

a first wafer comprising at least one first circuit means for processing signals on a first side of a first substrate layer, the first wafer being connected to the insulator sheet means such that the at least one first circuit means is located between the first substrate layer and the insulator sheet means; and

a second wafer comprising at least one second circuit means for processing signals

on a first side of a second substrate layer, the second wafer being connected to the first substrate layer such that the at least one second circuit means is located between the second substrate layer and the first substrate layer.

38. The chipset of claim 37, wherein the first substrate layer comprises first insulating layer means for insulating the at least one first circuit means from the second wafer.

39. The chipset of claim 37 wherein the first wafer and the second wafer each comprise a silicon-on-insulator (SOI) wafer.

40. The chipset of claim 37, wherein the at least one first circuit means comprises a plurality of CMOS transistors.

41. The chipset of claim 37, wherein the at least one second circuit means comprises or supports at least one passive circuit element.

42. The chipset of claim 37, wherein the at least one second circuit means comprises or supports at least one microelectromechanical (MEMS) element or at least one sensor.

43. The chipset of claim 37 integrated into at least one semiconductor die.

44. The chipset of claim 37 integrated into a device selected from the group consisting of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer.

45. The chipset of claim 37,

wherein the at least one first circuit means comprises a plurality of CMOS

transistors,

wherein the at least one second circuit means comprises or supports at least one passive component or at least one MEMS element,

wherein the first wafer is bonded directly to the insulator sheet means, and

wherein the second wafer is bonded directly to the first substrate layer.

46. The chipset of claim 37 wherein the insulator sheet means comprises a sheet of glass or a sheet of quartz or a sheet of sapphire.

47. A method of forming a chipset comprising:

steps for providing a first wafer comprising a first silicon substrate and at least one first circuit layer on the first silicon substrate;

steps for connecting the at least one first circuit layer to a sheet of glass, quartz or sapphire and steps for then removing a portion of the first silicon substrate;

steps for providing a second wafer comprising a second silicon substrate and at least one second circuit layer on the second silicon substrate; and

steps for connecting the at least one second circuit layer to the first silicon substrate and steps for then removing a portion of the second silicon substrate.

48. The method of claim 47, including steps for providing an insulating layer between the first silicon substrate and the second silicon substrate.

49. The method of claim 47, wherein the first silicon substrate includes a first insulating layer, a first body of silicon is located on a first side of the first insulating layer and the at least one first circuit layer is located on a second side of the first insulating layer and removing a portion of the first silicon substrate comprises steps for removing the first body of silicon, and

wherein the second silicon substrate includes a second insulating layer, a second body of silicon is located on a first side of the second insulating layer and the at least one second circuit layer is located on a second side of the second insulating layer and removing

a portion of the second silicon substrate comprises steps for removing the second body of silicon.

50. The method of claim 47, wherein the at least one second circuit layer comprises at least one passive component.

51. The method of claim 47, including steps for providing a third wafer comprising a third silicon substrate and at least one third circuit layer on the third silicon substrate, steps for connecting the at least one third circuit layer to the second silicon substrate and steps for then removing a portion of the third silicon substrate.

52. The method of claim 47 wherein the first silicon substrate includes a first insulating layer, a first body of silicon is located on a first side of the first insulating layer and the at least one first circuit layer is located on a second side of the first insulating layer and removing a portion of the first silicon substrate comprises steps for removing the first body of silicon,

wherein the second silicon substrate includes a second insulating layer, a second body of silicon is located on a first side of the second insulating layer and the at least one second circuit layer is located on a second side of the second insulating layer and removing a portion of the second silicon substrate comprises steps for removing the second body of silicon, and

wherein the third silicon substrate includes a third insulating layer, a third body of silicon is located on a first side of the third insulating layer and the at least one third circuit layer is located on a second side of the third insulating layer and removing a portion of the third silicon substrate comprises steps for removing the third body of silicon.

53. The method of claim 47 including steps for integrating the first wafer and the second SOI wafer into at least one semiconductor die.

54. The method of claim 47 including steps for integrating first wafer and the

second SOI wafer into a device selected from the group consisting of a set top box, a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant (PDA), a fixed location data unit, and a computer.

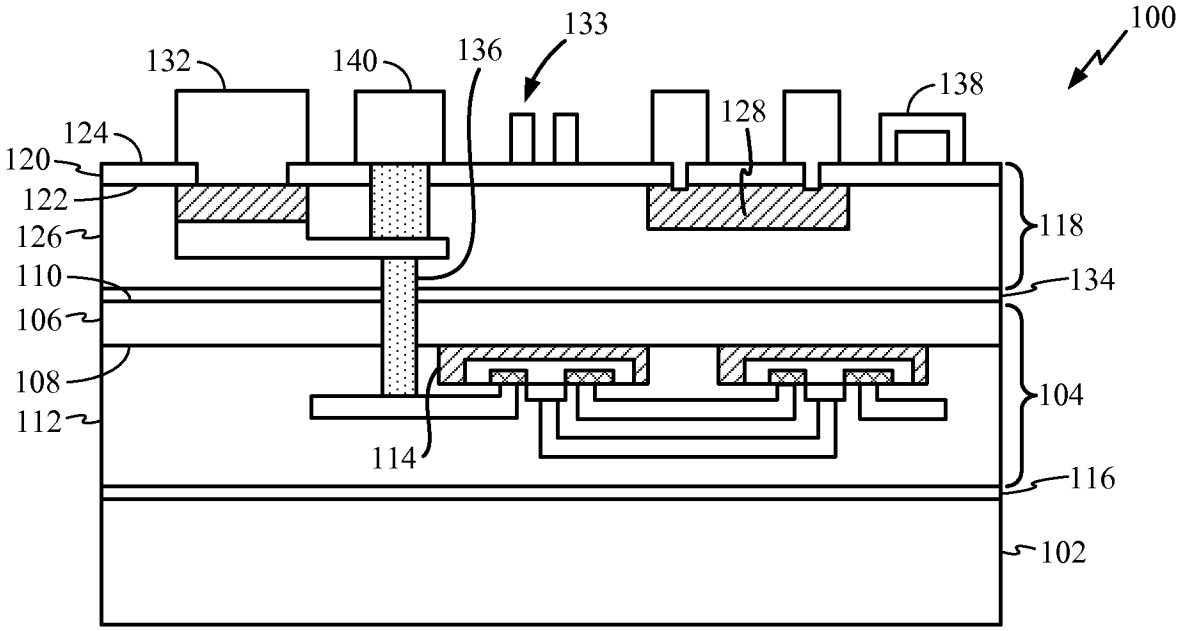
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FIG. 1

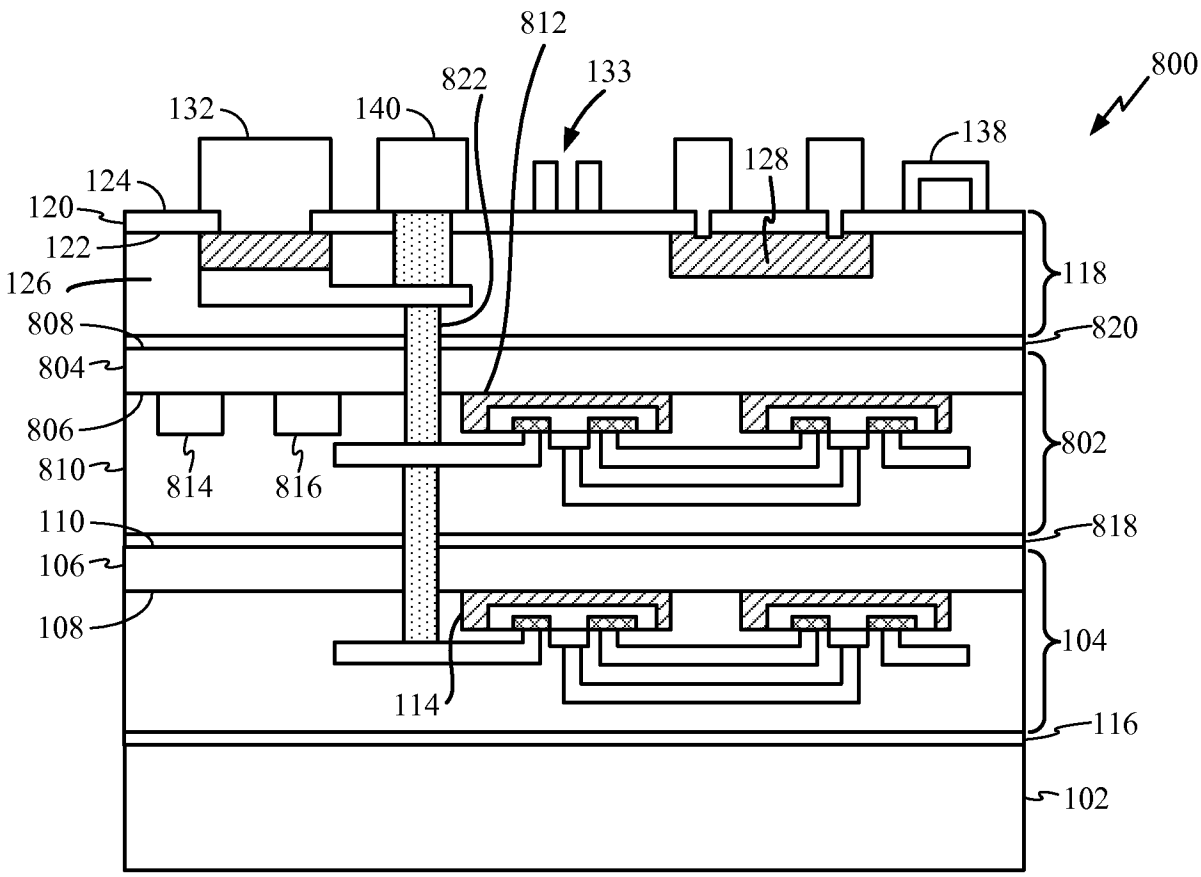
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FIG. 8

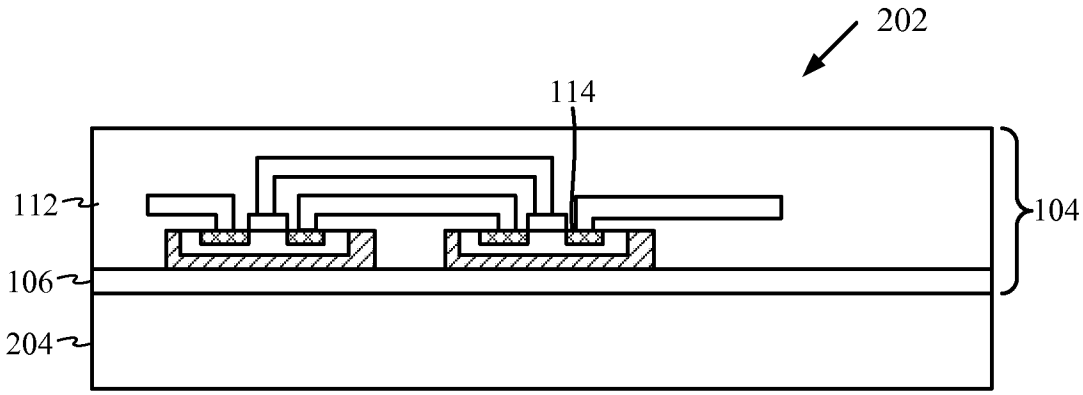

FIG. 2

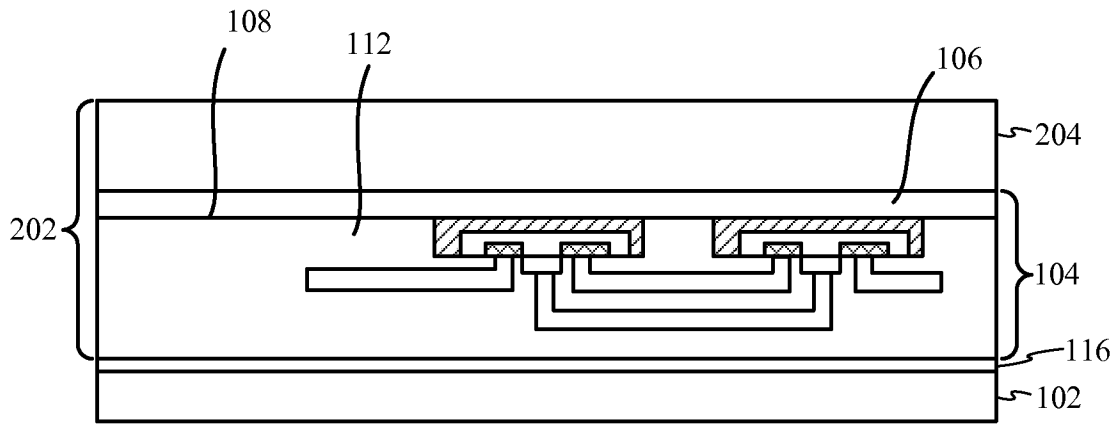

FIG. 3

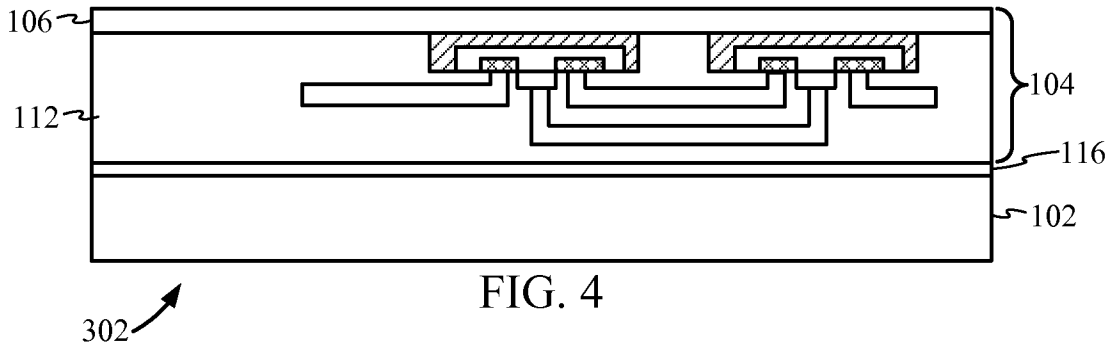

FIG. 4

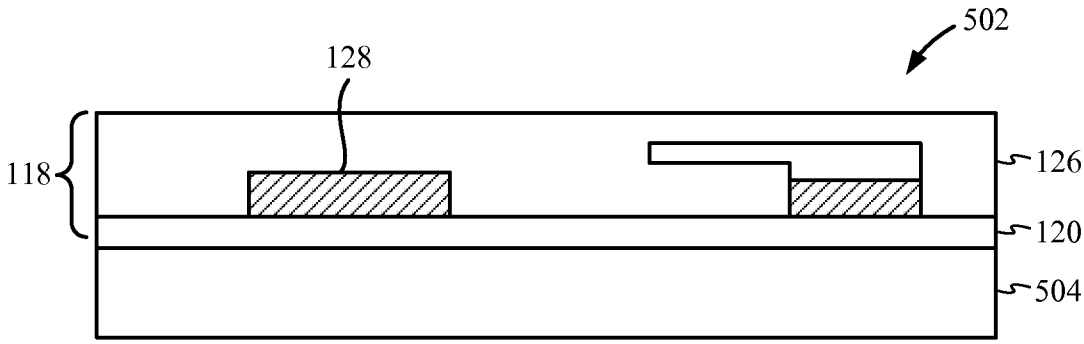

FIG. 5

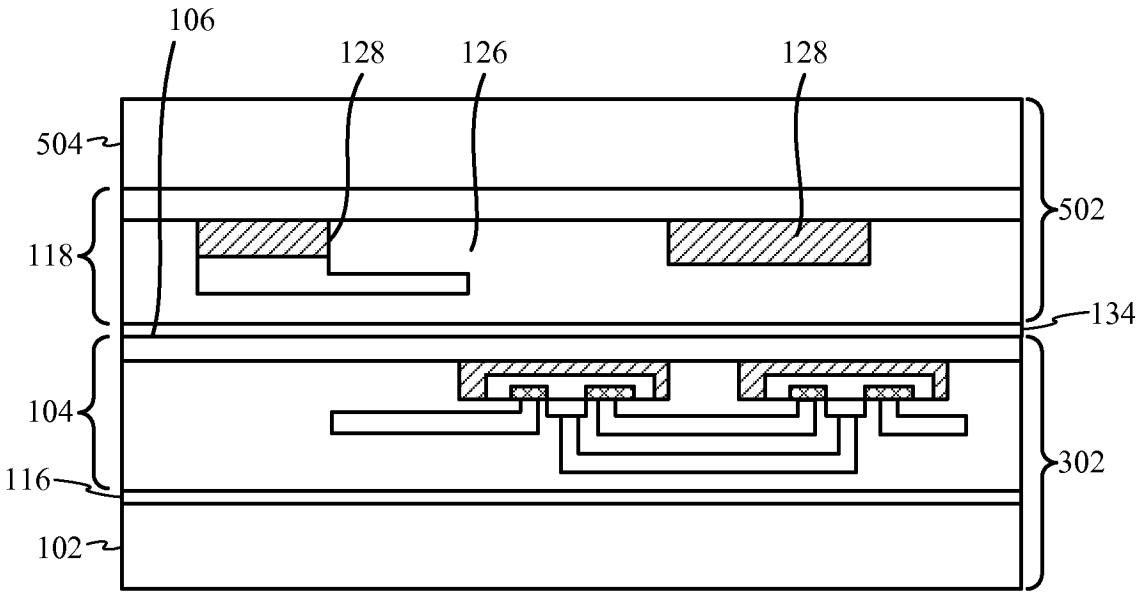

FIG. 6

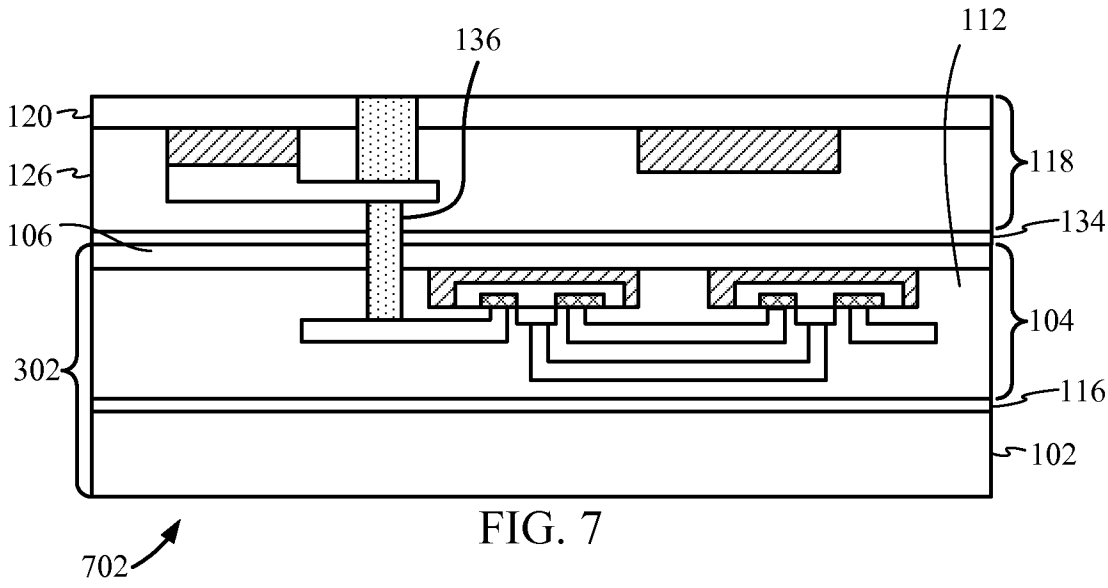

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/065644

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/149023 A1 (KOYANAGI MITSUMASA [JP]) 11 June 2009 (2009-06-11) paragraphs [0014], [0033], [0034], [0114], [0115], [0121], [0123], [0136], [0143]; figures 1-7,15,16	1-54
X	US 2007/207592 A1 (LU JAMES J [US] ET AL) 6 September 2007 (2007-09-06) paragraphs [0016], [0019], [0032], [0042], [0043], [0054], [0059]; figures 5-17,19,20	1-54
X	US 2005/023656 A1 (LEEDY GLENN J [US]) 3 February 2005 (2005-02-03) paragraphs [0081], [0085], [0441] - [0445], [0450] - [0452], [0460]; figure 2	1-23, 25-54

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 January 2013	31/01/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Seck, Martin

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/065644

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2012/065644

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