Jan. 9, 1968 D. PETZOLD 3,363,233

DIGITAL COMPARISON ELEMENT

Original Filed April 17, 1964 13 Sheets-Sheet 1

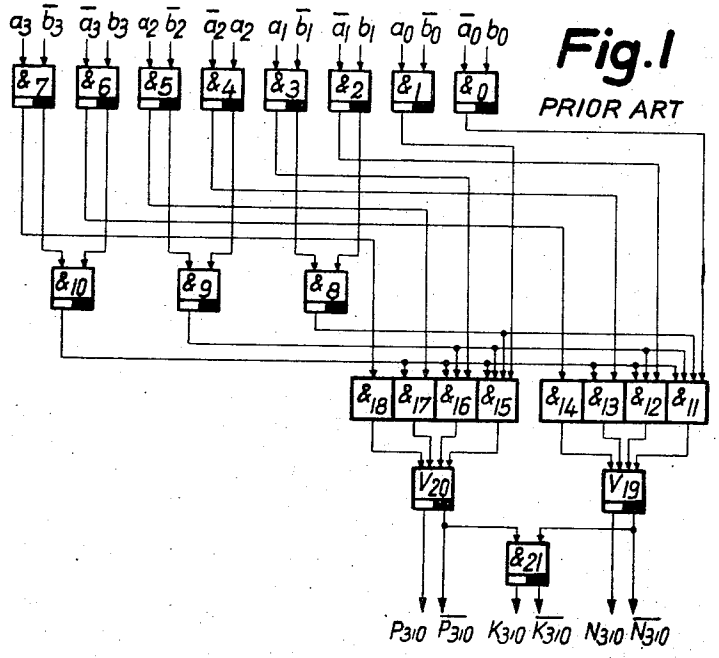

Fig.1
PRIOR ART

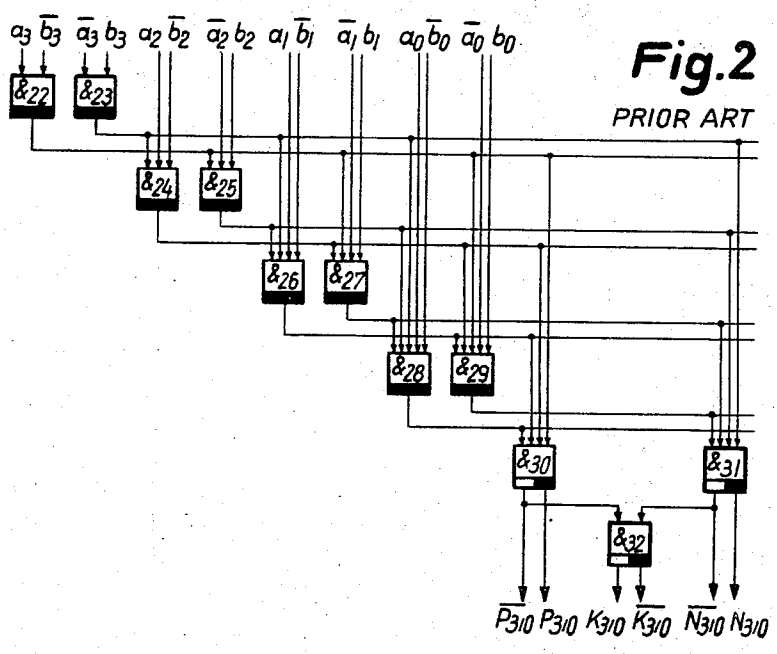

Fig.2
PRIOR ART

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Fig.3

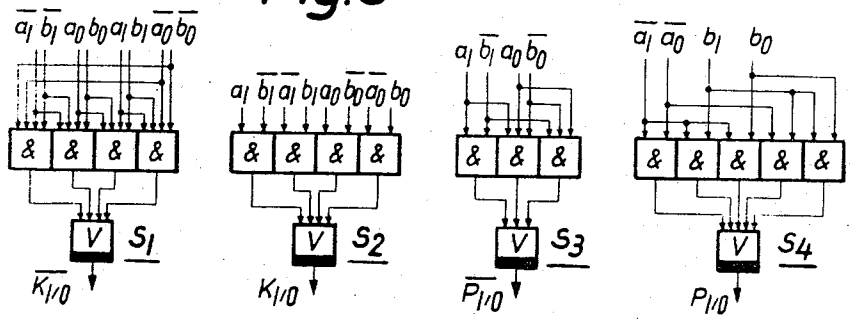
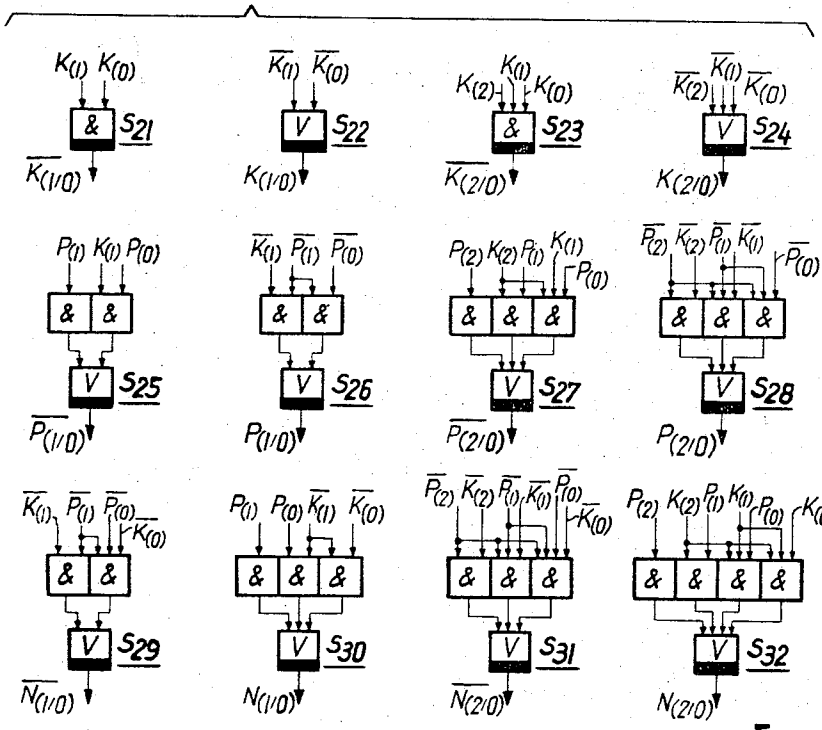


Fig.6



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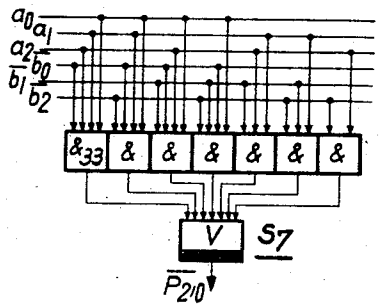

Fig.4

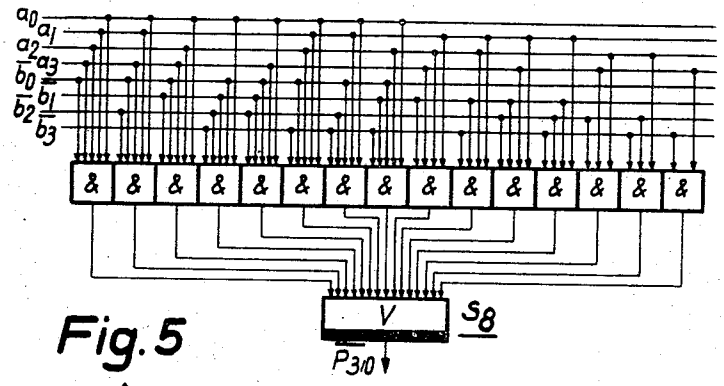

Fig.5

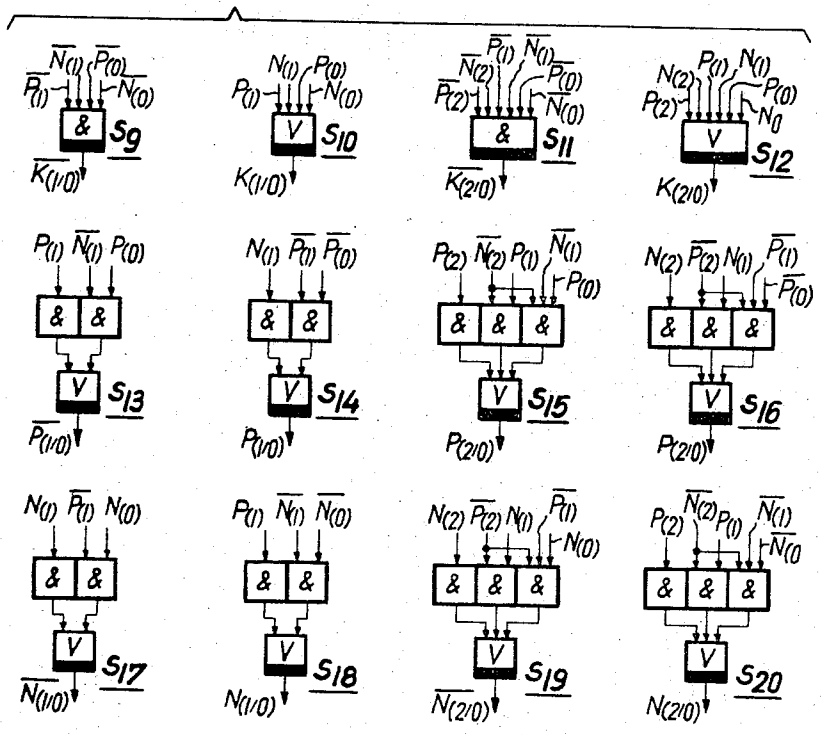

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Fig.7

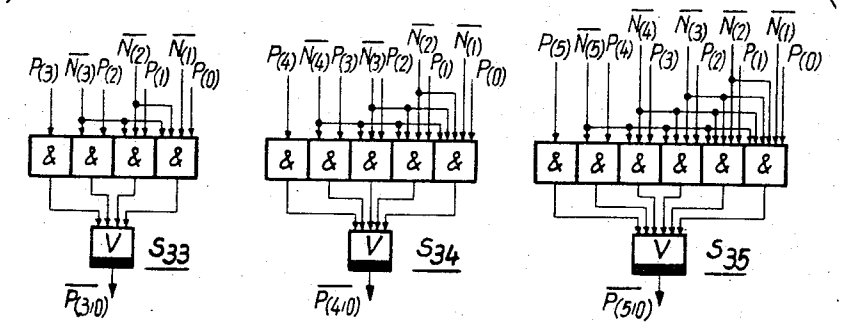

Fig.8

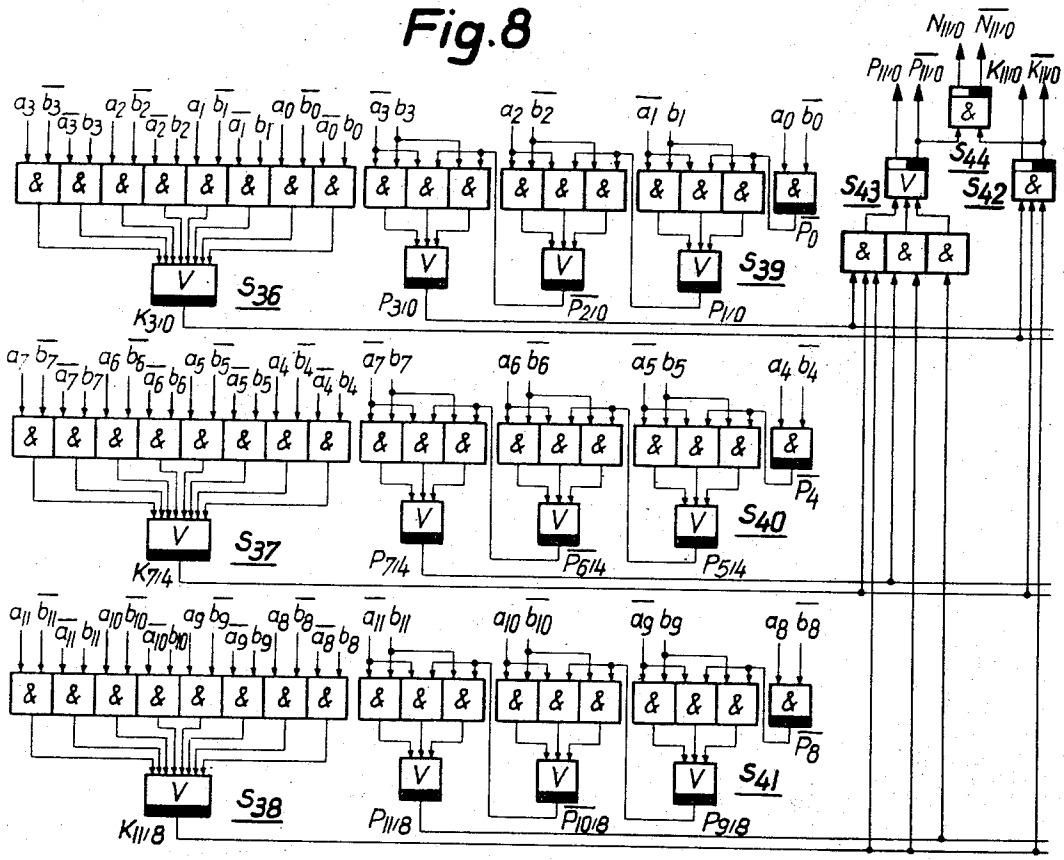

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Fig.9

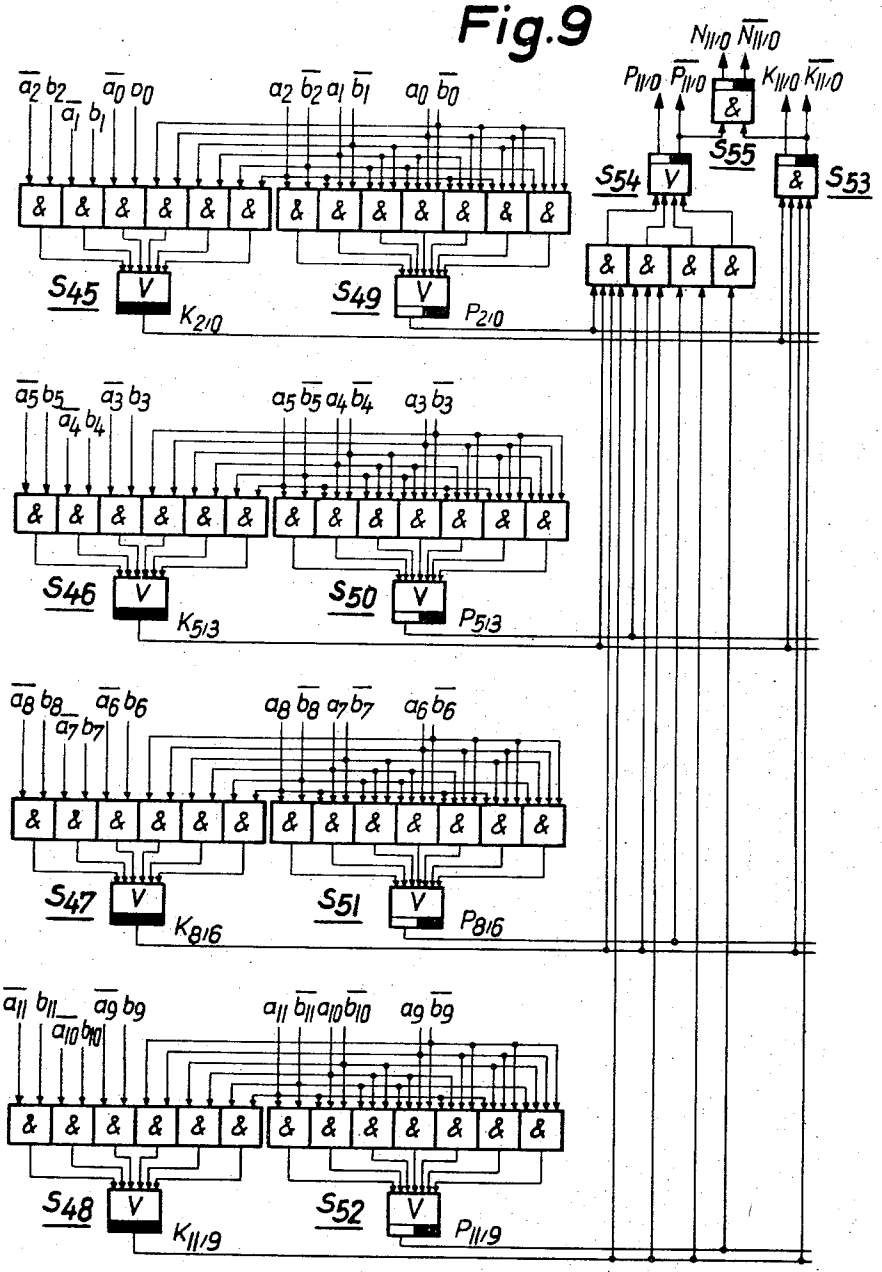

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Fig. 10

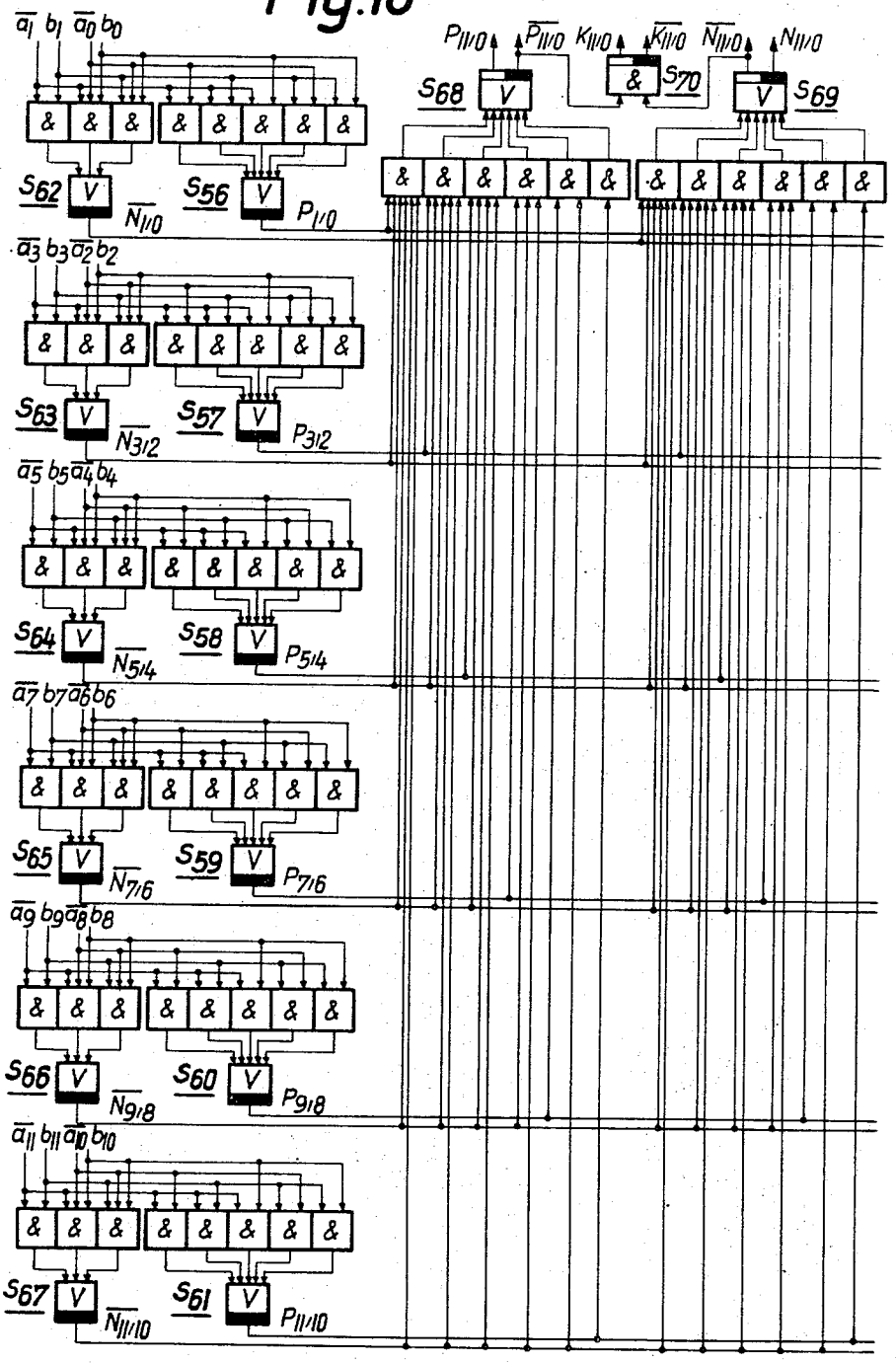

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Fig. 11

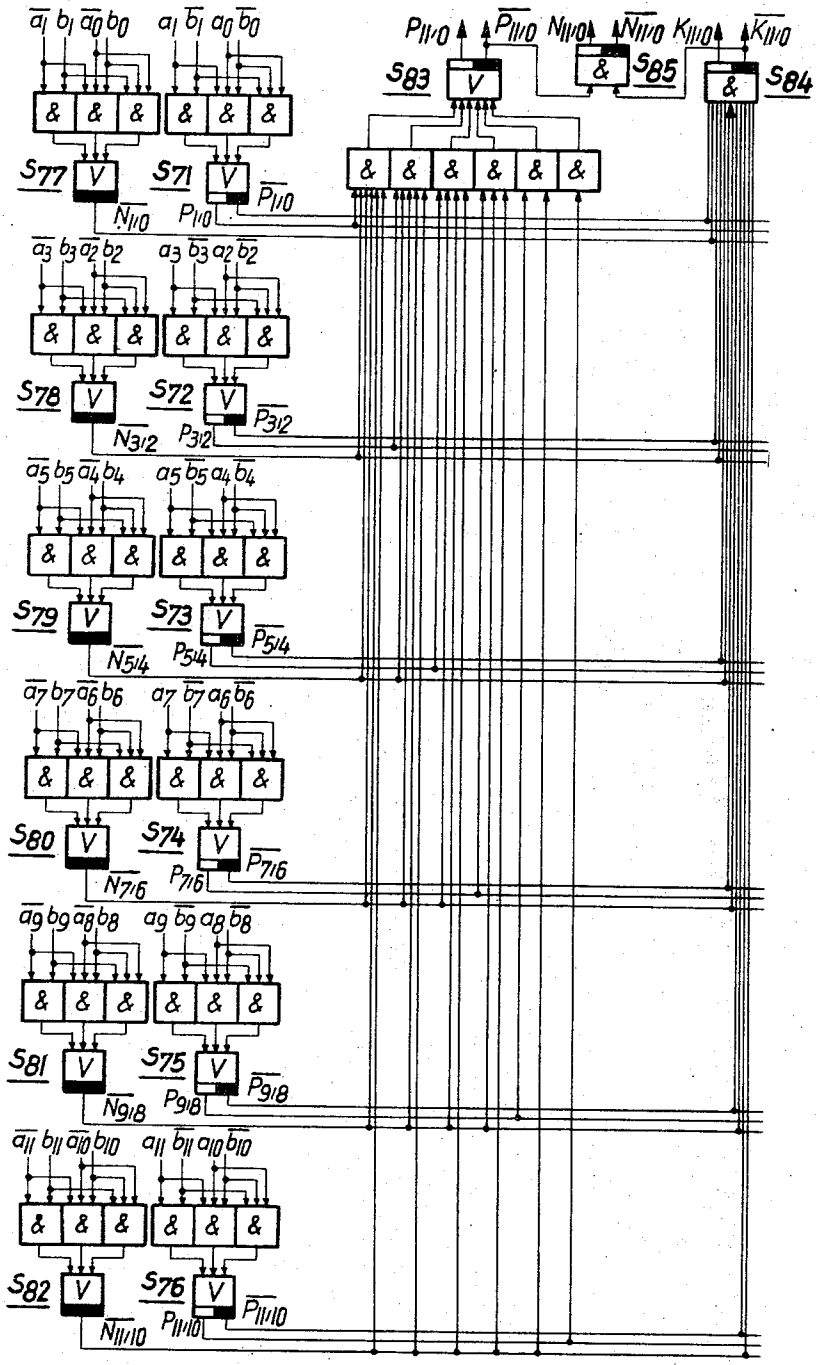

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Fig. 12

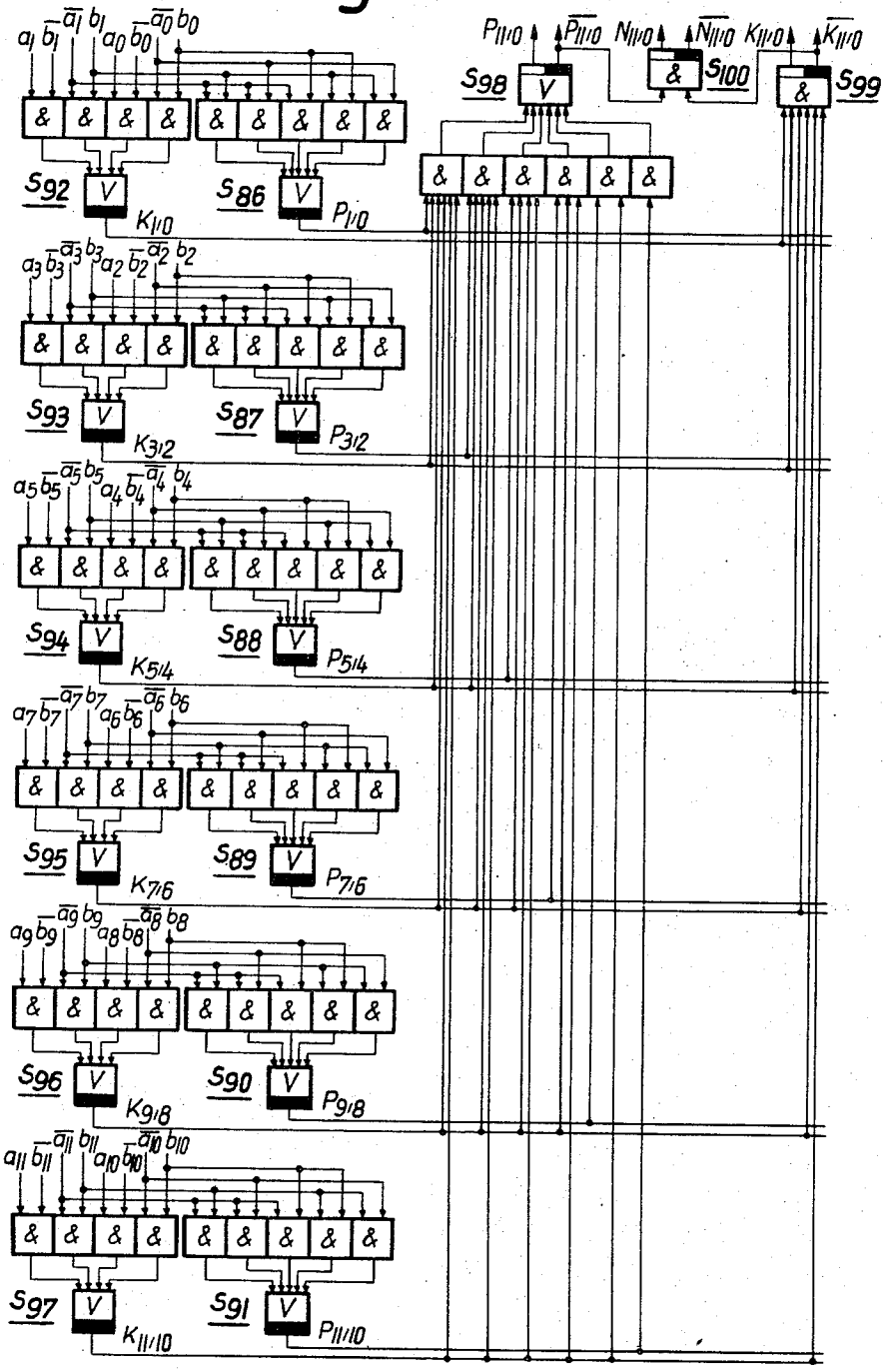

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Fig.13

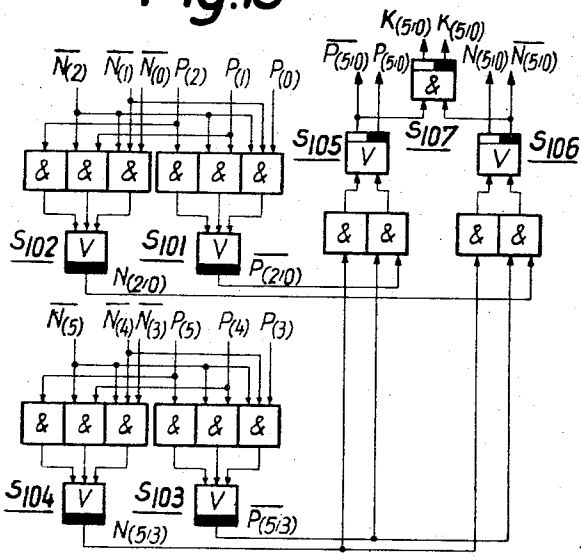
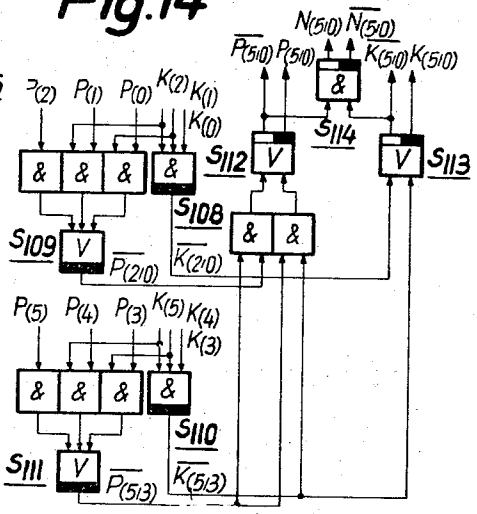


Fig.14



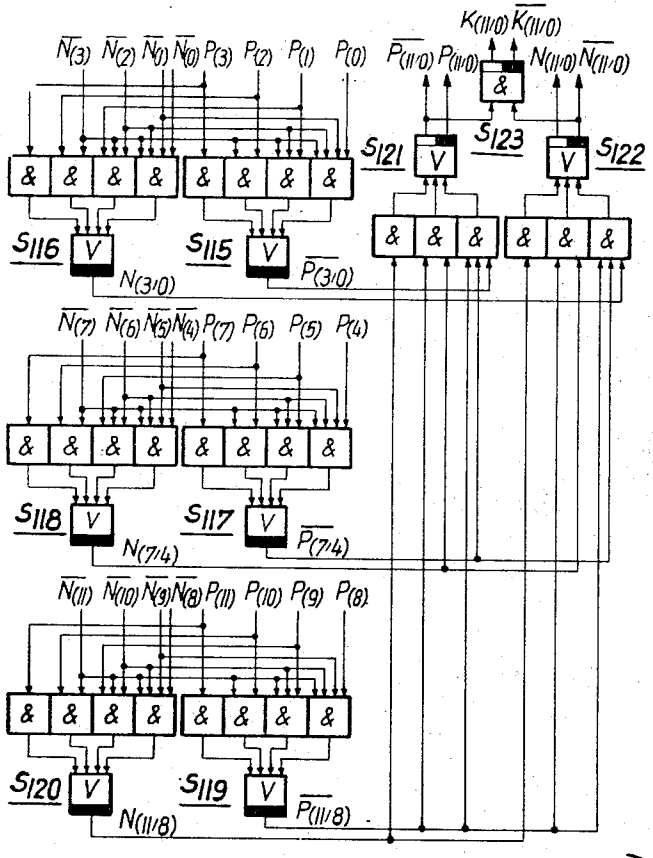


Fig.15

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Fig. 18

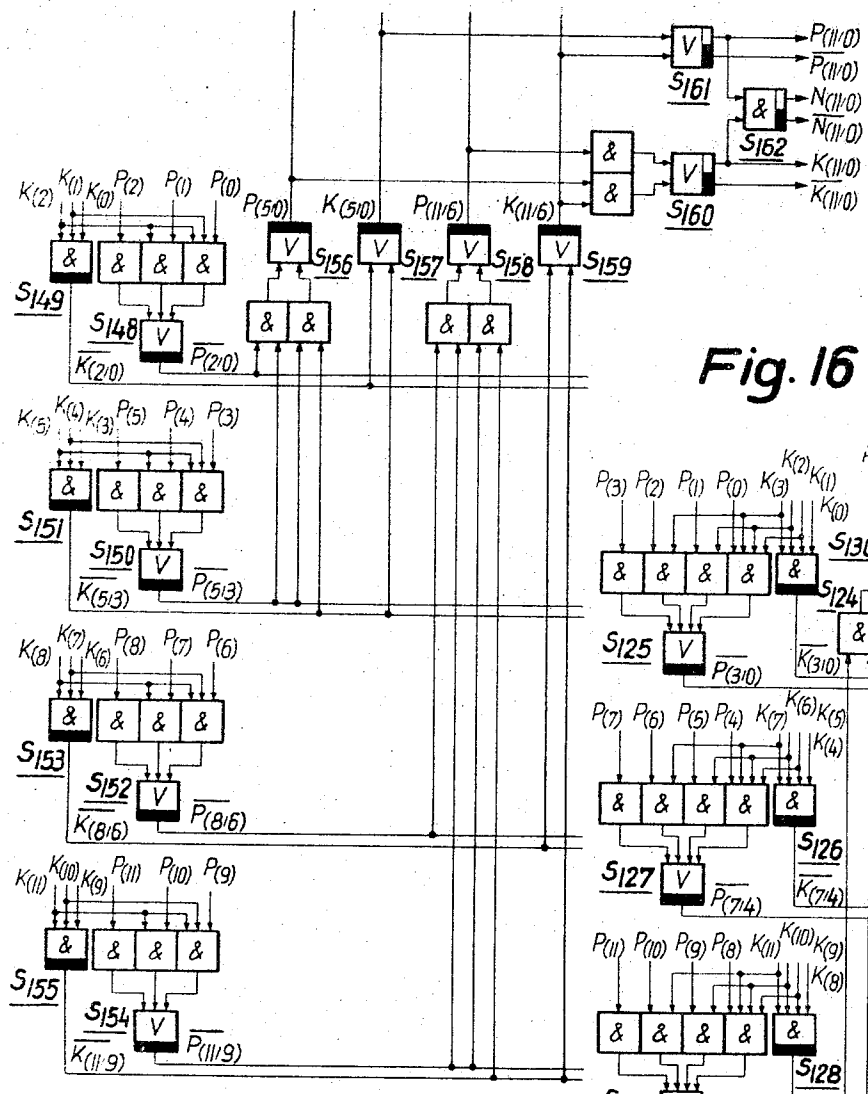

Fig. 16

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Fig.17

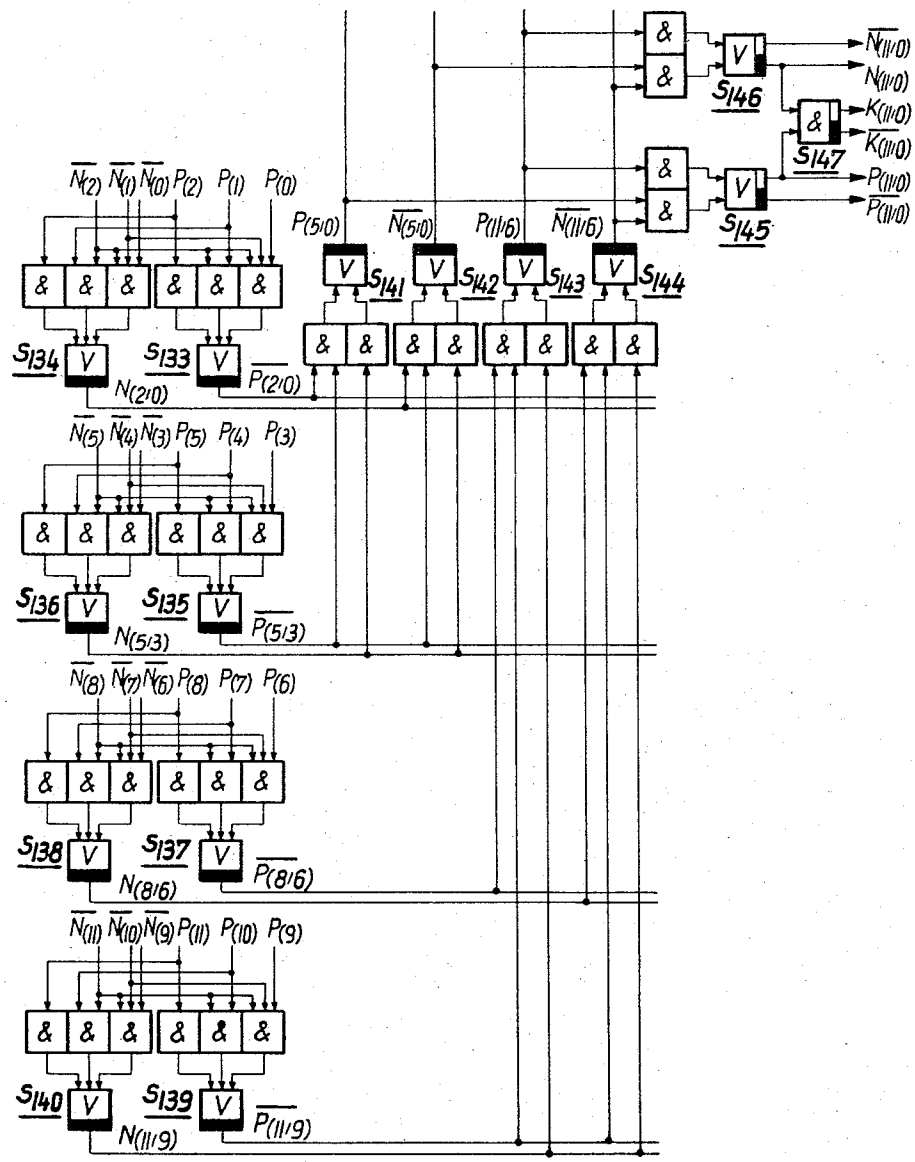

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Fig. 19a

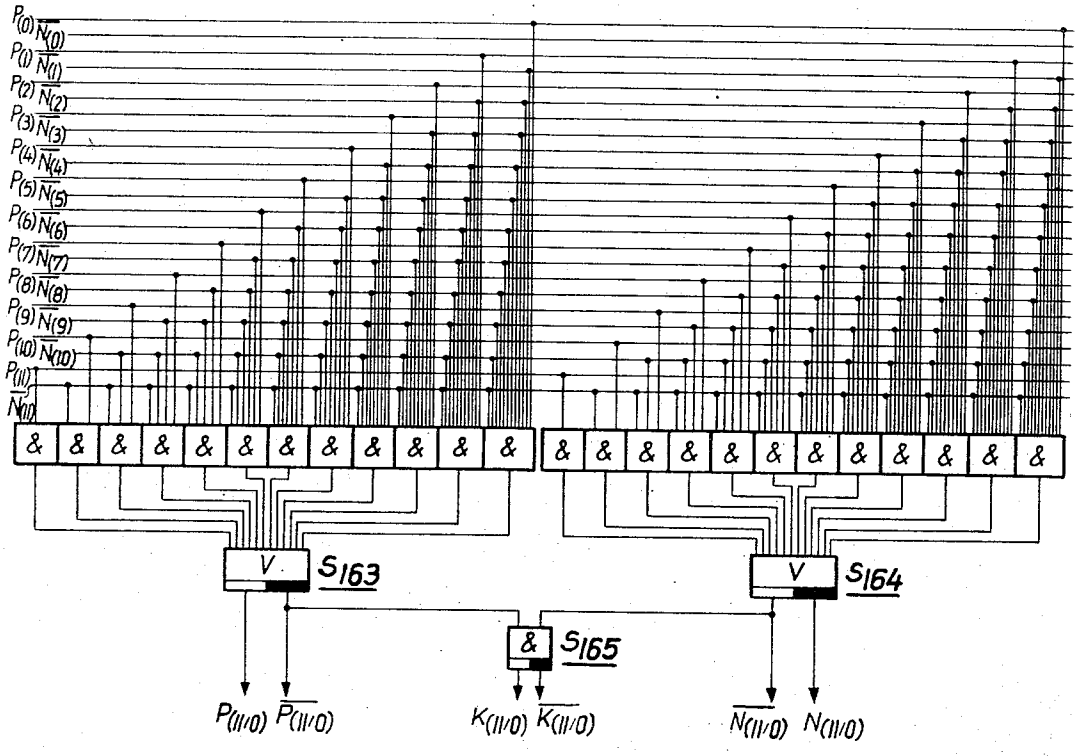

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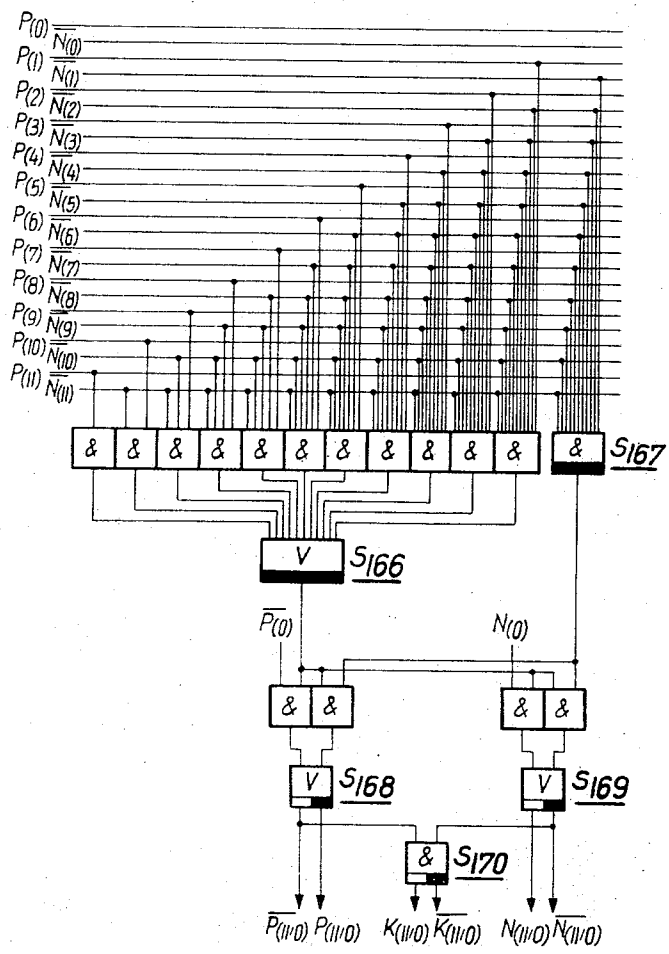
Fig. 19b



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3,363,233

DIGITAL COMPARISON ELEMENT

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Continuation of application Ser. No. 360,649, Apr. 17, 1964. This application Feb. 2, 1967, Ser. No. 613,686
Claims priority, application Germany, Apr. 22, 1963, L 44,690, L 44,691
1 Claim. (Cl. 340—146.2)

This application is a continuation of application Ser. No. 360,649 filed Apr. 17, 1964, now abandoned.

The present invention relates to a digital comparison element. Such a comparison element is a circuit component which is used, for various purposes, in digital control and computing systems whenever two binary numbers, a and b, are to be compared in order to establish whether these two numbers are equal to each other or, if they are unequal, the algebraic sign of their difference. The numbers are, for example, represented by direct current voltage signals which correspond to the binary numbers O and L, the capital letter L being used to represent the number 1 in the binary system.

Two such comparison elements are shown in the periodical ETZ–A (Elektrotechnische Zeitschrift, 1958) No. 18, and ETZ–A, 1962, No. 21/22.

FIGURES 1 and 2 show comparison elements according to the prior art. Each is shown as an element capable of comparing binary numbers consisting of four binary digits, the number a having digits a_0, a_1, a_2, a_3, and the number b having digits b_0, b_1, b_2, b_3. The comparison elements have outputs at which appear the signals $P_{3/0}$, $N_{3/0}$, $K_{3/0}$, as well as the antivalents or negated signals $\overline{P}_{3/0}$, $\overline{N}_{3/0}$, $\overline{K}_{3/0}$.

When:

$$a>b,\ P_{3/0}=L,\ N_{3/0}=O \text{ and } K_{3/0}=O$$
$$a<b,\ N_{3/0}=L,\ P_{3/0}=O \text{ and } K_{3/0}=O$$
$$a=b,\ K_{3/0}=L,\ P_{3/0}=O \text{ and } N_{3/0}=O$$

In each case, a negated signal will be O if its corresponding affirmative signal is L, and L if its corresponding affirmative signal is O.

In order to make a meaningful comparison of the circuit complexity of FIGURES 1 and 2, the circuits are so shown that passive stages are controlled only by active stages. This condition is, in practice, met for reasons of current economy. The passive stages are the AND-circuits and the OR-circuits, while the active stages are the negated or NOT-stages. The negated stages, which may, in practice, be constituted by a first transistor, are shown by the black rectangles. A further negation, effected, for example, by a second transistor which is controlled by the first transistor, is represented by the white rectangles. Each AND function is represented by the ampersand "&" and each OR function by "v." Where appropriate, the & and v are indexed by means of subscripts.

In the prior art comparison element of FIGURE 1, the signals representing the four-digit binary numbers a and b, namely, the signals a_0 to a_3, b_0 to b_3, as well as their negates $\overline{a}_0$ to $\overline{a}_3$ and $\overline{b}_0$ to $\overline{b}_3$, are applied to the AND/NOT/NOT-circuits $\&_0$ to $\&_7$. The outputs of circuits $\&_2$ to $\&_7$ are applied to the inputs of further AND/NOT/NOT-circuits $\&_8$ to $\&_{10}$, whose outputs, in turn, are applied to the inputs of AND-circuits $\&_{11}$ to $\&_{18}$. The outputs of AND-circuits $\&_{11}$ to $\&_{14}$ are applied to the inputs of an OR/NOT/NOT-circuit v_{19} while the outputs of AND-circuits $\&_{15}$ to $\&_{18}$ are applied to another OR/NOT/

NOT-circuit v_{20}. The negated outputs of v_{19} and v_{20} are applied to an AND/NOT/NOT-circuit $\&_{21}$. The affirmed outputs of $\&_0$ and $\&_1$ are applied, respectively, to the respective inputs of AND-circuits $\&_{11}$ and $\&_{15}$. The circuit v_{19} plus out the signals $N_{3/0}$, $\overline{N}_{3/0}$, the circuit v_{20} puts out the signals $P_{3/0}$, $\overline{P}_{3/0}$, and the circuit $\&_{21}$ puts out the signals $K_{3/0}$, $\overline{K}_{3/0}$.

The comparison element according to FIGURE 2 comprises eight AND/NOT-circuits $\&_{22}$ to $\&_{29}$, with the circuits $\&_{22}$ and $\&_{23}$ having applied to their inputs the signals corresponding to the highest-order digits of the binary numbers, with the next AND/NOT-circuits $\&_{24}$, $\&_{25}$, having applied to their inputs the signals pertaining to the next-lower order digits, and so on. The stages following the stages of the highest-order digits are additionally controlled by all preceding stages. The outputs of the AND/NOT-circuits $\&_{28}$ and $\&_{29}$ are applied to AND/NOT/NOT-circuits $\&_{30}$ and $\&_{31}$, at which appear the output signals $P_{3/0}$, $\overline{P}_{3/0}$, and $N_{3/0}$, $\overline{N}_{3/0}$, respectively. Connected to the affirmed outputs of circuits $\&_{30}$ and $\&_{31}$ are the inputs of a further AND/NOT/NOT-circuit $\&_{32}$, at whose outputs appear the signals $K_{3/0}$, $\overline{K}_{3/0}$.

The time required for forming the comparison signal is, for all practical purposes, set by the number of transistors connected in the cascade, this being represented by the white and black rectangles. For example, in the circuit of FIGURE 1, the signal $K_{3/0}$ is formed after six transistor switchings, while in the circuit of FIGURE 2, the same signal is formed after eight transistor switchings. Each of these switchings, of course, takes a certain time, so that it takes relatively long, once the input signals have been applied to the comparison element, to obtain a useful output signal which gives the desired indication.

It is, therefore the primary object of the present invention to provide a comparison element which is simpler than heretofore known comparison elements and which produce the desired output signals, namely, the signals representing the existence of coincidence, i.e., equality between the numbers being compared, or the signals representing the algebraic sign of the difference between the two numbers, more quickly than do the prior art comparison elements. Accordingly, the present invention resides in a comparison element which is characterized by the following features:

(1) The numbers to be compared are divided into "subnumbers" or groups of digits, each of which digits is represented by a signal.

(2) The signals of each group of digits control a set of two logic input circuits. One of these puts out a single intermediate signal that indicates whether the two digit groups are coincident, i.e., equal, to each other, whereas the other of the two logic input circuits puts out a signal which indicates whether there exists a positive or negative difference between the two groups of digits.

(3) Two logic output circuits have their inputs connected to the outputs of the input circuits of each digit group for combining the intermediate results produced by each set of two input circuits.

According to a further feature of the present invention, the input circuits have their outputs connected to auxiliary logic circuits, whose outputs are connected to the above-described output circuits. That is to say, the output circuits do not have the information applied to them directly by the input circuits, instead, the set of input circuits are combined into larger groups and have their signals passed on to the auxiliary or intermediate

logic circuit, and it is the output of these auxiliary logic elements which are then applied to the final output circuits.

Additional objects and advantages of the present invention will become apparent upon consideration of the following description when taken in conjunction with the accompanying drawings in which:

FIGURES 1 and 2, already referred to above, are block diagrams of comparison elements according to the prior art.

FIGURE 3 contains block diagrams of the six logic circuits for producing the K, N and P output signals, each of which circuit is capable of handling 2-digit numbers.

FIGURE 4 contains two block diagrams of logic circuits similar to FIGURE 3 but capable of handling 3-digit and 4-digit numbers, respectively.

FIGURE 5 contains block diagrams of logic circuits for obtaining, ultimately, the final output signals from intermediate values.

FIGURE 6 contains block diagrams of other logic circuits for producing ultimate output signals from intermediate values.

FIGURE 7 contains block diagrams of logic circuits for combining intermediate signals.

FIGURES 8 through 12 are block diagrams of comparison elements capable of handling numbers having up to 12 digits.

FIGURE 13 is a block diagram of a modified version of a part of the circuitry of FIGURE 10.

FIGURE 14 is a block diagram of a modified version of a part of the circuitry of FIGURE 12.

FIGURES 15 and 16 are block diagrams of modified versions of part of the circuitry of FIGURES 10 and 12.

FIGURES 17 and 18 are block diagrams of modifications of the circuitry of FIGURES 15 and 16.

FIGURE 19*a* is a block diagram of a part of the comparison element.

FIGURE 19*b* is a block diagram of a simplified version of the circuit of FIGURE 19*a*.

Before proceeding with the description of the figures, it is pointed out that, in the following description, the numbers to be compared will be considered to be the numbers "*a*" and "*b*" having digits a_0, a_1, a_2 . . . , b_0, b_1, b_2 . . . , with the index "0" identifying the lowest-order digit of the number, the index "1" the next higher-order digit, and so on. The digits are represented by correspondingly referenced D.C. voltage signals, which are identified by O and L.

The comparison element is to determine whether $a>b$, $a<b$, or $a=b$. The numbers a and b to be compared have to be so encoded that, when $a>b$, the binary value of the combination of L and O digits representing the number a is greater than the binary value of the combination of L and O digits representing the number b. Here, the binary value of a combination of L and O digits is to be understood as the numerical value of this L and O combination, were the same to be considered as a number encoded in the natural binary code.

For example:

Decimal Number	Encoded in Natural Binary Code	Tetrad Representation (each decimal digit encoded in Natural Binary Code)	Binary value of the Tetrad Representation at the left
a, 912.....	LLLOOLOOOO	LOOL OOOL OOLO	2,322
b, 857.....	LLOLOLLOOL	LOOO OLOL OLLL	2,135

The decimal number can be encoded in another suitable code, so long as the above limitation is observed.

The following applies for the comparison within each binary digit.

When:

$$a_i=b_i,\ K_i=L$$
$$a_i>b_i,\ P_i=L$$
$$a_i<b_i,\ N_1=L$$

For the negation:

$$a_1=b_i,\ \overline{K}_i=L$$
$$a_i\leqq b_i,\ \overline{P}_1=L$$
$$a_i\geqq b_i,\ \overline{N}_i=L$$

The reference K represents coincidence, the reference P represents a positive deviation, i.e., a difference which, for purposes of result, will be considered a positive difference, and the reference N represents a negative difference. When groups of digits, representing a part of the number or even the entire number, are compared, the index identifies the particular part of the number with which the comparison concerns itself. If, for instance, a number consisting of digits a_7, a_6, a_5, a_4, is larger than a number consisting of digits b_7, b_6, b_5, b_4, the signal $P_{7/4}=L$. Logic functions which have been found to be particularly advantageous for obtaining K, P and N, are set forth in the appendix, with logic functions (1) and (2) being applicable for forming as signal for indicating coincidence or non-coincidence, as the case may be.

Circuits S_1 and S_2 of FIGURE 3 show how the functions may be realized, for numbers having a width of 2 bits, by using AND-circuits whose outputs are connected to the inputs of an OR/NOT-circuit. The response conditions for K are better since here the number of the individual components progresses arithmetically only and the number of inputs to each component remains constant (equal to 2).

The functions (3) and (4) are used to obtain a signal indicating positive, or non-positive, difference, with circuits S_3 and S_4 of FIGURE 3 showing how these functions may be realized, again for numbers having a width of 2 bits. FIGURE 4 shows two further circuits S_7 and S_8, each likewise consisting of AND-circuits whose outputs are connected to an OR/NOT-circuit, for realizing the logic functions (3) for numbers having 3 and 4 bits, respectively. The circuits have a and $\overline{b}$ applied to them. The signals applied to each AND-circuit are best seen from the drawing; for example, the first AND-circuit $\&_{33}$ has the signals a_0, a_1, a_2, $\overline{b}_0$, applied to it, and so on.

The functions (5) and (6) are used to obtain a signal indicating the negative, or non-negative, difference, with circuits S_5 and S_6 of FIGURE 3 showing how these functions may be realized.

Functions (7), (8), (9) and (10) are functions for forming the signals indicating positive or negative differences, which functions differ from those set forth above. These functions (7) to (10) which are realized by a chain or cascade of serially connected logic circuits, can be re-written, for example, as functions (11) and (12) in which the solid zig-zag line represents the switching function of a circuit which uses input AND-circuits throughout, whereas the dashed zig-zag line represents the switching function of a circuit which uses an OR/NOT-circuit in its lowest-order digit.

The numbers to be compared are divided into groups of digits. According to the present invention, the groups of digits have assigned to them input circuits which are controlled by signals a, b, these inputs circuits being arranged to produce the above switching functions. The signals representing the intermediate results have their outputs connected to the inputs of the further circuits which form the final output result.

Functions (13), (14), (15), (16), (17) and (18) are the functions of these further circuits i.e., the auxiliary or intermediate circuits which are controlled by the signals P, N, $\overline{P}$, $\overline{N}$, appearing at the outputs of the circuits which themselves are controlled by the input signals a and b. The indices are shown in parentheses, this being intended to indicate that the functions apply, accordingly, in the

event the individual intermediate results are each formed for a plurality of bits. For example, in the first line of function (13), the index (0) can be replaced by the index (2/0) and the index (1) can be replaced by the index 5/3, in which case the final result would be $P_{5/0}$.

Once the signals P, K, $\overline{P}$, $\overline{K}$, are available at the outputs of the logic circuits controlled by the input signals, the further logic circuits connected to these input circuits will be circuits having the switching functions (19), (20), (21), (22), (23) and (24).

FIGURE 5 shows the circuitry for realizing the switching functions to obtain the final or ultimate output signals when there is coincidence, or positive or negative difference, from two or three, intermediate results (i.e., comparison by groups), the logic circuits being controlled by the P and N signals of the preceding logic circuits. The circuits S_9 and S_{12} are the coincidence or K circuits, circuits S_{13} to S_{16} are the P circuits, and circuits S_{17} to S_{20} are the N circuits.

FIGURE 6 shows other logic circuits for combining intermediate results. However, the circuits of FIGURE 6 differ from those of FIGURE 5 in that the control signals applied to them are the P and K signals, rather than the P and N signals, as was the case in FIGURE 5. Circuits S_{21} to S_{24} of FIGURE 6 are the K circuits. Circuits S_{25} to S_{28} are the P circuits, the same being controlled by the P and K output signals of the preceding logic circuits. Circuits S_{29} to S_{32} are the N circuits.

FIGURE 7 shows logic circuits S_{33} to S_{35} for the P circuit, adapted, respectively, for combining the results of 4, 5 and 6 group comparisons which produce, as intermediate results, the P and N signals.

FIGURES 8 through 12 show comparison elements for comparing numbers consisting of 12 binary digits each.

FIGURE 8 shows an element in which the intermediate results (group comparison) are formed of 4 bits each. The coincidence circuit consists of three groups S_{36} to S_{38} which are constructed in accordance with function (2). The P circuit consists of groups S_{39} to S_{41} which are constructed in accordance with function (11). Circuits S_{36} to S_{41} for the group comparison are controlled directly by the input signals *a*, *b*, with the circuits S_{36} to S_{39} being assigned to the four lowest-order digits, S_{37} to S_{40} being assigned to the next four digits, and S_{38} to S_{41} being assigned to the four highest of the twelve digits. In order to form the end result, the output signals of the groups of the K and P circuits are applied to circuit S_{42}, operating in accordance with function (21), and to circuit S_{43}, operating in accordance with function (19). The negated outputs of S_{42} and S_{43} are applied to an AND/NOT/NOT-circuit S_{44}.

FIGURE 9 shows an element in which each intermediate result is constituted by 3 bits. The coincidence circuit consists of four circuits S_{45} to S_{48}, operating in accordance with function (2), and the P circuit consists of circuits S_{49} to S_{52}, operating in accordance with function (3). The signals representing the intermediate results again control the output circuits S_{53} and S_{54}, operating in accordance with functions (21) and (19), respectively. The negated outputs of S_{53} and S_{54} are connected to the inputs of an AND/NOT/NOT-circuit S_{55}.

FIGURES 10, 11 and 12 show comparison elements in which the first logic input circuits, to which the signals *a*, *b*, are applied, are combined into groups of 2 bits each. In the case of the comparison elements of FIGURES 10 and 11, the intermediate results P and N are obtained at the outputs of the input circuits, while in the case of the element of FIGURE 12, the input circuits put out the intermediate results P and K. In the comparison element of FIGURE 10, P and N are derived, as final result, from the intermediate results, whereas in the comparison elements of FIGURES 11 and 12, P and K are first produced. The following switching functions apply:

Figure	Circuit	Logic Function
10	Input circuits S_{56}–S_{61} (P)	(4)
	Input circuits S_{62}–S_{67} (N)	(5)
	Output circuit S_{68}	(13)
	Output circuit S_{69}	(17)
11	Input circuits S_{71}–S_{76} (P)	(3)
	Input circuits S_{77}–S_{82} (N)	(5)
	Output circuit S_{83}	(13)
	Output circuit S_{84}	(15)
12	Input circuits S_{86}–S_{91} (P)	(4)
	Input circuits S_{92}–S_{97} (K)	(2)
	Output circuit S_{98}	(19)
	Output circuit S_{99}	(21)

The output circuits which are controlled directly by signals representing the intermediate results have connected to their outputs an AND/NOT/NOT-circuit S_{70} (FIGURE 10), S_{85} (FIGURE 11), S_{100} (FIGURE 12).

It will be seen that by switching the signals through in parallel, the final result is obtained very quickly. For example, in the case of FIGURE 12, the signal $\overline{K}_{11/0}$ is obtained after two transistor switchings, and the signal $K_{11/0}$ after three switchings.

The circuits S_{68} to S_{70} of FIGURE 10 can be replaced by a logic circuit arrangement such as is shown in FIGURE 13. Here, further auxiliary values are formed from the intermediate values put out by the input circuits which are controlled by the input signals, this being effected by means of circuits S_{101} to S_{104}, and only these auxiliary signals are applied to further logic circuits S_{105} and S_{106} to whose outputs is connected the AND/NOT/NOT-circuit S_{107}, which circuits S_{105} to S_{107} put out the final results P, N and K. Thus, if the circuitry of FIGURE 13 is used in the element of FIGURE 10, the indices (0), (1), (2) and (2/0) must be replaced, respectively, by the indices 1/0, 3/2, 5/4 and 5/0, and so on.

FIGURE 14 shows a circuit arrangement which can be used in place of circuits S_{98} to S_{100} of FIGURE 10. Here, too, auxiliary signals are formed from the P and K results which appear as intermediate values (circuits S_{108} to S_{111}). The logic circuits S_{112} and S_{113} form, from the auxiliary signals, the final results for P and K, and the AND/NOT/NOT-circuit S_{114} forms the final signals for N.

FIGURES 15 and 16 show circuit arrangements in which, as in the case of FIGURES 13 and 14, auxiliary signals, used in forming the final output signals, are first derived from the intermediate signals produced by the input circuits, this being effected by circuits S_{115} to S_{120} in the arrangement of FIGURE 15 and by the circuits S_{124} to S_{129} in the arrangement of FIGURE 16.

The circuit of FIGURE 15 can be replaced by the circuit of FIGURE 17, and the circuit of FIGURE 16 by that of FIGURE 18. The auxiliary circuits S_{133} to S_{140} in FIGURE 17 and S_{143} to S_{155} in FIGURE 18, which have applied to them the signals of the input circuits, representing the intermediate signals, have connected to their outputs further auxiliary circuits S_{141} to S_{144} in FIGURE 17 and S_{156} to S_{159} in FIGURE 18. Only those signals which are put out by the last-mentioned auxiliary circuits are applied to the final output circuits.

FIGURE 19*a* shows, as does FIGURE 15, a circuit arrangement for that part which is connected to the input stages, without, however, being divided into auxiliary and output circuits. FIGURE 19*b* shows how the arrangement of FIGURE 19*a* can be simplified.

It will be seen from the above that the present invention resides, basically, in a comparison element for comparing multiple-digit binary numbers to determine coincidence thereof, or in the case of non-coincidence, the algebraic sign of their difference, the numbers to be compared being divided into groups of digits each of which digits is represented by a signal. The comparison element itself comprises a plurality of logic input circuit means, cor-

responding in number to the number of groups of digits into which each of the numbers to be compared is divided. Each set is connected to receive the signals which represent the digits that are part of the two groups of digits to be compared by the respective set. Each set of input circuit means has first and second input circuits, the first input circuit indicating coincidence of the two groups of digits and the second input circuit indicating a positive or negative difference between the two groups of digits. Output circuit means are provided for combining the outputs of the input circuit means, these output circuit means including a first output circuit which is connected to receive the outputs of all of the first input circuits of all of the sets for combining the same, and a second output circuit which is connected to receive the outputs of all of the second input circuits of all of the sets for combining the same.

One practical application of the comparison element according to the present invention is in the machine tool control art, in which a machine tool is controlled numerically in accordance with a predetermined program so that the actual work tool, e.g., a milling cutter, will be made to follow a given path with respect to a work piece. If the work piece is clamped in place, the tool will be made to move relative to the bed of the machine. The actual position of the work tool relative to the work piece is measured by suitable photosensitive scanning means, which may incorporate digitally coded scales so that the scanning means produces, as its output, a digital number which represents the actual position of the work tool. This number is compared with the nominal position of the work tool, i.e., the position which the work tool should occupy relative to the work piece as dictated by the program. This nominal position may itself be expressed as a digital number. The digital numbers representing, respectively, the actual and the nominal position of the work tool relative to the work piece, and which, in practice, may have some twenty digits each, are then compared with each other. If they are equal, the position of the work tool is in agreement with the position dictated by the program. If the numbers are not equal to each other, the work tool is not in agreement with the programmed position and has to be advanced or retarded. This is accomplished by applying the appropriate control signal to the machine control system, and this signal is that put out by, or derived from, the comparison element which compares the two numbers. It is for this reason that the algebraic sign of the difference is significant, because, depending on whether the actual position is, numerically, greater or smaller than the programmed or nominal position, the tool will be advanced or retarded.

It will be understood that the above description of the present invention is susceptible to various modifications, changes, and adaptations, and the same are intended to be comprehended within the meaning and range of equivalents of the appended claims. For example the present invention is not limited to the precise application described above which is given only by way of example, as there are many other cases, in industrial and scientific fields, where two digital numbers have to be compared.

APPENDIX

[Logic functions]

(1)

$(\bar{a}_0 \& \bar{b}_0) \vee (a_0 \& b_0) = K_0$

$(\bar{a}_0 \& \bar{b}_0 \& \bar{a}_1 \& \bar{b}_1) \vee (a_0 \& b_0 \& \bar{a}_1 \& \bar{b}_1) \vee (\bar{a}_0 \& \bar{b}_0 \& a_1 \& b_1) \vee (a_0 \& b_0 \& a_1 \& b_1) = K_{1/0}$

$(\bar{a}_0 \& \bar{b}_0 \& \bar{a}_1 \& \bar{b}_1 \& \bar{a}_2 \& \bar{b}_2) \vee (a_0 \& b_0 \& \bar{a}_1 \& \bar{b}_1 \& \bar{a}_2 \& \bar{b}_2) \vee (\bar{a}_0 \& \bar{b}_0 \& a_1 \& b_1 \& \bar{a}_2 \& \bar{b}_2) \vee (a_0 \& b_0 \& a_1 \& b_1 \& \bar{a}_2 \& \bar{b}_2) \vee (\bar{a}_0 \& \bar{b}_0 \& \bar{a}_1 \& \bar{b}_1 \& a_2 \& b_2) \vee (a_0 \& b_0 \& \bar{a}_1 \& \bar{b}_1 \& a_2 \& b_2) \vee (\bar{a}_0 \& \bar{b}_0 \& a_1 \& b_1 \& a_2 \& b_2) \vee (a_0 \& b_0 \& a_1 \& b_1 \& a_2 \& b_2) = K_{2/0}$

(2)

$(a_0 \& \bar{b}_0) \vee (\bar{a}_0 \& b_0) = \bar{K}_0$

$(a_0 \& \bar{b}_0) \vee (\bar{a}_0 \& (\bar{a}_0 b_0) \vee (a_1 \& \bar{b}_1) \vee (\bar{a}_1 \& b_1) = \bar{K}_{1/0}$

$(a_0 \& \bar{b}_0) \vee (\bar{a}_0 \& b_0) \vee (a_1 \& \bar{b}_1) \vee (\bar{a}_1 \& b_1) \vee (a_2 \& \bar{b}_2) \vee (\bar{a}_2 \& b_2) = \bar{K}_{2/0}$

(3)

$(a_0 \& \bar{b}_0) = P_0$

$(a_1 \& \bar{b}_1) \vee (a_1 \& a_0 \& \bar{b}_0) \vee (\bar{b}_1 \& a_0 \& \bar{b}_0) = P_{1/0}$

$(a_2 \& \bar{b}_2) \vee (a_2 \& a_1 \& \bar{b}_1) \vee (a_2 \& a_1 \& a_0 \& \bar{b}_0) \vee (a_2 \& \bar{b}_1 \& a_0 \& \bar{b}_0) \vee (\bar{b}_2 \& a_1 \& \bar{b}_1) \vee (\bar{b}_2 \& a_1 \& a_0 \& \bar{b}_0) \vee (\bar{b}_2 \& \bar{b}_1 \& a_0 \& \bar{b}_0) = P_{2/0}$

(4)

$\bar{a}_0 \vee b_0 = \bar{P}_0$

$(\bar{a}_1 \& \bar{a}_0) \vee (\bar{a}_1 \& b_1) \vee (\bar{a}_1 \& b_0) \vee (b_1 \& \bar{a}_0) \vee (b_1 \& b_0) = \bar{P}_{1/0}$

$(\bar{a}_2 \& b_2) \vee (\bar{a}_2 \& \bar{a}_1 \& \bar{a}_0) \vee (\bar{a}_2 \& \bar{a}_1 \& b_0) \vee (\bar{a}_2 \& \bar{a}_1 \& b_1) \vee (\bar{a}_2 \& b_1 \& \bar{a}_0) \vee (\bar{a}_2 \& b_1 \& b_0) \vee (b_2 \& \bar{a}_1 \& a_0) \vee (b_2 \& \bar{a}_1 \& b_0) \vee (b_2 \& b_1 \& \bar{a}_0) \vee (b_2 \& b_1 \& b_0) = \bar{P}_{2/0}$

(5)

$(\bar{a}_0 \& b_0) = N_0$

$(\bar{a}_1 \& b_1) \vee (\bar{a}_1 \& \bar{a}_0 \& b_0) \vee (b_1 \& \bar{a}_0 \& b_0) = N_{1/0}$

$(\bar{a}_2 \& b_2) \vee (\bar{a}_2 \& \bar{a}_1 \& b_1) \vee (\bar{a}_2 \& \bar{a}_1 \& \bar{a}_0 \& b_0) \vee (\bar{a}_2 \& b_1 \& \bar{a}_0 \& b_0) \vee (b_2 \& \bar{a}_1 \& b_1) \vee (b_2 \& \bar{a}_1 \& \bar{a}_0 \& b_0) \vee (b_2 \& b_1 \& \bar{a}_0 \& b_0) = N_{2/0}$

(6)

$a_0 \vee \bar{b}_0 = \bar{N}_0$

$(a_1 \& a_0) \vee (a_1 \& \bar{b}_1) \vee (a_1 \& \bar{b}_0) \vee (\bar{b}_1 \& a_0) \vee (\bar{b}_1 \& \bar{b}_0) = \bar{N}_{1/0}$

$(a_2 \& \bar{b}_2) \vee (a_2 \& a_1 \& a_0) \vee (a_2 \& a_1 \& \bar{b}_0) \vee (a_2 \& a_1 \& \bar{b}_1) \vee (a_2 \& \bar{b}_1 \& a_0) \vee (a_2 \& \bar{b}_1 \& \bar{b}_0) \vee (\bar{b}_2 \& a_1 \& a_0) \vee (\bar{b}_2 \& a_1 \& \bar{b}_0) \vee (\bar{b}_2 \& \bar{b}_1 \& a_0) \vee (\bar{b}_2 \& \bar{b}_1 \& \bar{b}_0) = \bar{N}_{2/0}$

(7)

$(a_0 \& \bar{b}_0) = P_0$

$(a_1 \& \bar{b}_1) \vee (P_0 \& a_1) \vee (P_0 \& \bar{b}_1) = P_{1/0}$

$(a_2 \& \bar{b}_2) \vee (P_{1/0} \& a_2) \vee (P_{1/0} \& \bar{b}_2) = P_{2/0}$

$(a_3 \& \bar{b}_3) \vee (P_{2/0} \& a_3) \vee (P_{2/0} \& \bar{b}_3) = P_{3/0}$

(8)

$\bar{a}_0 \vee b_0 = \bar{P}_0$

$(\bar{a}_1 \& b_1) \vee (\bar{P}_0 \& \bar{a}_1) \vee (\bar{P}_0 \& b_1) = \bar{P}_{1/0}$

$(\bar{a}_2 \& b_2) \vee (\bar{P}_{1/0} \& \bar{a}_2) \vee (\bar{P}_{1/0} \& b_2) = \bar{P}_{2/0}$

$(\bar{a}_3 \& b_3) \vee (\bar{P}_{2/0} \& \bar{a}_3) \vee (\bar{P}_{2/0} \& b_3) = \bar{P}_{3/0}$

(9)

$(\bar{a}_0 \& b_0) = N_0$

$(\bar{a}_1 \& b_1) \vee (N_0 \& \bar{a}_1) \vee (N_0 \& b_1) = N_{1/0}$

$(\bar{a}_2 \& b_2) \vee (N_{1/0} \& \bar{a}_2) \vee (N_{1/0} \& b_2) = N_{2/0}$

$(\bar{a}_3 \& b_3) \vee (N_{2/0} \& \bar{a}_3) \vee (N_{2/0} \& b_3) = N_{3/0}$

(10)

$a_0 \vee \bar{b}_0 = \bar{N}_0$

$(a_1 \& \bar{b}_1) \vee (\bar{N}_0 \& a_1) \vee (\bar{N}_0 \& \bar{b}_1) = \bar{N}_{1/0}$

$(a_2 \& \bar{b}_2) \vee (\bar{N}_{1/0} \& a_2) \vee (\bar{N}_{1/0} \& \bar{b}_2) = \bar{N}_{2/0}$

$(a_3 \& \bar{b}_3) \vee (\bar{N}_{2/0} \& a_3) \vee (\bar{N}_{2/0} \& \bar{b}_3) = \bar{N}_{3/0}$

(11)

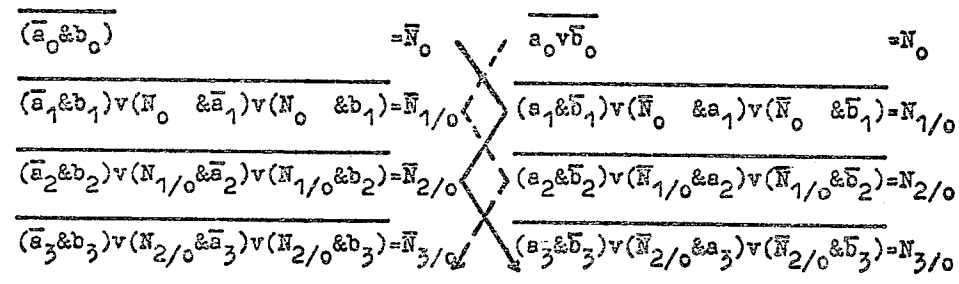
$\overline{(a_0 \& \bar{b}_0)} = \bar{P}_0 \qquad \overline{\bar{a}_0 \vee b_0} = P_0$

$\overline{(a_1 \& \bar{b}_1) \vee (P_0 \& a_1) \vee (P_0 \& \bar{b}_1)} = \bar{P}_{1/0} \qquad \overline{(\bar{a}_1 \& b_1) \vee (\bar{P}_0 \& \bar{a}_1) \vee (\bar{P}_0 \& b_1)} = P_{1/0}$

$\overline{(a_2 \& \bar{b}_2) \vee (P_{1/0} \& a_2) \vee (P_{1/0} \& \bar{b}_2)} = \bar{P}_{2/0} \qquad \overline{(\bar{a}_2 \& b_2) \vee (\bar{P}_{1/0} \& \bar{a}_2) \vee (\bar{P}_{1/0} \& b_2)} = P_{2/0}$

$\overline{(a_3 \& \bar{b}_3) \vee (P_{2/0} \& a_3) \vee (P_{2/0} \& \bar{b}_3)} = \bar{P}_{3/0} \qquad \overline{(\bar{a}_3 \& b_3) \vee (\bar{P}_{2/0} \& \bar{a}_3) \vee (\bar{P}_{2/0} \& b_3)} = P_{3/0}$

(12)



(13)

$P_{(1)} \vee (P_{(0)} \& \bar{N}_{(1)}) = P_{(1/0)}$
$P_{(2)} \vee (P_{(1)} \& \bar{N}_{(2)}) \vee (P_{(0)} \& \bar{N}_{(1)} \& \bar{N}_{(2)}) = P_{(2/0)}$
$P_{(3)} \vee (P_{(2)} \& \bar{N}_{(3)}) \vee (P_{(1)} \& \bar{N}_{(2)} \& \bar{N}_{(3)}) \vee (P_{(0)} \& \bar{N}_{(1)} \& \bar{N}_{(2)} \& \bar{N}_{(3)}) = P_{(3/0)}$

(14)

$N_{(1)} \vee (N_{(0)} \& \bar{P}_{(1)}) = N_{(1/0)}$
$N_{(2)} \vee (N_{(1)} \& \bar{P}_{(2)}) \vee (N_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) = N_{(2/0)}$
$N_{(3)} \vee (N_{(2)} \& \bar{P}_{(3)}) \vee (N_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (N_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) = N_{(3/0)}$

(15)

$\bar{P}_{(0)} \& \bar{N}_{(0)} \& \bar{P}_{(1)} \& \bar{N}_{(1)} = K_{(1/0)}$
$\bar{P}_{(0)} \& \bar{N}_{(0)} \& \bar{P}_{(1)} \& \bar{N}_{(1)} \& \bar{P}_{(2)} \& \bar{N}_{(2)} = K_{(2/0)}$
$\bar{P}_{(0)} \& \bar{N}_{(0)} \& \bar{P}_{(1)} \& \bar{N}_{(1)} \& \bar{P}_{(2)} \& \bar{N}_{(2)} \& \bar{P}_{(3)} \& \bar{N}_{(3)} = K_{(3/0)}$

(16)

$N_{(1)} \vee (\bar{P}_{(0)} \& \bar{P}_{(1)}) = \bar{P}_{(1/0)}$
$N_{(2)} \vee (N_{(1)} \& \bar{P}_{(2)}) \vee (\bar{P}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) = \bar{P}_{(2/0)}$
$N_{(3)} \vee (N_{(2)} \& \bar{P}_{(3)}) \vee (N_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (\bar{P}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) = \bar{P}_{(3/0)}$

(17)

$P_{(1)} \vee (\bar{N}_{(0)} \& \bar{N}_{(1)}) = \bar{N}_{(1/0)}$
$P_{(2)} \vee (P_{(1)} \& \bar{N}_{(2)}) \vee (\bar{N}_{(0)} \& \bar{N}_{(1)} \& \bar{N}_{(2)}) = \bar{N}_{(2/0)}$
$P_{(3)} \vee (P_{(2)} \& \bar{N}_{(3)}) \vee (P_{(1)} \& \bar{N}_{(2)} \& \bar{N}_{(3)}) \vee (\bar{N}_{(0)} \& \bar{N}_{(1)} \& \bar{N}_{(2)} \& \bar{N}_{(3)}) = \bar{N}_{(3/0)}$

(18)

$P_{(0)} \vee N_{(0)} \vee P_{(1)} \vee N_{(1)} = \bar{K}_{(1/0)}$
$P_{(0)} \vee N_{(0)} \vee P_{(1)} \vee N_{(1)} \vee P_{(2)} \vee N_{(2)} = \bar{K}_{(2/0)}$
$P_{(0)} \vee N_{(0)} \vee P_{(1)} \vee N_{(1)} \vee P_{(2)} \vee N_{(2)} \vee P_{(3)} \vee N_{(3)} = \bar{K}_{(3/0)}$

(19)

$P_{(1)} \vee (P_{(0)} \& K_{(1)}) = P_{(1/0)}$
$P_{(2)} \vee (P_{(1)} \& K_{(2)}) \vee (P_{(0)} \& K_{(1)} \& K_{(2)}) = P_{(2/0)}$
$P_{(3)} \vee (P_{(2)} \& K_{(3)}) \vee (P_{(1)} \& K_{(2)} \& K_{(3)}) \vee (P_{(0)} \& K_{(1)} \& K_{(2)} \& K_{(3)}) = P_{(3/0)}$

(20)

$(\bar{K}_{(1)} \& \bar{P}_{(1)}) \vee (\bar{K}_{(0)} \& \bar{P}_{(0)} \& \bar{P}_{(1)}) = N_{(1/0)}$
$(\bar{K}_{(2)} \& \bar{P}_{(2)}) \vee (\bar{K}_{(1)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) \vee (\bar{K}_{(0)} \& \bar{P}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) = N_{(2/0)}$
$(\bar{K}_{(3)} \& \bar{P}_{(3)}) \vee (\bar{K}_{(2)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (\bar{K}_{(1)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (\bar{P}_{(0)} \& \bar{K}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) = N_{(3/0)}$

(21)

$K_{(0)} \& K_{(1)} = K_{(1/0)}$
$K_{(0)} \& K_{(1)} \& K_{(2)} = K_{(2/0)}$
$K_{(0)} \& K_{(1)} \& K_{(2)} \& K_{(3)} = K_{(3/0)}$

(22)

$(\bar{K}_{(1)} \& \bar{P}_{(1)}) \vee (\bar{P}_{(0)} \& \bar{P}_{(1)}) = \bar{P}_{(1/0)}$
$(\bar{K}_{(2)} \& \bar{P}_{(2)}) \vee (\bar{K}_{(1)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) \vee (\bar{P}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)}) = \bar{P}_{(2/0)}$
$(\bar{K}_{(3)} \& \bar{P}_{(3)}) \vee (\bar{K}_{(2)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (\bar{K}_{(1)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) \vee (\bar{P}_{(0)} \& \bar{P}_{(1)} \& \bar{P}_{(2)} \& \bar{P}_{(3)}) = \bar{P}_{(3/0)}$

(23)

$P_{(1)} \vee (P_{(0)} \& K_{(1)}) \vee (K_{(0)} \& K_{(1)}) = \bar{N}_{(1/0)}$
$P_{(2)} \vee (P_{(1)} \& K_{(2)}) \vee (P_{(0)} \& K_{(1)} \& K_{(2)}) \vee (K_{(0)} \& K_{(1)} \& K_{(2)}) = \bar{N}_{(2/0)}$
$P_{(3)} \vee (P_{(2)} \& K_{(3)}) \vee (P_{(1)} \& K_{(2)} \& K_{(3)}) \vee (P_{(0)} \& K_{(1)} \& K_{(2)} \& K_{(3)}) \vee (K_{(0)} \& K_{(1)} \& K_{(2)} \& K_{(3)}) = \bar{N}_{(3/0)}$

(24)

$\bar{K}_{(0)} \vee \bar{K}_{(1)} = \bar{K}_{(1/0)}$
$\bar{K}_{(0)} \vee \bar{K}_{(1)} \vee \bar{K}_{(2)} = \bar{K}_{(2/0)}$
$\bar{K}_{(0)} \vee \bar{K}_{(1)} \vee \bar{K}_{(2)} \vee \bar{K}_{(3)} = \bar{K}_{(3/0)}$

What is claimed is:

1. In a digital comparison element for comparing two series of signals which represent numbers, which series of signals are arranged in multiple-digit signal groups, there being first means for testing whether or not there is coincidence of signal representation of said numbers and forming a first intermediate signal, second means for testing the algebraic sign of the difference between said signal representations of said numbers and forming a second intermediate signal, said first and second means being constituted, respectively, by two logic input circuits which each signal group has associated with it and which input circuits are controlled by the signals of the respective signal group, there further being third means for putting out a coincidence signal and an algebraic sign signal, said third means being constituted by two logic output circuits which are controlled by the intermediate signals of all of said logic input circuits, wherein the improvement comprises the arrangement that each signal group encompasses two or three binary digits and each logic input circuit for testing for coincidence has, for each binary digit of the signal group, two input AND-circuits which are controlled by the signals of the respective signal group, there being OR/NOT-circuit means for combining the output signals of all of said AND-circuits into said first intermediate signal; said improvement further comprising the arrangement that the logic input circuit which pertains to the signal group and which is provided for testing the algebraic sign of the difference has input AND-circuits whose number is determined by the number of binary digits of the signal group, there being OR/NOT circuit means for combining the output signals of all of said last-mentioned AND-circuits into said second intermediate signal.

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