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<p>(21) International Application Number: PCT/US90/02184</p> <p>(22) International Filing Date: 23 April 1990 (23.04.90)</p> <p>(30) Priority data: 393,199 14 August 1989 (14.08.89) US</p> <p>(71) Applicant: HUGHES AIRCRAFT COMPANY [US/US]; 7200 Hughes Terrace, Los Angeles, CA 90045-0066 (US).</p> <p>(72) Inventors: BARDAL, Zaher ; 5229 Doris Way, Torrance, CA 90505 (US). ROLPH, Randy, K. ; 1011 Avenue C, Redondo Beach, CA 90277 (US). LAMB, Arlene, E. ; 2010 Curtis Avenue, Redondo Beach, CA 90278 (US). LONGO, Robert, T. ; 734 Callita Street, Arcadia, CA 91006 (US). MANOLY, Arthur, E. ; 26630 Basswood Avenue, Rancho Palos Verdes, CA 90274 (US). FORMAN, Ralph ; 21516 Hilliard Blvd., Rocky River, OH 44116 (US).</p>		<p>(74) Agents: GUDMESTAD, Terje et al.; Hughes Aircraft Company, P.O. Box 45066, Bldg. C1, MS A126, 7200 Hughes Terrace, Los Angeles, CA 90045-0066 (US).</p> <p>(81) Designated States: AT (European patent), BE (European patent), CA, CH (European patent), DE (European patent)*, DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KP, LU (European patent), NL (European patent), SE (European patent).</p> <p>Published <i>With international search report.</i></p>	
<p>(54) Title: SELF-ALIGNED GATE PROCESS FOR FABRICATING FIELD EMITTER ARRAYS</p>			
<p>(57) Abstract</p> <p>Conical field emitter elements (12) are formed on a surface of a substrate (11) after which a layer of metal (20) is deposited on top of the substrate surface (11) and over the field emitter elements (12). A layer of oxide (13) is then deposited over the metal layer (20). Another layer of metal (14) is deposited over the layer of oxide (13) to form a gate metal layer (14). A layer of photoresist (15) is then deposited over the gate metal layer (14). The layer of photoresist (15) is then plasma etched in an oxygen atmosphere to cause portions of the photoresist (15) above respective field emitter elements (12) to be removed and provide self-aligned holes in the photoresist (15) over each of the field emitter elements (12). The size of the holes may be controlled by appropriately controlling process parameter, including plasma etching time and power and/or initial photoresist thickness. The exposed gate metal layer (14) is etched using the layer of photoresist (15) as a mask. The photoresist layer (15) is removed, and the layer of oxide (13) is etched to expose the field emitter elements (12). Another oxide layer (17) and an anode metal layer (18) also may be formed over the gate metal layer (14) to produce a self-aligned triode structure.</p>			

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SELF-ALIGNED GATE PROCESS FOR FABRICATING
FIELD EMITTER ARRAYS

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BACKGROUND

The present invention relates generally to field emitter arrays, and more particularly to a process for fabricating self-aligned micron-sized field emitter arrays.

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Recently there has been considerable interest in field emitter arrays for reasons discussed by H. F. Gray et al. in "A Vacuum Field Effect Transistor Using Silicon Field Emitter Arrays", IEDM, 1986, pages 776-779. Field emitter arrays typically comprise a metal/insulator/metal

10 film sandwich with a cellular array of holes through the upper metal and insulator layers, leaving the edges of the upper metal layer (which serves as an accelerator electrode) effectively exposed to the upper surface of the lower metal layer (which serves as an emitter electrode).

15 A number of conically-shaped electron emitter elements are mounted on the lower metal layer and extend upwardly therefrom such that their respective tips are located in respective holes in the upper metal layer. If appropriate voltages are applied between the emitter electrode,

1 accelerator electrode, and an anode located above the
accelerator electrode, electrons are caused to flow from
the respective cone tips to the anode. Further details
regarding these devices may be found in the papers by C. A.
5 Spindt, "A Thin-Film Field-Emission Cathode", Journal of
Applied Physics, Vol. 39, No. 7, June 1986, pages
3504-3505, C. A. Spindt et al., "Physical Properties of
Thin-Film Field Emission Cathodes with Molybdenum Cones",
Journal of Applied Physics, Vol. 47, No. 12, December 1976,
10 pages 5248-5263, and C. A. Spindt et al., "Recent Progress
in Low-Voltage Field-Emission Cathode Development", Journal
de Physique, Vol. 45, No. C-9, December 1984, pages
269-278, and in U.S. Patent No. 3,453,478 to K. R.
Shoulders et al. and U.S. Patents Nos. 3,665,241 and
15 3,755,704 to C. A. Spindt et al. Additional patents
disclosing methods for fabricating field emitter array
devices are U.S. Patent No. 3,921,022 to J. D. Levine, U.S.
Patent No. 3,998,678 to S. Fukase et al., U.S. Patent
4,008,412 to I. Yuito et al., U.S. Patent No. 4,307,507 to
20 H. F. Gray et al., and U.S. Patent No. 4,513,308 to R. F.
Greene et al.

In the conventional approaches to fabrication of
field emitter arrays, precise alignment and hole size
control has been very difficult to achieve, because of the
25 very small geometries and tolerances in the devices.
Typically, in order to obtain precise alignment, it has
been necessary to employ a difficult and time-consuming
mask step to insure proper alignment and formation.

Accordingly, it would be advantageous to have a
30 process of fabricating field emitter arrays that was
self-aligning and that is less difficult and costly to
implement.

1

SUMMARY OF THE INVENTION

In order to provide for an improved process by which to form field emitter arrays, the present invention fabricates the arrays in accordance with the following process steps. Substantially conical field emitter elements are formed on a surface of a substrate, after which a layer of oxide is deposited on the substrate surface and over the field emitter elements. A layer of metal is then deposited over the layer of oxide to form a gate metal layer. A layer of photoresist is then deposited over the gate metal layer.

The layer of photoresist is then plasma etched in an oxygen atmosphere to cause portions of the photoresist above respective field emitter elements to be removed and thereby provide self-aligned holes in the photoresist over each of the field emitter elements. The exposed gate metal layer above the field emitter elements is then etched using the layer of photoresist as a mask. The photoresist layer is removed, and the layer of oxide is etched to expose the field emitter elements.

In addition, further processing may be performed to provide a second oxide layer and an anode metal layer in field emission triode devices.

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BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIGS. 1 through 8 illustrate a preferred process of fabricating a field emitter array in accordance with the principles of the present invention; and

FIGS. 9 and 10 illustrate additional processing steps employed in fabricating a field emission triode.

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DETAILED DESCRIPTION

Referring to the drawings, FIGS. 1 and 2 show side and top views, respectively, of a substrate 11 having field emitter elements 12 formed on a surface of the substrate.

5 The substrate 11 and the field emitter elements 12 may be of polysilicon, for example. The substrate 11 is fabricated in a conventional manner to provide an array of emitter elements thereon, with FIG. 2 showing a typical field emitter array. Typically, the substrate 11 and the
10 field emitter elements 12 have a metal layer 20 disposed thereover. This metal layer 20 may be of molybdenum, for example. The metal layer 20 is typically deposited over elements 12 and substrate 11 to a thickness of from about 250Å to about 2000Å, for example. It should be understood,
15 however, that the metal layer 20 may be eliminated in some applications.

Referring to FIG. 3, a layer of oxide 13 is deposited over the surface of the substrate 11 and the field emitter elements 12 (or the metal layer 20 if it is employed). The
20 oxide layer 13 is typically formed using a chemical vapor deposition process. The oxide layer 13 is deposited to a thickness of from about 5000Å to about 15000Å, for example. A gate metal layer 14, comprising a layer of chromium and a layer of gold, for example, is then
25 deposited over the layer of oxide 13. The chromium layer may have a thickness of from about 300Å to about 1000Å, while the gold layer may have a thickness of from about 2000Å to about 5000Å, for example.

With reference to FIG. 4, a layer of photoresist 15
30 is then deposited over the gate metal layer 14. The layer of photoresist 15 is typically deposited using a conventional spin-on procedure employing Hoechst AZ 1370 photoresist spun on at 4000 RPM for about 20 seconds, for example.

1 The structure of FIG. 4 is then processed to cause
portions of the layer of photoresist 15 above respective
field emitter elements 12 to be removed, as shown in FIG.
5, and thereby expose respective portions of the gate metal
5 layer 14 above respective tip regions of the field emitter
elements 12. This may be accomplished by plasma etching
the layer of photoresist 15 in an oxygen environment. The
plasma etching operation may be carried out in a plasma
discharge stripping and etching system Model No. PDS/PDE-
10 301 manufactured by LFE Corporation, Waltham,
Massachusetts, for example. As a specific example for
illustrative purposes, in performing such a plasma etching
process on a field emitter array structure having the
aforementioned specific parameters, the aforementioned
15 plasma discharge system may be initially evacuated to a
pressure of about 0.1 torr, after which a regulated flow of
oxygen gas may be passed through the system at a flow rate
of about 240 cc per minute and at a pressure of about 3
torr before commencement of the plasma discharge. A plasma
20 discharge is then established in the system for a
predetermined time to achieve the desired photoresist
removal. As a specific example for illustrative purposes,
when a single 2-inch wafer having a field emitter array
structure formed thereon with the aforementioned parameter
25 values is processed in the aforementioned system at a
plasma discharge power setting of about 250 watts, a plasma
etching duration of about 2 minutes has achieved the
desired photoresist removal.

 As a result of the plasma etching step,
30 precisely-aligned openings 16 are formed directly over
respective field emitter elements 12 of the array. The
size of the openings 16 may be controlled by appropriately
controlling process parameters, including time and power
setting of the plasma discharge apparatus and/or the
35 initial thickness of the layer of photoresist 15.

1 With reference to FIG. 6, the field emitter elements
12 that have been exposed via openings 16 in the preceding
step are then etched by means of a conventional etching
procedure, for example, using the layer of photoresist 15
5 as a mask. For example, a mixture of water and potassium
iodide may be employed for a time duration of from about 1
minute to about 5 minutes to etch the gold, for example,
and potassium permanganate for about 7 seconds, and oxalic
for about 7 seconds may be employed to etch the chromium,
10 for example.

Referring to FIGS. 7 and 8, the layer of photoresist
15 is then removed, and the layer of oxide 13 is etched
using a conventional etching procedure using buffered
hydrogen fluoride, for example, to expose the field emitter
15 elements 12. This results in a self-aligned cathode
structure as shown in FIG. 8.

With reference to FIGS. 9 and 10, additional
processing steps are illustrated that enable fabrication of
a self-aligned anode structure above the field emission
20 cathode structure fabricated pursuant to the process of
FIGS. 1-8. To fabricate the anode structure after the
photoresist layer 15 is removed as shown in FIG. 7, a
second layer of oxide 17 is deposited on top of the gate
metal layer 14, after which an additional layer of metal
25 18, which may serve as an anode metal layer in the
resultant device, is deposited over the second layer of
oxide 17.

Next, the structure of FIG. 9 is processed in a
manner described above with respect to FIGS. 4-8. In
30 particular, a layer of photoresist is applied to the top
surface of the anode metal layer 18 and is then plasma
etched to remove portions of the layer of photoresist above
the elements 12. The anode metal layer 18 is then etched
using the layer of photoresist as a mask. The layer of
35 photoresist is then removed, and the first and second oxide
layers 13, 17 are etched to expose the field emitter
elements 12, resulting in the structure shown in FIG. 10.

1 It is to be understood that the above-described
embodiments are merely illustrative of some of the many
specific embodiments utilizing the principles of the
present invention. Clearly, numerous and other
5 arrangements can be readily devised by those skilled in the
art without departing from the scope of the invention. For
example, metal may be used instead of polysilicon to form
the substrate and the emitter elements. Also, dry etching
of the oxide and metal layers may be employed where
10 anisotropic etching is critical. In addition, the gate
metal layer may be comprised of metal alloys other than
chromium and gold, such as by molybdenum, for example.

CLAIMS

What is claimed is:

- 1 1. A process for fabricating a field emitter array,
said process comprising the steps of;
 forming substantially conical field emitter elements
on a surface of a substrate;
5 depositing a layer of oxide over said substrate
surface and said field emitter elements;
 depositing a layer of metal over said layer of oxide
to form a gate metal layer;
 depositing a layer of photoresist over said gate
10 metal layer;
 plasma etching said layer of photoresist in an oxygen
atmosphere to cause portions of photoresist above
respective field emitter elements to be removed and thereby
expose respective portions of said gate metal layer above
15 respective tip regions of said field emitter elements;
 etching the exposed portions of said gate metal layer
using said layer of photoresist as a mask;
 removing said layer of photoresist; and
 etching the exposed portions of said layer of oxide
20 to expose said field emitter elements.
- 1 2. A process according to Claim 1 wherein said
substrate and said field emitter elements are of
polysilicon.

1 3. A process according to Claim 1 wherein the step
of depositing a layer of metal over said layer of oxide
comprises the steps of:

 depositing a layer of chromium on said layer of
5 oxide; and
 depositing a layer of gold on said layer of chromium.

1 4. A process according to Claim 1 wherein the step
of plasma etching said layer of photoresist comprises the
steps of:

 placing said substrate in plasma discharge apparatus;
5 evacuating the apparatus to a predetermined pressure;
 passing a regulated flow of oxygen gas over said
substrate; and
 establishing a plasma discharge in said apparatus for
a predetermined time.

1 5. A process for fabricating a field emitter array,
said process comprising the steps of;

 forming substantially conical field emitter elements
on a surface of a substrate;

5 depositing a first layer of metal on said substrate
surface and over said field emitter elements;

 depositing a layer of oxide over said first layer of
metal;

 depositing a second layer of metal over said layer of
10 oxide to form a gate metal layer;

 depositing a layer of photoresist over said gate
metal layer;

plasma etching said layer of photoresist in an oxygen atmosphere to cause portions of photoresist above
15 respective field emitter elements to be removed and thereby
expose respective portions of said gate metal layer above
respective tip regions of said field emitter elements;

etching the exposed portions of said gate metal layer
using the layer of photoresist as a mask;

20 removing said layer of photoresist; and

etching the exposed portions of said layer of oxide
to expose said field emitter elements.

1 6. A process according to Claim 5 wherein said
substrate and said field emitter elements are of
polysilicon.

1 7. A process according to Claim 5 wherein said
first layer of metal is of molybdenum.

1 8. A process according to Claim 5 wherein the step
of depositing a second layer of metal over said layer of
oxide comprises the steps of:

5 depositing a layer of chromium on said layer of
oxide; and

depositing a layer of gold on said layer of chromium.

1 9. A process according to Claim 5 wherein the step
of plasma etching said layer of photoresist comprises the
steps of:
placing said substrate in plasma discharge apparatus;

- 5 evacuating the apparatus to a predetermined pressure;
 passing a regulated flow of oxygen gas over said
 substrate; and
 establishing a plasma discharge in said apparatus for
 a predetermined time.

- 1 10. A process for fabricating a field emitter
 triode array, said process comprising the steps of:
 forming substantially conical field emitter elements
 on a surface of a substrate;
5 depositing a first layer of oxide over said substrate
 surface and said field emitter elements;
 depositing a layer of metal over said layer of oxide
 to form a gate metal layer;
 depositing a first layer of photoresist over said
10 gate metal layer;
 plasma etching said first layer of photoresist in an
 oxygen atmosphere to cause portions of photoresist above
 respective field emitter elements to be removed and thereby
 expose respective portions of said gate metal layer above
15 respective tip regions of said field emitter elements;
 etching the exposed portions of said gate metal layer
 using said first layer of photoresist as a mask;
 removing said first layer of photoresist;
 depositing a second layer of oxide over said gate
20 metal layer and over respective portions of said first
 oxide layer not covered by said gate metal layer;
 depositing a layer of metal over said second layer of
 oxide to form an anode metal layer;
 depositing a second layer of photoresist over said
25 anode metal layer;

plasma etching said second layer of photoresist in an oxygen atmosphere to cause portions of photoresist in said second layer above respective field emitter elements to be removed and thereby expose respective portions of said anode metal layer above respective tip regions of said field emitter elements;

etching the exposed portions of said anode metal layer using said second layer of photoresist as a mask; and etching the exposed portions of said first and second layers of oxide to expose said field emitter elements.

11. A process according to Claim 10 wherein said substrate and said field emitter elements are of polysilicon.

12. A process according to Claim 11 wherein the step of depositing a layer of metal over said layer of oxide to form a gate metal layer comprises the steps of:

depositing a layer of chromium on said layer of oxide; and depositing a layer of gold on said layer of chromium.

13. A process according to Claim 1 wherein the steps of plasma etching said first and said second layers of photoresist each comprises the steps of:

placing said substrate in plasma discharge apparatus; evacuating the apparatus to a predetermined pressure; passing a regulated flow of oxygen gas over said substrate; and

establishing a plasma discharge in said apparatus for a predetermined time.

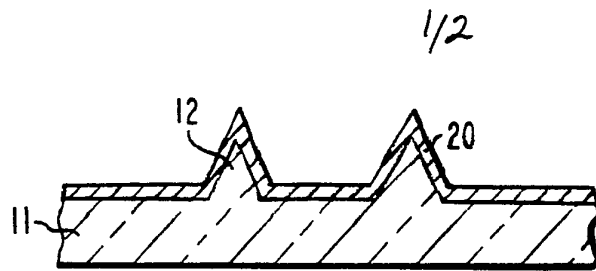


Fig. 1.

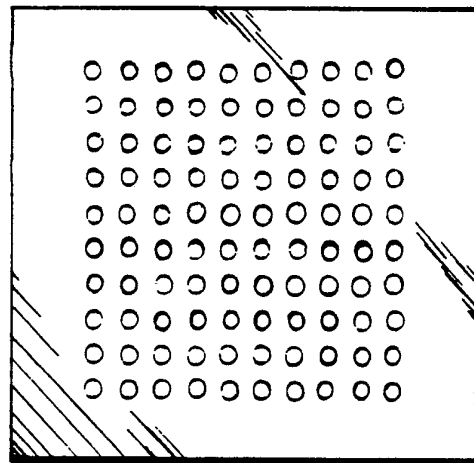


Fig. 2.

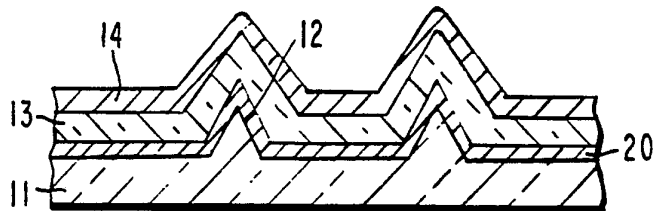


Fig. 3.

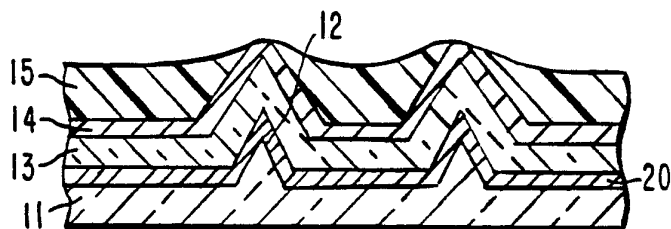


Fig. 4.

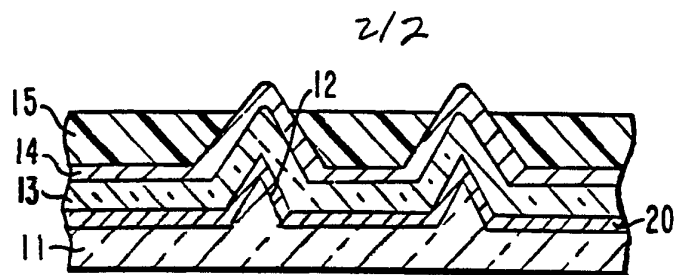


Fig. 5.

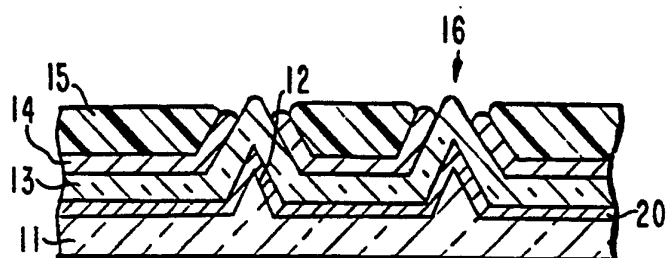


Fig. 6.

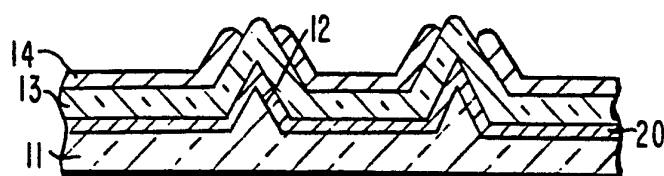


Fig. 7.

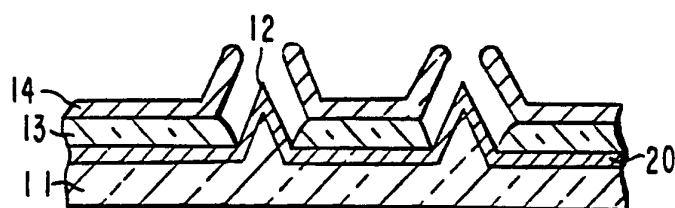


Fig. 8.

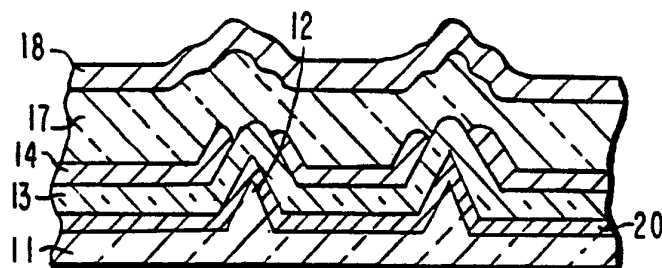


Fig. 9.

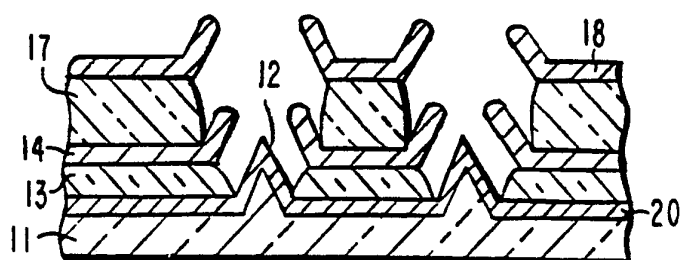


Fig. 10.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 90/02184

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)⁶

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01J09/02

II. FIELDS SEARCHED

Minimum Documentation Searched⁷

Classification System

Classification Symbols

Int.Cl. 5

H01J09/00 ; H01J01/00

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched⁸III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹

Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
A	EP,A,0306173 (GEC) 08 March 1989 see column 3, line 29 - column 5, line 57 see column 6, lines 32 - 43; figures 1-12, 16, 17 ---	1, 2, 5, 6, 7, 10, 11
A	US,A,4008412 (HITACHI) 15 February 1977 see column 3, lines 47 - 67 see column 6, lines 1 - 68; figures 4a-7b (cited in the application) ---	2-4, 6, 8, 9, 11-13

¹⁰ Special categories of cited documents : ¹⁰¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance¹⁰ "E" earlier document but published on or after the international filing date¹⁰ "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)¹⁰ "O" document referring to an oral disclosure, use, exhibition or other means¹⁰ "P" document published prior to the international filing date but later than the priority date claimed¹⁰ "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention¹⁰ "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step¹⁰ "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.¹⁰ "&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search

03 AUGUST 1990

Date of Mailing of this International Search Report


28. 08. 90

International Searching Authority

EUROPEAN PATENT OFFICE

Signature of Authorized Officer

ROWLES K.E.G.



**ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.**

US 9002184
SA 36859

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
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03/08/90

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0306173	08-03-89	GB-A- 2209432 JP-A- 1128332	10-05-89 22-05-89

US-A-4008412	15-02-77	JP-A,B,C51021471 DE-A,B,C 2536363	20-02-76 26-02-76
