



(51) International Patent Classification:

H04B 1/16 (2006.01) H03D 1/22 (2006.01)

(21) International Application Number:

PCT/EP2019/064182

(22) International Filing Date:

31 May 2019 (31.05.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: STICHTING IMEC NEDERLAND

[NL/NL]; High Tech Campus 31, 5656 AE Eindhoven (NL).

(72) Inventors: KLUMPERINK, Eric Antonius Maria; c/o

IMEC VZW, patent department Kapeldreef 75, 3001 Leuven Belgium (BE). PURUSHOTHAMAN, Vijaya Kumar; c/o IMEC VZW, patent department Kapeldreef 75, 3001 Leuven Belgium (BE).

(74) Agent: KÖRFER ET AL., Thomas; Mitscherlich

PartmbB, Patent- und Rechtsanwälte, Sonnenstraße 33, 80331 München (DE).

(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

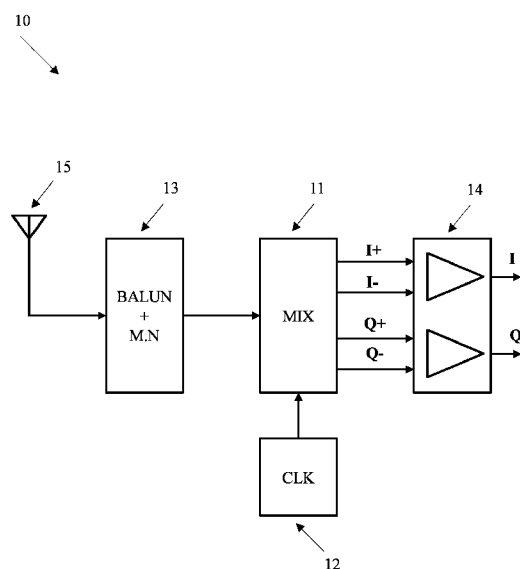
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: RADIO FREQUENCY RECEIVER AND METHOD FOR DOWN-CONVERTING SIGNALS TO BASEBAND SIGNAL COMPONENTS



(57) Abstract: A radio frequency receiver (10) comprising a mixer circuitry (11) to down-convert a received signal, which is transported on a signal line (41, 43), to baseband signal components is provided. The mixer circuitry (11) comprises a plurality of switched capacitors (C_{R1} - C_{R8}), each connected to the signal line (41, 43) through a signal side node (45₁-45₈) and to a corresponding switch (M_1 - M_4) through a switch side node (47₁-47₈). In this context, a voltage is sensed at each switch side node (47₁-47₈) of the plurality of switched capacitors (C_{R1} - C_{R8}) and is read out through a respective grounded capacitor (C_{B1} - C_{B4}).

Fig. 3

**Radio frequency receiver and method for down-converting
signals to baseband signal components**

The invention relates to a radio frequency receiver and a
5 corresponding method to down-convert a received signal to
baseband signal components, especially for a mixer-first
receiver construction which omits a low noise amplifier
before the mixer.

10 In order to realize a highly-linear band-selective
electronic receiver for data communication purposes in
Complementary Metal-Oxide Semiconductor (CMOS) integrated
circuit technology, mixer-first receivers have been
proposed which omit a low noise amplifier before the
15 mixer, but rather put the mixer first. A passive mixer-
first receiver comprising switched R-C circuits can
advantageously provide both frequency conversion and
narrow-band high-Q filtering with a center frequency that
is controlled by the switching frequency. Generally, such
20 a passive mixer-first receiver comprises N number of
switched R-C signal paths that are driven by non-
overlapping clocks with the same frequency but with
different phases, separated by $360/N$ degrees.

25 The switched R-C circuits with Metal-Oxide Semiconductor
Field Effect Transistor (MOSFET) switches in N-path mixers
exploit the condition that the voltage on the capacitors
becomes virtually constant for an input frequency close to
the switching frequency by assuming the RC time constants
30 much larger than the on-time of the switches. Fig. 1a
illustrates a technique for top-plate mixing where V_{IN} is
the amplitude of the antenna signal and a switch is placed
between the antenna signal node V_{RF} and the top plate of a
grounded capacitor C. The baseband signal is stored in the

grounded capacitor C and is read out during the time when the switch is open and the antenna signal V_{IN} is no longer directly affecting the capacitor voltage. However, the MOSFET switch suffers from the modulation of channel resistance that significantly limits its linearity.

Fig. 1b illustrates a technique for bottom-plate mixing where the antenna signal node V_{RF} is connected to the top plate of the capacitor C and the bottom plate is switched to ground. In this case, the capacitor C remains always connected to the antenna signal V_{IN} and thereby the antenna signal V_{IN} and the baseband signal both affect the capacitor voltage. By avoiding modulation of the source voltage of the MOSFET, the channel resistance induced distortion is effectively reduced and therefore the bottom-plate mixing technique achieves superior linearity compared to the top-plate mixing technique. However, the bottom-plate mixing technique introduces a baseband signal read out problem since the baseband signal is no longer available on a grounded capacitor as described above. When the switch is open, the capacitor C becomes floating and stores the down-converted baseband voltage across its terminal without being referenced to ground. Conventionally, a read out of the baseband signal is performed in the current domain using resistors that perform V-I conversion. Disadvantageously, such method for reading out the baseband signal in a bottom-plate mixing configuration introduces gain loss and additional noise.

For example, U.S. Patent No. 9,692,471 B2 discloses a wireless receiver with bottom-plate configuration, having an out-band signal bypass filter, a mixer and a baseband circuit. The out-band signal bypass filter provides an out-band signal bypass path from where the mixer receives

a filtered signal. The baseband circuit is coupled to the mixer for generation of an in-phase signal and a quadrature phase signal. As illustrated in Fig. 2, the bottom-plate configuration 1 is simply used as band-pass filter since the bottom-plate configuration 1 complicates the possibility of extracting the baseband signal from the capacitors 2, 2'. The RF voltage 3, 3' from the top-plate of the capacitors 2, 2' is down-converted using a cross-coupled switch R-C network 4.

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Accordingly, the object of the invention is to provide a radio frequency receiver and a method to down-convert a received signal to baseband signal components, especially for a mixer-first receiver construction that utilizes bottom-plate mixing technique to achieve high linearity without requiring additional V-I conversion.

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The object is solved by the features of the first independent claim for the radio frequency receiver and by the features of the second independent claim for the method. The dependent claims contain further developments.

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According to a first aspect of the invention, a radio frequency receiver comprising a mixer circuitry to down-convert a received signal, which is transported on a signal line, to baseband signal components is provided. The mixer circuitry comprises a plurality of switched capacitors, each connected to the signal line through a signal side node and to a corresponding switch through a switch side node. A voltage is sensed at each switch side node of the plurality of switched capacitors and is read out through a respective grounded capacitor. In this context, the voltages at the switch side nodes of the plurality of switched capacitors correspond to baseband

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signal components. Close to the local oscillator frequency, the signal contributions on two switched capacitors with 180 degree phase difference have approximately equal but opposite amplitudes, and hence the capacitor voltages are intrinsically added. Therefore, reading out the baseband signal is performed by directly sensing the voltage at the bottom plate of the switched capacitors, which advantageously eliminates the necessity for an additional V-I conversion.

10

According to a first preferred implementation form of said first aspect of the invention, the mixer circuitry comprises an even number of mixing paths, each comprising at least one of the plurality of switched capacitors.

15 Advantageously, a circuital symmetry can be achieved.

According to a second preferred implementation form of said first aspect of the invention, the mixer circuitry further comprises a plurality of read-out switches, coupled between each of the switch side nodes and the respective grounded capacitor. In addition, each grounded capacitor can be advantageously reused for reading out voltages from different switch side nodes by means of the plurality of read-out switches.

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According to a further preferred implementation form of said first aspect of the invention, the radio frequency receiver further comprises a clock generating circuitry to generate non-overlapping clocks, preferably at least four-phase non-overlapping clocks in order to drive the plurality of switched capacitors and the plurality of read-out switches. A higher order non-overlapping clocks, for instance, eight-phase or twelve-phase non-overlapping clocks can be implemented if harmonic rejection mixing is

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targeted. A four-phase non-overlapping clock generation is indeed useful for I/Q generation, however, an eight-phase non-overlapping clocks might also be useful as it reduces conversion loss, and a corresponding eight signal read-out
5 may enable harmonic rejection. Advantageously, synchronous switching is achieved for the switched capacitors as well as for the read-out switches.

According to a further preferred implementation form of
10 said first aspect of the invention, the switched capacitors are driven in rotation such that at a given clock phase at least two switched capacitors are out of phase to each other and are connected in series. Since the mixer circuitry comprises an even number of mixing paths,
15 there are at least two mixing paths that are out of phase to each other for any given clock phase. Furthermore, considering the fact that a series connection of two capacitor voltages allows for subtracting voltage signals, the two anti-phase signals corresponding to the out of
20 phase mixing paths lead the series capacitor subtraction to addition of the amplitudes, thereby doubling the amplitude of the sensed voltage at a given switched capacitor. Advantageously, a doubling of voltage gain is achieved for the baseband signal.

25

According to a further preferred implementation form of said first aspect of the invention, the radio frequency receiver further comprises an input circuitry, configured to transform the received signal into a differential
30 signal having a positive and a negative partial signal. Advantageously, a fully differential configuration is realized with balanced radio frequency input voltages having an equal amplitude with 180 degree phase shift.

According to a further preferred implementation form of said first aspect of the invention, the input circuitry further comprises an impedance matching network, preferably a low-loss LC network. Advantageously, the low-
5 loss LC network also provides additional filtering of high-frequency folding products.

According to a further preferred implementation form of said first aspect of the invention, the mixer circuitry
10 further comprises bias switches to set a common-mode bias voltage of the mixer circuitry and the plurality of read-out switches through an external supply. Therefore, sufficient DC offset voltage is provided to turn on the switches and to be biased in the active region.

15 According to a further preferred implementation form of said first aspect of the invention, the radio frequency receiver further comprises an output circuitry coupled to the mixer circuitry to output the baseband signal components. The output circuitry preferably comprises
20 differential amplification means to amplify the difference between two input voltages but suppresses any voltage common to the two inputs such that the output is proportional to the difference between the two inputs.

25 According to a further preferred implementation form of said first aspect of the invention, the radio frequency receiver further comprises an antenna for receiving radio frequency signals. Additionally or alternatively, the
30 radio frequency receiver comprises radio frequency connectors to receive radio frequency signals via wires.

According to a second aspect of the invention, a method for down-converting a received signal, which is

transported on a signal line, to baseband signal components in a radio frequency receiver is provided. The method comprises the steps of connecting each of a plurality of switched capacitors to the signal line through a signal side node, connecting each of the plurality of switched capacitors to a corresponding switch through a switch side node, and sensing a voltage at each switch side node of the plurality of switched capacitors and reading it out through a respective grounded capacitor. As a result, reading out the baseband signal is performed by directly sensing the voltage at the bottom plate of the switched capacitors, which advantageously eliminates the necessity for an additional V-I conversion.

According to a first preferred implementation form of said second aspect of the invention, the method further comprises the step of arranging an even number of mixing paths, each comprising at least one of the plurality of switched capacitors. Advantageously a circuitual symmetry can be achieved.

According to a second preferred implementation form of said second aspect of the invention, the method further comprises the step of driving the switched capacitors in rotation such that at a given clock phase at least two switched capacitors are out of phase to each other and are connected in series. Since the mixer circuitry comprises an even number of mixing paths, there are at least two mixing paths that are out of phase to each other for any given clock phase. Furthermore, considering the fact that a series connection of two capacitor voltages allows for subtracting voltage signals, the two anti-phase signals corresponding to the out of phase mixing paths lead the series capacitor subtraction to addition of the amplitudes

and thereby doubling the amplitude of the sensed voltage at a given switched capacitor. Advantageously, a doubling of voltage gain is achieved for the baseband signal.

5 Exemplary embodiments of the invention are now further explained with respect to the drawings by way of example only, and not for limitation. In the drawings:

10 Fig. 1a shows a top-plate mixing technique for switched R-C mixing path,

Fig. 1b shows a bottom-plate mixing technique for switched R-C mixing path,

15 Fig. 2 shows a wireless receiver using bottom-plate configuration according to the prior art,

20 Fig. 3 shows a block diagram of the radio frequency receiver according to the first aspect of the invention,

25 Fig. 4 shows a first exemplary embodiment of the mixer circuitry according to the first aspect of the invention,

Fig. 5a shows the read out technique for a single ended configuration at a clock phase 0^0 ,

30 Fig. 5b shows the read out technique for a single ended configuration at a clock phase 90^0 ,

Fig. 6a shows the read out technique for a fully differential configuration at a phase 0^0 ,

Fig. 6b shows the read out technique for a fully differential configuration at a phase 180^0 ,

Fig. 7 shows a second exemplary embodiment of the mixer circuitry according to the first aspect of the invention, and

Fig. 8 shows a flow chart of an exemplary embodiment of the second aspect of the invention.

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Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings. However, the following embodiments of the present invention may be variously modified and the range of the present invention is not limited by the following embodiments.

15

Fig. 1a, Fig. 1b and Fig. 2 have already been described with respect to the background of the invention.

20

In Fig. 3, a block diagram of the radio frequency receiver 10 according to the first aspect of the invention is illustrated. The radio frequency receiver comprises a mixer circuitry 11, a clock generating circuitry 12, and input circuitry 13, an output circuitry 14 and an antenna 15. The input circuitry 13 receives a radio frequency signal through the antenna 15 and transforms the received radio frequency signal into a differential signal having a positive partial signal RF+ and a negative partial signal RF-, which are not shown in Fig. 3. In this context, the antenna 15 can be generalized as a radio frequency signal source with a series source resistance. The transformation of the received signal into the differential signal can be achieved by means of, for example a balanced to unbalanced

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radio frequency transformer (Balun) with a preferable turns ratio.

The input circuitry 13 might further comprise a low-loss
5 LC network to perform impedance matching at the input side
that is coupled to the mixing circuitry 11. The
functionalities and constructions of a Balun and a LC
impedance matching network are known in the art, therefore
these circuitries are not described here in greater
10 details. Instead of receiving radio frequency signals
through the antenna 15, the input circuitry 13 may
comprise radio frequency connectors to receive signals
via, for example, a coaxial cables.

15 The clock generating circuitry 12 comprises for instance,
frequency divider means, for example a modulo counter to
provide non-overlapping clocks. The number of clock phases
and the duty cycle depend on the number of mixing paths
utilized in the mixer circuitry 11. In the following
20 embodiments, four-phase non-overlapping clocks are
illustrated with a 25% duty cycle that are generated by a
divide-by-2 circuit. However, the invention is not limited
to said arrangement only and any divide-by circuit of N
order with different duty cycle or other means to generate
25 multi-phase clocks is covered within the scope of the
invention.

The mixer circuitry 11 performs modulation of the
differential radio frequency signal and with respect to
30 the clock phases that drive the mixing paths, the
differential in-phase baseband signal components I+, I-
and the differential quadrature baseband signal components
Q+, Q- are fed to the output circuitry 14 that is coupled
to the mixer circuitry 11. The output circuitry 14

performs differential amplification such that the output is proportional to the difference between the two inputs. The output circuitry 14 outputs the in-phase baseband signal component I and the quadrature baseband signal component Q.

In Fig. 4, a first exemplary embodiment of the mixer circuitry according to the first aspect of the invention is illustrated. The differential signal from the input circuitry 13 is transported on the signal paths 41, 43 of the mixer circuitry 11. Herein the mixer circuitry 11 comprises four mixing paths, however it is clear that any lower or higher number of mixing paths can be used. Although it is advantageous that the mixer circuitry 11 comprises an even number of mixing paths so that there are at least two mixing paths which are out of phase during a given clock phase.

In this embodiment the mixer circuitry 11 comprises a plurality of switched capacitors C_{R1} , C_{R2} , C_{R3} , C_{R4} , C_{R5} , C_{R6} , C_{R7} , C_{R8} that comprise a respective signal side node 45₁, 45₂, 45₃, 45₄, 45₅, 45₆, 45₇, 45₈ and a respective switch side node 47₁, 47₂, 47₃, 47₄, 47₅, 47₆, 47₇, 47₈. Each of the signal side node 45₁-45₈ is connected to corresponding signal lines 41, 43 that comprise the positive partial signal and the negative partial signal RF+, RF-. Particularly, the signal side nodes 45₁-45₄ are connected to the signal line 41 that transports the positive partial signal RF+ and the signal side nodes 45₅-45₈ are connected to the signal line 43 that transports the negative partial signal RF-.

In this embodiment each pair of the switched side node 47₁-47₈ is differentially connected to each other through

a respective switch M_1 , M_2 , M_3 , M_4 . Particularly, node 47₁ is differentially connected to node 47₅ through the switch M_1 , node 47₂ is differentially connected to node 47₆ through the switch M_2 , node 47₃ is differentially connected to node 47₇ through the switch M_3 and node 47₄ is differentially connected to node 47₈ through the switch M_4 . Hence, the total number of switched capacitors C_{R1} - C_{R8} depends on the number of mixing paths as well as on the differential configuration of the mixer circuitry 11.

10

The mixer circuitry 11 further comprises grounded capacitors C_{B1} , C_{B2} , C_{B3} , C_{B4} which correspond to each of the differential in-phase and quadrature baseband signal components. The grounded capacitors C_{B1} - C_{B4} are alternatively connected to each switch side node 47₁-47₈ through read-out switches 49₁, 49₂, 49₃, 49₄, 49₅, 49₆, 49₇, 49₈. To facilitate clear understanding of the operation, the grounded capacitors C_{B1} - C_{B4} along with the read-out switches 49₁-49₈ are drawn separately where similar node references are maintained to translate an electrical connection. The read-out switches 49₁-49₈ are switched with respect to the clock phases and the corresponding differential baseband component is stored in the respective grounded capacitor C_{B1} - C_{B4} . For example, the grounded capacitor C_{B1} is used to read-out the baseband signal component at the switch side node 47₇ of the switched capacitor C_{R7} through the read-out switch 49₇ during the clock phase Φ_1 . The same grounded capacitor C_{B1} is re-used to read-out the baseband signal component at the switch side node 47₁ of the switched capacitor C_{R1} through the read-out switch 49₁ during the clock phase Φ_3 .

The mixer circuitry 11 further comprises bias switches 48₁, 48₂, 48₃, 48₄, 48₅, 48₆, 48₇, 48₈ to periodically set a

common-mode bias voltage V_C of the mixer circuitry 11 and the plurality of read-out switches 49₁-49₈ through an external supply that is not shown in Fig. 4.

5 Referring to Fig. 5a and Fig. 5b, the baseband signal component read-out technique in a single ended configuration is illustrated in greater details. A four-path single ended mixer with bottom plate configuration is shown where the input radio frequency signal RF is down
10 converted to baseband signal components by clocks Φ_0 , Φ_{90} , Φ_{180} and Φ_{270} operating at phases 0° , 90° , 180° and 270° on the switches M_1 , M_2 , M_3 and M_4 respectively. It is assumed that the down-converted baseband voltage across the switched capacitors C_{R1} - C_{R4} are V_{R0} , V_{R90} , V_{R180} and V_{R270}
15 respectively.

In Fig. 5a, read-out of the baseband voltage is performed at the clock phase Φ_0 . The baseband voltages V_{R0} and V_{R180} are in anti-phase since the clock phases Φ_0 and Φ_{180} that
20 are driving their corresponding switches M_1 and M_3 are 180 degree phase-shifted. Therefore, the in-band instantaneous voltages can be expressed as:

$$V_{R0} = -V_{R180}$$

25

When switch M_1 is conducting, the bottom-plate of the capacitor C_{R1} is connected to ground and the other capacitors C_{R2} , C_{R3} , C_{R4} remain floating. When sensing from node A, the capacitors C_{R3} and C_{R1} are connected in series
30 to ground. Therefore the resultant voltage at node A is:

$$V_A = -V_{R180} + V_{R0} = 2 \times V_{R0}$$

As a result, a voltage gain of 2 is achieved for baseband signals by simply sensing the voltage from the node A.

In Fig. 5b, read-out of the baseband voltage is performed
 5 at the clock phase Φ_{90} . The baseband voltages V_{R90} and V_{R270} are in anti-phase since the clock phases Φ_{90} and Φ_{270} that are driving their corresponding switches M_2 and M_4 are 180 degree phase-shifted. Therefore, the in-band instantaneous voltages can be expressed as:

10

$$V_{R90} = -V_{R270}$$

When switch M_2 is conducting, the bottom-plate of the capacitor C_{R2} is connected to ground and the other
 15 capacitors C_{R1} , C_{R3} , C_{R4} remain floating. When sensing from node B, the capacitors C_{R2} and C_{R4} are connected in series to ground. Therefore the resultant voltage at node B is:

20

$$V_B = -V_{R270} + V_{R90} = 2 \times V_{R90}$$

As a result, a voltage gain of 2 is achieved for baseband signals by simply sensing the voltage from the node B.

Referring to Fig. 6a and Fig. 6b, the baseband signal
 25 component read-out technique in a fully differential configuration is illustrated in greater details. A four-path fully differential mixer with bottom plate configuration is shown where the balanced radio frequency input signals $RF+$, $RF-$ are down converted to baseband
 30 signal components by clocks Φ_0 , Φ_{90} , Φ_{180} and Φ_{270} operating at phases 0° , 90° , 180° and 270° on the switches M_1 , M_2 , M_3 and M_4 respectively. The balanced differential inputs $RF+$, $RF-$ result in a zero voltage point that occurs in the middle of the inversion region in the channel when a

switch M_1 - M_4 is closed. It is assumed that the down-converted baseband voltage across the switched capacitors C_{R1} - C_{R4} is V_{R0} , V_{R90} , V_{R180} and V_{R270} , respectively. Likewise, the down-converted baseband voltage across the switched capacitors C_{R5} - C_{R8} are assumed to be $-V_{R0}$, $-V_{R90}$, $-V_{R180}$ and $-V_{R270}$, respectively.

In Fig. 6a, read-out of the baseband voltage is performed at the clock phase Φ_0 . The baseband voltages V_{R0} and V_{R180} are in anti-phase since the clock phases Φ_0 and Φ_{180} that are driving their corresponding switches M_1 and M_3 are 180 degree phase-shifted. When M_1 is conducting, the positive portion of the baseband signal components can be sensed at the bottom-plate of the switched capacitor C_{R3} and the negative portion of the baseband signal component can be sensed at the bottom-plate of the switched capacitor C_{R7} . Since, the zero voltage point behaves similar to ground in the single-ended configuration, the resulting positive baseband signal component V_{B+} as well as the resulting negative baseband signal component V_{B-} correspond to a double voltage gain of the respective positive and negative baseband signal components as shown in Fig. 5a. The additional read-out capacitors C_{B1} and C_{B2} are used to read-out the respective baseband signal components V_{B+} , V_{B-} .

In Fig. 6b, the additional read-out capacitors C_{B1} , C_{B2} are re-used at the clock phase Φ_{180} . When M_3 is conducting the positive portion of the baseband signal components can be sensed at the bottom-plate of the switched capacitor C_{R5} and the negative portion of the baseband signal component can be sensed at the bottom-plate of the switched capacitor C_{R1} . Since the input signal is fully differential and 180 degree phase shifted clocks are

driving the switches M_1 and M_3 , the read-out capacitors C_{B1} , C_{B2} are effectively re-used to read-out the respective baseband signal components V_{B+} , V_{B-} . Furthermore, an additional order of infinite impulse response filtering is achieved in this technique since the read-out capacitors C_{B1} , C_{B2} share the charges with two switched capacitors C_{R1} , C_{R3} resp. C_{R5} , C_{R7} at different time instants.

In Fig. 7, a second exemplary embodiment of the mixer circuitry 21 according to the first aspect of the invention is illustrated. The second exemplary embodiment of the mixer circuitry 21 differs from the first exemplary embodiment of the mixer circuitry 11 according to Fig. 4 in that the grounded capacitors C_{B1} , C_{B2} , C_{B3} , C_{B4} , C_{B5} , C_{B6} , C_{B7} , C_{B8} are not re-used and each of the grounded capacitors C_{B1} - C_{B8} are dedicated to a corresponding switch side node 47_1 - 47_8 through the plurality of read-out switches 49_1 - 49_8 . Such a configuration of reading out the baseband signal components through dedicated grounded capacitors C_{B1} - C_{B8} facilitates direct digital conversion of the baseband signal components.

In Fig. 8, a flow chart of an exemplary embodiment of the inventive method according to the second aspect of the invention is illustrated. In a first step S1, each of a plurality of switched capacitors are connected to the signal line through a signal side node. In a second step S2, each of the plurality of switched capacitors are connected to a corresponding switch through a switch side node. Finally, in a third step S3, a voltage at each switch side node of the plurality of switched capacitors is sensed and is read out through a respective grounded capacitor.

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Numerous changes to the disclosed embodiments
5 can be made in accordance with the disclosure herein without departing from the spirit or scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above described embodiments. Rather, the scope of the invention
10 should be defined in accordance with the following claims and their equivalents.

Although the invention has been illustrated and described with respect to one or more implementations, equivalent
15 alterations and modifications will occur to others skilled in the art upon the reading and understanding of this specification and the annexed drawings. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several
20 implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application.

Claims

1. A radio frequency receiver (10) comprising a mixer circuitry (11) to down-convert a received signal, which is transported on a signal line (41, 43), to baseband signal components, wherein the mixer circuitry (11) comprises a plurality of switched capacitors (C_{R1} - C_{R8}), each connected to the signal line (41, 43) through a signal side node (45₁-45₈) and to a corresponding switch (M_1 - M_4) through a switch side node (47₁-47₈),

characterized in that,

a voltage is sensed at each switch side node (47₁-47₈) of the plurality of switched capacitors (C_{R1} - C_{R8}) and is read out through a respective grounded capacitor (C_{B1} - C_{B4}).

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2. The radio frequency receiver according to claim 1, wherein the voltages at the switch side nodes (47₁-47₈) of the plurality of switched capacitors (C_{R1} - C_{R8}) correspond to baseband signal components.

20

3. The radio frequency receiver according to claim 1 or 2, wherein the mixer circuitry (11) comprises an even number of mixing paths, each comprising at least one of the plurality of switched capacitors (C_{R1} - C_{R8}).

25

4. The radio frequency receiver according to any of claims 1 to 3, wherein the mixer circuitry (11) further comprises a plurality of read-out switches (49₁-49₈), coupled between each of the switch side nodes (47₁-47₈) and the respective grounded capacitor (C_{B1} - C_{B4}).

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5. The radio frequency receiver according to any of claims 1 to 4,

further comprising a clock generating circuitry (12) to generate non-overlapping clocks, preferably at least four-phase non-overlapping clocks in order to drive the plurality of switched capacitors (C_{R1} - C_{R8}) and the plurality of read-out switches (C_{B1} - C_{B4}).

6. The radio frequency receiver according to claim 5, wherein the switched capacitors (C_{R1} - C_{R8}) are driven in rotation such that at a given clock phase at least two switched capacitors (C_{R1} - C_{R8}) are out of phase to each other and are connected in series.

7. The radio frequency receiver according to any of claims 1 to 6, further comprising an input circuitry (13), configured to transform the received signal into a differential signal having a positive and a negative partial signal.

8. The radio frequency receiver according to claim 7, wherein the input circuitry (13) further comprises an impedance matching network, preferably a low-loss LC network.

9. The radio frequency receiver according to any of claims 1 to 8, wherein the mixer circuitry (11) further comprises a first terminal (41) and a second terminal (43) to receive the positive and negative partial signal of the differential signal respectively.

10. The radio frequency receiver according to any of claims 1 to 9, wherein the mixer circuitry (11) further comprises bias switches (48_1 - 48_8) to set a common-mode bias voltage of

the mixer circuitry (11) and the plurality of read-out switches (C_{B1} - C_{B4}) through an external supply.

11. The radio frequency receiver according to any of
5 claims 1 to 10,

further comprising an output circuitry (14) coupled to the mixer circuitry (11) to output the baseband signal components.

10 12. The radio frequency receiver according to any of claims 1 to 11,

further comprising an antenna (15) for receiving radio frequency signals.

15 13. A method for down-converting a received signal, which is transported on a signal line, to baseband signal components in a radio frequency receiver comprising a mixer circuitry, wherein the method comprises the steps of:

20 connecting each of a plurality of switched capacitors to the signal line through a signal side node, and

connecting each of the plurality of switched capacitors to a corresponding switch through a switch side node,

25 **characterized by**

sensing a voltage at each switch side node of the plurality of switched capacitors and reading it out through a respective grounded capacitor.

30 14. The method according to claim 13,
wherein the method further comprises the step of arranging an even number of mixing paths, each comprising at least one of the plurality of switched capacitors.

15. The method according to claim 13,
wherein the method further comprises the step of driving
the switched capacitors in rotation such that at a given
clock phase at least two switched capacitors are out of
5 phase to each other and are connected in series.

1/8

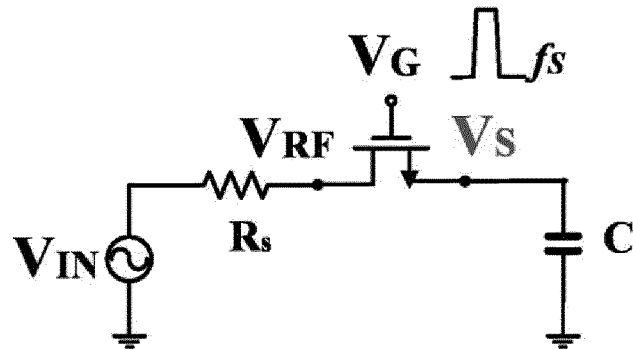


Fig. 1a - Prior Art

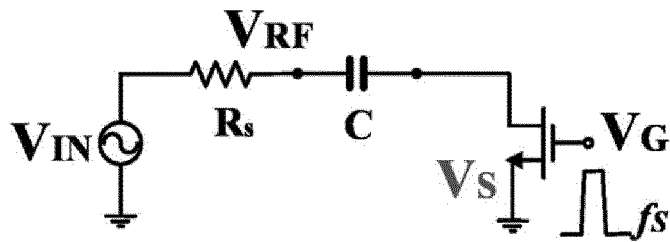


Fig. 1b - Prior Art

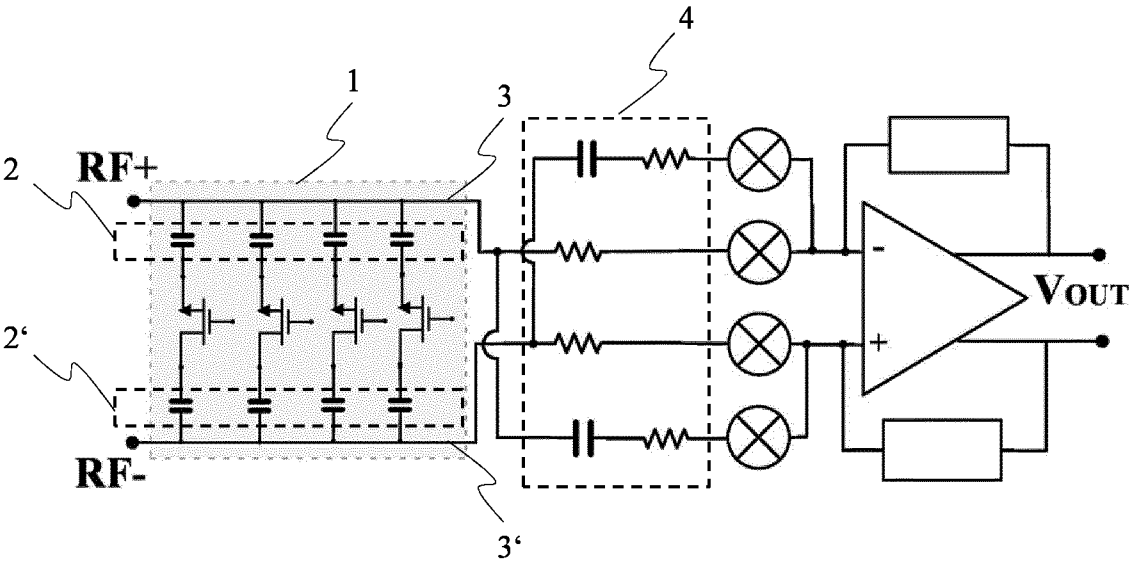


Fig. 2 - Prior Art

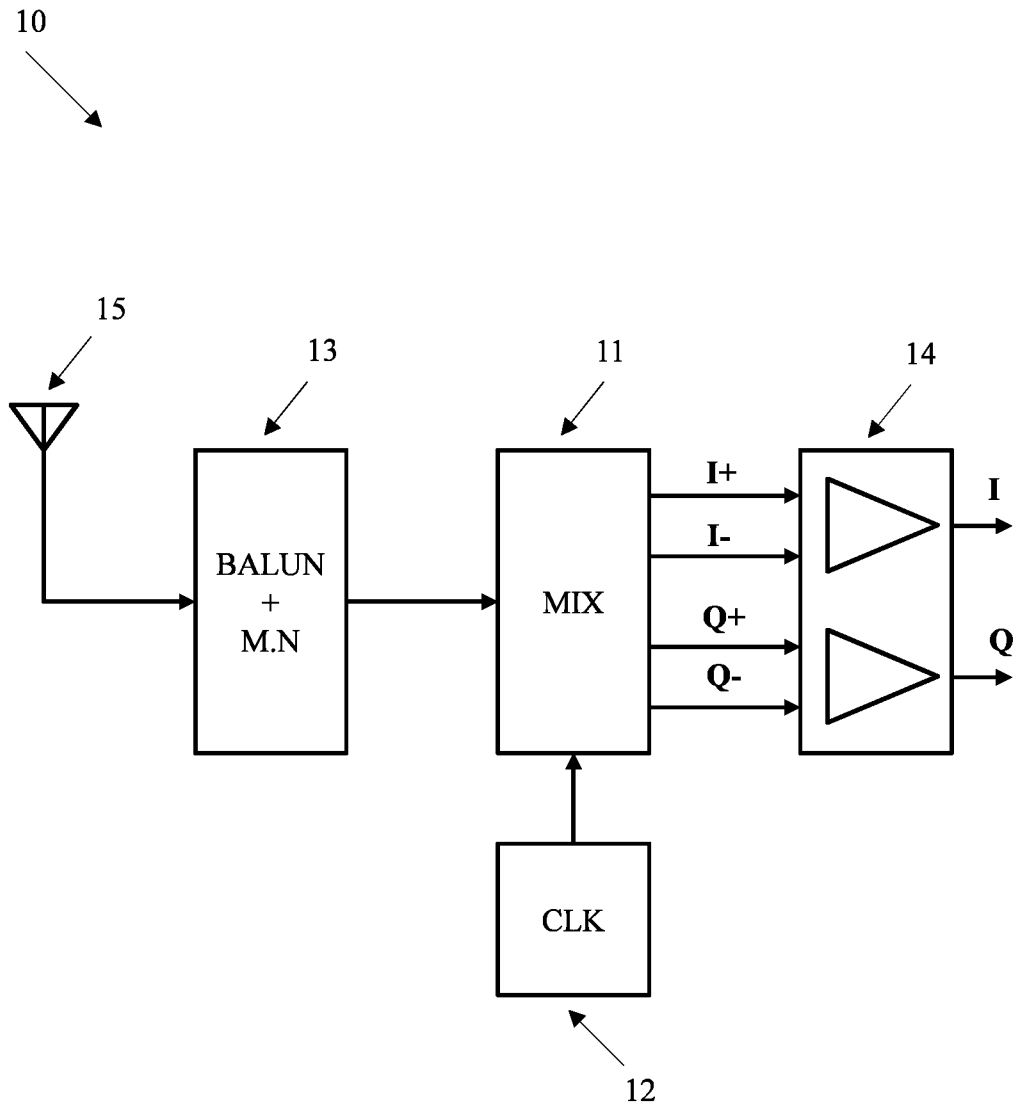


Fig. 3

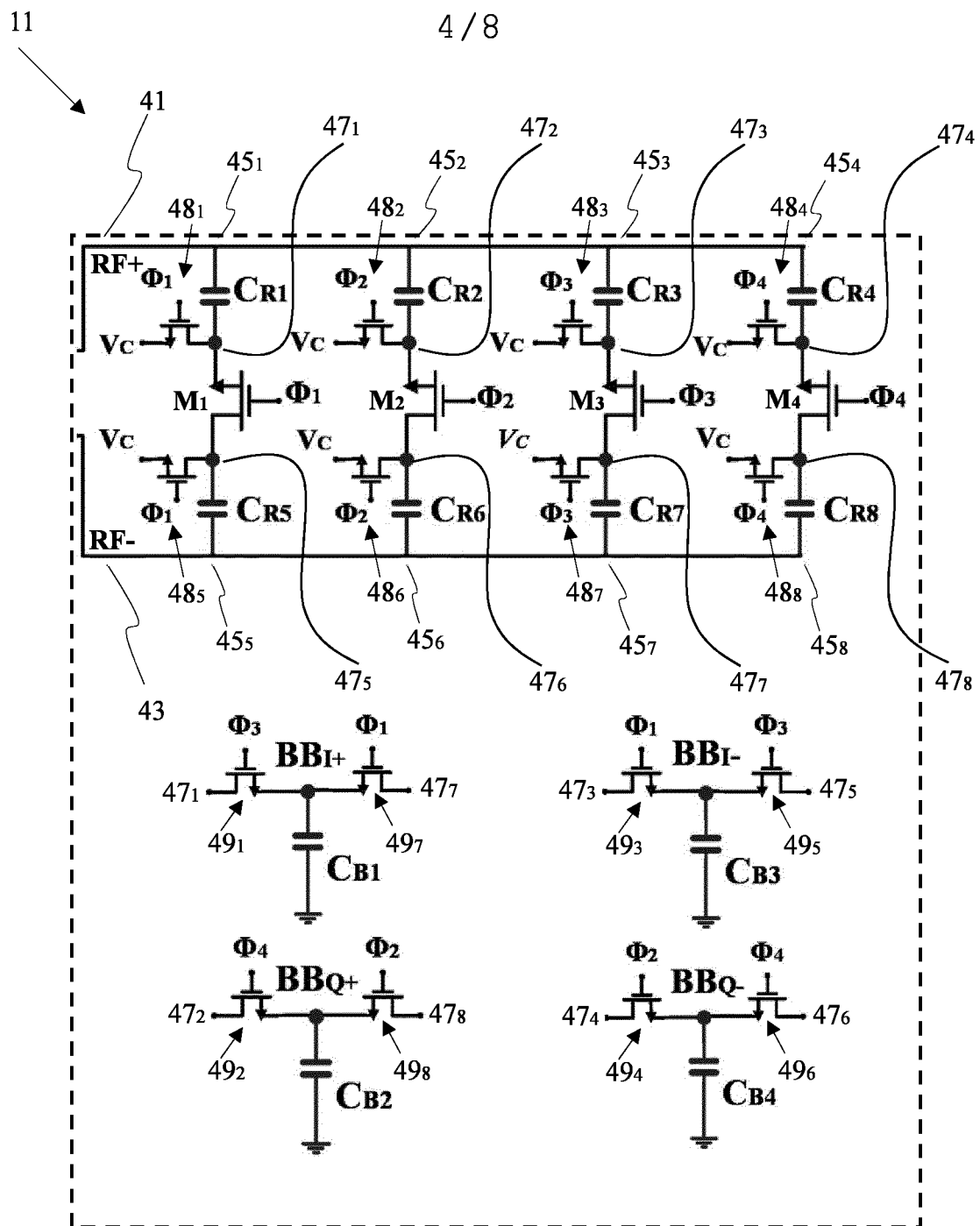


Fig. 4

5/8

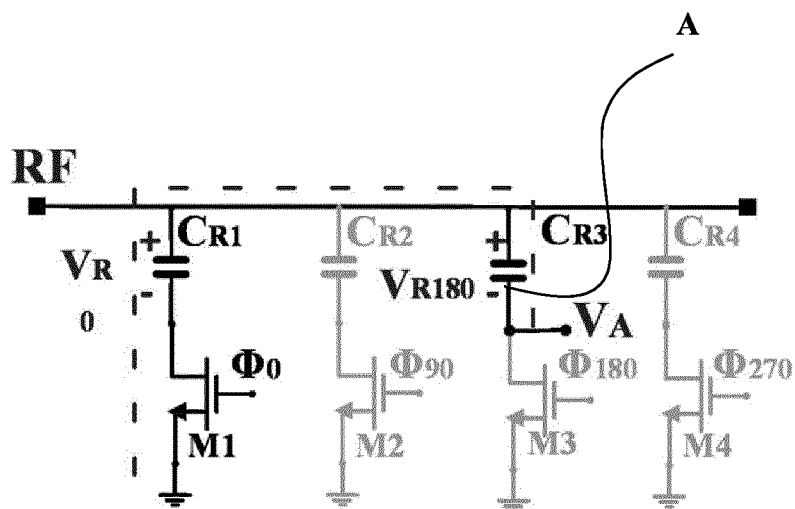


Fig. 5a

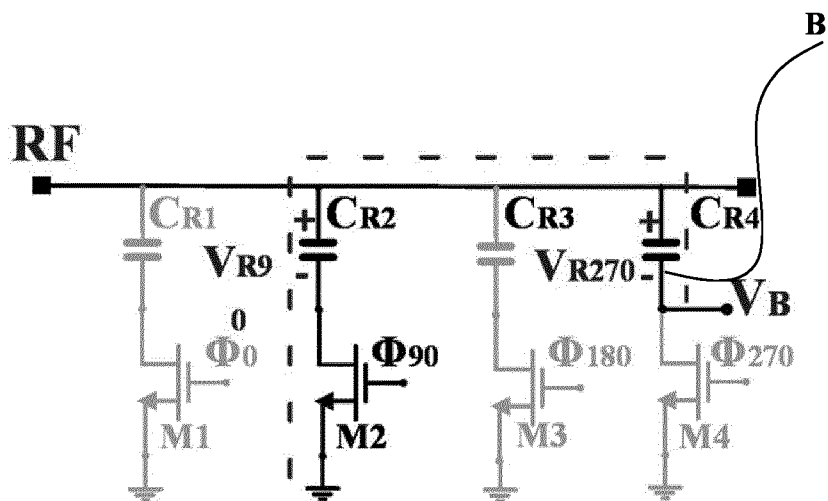


Fig. 5b

6 / 8

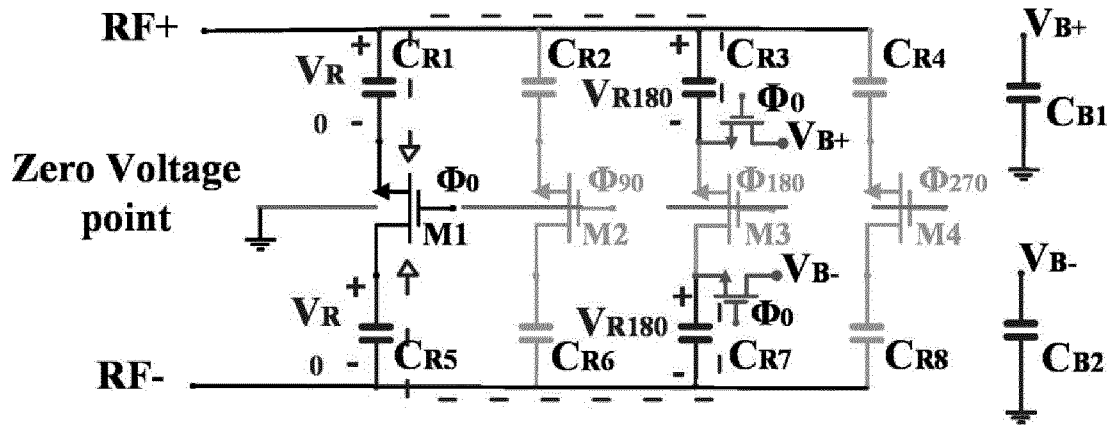


Fig. 6a

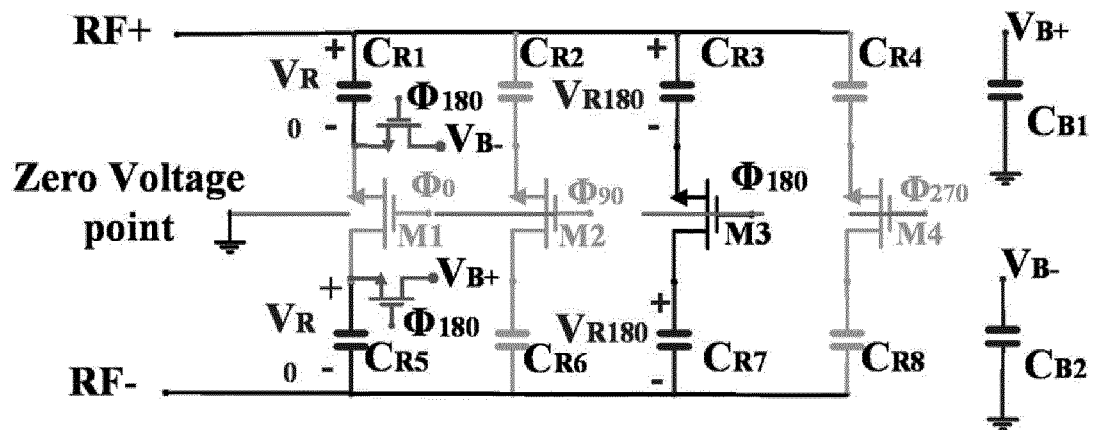


Fig. 6b

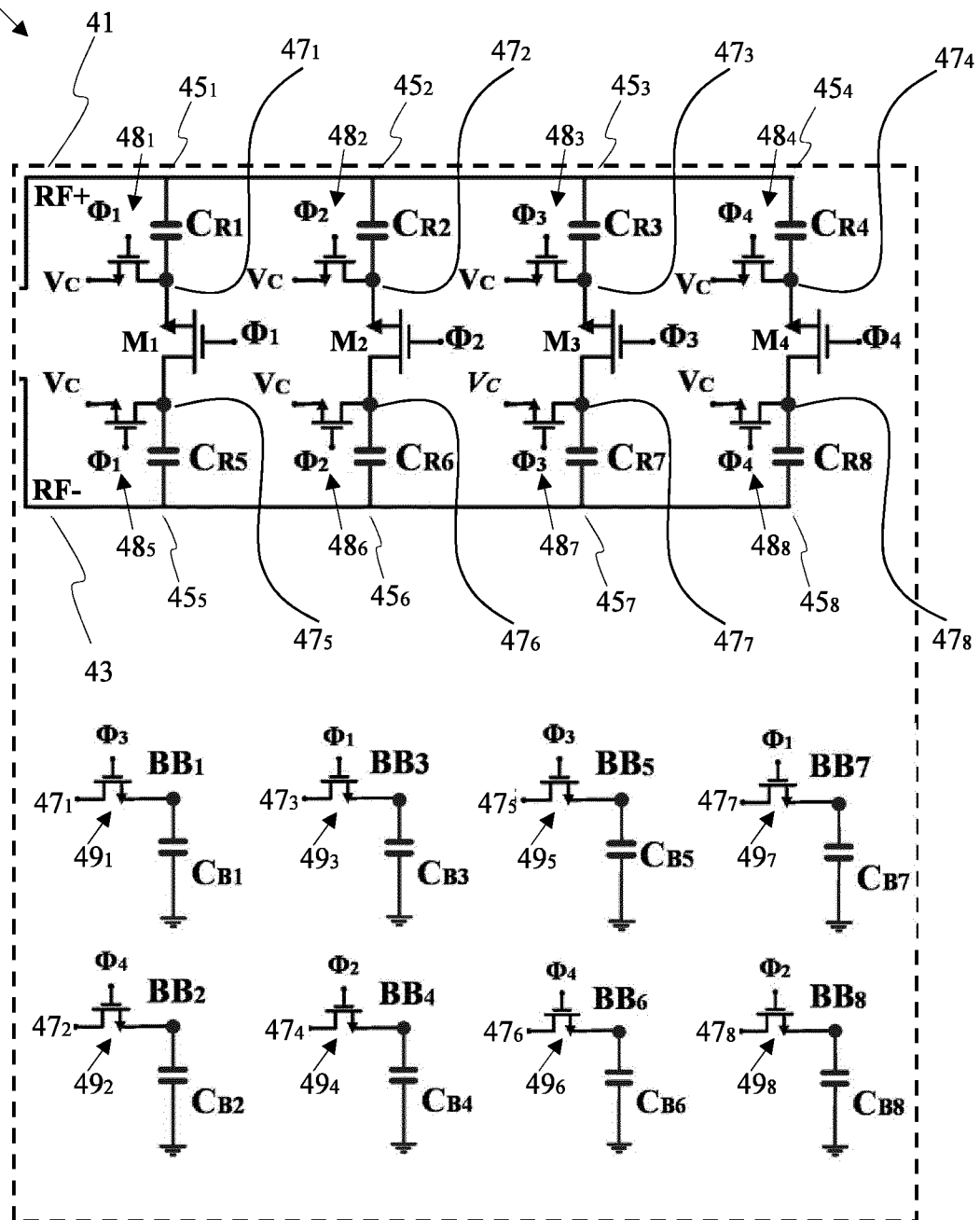
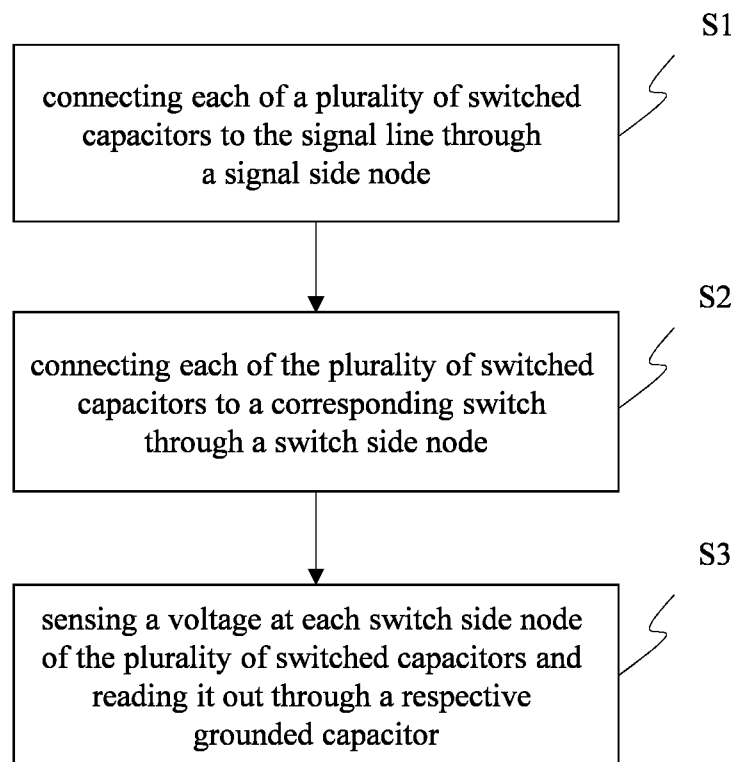


Fig. 7

8 / 8

**Fig. 8**

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/064182

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B1/16 H03D1/22
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/041361 A1 (OJO ADEDAYO [US]) 18 February 2010 (2010-02-18) abstract; figures 2B, 2C paragraphs [0043] - [0045] -----	1-15
A	US 2008/139149 A1 (MU FENGHAO [SE] ET AL) 12 June 2008 (2008-06-12) abstract; figures 3,4 paragraphs [0026] - [0040], [0043] - [0048]; figure 7 -----	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search

26 February 2020

Date of mailing of the international search report

05/03/2020

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Almenar Muñoz, M

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2019/064182

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