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(71) Applicant: **HEWLETT PACKARD ENTERPRISE DEVELOPMENT LP** [US/US]; Hewlett-Packard Development Company, L.P., 11445 Compaq Center Drive West, Houston, TX 77070 (US).

(72) Inventors: **ENGLER, David W.**; 11445 Compaq Center Dr. W., Houston, Texas 77070 (US). **ENGLER, Jennifer Kleiman**; 11445 Compaq Center Dr. W., Houston, Texas 77070 (US). **KAPOOR, Mark V.**; 11445 Compaq Center Dr. W., Houston, Texas 77070 (US).

(74) Agents: **SHOOKMAN, Jeb A.** et al.; Hewlett Packard Enterprise, 3404 E. Harmony Road, Mail Stop 79, Fort Collins, CO 80528 (US).

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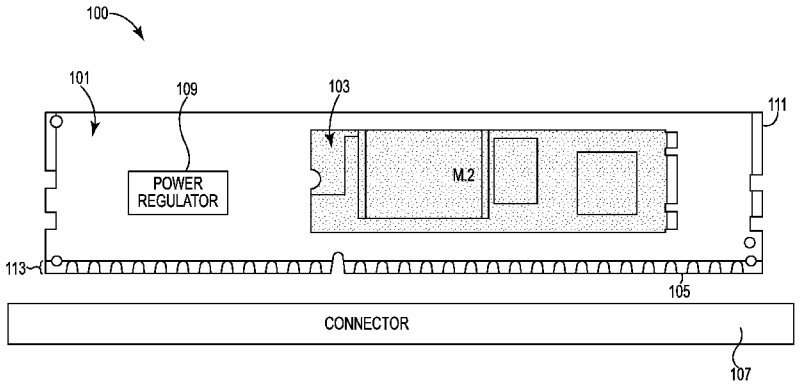


Fig. 1

(57) Abstract: Example implementations relate to an in-line memory module carrier for an M.2 form factor. For example, an in-line memory module carrier can include a circuit board having an in-line memory module form factor to receive an M.2 form factor module, an edge interface on a longitudinal edge of the circuit board for transmission of power between the M.2 form factor module and a host connector, the edge interface having an electrical contact, and a power regulator to receive a first voltage from the host connector and convert the first voltage to a second voltage to power the M.2 form factor module.

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IN-LINE MEMORY MODULE CARRIER FOR AN M.2 FORM FACTOR MODULE

Background

[0001] Computers and computer systems, such as servers, house many electronic devices, such as circuit boards, processors, memory devices, power supplies, and cooling fans, within a limited amount of space. Spare space interior to such systems is generally limited. As a result, in the limited spare space that does exist, tradeoffs may be made based on the dimensions of various devices.

Brief Description of the Drawings

[0002] Figure 1 illustrates a diagram of an example of an in-line memory module carrier, according to the present disclosure.

[0003] Figure 2 further illustrates a diagram of an example of an in-line memory module carrier, according to the present disclosure.

[0004] Figure 3 illustrates an example of an in-line memory module carrier system, according to the present disclosure.

[0005] Figure 4 illustrates a diagram of an example of SATA connections used in an in-line memory module carrier system, according to the present disclosure.

[0006] Figure 5 illustrates a diagram of an example of PCIe connections used in an in-line memory module carrier system, according to the present disclosure.

[0007] Figure 6 illustrates a block diagram of an example system for implementing an in-line memory module carrier for an M.2 form factor module, according to the present disclosure.

Detailed Description

[0008] Customers are adopting M.2 media for servers as well as higher performing personal system workloads. M.2 media, also known as Next Generation Form Factor (NGFF) media, can allow for fast, cheap, and mirrored boot compared to standard spinning media or Serial Advanced Technology Attachment (SATA) hard drives. Cheaper boot options help to drive down total cost of ownership for servers.

[0009] Currently, M.2 modules may be plugged in directly to an M.2 connector on a motherboard or mounted on Peripheral Component Interconnect Express (PCIe) cards. This takes up valuable motherboard space and/or valuable slot space on the motherboard. Some dense servers such as blades servers do not support slots for standard PCIe cards, so PCIe cards are not even an option for them. Additionally, having M.2 modules plug directly into the motherboard limits the number of M.2 modules that can be installed in the system.

[0010] In contrast, by using in-line memory module connectors, such as dual in-line memory module (DIMM) connectors, single in-line memory module (SIMM) connectors, or the like, to connect M.2 modules according to the present disclosure, larger (e.g., 22x80 mm, 21x110 mm or larger, for example) M.2 modules can be incorporated into the server system where they previously may not have been able to fit. Further, by using in-line memory module connectors to connect M.2 modules according to the present disclosure, can improve the overall performance of the server system relative to traditional server systems.

[0011] An in-line memory module carrier for an M.2 form factor module in accordance with the present disclosure can allow unused in-line memory module connectors on the motherboard to connect an M.2 module. Using the in-line memory module carrier for an M.2 form factor module can allow more M.2 modules to be integrated into the server. Further, an in-line memory module carrier for an M.2 form factor module in accordance with examples of the present disclosure, does not require any cables to connect the M.2 modules and can connect a standard M.2 form factor module, as described further herein. However, in some examples, a separate cable can be used to connect the M.2 modules for various signals, such as high speed signals.

[0012] Figure 1 illustrates a diagram of an example of an in-line memory module carrier 100, according to the present disclosure. The in-line memory module carrier 100 can include a circuit board 101 having an in-line memory module form factor to receive an M.2 form factor module 103. In some examples, the circuit board 101 can be a printed circuit board (PCB), although examples are not so limited. As used herein, a form factor is a specification of a particular circuit board, including the dimensions, power supply type, location of mounting holes, and/or number of ports, among other specifications. That is, an in-line memory module form factor can refer to a specification commonly used for in-line memory modules. Examples of an in-line memory module form factor can include 38mm and/or 43mm Single Data Rate Synchronous Dynamic Random Access Memory (SDR DRAM) in-line memory modules, Low Profile (LP) 30mm in-line memory modules, Very Low Profile (VLP) 18mm in-line memory modules, 30mm Double Data Rate (DDR)2 and DDR3 in-line memory modules, 31mm DDR4 in-line memory modules, and/or 19mm VLP DDR4 in-line memory modules, among others. While examples are provided herein, describing form factors for various DDR in-line memory modules, examples are not so limited and can include in-line memory modules other than those listed, such as DDR5.

[0013] The circuit board 101 can be configured to receive an M.2 form factor module 103. For example, the circuit board 101 can be configured to receive an M.2 form factor module 103 installed by a user. The circuit board 101 can have multiple screw holes to allow for varying sizes of M.2 form factor modules to be attached. The circuit board 101 can allow for any size M.2 form factor module 103 to be attached, such as 22x42mm M.2 modules, 22x60 M.2 modules, 22x80mm M.2 modules, and/or 22x110 M.2 modules, among others. In such examples, a user can add and/or remove the M.2 form factor module 103 as needed, and/or add additional M.2 form factor modules, as discussed further herein. Examples are not so limited, however, and the circuit board 101 can be prefabricated to include an M.2 form factor module 103 already installed.

[0014] The in-line memory module carrier 100 can also include an edge interface 113 along a longitudinal edge 105 of the circuit board 101 for coupling the circuit board 101 to a host connector 107. A host connector can refer to a connector or slot coupled to a motherboard, where the host connector is configured to transmit information and/or power between the motherboard and a circuit board inserted in

the host connector. In some examples, as further discussed in relation to Figure 3, the host connector 107 can be an in-line memory module slot.

[0015] As illustrated in Figure 1, the in-line memory module carrier 100 can also include a power regulator 109. The power regulator 109 can refer to a voltage regulator and/or other device that is capable of reducing power provided to a component in the server system. For example, the power regulator 109 can receive a first voltage from the host connector 107 and convert the first voltage to a second voltage that is different (e.g., less) than the first voltage. The second voltage can be provided to the M.2 form factor module 103, as discussed further herein. For instance, the power regulator 109 can receive a first voltage of 12 volts (V) from the host connector 107, and can convert the first voltage to a second voltage of 3.3 volts. However, examples are not so limited and the power regulator 109 can regulate the voltage received from the host connector 107 to other voltages suitable for the M.2 form factor module 103. By utilizing the power regulator 109, the M.2 form factor module 103 can plug into an empty in-line memory module connector (e.g., 107) and utilize the existing power interface to the in-line memory module connector, such as a 12V power interface in a DDR4 form factor, the necessity for a dedicated power connector for the M.2 form factor module 103 can be eliminated.

[0016] Electrical contacts on the edge interface 113 of the circuit board 101 can transmit power between the M.2 form factor module 103 and the host connector 107. For instance, the longitudinal edge 105 can include a plurality of electrical contact pads, or “gold fingers” that allow for the transmission of information between the circuit board 101 and a motherboard. The in-line memory module carrier 100 can be coupled to the host connector 107 by inserting the in-line memory module carrier 100 into the host connector 107. Coupling the in-line memory module carrier 100 to the host connector 107 can include coupling an edge connector of the circuit board 101 to a number of contacts that are part of the host connector 107. Coupling the in-line memory module carrier 100 to the host connector 107 can give a computing device access to the memory that is associated with the in-line memory module carrier 100. While Figure 1 illustrates an M.2 form factor module 103 one side of the circuit board 101, examples are not so limited, and additional M.2 form factor modules can be attached to the circuit board 101, as discussed further in relation to Figure 2.

[0017] In some examples, the circuit board 101 can be configured to receive the M.2 form factor module 103 parallel to a plane formed by the longitudinal edge 105 and a short edge 111 of the circuit board 101 transverse to the longitudinal edge 105. For example, the longitudinal edge 105 and the short edge 111 of the circuit board 101 can define a plane of the circuit board 101 having a top surface and a bottom surface. The circuit board 101 can receive the M.2 form factor module 103 on the top surface and/or the bottom surface of the circuit board 101, as described further in relation to Figure 2.

[0018] Figure 2 further illustrates a diagram of an example of an in-line memory module carrier 200 according to the present disclosure. As illustrated in Figure 2, the in-line memory module carrier 200 can be configured to receive a plurality of M.2 form factor modules 203-1, 203-2, collectively referred to as M.2 form factor modules 203. In such examples, the circuit board 201 can be configured to receive M.2 form factor modules 203 on each of the top surface 215-1 and the bottom surface 215-2. As such, the top surface 215-1 and the bottom surface 215-2 of the circuit board 201 can each include an electrical contact to receive an M.2 form factor module 203-1 and 203-2, respectively. While Figure 2 illustrates a single M.2 form factor module installed on each surface of the circuit board 201, examples are not so limited. The circuit board 201 can receive more or fewer M.2 form factor modules than illustrated in Figures 1 and 2. As illustrated in Figure 2, an M.2 form factor module can be connected on each side of the circuit board 101. Circuit board 101 can have multiple screw holes to allow for varying sizes of M.2 form factor modules. For instance, any M.2 form factor module size can be supported such as 22x42mm, 22x60mm or 22x80mm and 22x110mm. Therefore, the in-line memory module carrier 200 is not limited to a single size of M.2 form factor module, and different M.2 form factor modules can be added and/or removed depending on procurement needs and pricing as different options come to market.

[0019] In some examples, the overall thickness “h” of the circuit board 201 and the M.2 form factor modules 203 can be less than a threshold thickness. For instance, the thickness “h” of M.2 form factor module 203-1, circuit board 201, and M.2 form factor module 203-2 can be less than or equal to the distance between adjacent in-line memory module slots having M.2 form factor modules attached, such as 7.3mm.

[0020] The circuit board 201 can also include contacts to receive the M.2 form factor modules 203. For instance, the circuit board 201 can include a contact on each of a first surface 215-1 of the plane and a second surface 215-2 of the plane opposite of the first surface, where each contact receives a respective M.2 form factor module 203. In some examples, the contact can be a contact that is perpendicular (e.g., orthogonal) to the plane of the circuit board 201, such as contacts 217-1 and 217-2 illustrated in Figure 2.

[0021] As illustrated in Figure 2, each M.2 form factor module 203-1 and 203-2 can connect to the circuit board 201 via contacts 217-1 and 217-2 on the circuit board 201. In some examples, the contacts 217-1 and 217-2 can be female contacts that receive and secure the M.2 form factor modules 203-1 and 203-2 to the circuit board 201. In other words, the M.2 form factor modules 203-1 and 203-2 can be inserted and/or removed from the circuit board 201 by connecting and detaching the M.2 form factor modules 203-1 and 203-2 from the contacts 217-1 and 217-2, respectively. For example, the M.2 form factor modules can be inserted into the contacts 217-1 and 217-2 in a direction parallel to the plane, parallel to the longitudinal edge (e.g., longitudinal edge 105 as illustrated in Figure 1) and perpendicular to the short edge (e.g., short edge 111 illustrated in Figure 1).

[0022] As illustrated in Figure 2, in some examples, the contacts 217-1 and 217-2 can be raised connectors, in that each contact extends outward from the surface of the circuit board 201. Each of the contacts 217-1 and 217-2 can transmit information between the M.2 form factor modules 203-1 and 203-2 (respectively), and the host connector 207.

[0023] Figure 3 illustrates an example of an in-line memory module carrier system 302 according to the present disclosure. As illustrated in Figure 3, the in-line memory module carrier system 302 can include a circuit board 301 having an in-line memory module form factor configured to receive a memory module 303, as described in relation to Figures 1 and 2. The circuit board 301 can be analogous to the circuit board 101 described in relation to Figure 1 and circuit board 201 described in relation to Figure 2. Also, the in-line memory module carrier system 302 can include a second circuit board 304. The second circuit board 304 can further include an in-line memory module slot 307 to receive the circuit board 301. As used herein, an in-line memory module slot can refer to a specialized memory slot on the motherboard that supports a variety of memory types, including DDR, DDR2 and

DDR3 RAM, among others. The in-line memory module slot 307 can be analogous to the host connector 107 illustrated in Figure 1.

[0024] The in-line memory module carrier system 302 can include a sensing interface 308 to sense a type of memory module coupled to the circuit board 301. For example, in response to insertion of the circuit board 301 (e.g., a first circuit board) in the in-line memory module slot 307, the sensing interface 308 can detect whether a memory module is coupled to the circuit board 301, and if so, what type of memory module is coupled to the circuit board 301. If an M.2 module, such as the M.2. form factor module 303, is coupled to the circuit board 301, then the sensing interface 308 can detect the presence of the M.2 form factor module 303. Additionally and/or alternatively, the sensing interface 308 can detect that an M.2 form factor module is not connected to the circuit board 301, as discussed further herein. In some examples, the sensing interface 308 can be an inter-integrated circuit (I2C). In such examples, the I2C signals can connect to a serial presence detect (SPD) on an in-line memory module carrier 300 without an M.2 form factor module 303, or a field replaceable unit (FRU) device on an in-line memory module carrier 300 with an M.2 form factor module 303. The in-line memory module carrier 300, in some examples, can have a contact structure that conforms to existing standards for transmitting power and information to and/or from the in-line memory module 307.

[0025] The in-line memory module carrier system 302 can also include a multiplexor 310. As used herein, a multiplexor is a device that selects one of several analog or digital input signals and forwards the selected input to a single line. The multiplexer 310 can transmit information between the in-line memory module slot 307 and one of a volatile memory controller 312 and a non-volatile memory controller 314 based on the type of memory module sensed by the sensing interface 308. For example, the default connection on the multiplexor 310 can be to enable DDR signaling. If an M.2 form factor module 303 is connected to the first circuit board 301, then the multiplexor can connect the non-volatile memory controller 314 signals to the circuit board 301. Conversely, if the M.2 form factor module 303 is not connected to the circuit board 301, then the volatile memory controller 312 signals can be connected to the circuit board 301. As used herein, a memory controller refers to a digital circuit that manages the flow of data going to and from the computer's main memory. A non-volatile memory controller refers to a controller that

manages the flow of data going to and from a non-volatile memory module. A volatile memory controller refers to a controller that manages the flow of data going to and coming from a volatile memory module.

[0026] For example, the second circuit board 304 can comprise a motherboard that further includes a volatile memory controller 312 and a non-volatile memory controller 314. The non-volatile memory controller 314 can be one of a SATA controller and PCIe controller. In response to detecting that the M.2 form factor module 303 is connected to the circuit board 301, signals can be sent via the multiplexor to the non-volatile memory controller 314 (e.g., the SATA controller or the PCIe controller). In contrast, in response to not detecting that the M.2 form factor module 303 is connected to the circuit board 301, signals can be sent via the multiplexor to the volatile memory controller 312.

[0027] The M.2 form factor module 303 can use either a SATA or PCIe interface, among other types of non-volatile memory interfaces. When the M.2 form factor module 303 is using the SATA interface, a transmit and receive differential pair is used from the chipset or other SATA controller. Similarly, when the M.2 form factor module 303 is using the PCIe interface, transmit and receive differential pairs along with a reset and a 100MHz differential clock are used. PCIe controllers may be found in the central processing unit (CPU) or chipset and a clock chip may be used to provide the 100MHz clock.

[0028] In examples of the present disclosure, SATA and/or PCIe signals can be multiplexed with other signals that are used by the DDR interface. The default connection on the multiplexor 310 can be to enable DDR signaling. For example, unless the sensing interface 308 senses that an M.2 form factor module 303 is coupled to the circuit board 301, the multiplexor will enable DDR signaling and transmit signals to the volatile memory controller 312, such as a DDR4 controller. In some examples, if the sensing interface 308 senses that an M.2 form factor module is coupled to the circuit board 301, the multiplexor 310 can enable SATA or PCIe signaling and transmit signals to a non-volatile memory controller 314.

[0029] The multiplexor 310 can transmit and/or receive signals between the non-volatile memory controller 314, the volatile memory controller 312, and the in-line memory module slot 307. For instance, the multiplexor 310 can multiplex transmit and receive differential pair signals between the non-volatile memory controller 314 and the in-line memory module slot 307. Similarly, the multiplexor 310

can multiplex signals between the volatile memory controller 312 and the in-line memory module slot 307.

[0030] In an example, the non-volatile memory controller 314 can be a PCIe controller. In such an example, the multiplexor 310 can multiplex transmit and receive differential pair signals between the non-volatile memory controller 314 (e.g., the PCIe controller) and the in-line memory module slot 307, and multiplex a reset signal between a processing resource (not shown in Figure 3) and the in-line memory module slot 307. Additionally, when an M.2 form factor module 303 is connected to the circuit board 301, the multiplexor 310 can multiplex a differential clock signal between a clock circuit (not shown in Figure 2) and the in-line memory module slot 307.

[0031] Figure 4 illustrates a diagram of an example of SATA connections used in an in-line memory module carrier system, according to the present disclosure. Specifically, Figure 4 illustrates SATA connections to a DDR connector (e.g. host connector 107 illustrated in Figure 1, and host connector 307 illustrated in Figure 3). As illustrated in Figure 4, the multiplexor 410 can multiplex signals between a DDR4 connector 407, and a SATA controller 414. As discussed in relation to Figures 1-4, the multiplexor 410 would multiplex signals to the SATA controller 414 in response to detecting an M.2 form factor module (e.g., M.2 form factor module 103) attached to the circuit board (e.g., circuit board 101).

[0032] As illustrated in Figure 4, the multiplexor 410 can multiples a number of signals between the DDR4 connector 407 and the SATA controller 414. For instance, the multiplexor 410 can multiplex a SATA transmission differential signal (SATA TX DN and SATA TX DP, illustrated in Figure 4). Further, the multiplexor 410 can multiplex a SATA receive differential signal (SATA RX DN and SATA RX DP, illustrated in Figure 4).

[0033] Also, as illustrated in Figure 4, the multiplexor 410 can send and/or receive signals from the sensing interface (e.g., sensing interface 308 illustrated in Figure 3). For instance, the sensing interface 308 can include an SPD. The SPD can have three signals, illustrated as SA0, SA1, and SA2, as well as a ground, illustrated as GND, which can transmit signals to the multiplexor 410. The SA0, SA1, and SA2 signals can be transmitted to the multiplexor 410 indicating a type of memory module that is connected to the in-line memory module carrier. Additionally, the multiplexor 410 can receive a control signal, illustrated as CTRL in Figure 4.

[0034] Figure 5 illustrates a diagram of an example of PCIe connections used in an in-line memory module carrier system, according to the present disclosure. Specifically, Figure 5 illustrates PCIe connections to a DDR connector (e.g. host connector 107 illustrated in Figure 1, and host connector 307 illustrated in Figure 3). As illustrated in Figure 5, the multiplexor 510 can multiplex signals between a DDR4 connector 507, and a PCIe controller 514. As discussed in relation to Figures 1-4, the multiplexor 510 would multiplex signals to the PCIe controller 514 in response to detecting an M.2 form factor module (e.g., M.2 form factor module 103) attached to the circuit board (e.g., circuit board 101).

[0035] As illustrated in Figure 5, the multiplexor 510 can multiplex a number of signals between the DDR4 connector 507 and the SATA controller 514. Notably, many of the same signals from the DDR4 connector 507 can be used for PCIe signaling, as compared to SATA signaling, as illustrated in Figure 4. For instance, signals 140, 139, 238 and 239 on the DDR4 connector 507 can send and receive signals to and/or from the multiplexor 510, regardless of the interface to which the multiplexor 510 sends signals. However, if the multiplexor 510 multiplexes signals to the PCIe controller 514, as illustrated in Figure 5, additional signals 57, 58, and 78 on the DDR4 connector 507 may be used.

[0036] The multiplexor 510 can multiplex a number of signals to the PCIe controller and other devices. For instance, the multiplexor 510 can multiplex a PCIe transmission differential signal (PCIe TX DN and PCIe TX DP, illustrated in Figure 5). Further, the multiplexor 510 can multiplex a PCIe receive differential signal (PCIe RX DN and PCIe RX DP, illustrated in Figure 5).

[0037] Also, as illustrated in Figure 5, the multiplexor 510 can send and/or receive signals from the sensing interface (e.g., sensing interface 308 illustrated in Figure 3). For instance, the sensing interface 308 can include an SPD. The SPD can have three signals, illustrated as SA0, SA1, and SA2, as well as a ground, illustrated as GND, which can transmit signals to the multiplexor 510. The SA0, SA1, and SA2 signals can be transmitted to the multiplexor 510 indicating a type of memory module that is connected to the in-line memory module carrier. Additionally, the multiplexor 510 can receive a control signal, illustrated as CTRL in Figure 5.

[0038] In comparison to the SATA signaling illustrated in Figure 4, PCIe signaling can include additional clock, reset, and event signals. For instance, as described in relation to Figure 3, when the M.2 form factor module 303 is using the

PCIe interface, transmit and receive differential pairs along with a reset and a 100MHz differential clock is used. Accordingly, the multiplexor 510 can multiplex a 100MHz differential clock signal (CLK 100 DN and CLK 100 DP, illustrated in Figure 5), a DDR4 reset signal (DDR4 RESET N, illustrated in Figure 5), and a DDR4 event signal (DDR4 EVENT N, illustrated in Figure 5). Further, the multiplexor 510 can multiplex a PCI RST signal (PCI RST N, illustrated in Figure 5).

[0039] Figure 6 is a block diagram of an example system 619 for implementing an in-line memory module carrier for an M.2 form factor module, according to the present disclosure. System 619 may include at least one computing device that is capable of communicating with at least one remote system. System 619 may be similar to system 302 of Figure 3, for example. In the embodiment of Figure 6, system 619 includes a processor 621 and a machine-readable storage medium 623. Although the following descriptions refer to a single processor and a single machine-readable storage medium, the descriptions may also apply to a system with multiple processors and multiple machine-readable storage mediums. In such examples, the instructions may be distributed (e.g., stored) across multiple machine-readable storage mediums and the instructions may be distributed (e.g., executed by) across multiple processors.

[0040] Processor 621 may be one or more central processing units (CPUs), microprocessors, and/or other hardware devices suitable for retrieval and execution of instructions stored in machine-readable storage medium 623. In the particular embodiment shown in Figure 6, processor 621 may fetch, decode, and execute instructions 626, 627, 628 for implementing an in-line memory module carrier for an M.2 form factor module. As an alternative or in addition to retrieving and executing instructions, processor 621 may include one or more electronic circuits comprising a number of electronic components for performing the functionality of one or more of the instructions in machine-readable storage medium 623. With respect to the executable instruction representations (e.g., boxes) described and shown herein, it should be understood that part or all of the executable instructions and/or electronic circuits included within one box may, in alternate embodiments, be included in a different box shown in the figures or in a different box not shown.

[0041] Machine-readable storage medium 623 may be any electronic, magnetic, optical, or other physical storage device that stores executable instructions. Thus, machine-readable storage medium 623 may be, for example, Random Access Memory (RAM), an Electrically-Erasable Programmable Read-Only Memory

(EEPROM), a storage drive, an optical disc, and the like. Machine-readable storage medium 623 may be disposed within system 619, as shown in Figure 6. In this situation, the executable instructions may be "installed" on the system 619. Alternatively, machine-readable storage medium 623 may be a portable, external or remote storage medium, for example, that allows system 619 to download the instructions from the portable/external/remote storage medium. In this situation, the executable instructions may be part of an "installation package". As described herein, machine-readable storage medium 623 may be encoded with executable instructions for implementing an in-line memory module carrier for an M.2 form factor module.

[0042] Referring to Figure 6, sensing a type of a memory module instructions 626, when executed by a processor (e.g., 621), may cause system 619 to sense, using an inter-integrated circuit (I2C), a type of a memory module coupled to a first circuit board, wherein the first circuit board has an in-line memory module form factor and receives the memory module. For instance, the machine readable storage medium 623 can store instructions that when executed by the processor 621, can sense whether an M.2 form factor module (e.g., M.2 form factor module 103 illustrated in Figure 1) is coupled to the circuit board (e.g., circuit board 101 illustrated in Figure 1).

[0043] Receiving data signals from a multiplexor instructions 627, when executed by a processor (e.g., 621), may cause system 619 to receive data signals from a multiplexor on a second circuit board, in response to insertion of the first circuit board in a connector of the second circuit board. For example, the machine readable storage medium 623 can store instructions that when executed by the processor 621, can receive signals from the multiplexor (e.g., multiplexor 310 illustrated in Figure 3) on a motherboard (e.g., board 304), indicating that a circuit board (e.g., circuit board 301 illustrated in Figure 3) has been inserted into a connector (e.g., host connector 307 illustrated in Figure 3) on the motherboard.

[0044] Directing data signal instructions 628, when executed by a processor (e.g., 621), may cause system 619 to direct, using the multiplexor, the data signals to either SATA circuitry or PCIe circuitry based on the type of the memory module coupled to the first circuit board. For instance, as discussed in relation to Figures 1-5, the multiplexor (e.g., multiplexor 310 illustrated in Figure 3) can direct signals from the connector (e.g., host connector 307 illustrated in Figure 3) to a SATA connector or a PCIe connector (such as non-volatile memory controller 314 illustrated in Figure

3) rather than to a volatile memory controller (such as volatile memory controller 312 illustrated in Figure 3) if an M.2 form factor module is connected to the circuit board.

[0045] In some examples, the machine readable storage medium 623 can store instructions that when executed by the processor 621can adjust a fan speed based on the type of memory module coupled to the circuit board. For instance, if an M.2 form factor module (e.g., M.2 form factor module 303 illustrated in Figure 3) is connected to the circuit board (e.g., circuit board 301 illustrated in Figure 3), the fan speed in the in-line memory module carrier system 302 can be reduced.

[0046] Additionally, the machine readable storage medium 623 can store instructions that when executed by the processor 621 can receive a first voltage from the second circuit board (e.g., motherboard 304 illustrated in Figure 3), convert the first voltage to a second voltage lower than the first voltage, and supply the second voltage to the memory module, in response to sensing that the memory module is an M.2 form factor module. For instance, referring to Figure 3, a first voltage of 12V can be received by the circuit board 301 from the motherboard 304, and can be converted to a second voltage of 3.3V, in response to sensing that the M.2 form factor module 303 is coupled to the circuit board 301. The lower, 3.3V power can then be supplied to the M.2 form factor module 303.

[0047] In the foregoing detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how examples of the disclosure may be practiced. These examples are described in sufficient detail to enable those of ordinary skill in the art to practice the examples of this disclosure, and it is to be understood that other examples may be utilized and that process, electrical, and/or structural changes may be made without departing from the scope of the present disclosure.

[0048] The figures herein follow a numbering convention in which the first digit corresponds to the drawing figure number and the remaining digits identify an element or component in the drawing. Elements shown in the various figures herein can be added, exchanged, and/or eliminated so as to provide a number of additional examples of the present disclosure. In addition, the proportion and the relative scale of the elements provided in the figures are intended to illustrate the examples of the present disclosure, and should not be taken in a limiting sense. Further, as used

herein, "a number of" an element and/or feature can refer to one or more of such elements and/or features.

[0049] As used herein, “logic” is an alternative or additional processing resource to perform a particular action and/or function, etc., described herein, which includes hardware, e.g., various forms of transistor logic, application specific integrated circuits (ASICs), etc., as opposed to computer executable instructions, e.g., software firmware, etc., stored in memory and executable by a processor.

What is claimed:

1. An in-line memory module carrier comprising:

a circuit board having an in-line memory module form factor to receive an M.2 form factor module;

an edge interface on a longitudinal edge of the circuit board for transmission of power between the M.2 form factor module and a host connector, the edge interface having an electrical contact; and

a power regulator to receive a first voltage from the host connector and convert the first voltage to a second voltage to power the M.2 form factor module.

2. The in-line memory module carrier of claim 1, including the circuit board to receive the M.2 form factor module parallel to a plane formed by the longitudinal edge and a short edge of the circuit board transverse to the longitudinal edge.

3. The in-line memory module carrier of claim 2, further including a contact on each of a first side of the plane and a second side of the plane opposite of the first side, each contact to receive a respective M.2 form factor module.

4. The in-line memory module carrier of claim 2, further including a contact that is perpendicular to the plane to receive the M.2 form factor module.

5. The in-line memory module carrier of claim 4, wherein the contact is a female contact that receives and secures the M.2 form factor module.

6. The in-line memory module carrier of claim 1, further including a raised connector on a surface of the circuit board for transmission of information between the M.2 form factor module and the host connector.

7. The in-line memory module carrier of claim 1, wherein the first voltage comprises 12 volts and wherein the second voltage comprises 3.3 volts.

8. An in-line memory module carrier system, comprising:

a circuit board having an in-line memory module form factor configured to receive a memory module;

a second circuit board including:

an in-line memory module slot to receive the first circuit board;

a sensing interface to sense a type of memory module coupled to the first circuit board, in response to insertion of the first circuit board in the in-line memory module slot; and

a multiplexor to transmit information between the in-line memory module slot and one of a volatile memory controller and a non-volatile memory controller based on the type of memory module sensed by the sensing interface.

9. The in-line memory module carrier system of claim 8, wherein the second circuit board comprises a motherboard that further includes the volatile memory controller and the non-volatile memory controller; and

wherein the non-volatile memory controller comprises one of a serial advanced technology attachment (SATA) controller and peripheral component interconnect express (PCIe) controller.

10. The in-line memory module carrier system of claim 8, including the multiplexor to:

multiplex transmit and receive differential pair signals between the non-volatile memory controller and the in-line memory module slot; and

multiplex signals between the volatile memory controller and the in-line memory module slot; and

wherein the non-volatile memory controller comprises a SATA controller.

11. The in-line memory module carrier system of claim 8, including the multiplexor to:

multiplex transmit and receive differential pair signals between the non-volatile memory controller and the in-line memory module slot;

multiplex a reset signal between a processing resource and the in-line memory module slot; and

multiplex signals between the volatile memory controller and the in-line memory module slot; and

wherein the non-volatile memory controller comprises a PCIe controller.

12. The in-line memory module carrier system of claim 11, including the multiplexor to multiplex a differential clock signal between a clock circuit and the in-line memory module slot.

13. A non-transitory machine readable medium storing instructions executable by a processor of a system to cause the system to:

sense, using an inter-integrated circuit (I2C), a type of a memory module coupled to a first circuit board, wherein the first circuit board has an in-line memory module form factor and receives the memory module;

receive data signals from a multiplexor on a second circuit board, in response to insertion of the first circuit board in a connector of the second circuit board; and

direct, using the multiplexor, the data signals to either serial advanced technology attachment (SATA) circuitry or peripheral component interconnect (PCIe) circuitry based on the type of the memory module coupled to the first circuit board.

14. The non-transitory medium of claim 13, including instructions to adjust a fan speed based on the type of memory module coupled to the first circuit board.

15. The non-transitory medium of claim 13, further including instructions executable by the processor to:

receive a first voltage from the second circuit board;

convert the first voltage to a second voltage lower than the first voltage; and

supply the second voltage to the memory module, in response to sensing that the memory module is an M.2 form factor module.

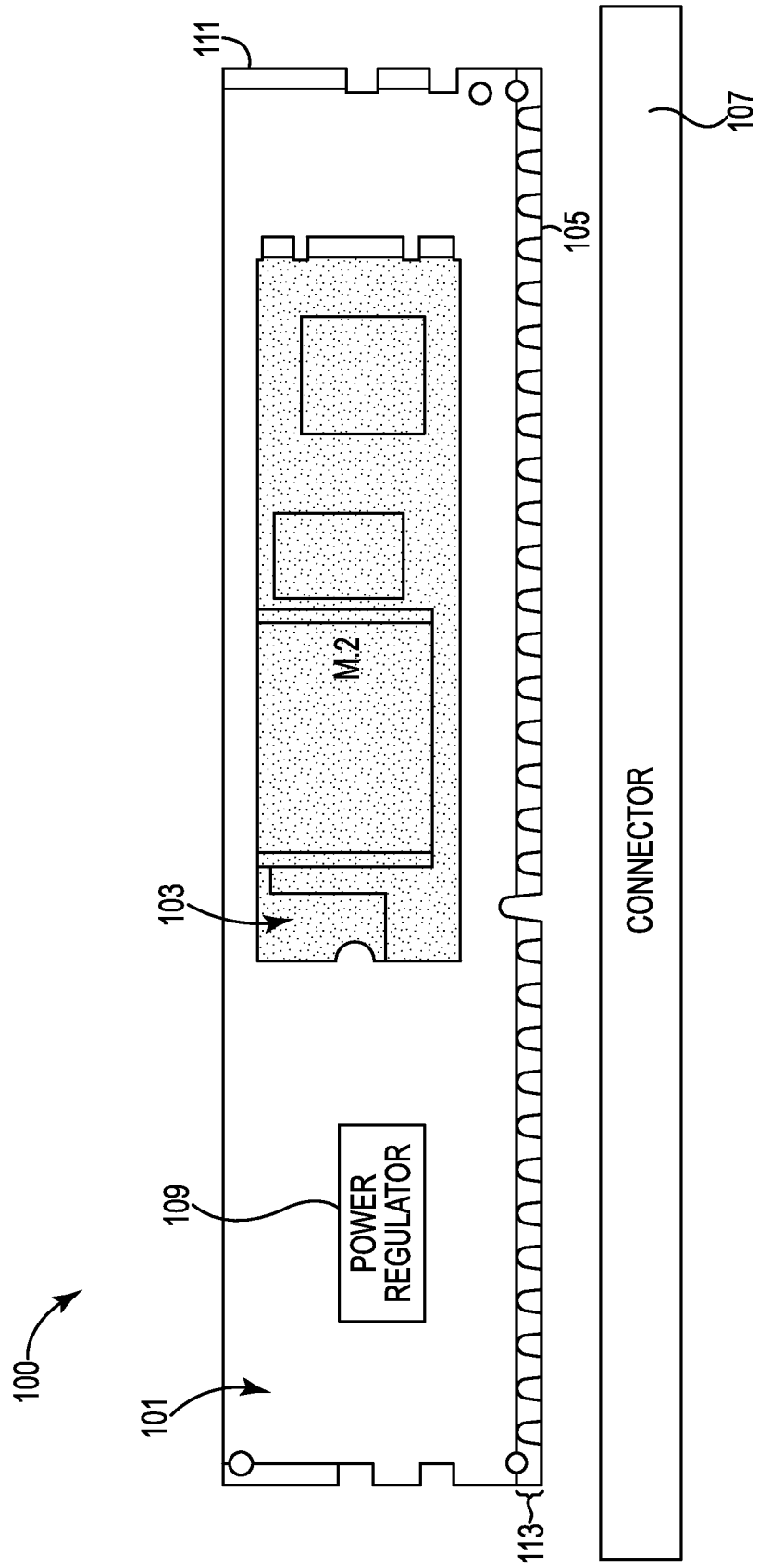


Fig. 1

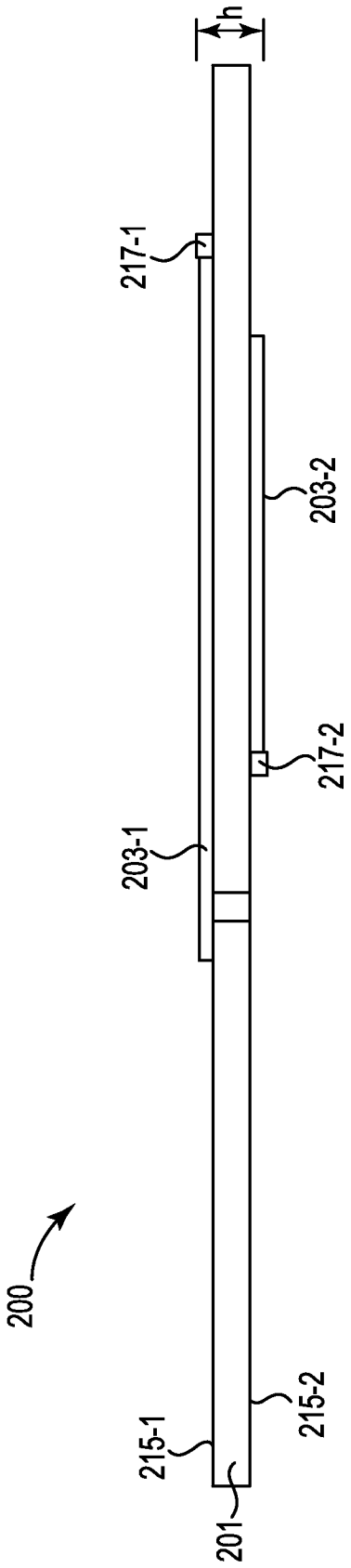


Fig. 2

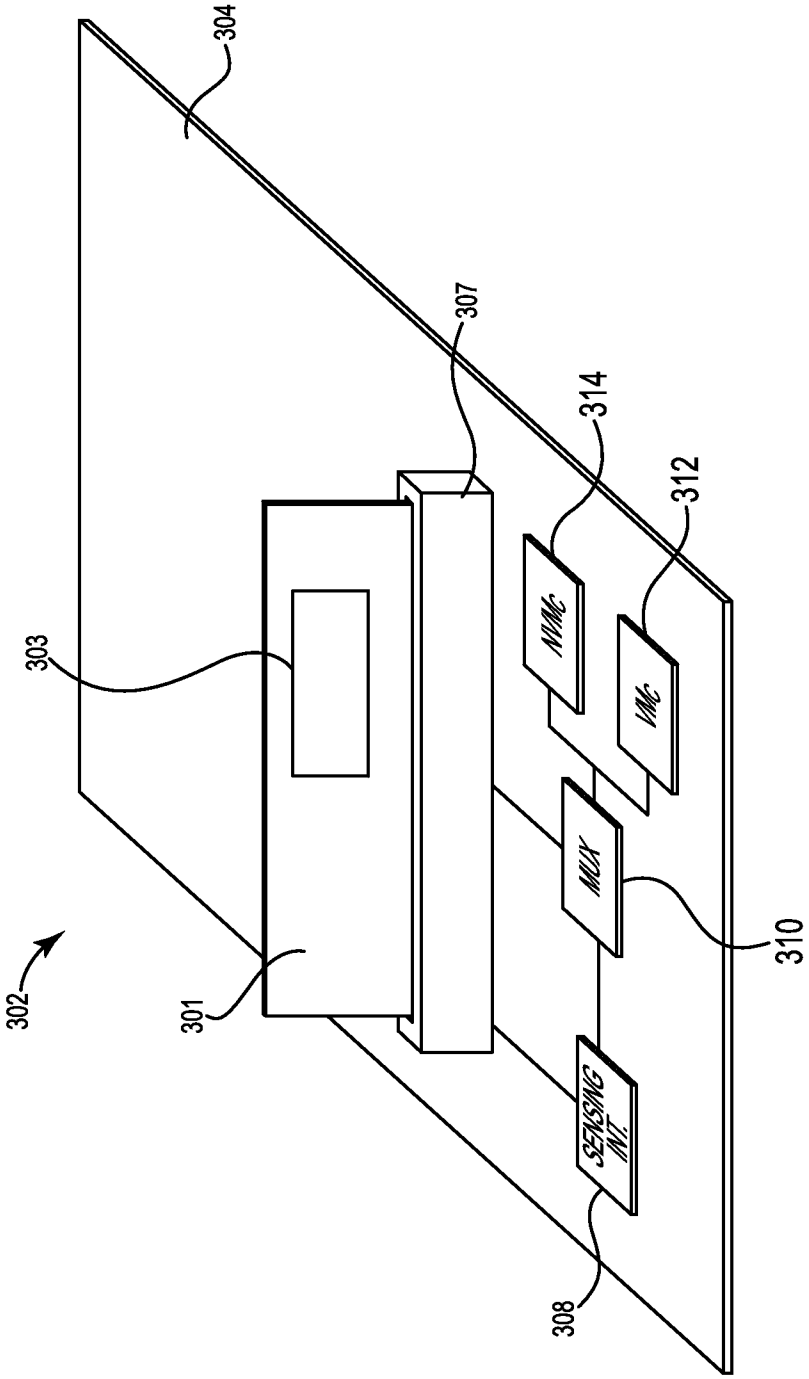


Fig. 3

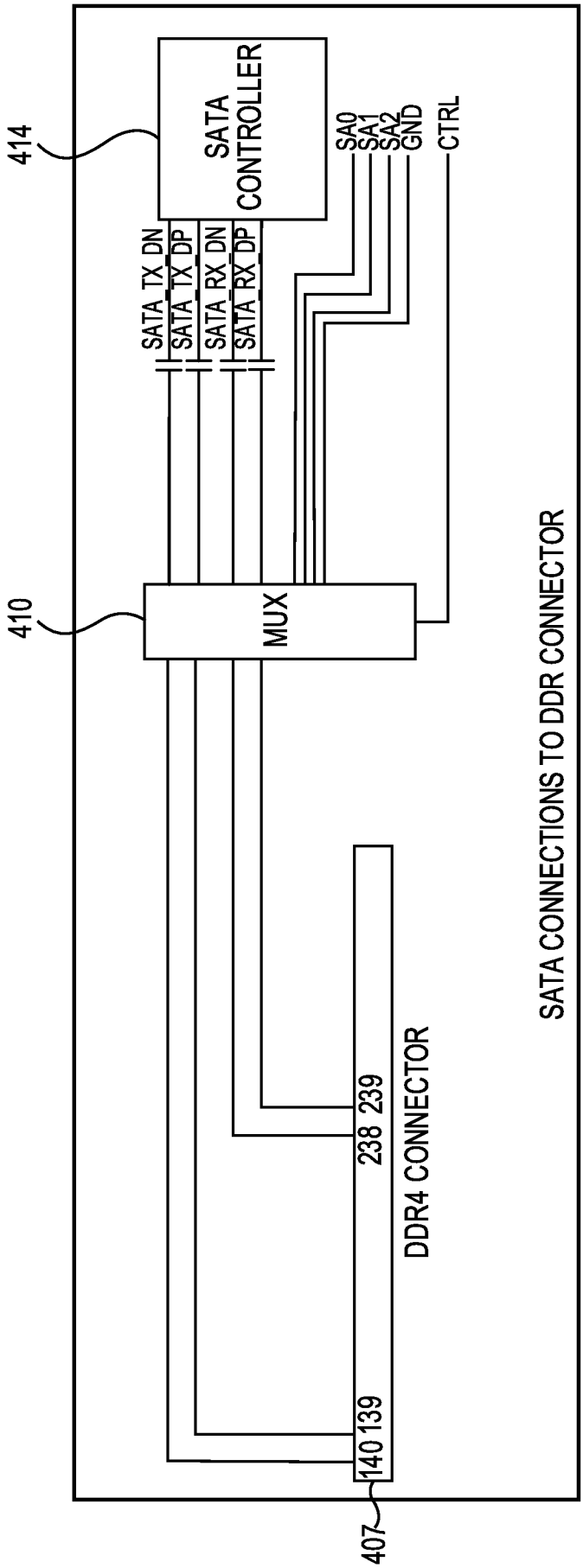

414
SATA CONTROLLER
SA0
SA1
SA2
GND
CTRL
SATA_TX_DN
SATA_TX_DP
SATA_RX_DN
SATA_RX_DP
410
MUX
238 239
140 139
DDR4 CONNECTOR
SATA CONNECTIONS TO DDR CONNECTOR
407

Fig. 4

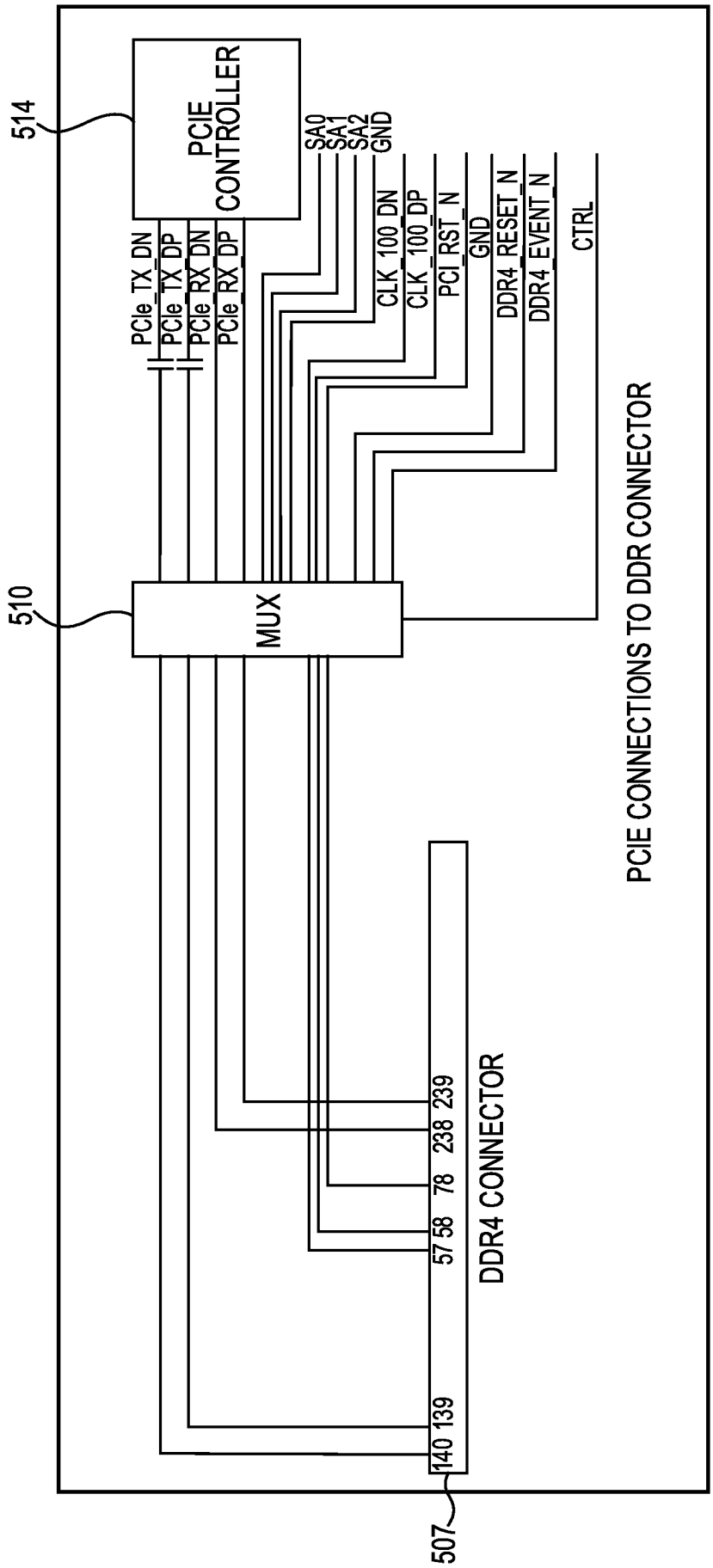

514
PCIE CONTROLLER
SA0
SA1
SA2
GND
PCIe_TX_DN
PCIe_TX_DP
PCIe_RX_DN
PCIe_RX_DP
CLK_100_DN
CLK_100_DP
PCI_RST_N
GND
DDR4_RESET_N
DDR4_EVENT_N
CTRL
510
MUX
PCIE CONNECTIONS TO DDR CONNECTOR
239
238
78
57 58
DDR4 CONNECTOR
140 139
507

Fig. 5

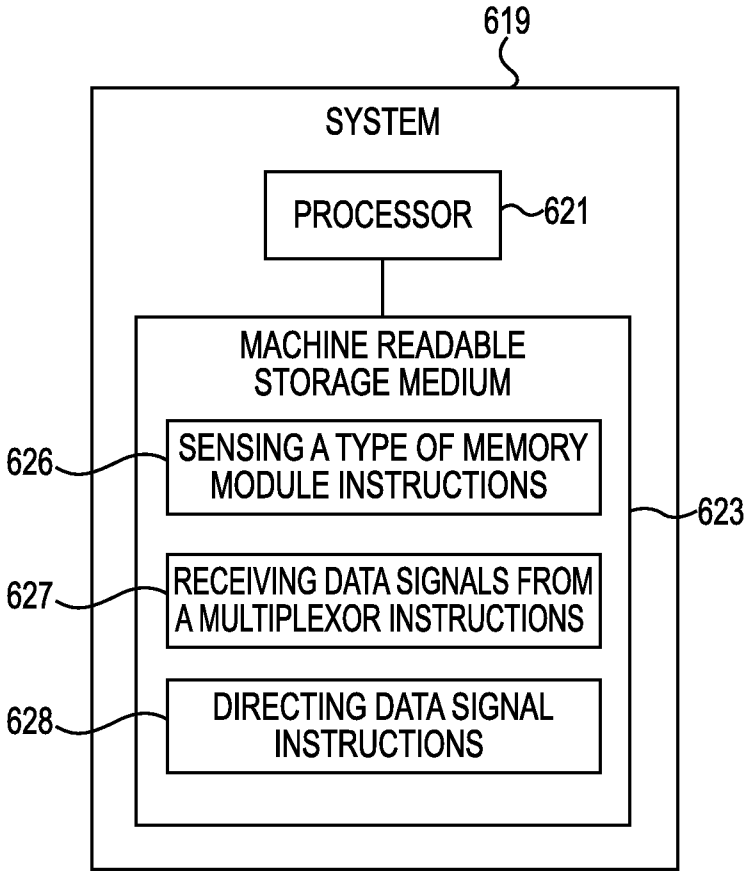

619
SYSTEM
PROCESSOR
621
MACHINE READABLE STORAGE MEDIUM
626
SENSING A TYPE OF MEMORY MODULE INSTRUCTIONS
623
627
RECEIVING DATA SIGNALS FROM A MULTIPLEXOR INSTRUCTIONS
628
DIRECTING DATA SIGNAL INSTRUCTIONS

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/013080

A. CLASSIFICATION OF SUBJECT MATTER

G11C 5/02(2006.01)i, G11C 5/14(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 5/02; G06F 3/06; G06F 12/00; G06F 13/42; G06F 13/00; G06F 11/00; G11C 5/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: in-line, memory, module, carrier, circuit, board, form, factor, edge, interface, power, regulator, connector

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0006729 A1 (CHRISTOPHER E. COX et al.) 02 January 2014 See paragraph [0026]; and figure 2.	1-15
A	US 6092146 A (TIMOTHY JAY DELL et al.) 18 July 2000 See column 2, lines 50-63; and figure 1.	1-15
A	US 2002-0112119 A1 (JOHN B. HALBERT et al.) 15 August 2002 See paragraph [0009]; and figure 2.	1-15
A	US 2014-0289434 A1 (SRIDHARAN RANGANATHAN et al.) 25 September 2014 See paragraphs [0079]-[0095]; and figure 10.	1-15
A	US 2008-0183957 A1 (DANIEL M. DREPS et al.) 31 July 2008 See paragraph [0004]; and figure 2.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 October 2015 (13.10.2015)	**15 October 2015 (15.10.2015)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
BYUN, Sung Cheal
Telephone No. +82-42-481-8262

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/013080

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